

No.3353A

LA7956

Video Switch for TV / VCR Use

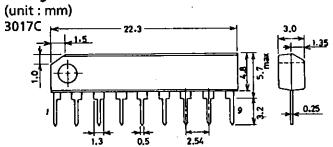
Features

- \cdot 4 inputs, 1 output, 75 $\!\Omega$ termination, driver on-chip
- · 6dB amp on-chip
- · Excellent crosstalk characteristic
- · Wide band

Maximum Ratings at Ta = 25%	C				unit	
Maximum Supply Voltage		V7 max		14	V	
Maximum Input Supply Voltage (1)		nax, V6 max		8	V	
		nax, V9 max,		Ŭ	•	
Maximum Input Supply Volta		nax, V3 max V _{CC} =14V		14	V	•
Maximum Output Current		ax		10	mA	
Allowable Power Dissipation		ax Ta≤65°C	540		mW	
Operating Temperature		Topr		+65	°C	
Storage Temperature		rstg -		150	°C	
	J		00 00 1	100	Ŭ	
Operating Conditions at Ta = :	25°C				unit	
Operating Voltage Range		V _{CC} op		13.5	V	
Recommended Supply Voltage		-		12	v	
Omanati wali						
Operating Characteristics at		$_{\rm CC} = 12 \text{V}$	min	typ	max	unit
Quiescent Current	I _{CC}		15	21	30	mA
Input Bias Voltage	V4, V6,		3.5	3.8	4.1	V
0.1	V8, V9					
Output Bias Voltage	V1		4.6	6.1	7.6	V
	$\mathbf{v_{os}}$	(Note 1)	-50	0	+50	mV
Control Threshold Voltage	V2H, V3H,		2.3			v
	V2L, V3L				0.7	V
	12, 13		-20	-6		μΑ
Voltage Gain	GV	$f = 1MHz, V_{IN} = 2Vpp (Note 1)$	5.6	6.1	6.4	dΒ

Continued on next page.

Package Dimensions



SANYO: SIP9

Continued from preceding page.

, 0, 0						• .
		•	mın	typ	max	unit
Frequency Characteristic	GV-f	$\begin{cases} 0dB & \text{at } f = 100kHz \text{ (Note 1)} \\ f = 10MHz, V_{IN} = 1Vpp \end{cases}$	-3	0		dB
Output Dynamic Range	$ m V_{DR}$	$f = 15kHz, V_{IN} = 1.5p-p \text{ (Note 1)}$	1.4	1.5		Vpp
Crosstalk (Note 2)	\mathbf{CT}	$V_{IN} = 1V_{p-p,f} = 3MHz$ (Note 1)	50	58		dB
			(48)	(55)		
•		$V_{IN} = 1V_{p-p,f} = 5MHz$ (Note 1)	45	5 5		dΒ
			(45)	(52)		

^{*} The current flowing into the IC is defined as positive and current from the IC is defined as negative.

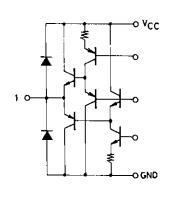
Video Switch Truth Table

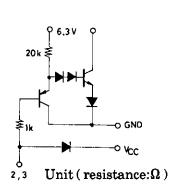
S2 (Pin 2)	S3 (Pin 3)	V _{IN} 1 (Pin 4)	V _{IN} 2 (Pin 6)	V _{IN} 3 (Pin 8)	V _{IN} 4 (Pin 9)
H	Н	ON	OFF	OFF	OFF
L	Н	OFF	ON	OFF	OFF
H	L	OFF	OFF	ON	OFF
L	L	OFF	OFF	OFF	ON

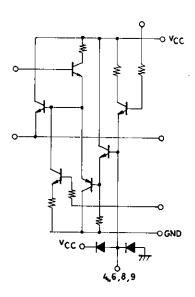
Note 1: Refer to this Truth Table and make measurements by switching S2, S3.

Note 2:(): Crosstalk between pins 8 and 9

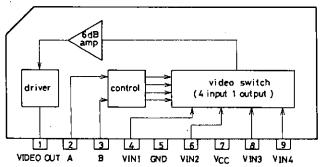
Input/Output Equivalent Circuit



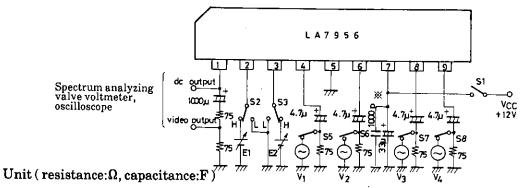




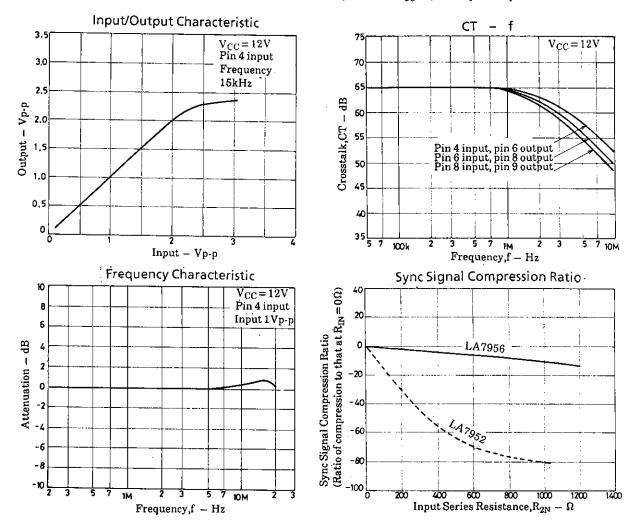
Equivalent Circuit Block Diagram



Test Circuit



X: Connect the bypass capacitor for V_{CC} as close to pin 7 as possible.



Design Notes

An improvement in the DC clamp circuit has improved the sync signal compression attributable to the signal source impedance, but the response time of the DC clamp is made longer accordingly than that of the LA7952. Make adjustments by connecting a high resistance (several hundred $k\Omega$) across input pin and GND (decreasing the resistance makes the sync signal compression larger).

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