Ordering number : ENN7045

Monolithic Linear IC

LA0205

Optoelectronic IC for CD-R Drive Pickup Applications

Overview

The LA0205 is a pick-up OE-IC for CD-R drives supporting (CD-ROM 32 × drive and CD-R/RW 8 × drive).

Features

- High speed photo processing.
- 32 × speed reading.
- Miniature clear package FP-14 (Package size excluding lead section: 3 × 4mm, pin pitch: 0.5mm).

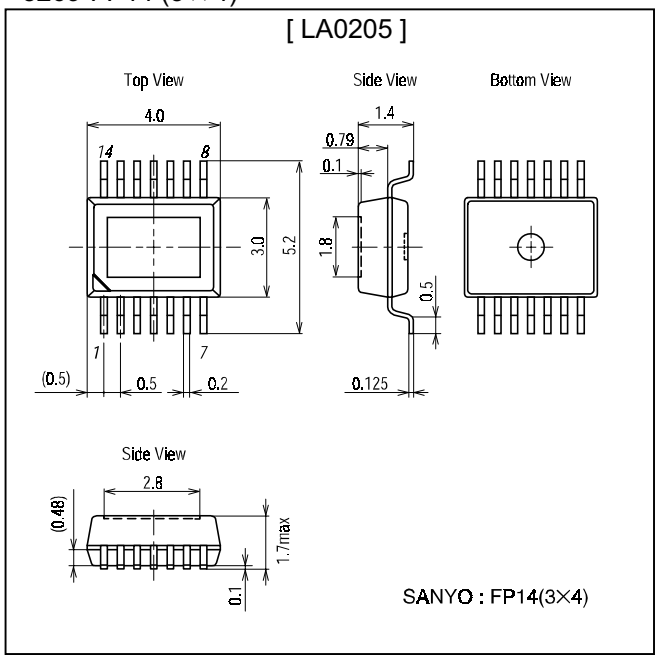
Functions

- Integrates 8-division PIN photodiode and amplifier circuit. onto a single chip.
- Built-in clipping limiter circuit.
- I/V converter amplifier.

Package Dimensions

unit: mm

3269-FP14 (3 × 4)



Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		7	V
Allowable power dissipation	Pd max	Ta ≤ 70°C With a flexible substrate for pick-up Size: 15.4 × 3.8 × 1.0t mm	125	mW
Operating temperature	Topr		-10 to +70	°C
Storage temperature	Tstg		-40 to +85	°C

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Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Ratings	Unit
Recommended supply voltage	V_{CC}	5.0	V
Operating supply voltage range	Vccopg	4.5 to 5.5	V
Recommended reference voltage	Vref	2.5	V
Reference voltage range	Vrefopg	2.0 to 2.8	V

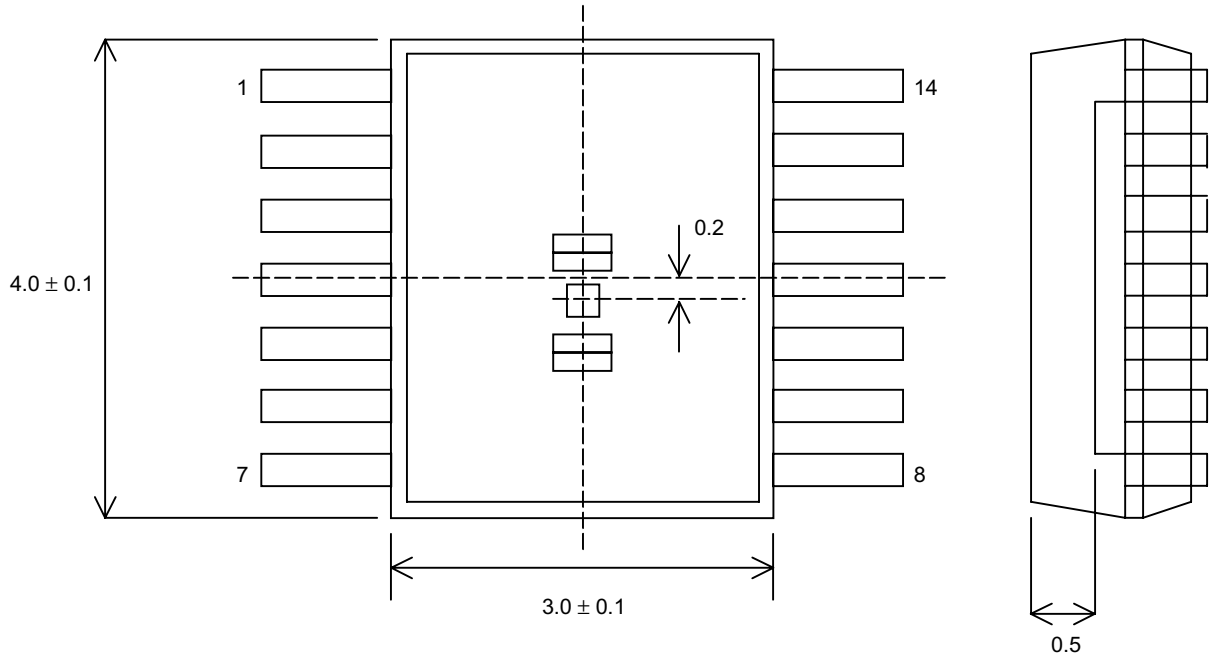
Optoelectronic Characteristics at Ta = 25°C, V_{CC} = 5 V, Vref = 2.5 V, RL = 4.7 kΩ, CL = 22 pF

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply current	I_{CCO}	With the light shaded	10	14	19	mA
Output voltage	VoAD	Pins A to D: PI=10 μW, λ=780 nm	64	80	96	mV
	VoEH	Pins E to H: PI=10 μW, λ=780 nm	160	200	240	mV
Output offset voltage	Vofset	Pins A to H: with the light shaded	-10	0	10	mV
Difference of offset voltage	ΔVofset	With the light shaded, (A+B)-(C+D)	-15	0	15	mV
		With the light shaded, (A+D)-(B+C)	-15	0	15	mV
		With the light shaded, (A+C)-(B+D)	-15	0	15	mV
		With the light shaded, (E+H)-(F+G)	-15	0	15	mV
Sum of output offset voltage	VofsetAD	Pins A to D: with the light shaded, A+B+C+D	-20	0	20	mV
	VofsetEH	Pins E to H: with the light shaded, E+F+G+H	-22	0	22	mV
Output offset / reference voltage fluctuation	VofsfAD	Pins A to D: output offset fluctuation when the voltage is increased by +100 mV to the Vref of 2.5 V		-0.3		mV
	VofsfEH	Pins E to H: output offset fluctuation when the voltage is increased by +100 mV to the Vref of 2.5 V		-0.6		mV
Limiter voltage	Vlimit	Pins A to D: PI=300 μW, λ=780 nm	3.8	4.1		V
	Vlimit	Pins E to H: PI=100 μW, λ=780 nm	3.8	4.1		V
Frequency characteristics	FcAD	Pins A to D: λ=780 nm, -3dB points for 100 KHz	45	65		MHz
	FcEH	Pins E to H: λ=780 nm, -3dB points for 100 KHz	15	25		MHz
Group delay deviation	ΔGd	Pins A to D: 100 KHz to 23 MHz		1.5	2	ns
Settling time	TsetAD5	Pins A to D: output 1.8 V to 18 mV			50	ns
	TsetAD8	Pins A to D: output 1.8 V to 1.8 mV			80	ns
	TsetEH	Pins R to H: output 1.8 V to 18 mV			50	ns
Output noise level	VnAD	Pins A to D: F=23 MHz, RBW=30 KHz		-90	-85	dBm
Output impedance	RoAD	Pins A to D		100		Ω
	RoEH	Pins E to H		125		Ω

Note: 1. Output voltage and output offset voltage are referenced to Vref.
2. Limiter voltage is referenced to GND.
3. Output voltage, frequency characteristics, group delay, settling time, output noise voltage, and output impedance are design confirmation values.

Photo Diode Layout

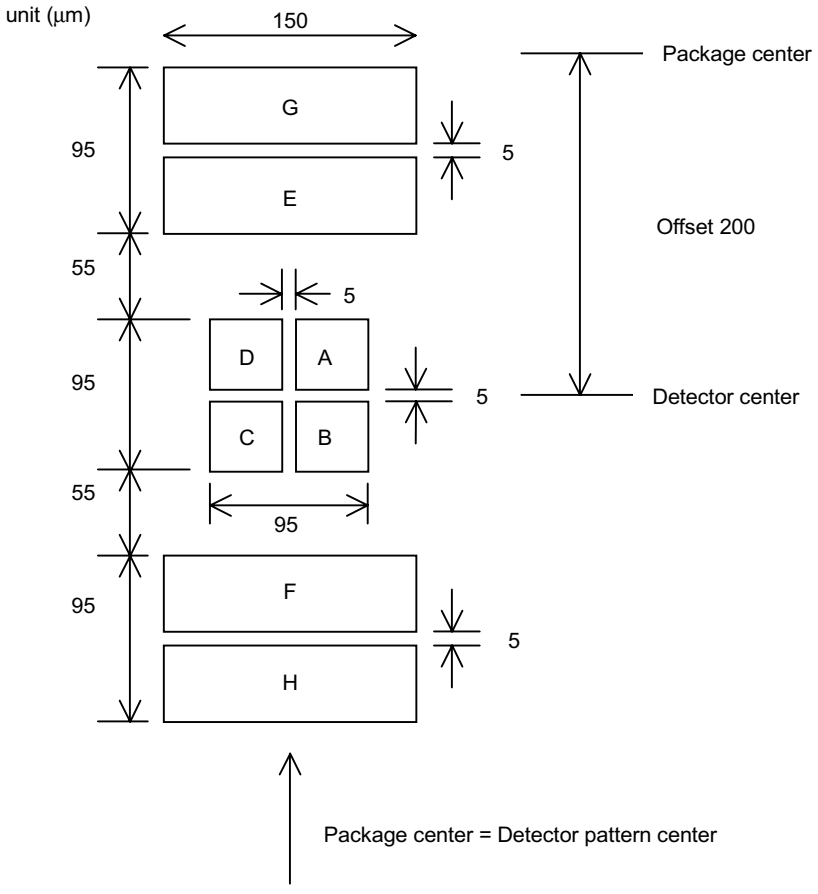
unit (mm)



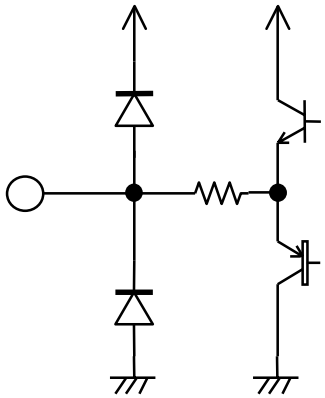
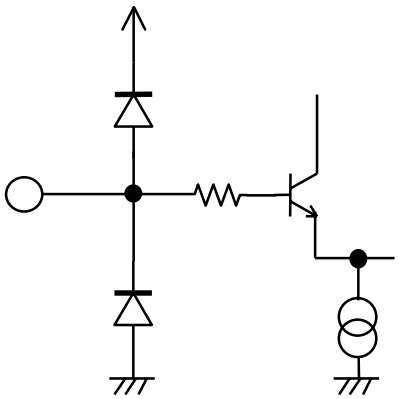
The tolerance between the package center and the detector pattern center :

X,Y direction ± 0.2 max
Z direction ± 0.2 max

Detecting Pattern of Photo Diode



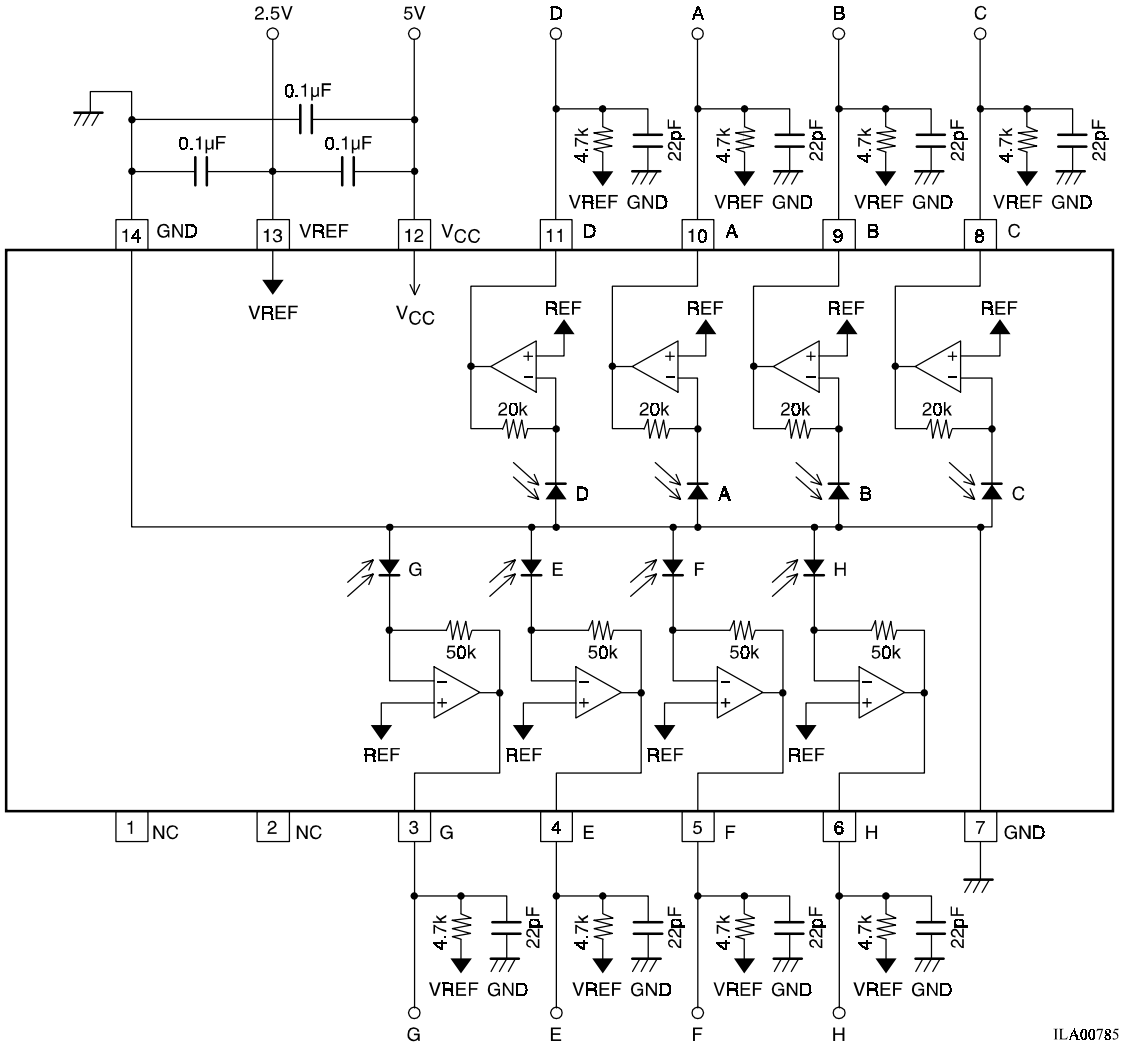
Pin Description

Pin no.	Pin name	Equivalent circuit	Note
1 2	NC NC		No connection pins
3 4 5 6 8 9 10 11	G E F H C B A D		Output pins for each photo-diode
12	V_{CC}		
13	Vref		Vref pin. This pin has no internal circuit to generate voltage. Therefore, external supply of voltage and about 20 μA current (up to 50 μA) as a differential amplifier base current is required.
7, 14	GND		

Package Material Characteristics

Parameter	Reference values
Penetration efficiency	97.0% at 1.0 mmt, 780 nm
Refractive index	1.57 using Abbe technique

Block Diagram and Test Circuit Diagram



Package: FP-14 (3 × 4)

Notes: 1. Place the 0.1- µF capacitors between V_{CC} pin and GND pin as close as possible to the pins.
2. The values of 22 pF capacitance and 4.7 kΩ resistance for output pins are test circuit load conditions.