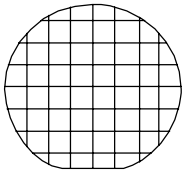
L9377

DUAL INTELLIGENT POWER LOW SIDE SWITCH

- DUAL POWER LOW SIDE DRIVER WITH 2 x 5A
- LOW R_{DSON} TYPICALLY 200mΩ @ T_J = 25°C
- INTERNAL OUTPUT CLAMPING DIODES V_{FB}=50V FOR INDUCTIVE RECIRCULATION
- LIMITED OUTPUT VOLTAGE SLEW RATE FOR LOW EMI
- µP COMPATIBLE ENABLE AND INPUT
- WIDE OPERATING SUPPLY VOLTAGE RANGE 4.5V TO 45V
- REAL TIME DIAGNOSTIC FUNCTIONS:
  - OUTPUT SHORTED TO GND
  - OUTPUT SHORTED TO VSS
  - OPEN LOAD
  - LOAD BYPASS
- DEVICE PROTECTION FUNCTIONS:
  - OVERLOAD DISABLE
  - REVERSE BATTERY UP TO -16V @ V_S
  - THERMAL SHUTDOWN

MULTIPOWER BCD TECHNOLOGY



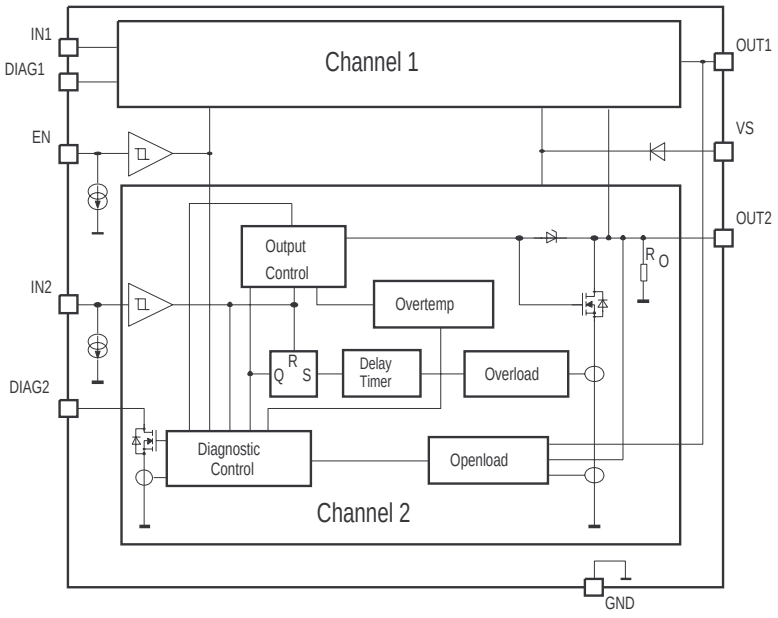
DIE

ORDERING NUMBER: L9377DIE1

DESCRIPTION

The L9377 is a monolithic integrated dual low side driver realized in an advanced Multipower-BCD mixed technology. It is especially intended to drive valves in automotive environment. Its inputs are µP compatible for easy driving. Particular care has been taken to protect the device against failures, to avoid electro-magnetic interferences and to offer extensive real time diagnostic.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (no damage or latch)

Symbol	Parameter	Value	Unit
VS_{DC}	DC supply voltage	-16 to 45	V
VS_{TR}	Transient supply voltage ($t \leq 500ms$)	60	V
$V_{IN,EN}$	Input voltage ($\| \leq \| 10mA \|$)	-1.5 to 6	V
VD_{DC}	Diagnostic DC output voltage ($\| \leq \| 50mA \|$)	-0.3 to 16	V
VO_{DC}	DC output voltage	45	V
VO_{TR}	Transient output voltage ($R_L \geq 4\Omega$)	60	V
I_O	Output load current	internal limited	
I_{OR}	Reverse output current limited by load	-4	A
EO	Switch-off energy for inductive loads (t_{EO} = 250µs, T = 5ms)	50	mJ
T_{jEO}	Junction temperature during switch-off $\sum t \leq 30min$ $\sum t \leq 15min$	175 190	°C °C
T_j	Junction temperature	-40 to +150	°C
T_a	Storage temperature	-55 to +150	°C
T_{jDIS}	Thermal disable junction temp, threshold	180 to 210	°C

ELECTRICAL CHARACTERISTICS (Operating Range) - The electrical characteristics are valid within the below defined operative range, unless otherwise specified.

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_S	Board supply voltage		4.5	12	32	V
V_D	Stabilized diagnostic output voltage		-0.3	5	16	V
T_{j1}	Junction Temperature		-40		150	°C
T_{j2}	Junction temperature $\sum t \leq 15min$ *)		150		210	°C

*) Parameter will be guaranted by correlation

Symbol	Parameter	Test Condition	Value T_{j1}			Value T_{j2}		Unit
			Min.	Typ.	Max.	Min.	Max.	
IS_{SB}	Static standby supply current	b) c) V_{EN} = L, VO ≥ VO_{UV}		0.73	1.5 15			mA mA
IS	DC supply current	b) c) $V_{EN} = V_{IN}$ = H		1.3	5 15			mA mA
VD_L	Diagnostic ouput low voltage	b) I_D = 2mA c) I_D = 1mA		0.35	0.5		0.7	V
ID_{LE}	Diagnostic output leakage current	VS = 0V or VS = open; VD = 5.5V $T_j \leq 125°C$		0.1	2		20	µA
ID	Diagnostic output current capability	VD ≤ 16V DIAG = L	2	6	30			mA
VO_{UV}	Open load voltage threshold	V_{EN} = X, V_{IN} = L	0.51 x VS	0.55 x VS	0.59 x VS	0.5 x VS	0.65 x VS	V
$\Delta VO_{UV1,2}$	Open load difference voltage threshold	b) VEN = X, VIN1,2 = L 16V ≥ VO_C ≥ VO_{UV} VO_C = output voltage of other channel c)	VO_C-0.9V VO_C-0.7V	VO_C-1.25V VO_C-1.25V	VO_C-1.6V VO_C-1.8V	0.8	1.7	V[1)] V
IO_{UC}	Open load current threshold	a) $V_{EN} = V_{IN}$ = H c)	100 20	320	480		580	mA mA

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Value T_{j1}			Value T_{j2}		Unit
			Min.	Typ.	Max.	Min.	Max.	
IO_{OC}	Over load current threshold	b)	5	7		4		A
VO_{CL}	Output voltage during clamping	$IO_{CL} \geq 100mA$	45	52	60			V
$S_{ON,OFF}$	Output (fall, rise) slew rate	a) Fig. 2	200	1500	3200	200	3500	V/rms
R_{IO}	Internal output pull down resistor	V_{EN} = L	10	20	40		50	KΩ
R_{DSON}	Output on resistance	VS > 9.5V IO = 2A T_j = 25°C; T_j = 150°C		200	300 500			mΩ mΩ
$V_{(EN,IN)L}$	Logic input low voltage	$\|I_{EN, IN}\| \leq 10mA$	-1.5		1		0.8	V
$V_{(EN,IN)H}$	Logic input high voltage		2		5.5			V
$V_{(EN,IN)hys}$	Logic input hysteresis		0.2	0.4	0.8			V
I_{EN}	Enable input sink current	$1V \leq V_{EN} \leq 5.5V$	10	30	60		80	µA
I_{IN}	Logic input sink current	$1V \leq V_{IN} \leq 5.5V$	40	95	180		240	µA
$t_{D\ ON}$	Output delay ON time	Fig. 2		4	25			µs
$t_{D\ OFF}$	Output delay OFF time		5	15	30			µs
$t_{D\ H-L,\ Diag.}$	Diag. delay output OFF time		5		65		90	µs
$t_{D\ IOu}$	Diagnostic open load delay time	Fig. 4		8	50			µs
t_{DOL}	Diagnostic overload delay switch-off time	Fig. 1	50	160	300			µs

a) $9V \leq V_S \leq 16V$ (Nominal operating range)
$R_L \leq 6\Omega$,
$I_O \leq IO_{OC}$
b) $6.5V \leq V_S \leq 16V$ (Diagnostic operation range)
c) $4.5V \leq V_S < 6.5V$ and $16V < V_S \leq 32V$ (Extended operation range)
1) Limit under evaluation.

DIAGNOSTIC TABLE (Operating range: $4.5V \leq V_S \leq 32V$)

Conditions		EN	IN	Out	Diag.
Normal function		L H H	X L H	off off on (*)	L L H
GND short	$VO_{typ} < 0.55V$	L	X	off	H
Load bypass	$VO_{1,2} \geq 1.25V$	H	L	off	H
Open load	$IO_{typ} < 320mA$	H	H	on (*)	L
$T_{j\ typ} \geq 175°C$ Overtemperature (**)		X X	L H	off off	H L
Latched Over load $IO_{min} > 5A$		X	H	off	L
Reset over load latch		X	↘	D.C.	D.C.

(*) for $4.5V \leq VS < 6.5V$, $IO \leq 2A$ diag. table is valid.

(**) If one diag. status shows the overtemp. recognition, in parallel this output will be switched OFF internally. The corresponding channel should be switched OFF additional by its Input or ENABLE signal, otherwise the overload latch will be set after t_{DOL} is passed. This behaviour will be related to the overdrop sensing which will be used as over load recognition.

Figure 1: Diagnostic overload delay time

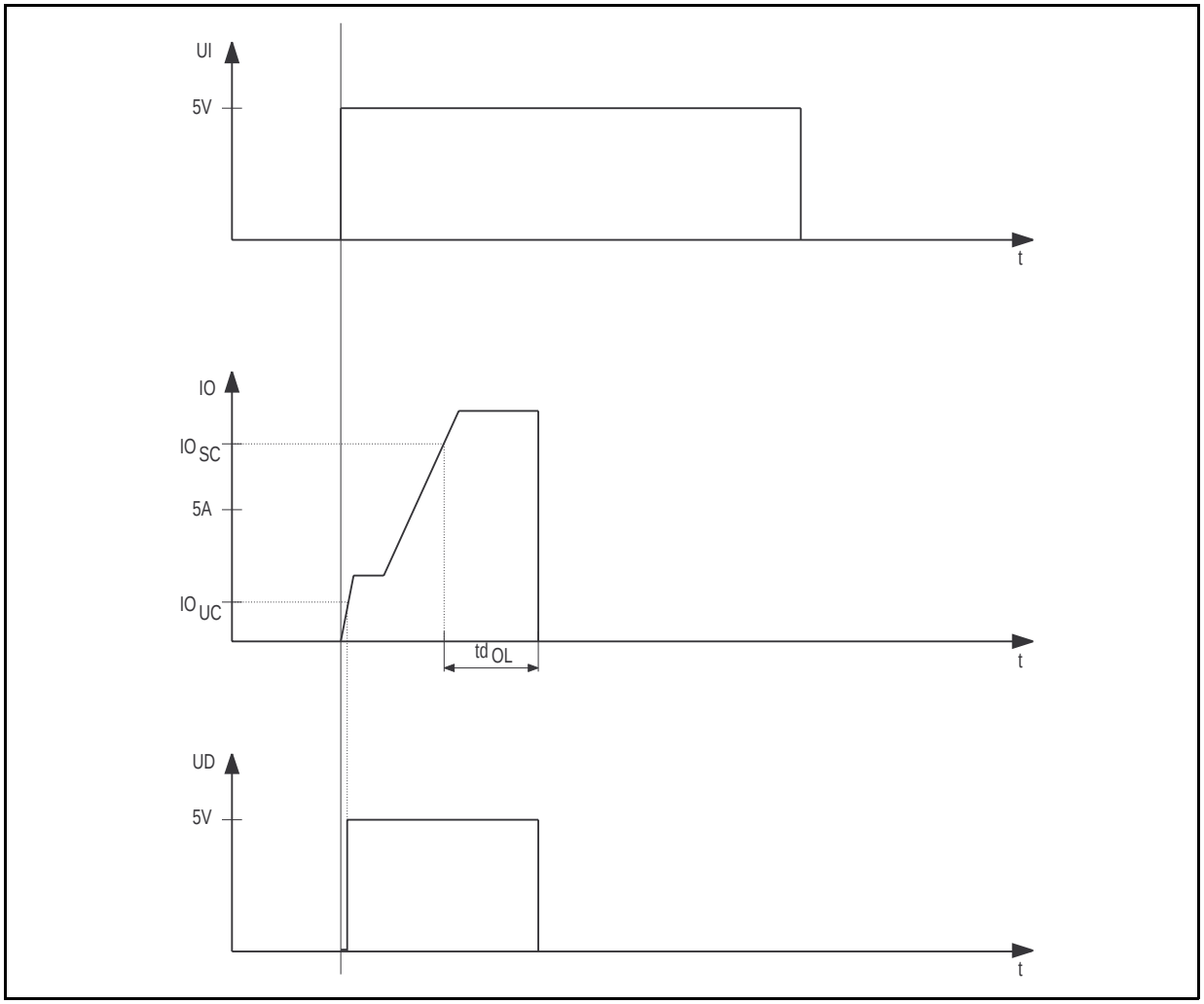


Figure 2: Output slope.

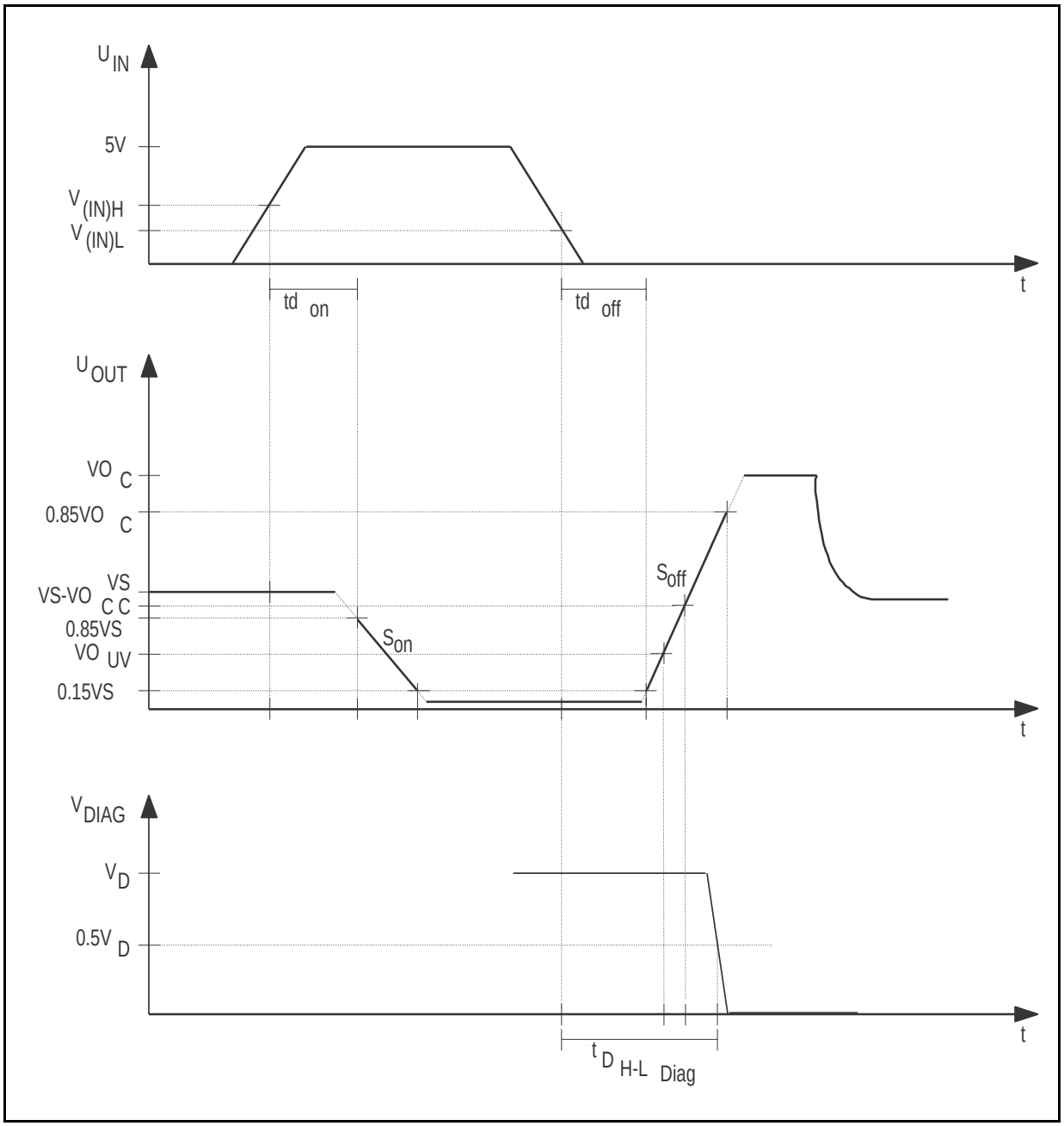


Figure 3: Block diagram - Open load voltage detection.

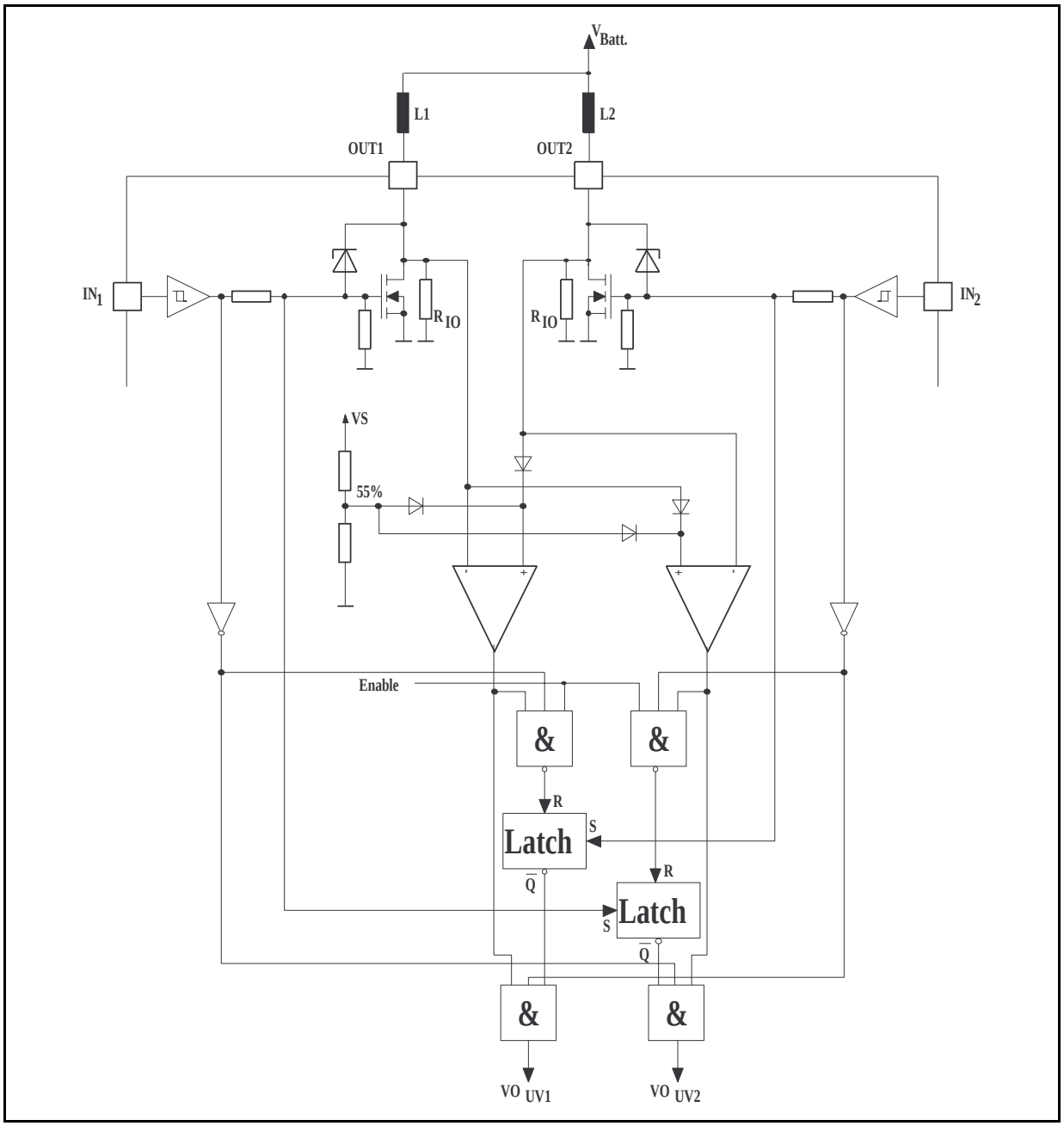
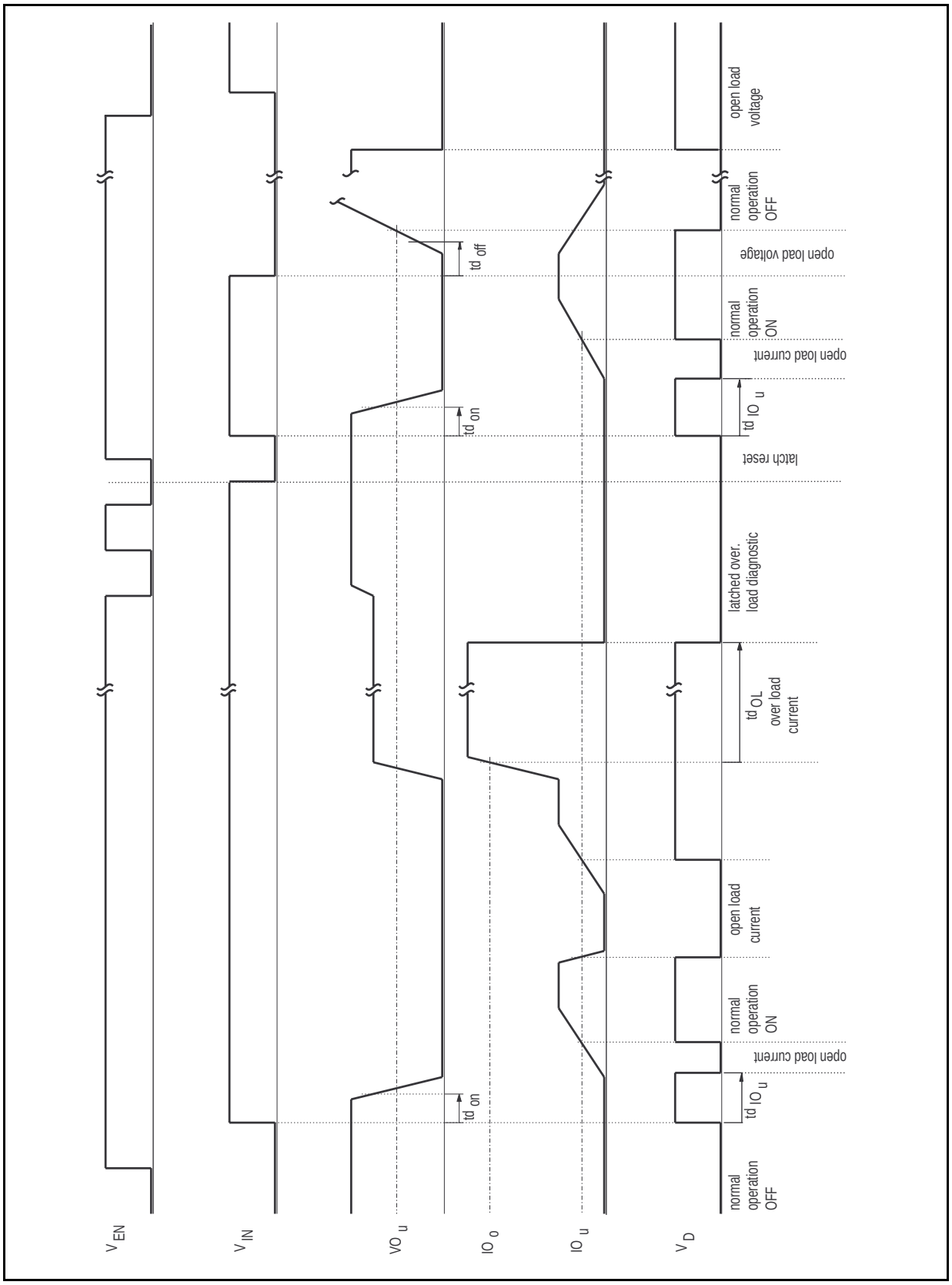


Figure 4: Logic diagram.



CIRCUIT DESCRIPTION

The L9377 is a dual low side driver for inductive loads like valves in automotive environment. The device is enabled by a common CMOS compatible ENABLE high signal. The internal pull down current sources at the ENABLE and INPUT pins protect the device in open input conditions against malfunctions. An output slope limitation for du/dt is implemented to reduce the EMI. An integrated active flyback voltage limitation clamps the output voltage during the flyback phase to 50V.

Each driver is protected against short circuit and thermal overload. In short circuit condition the output will be disabled after a short delay time t_{DOL} to suppress spikes. This disable is latched until a negative slope occure at the correspondent input pin. The thermal disable for $T_J > 175°C$ of the output will be reseted if the junction temperature decreases about 20°C below the disable threshold temperature.

For the real time error diagnosis the voltage and the current of the outputs are compared with internal fixed values VO_{UV} for OFF and IO_{UC} for ON conditions to recognize open load ($R_L \geq 20K\Omega$, $R_L > 38\Omega$) in ON and OFF conditions. The diagnostic operates also in the extended supply voltage range of $4.5V \leq VS \leq 32V$.

Also the output voltages $VO_{1,2}$ are compared against each other in OFF condition with a fixed offset of $\Delta VO_{UV\ 1,2}$ to recognize GND bypasses. To suppress mail ΔVO diagnoses during the flyback phases of the compared output, the ΔVO diagnostic includes a latch function. Reaching the flyback clamping voltage VO_C the diagnostic signal is reseted by a latch. To activate again this kind of diagnostic a low signal at the correspondent INPUT or the ENABLE pin must occur (see also Fig.3).

The diagnostic output level in connection with different ENABLE and INPUT conditions allows to recognize different fail states, like overtemp, short to VSS, short to GND, bypass to GND and disconnected load (see also page 7 diagnostic table).

The diagnostic output is also protected against short to UD_{max}. Oversteping the over load current threshold IO_o, the output current will be limited internally during the diagnostic overload delay switch-off time t_{DOL}.

Figure 5: Application circuit diagram.