SGS-THOMSON MICROELECTRONICS

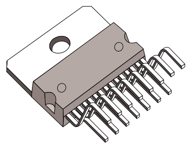
L9341

QUAD LOW SIDE DRIVER

AVANCE DATA

- DU/DT AND DI/DT CONTROL
- PWM CONTROLLED OUTPUT CURRENT
- SHORT CURRENT PROTECTION AND DIAGNOSTIC
- INTEGRATED FLYBACK DIODE
- UNDERVOLTAGE SHUTDOWN
- OVERVOLTAGE AND UNDERVOLTAGE DIAGNOSTIC
- OVERTEMPERATURE DIAGNOSTIC

MULTIPOWER BCD TECHNOLOGY



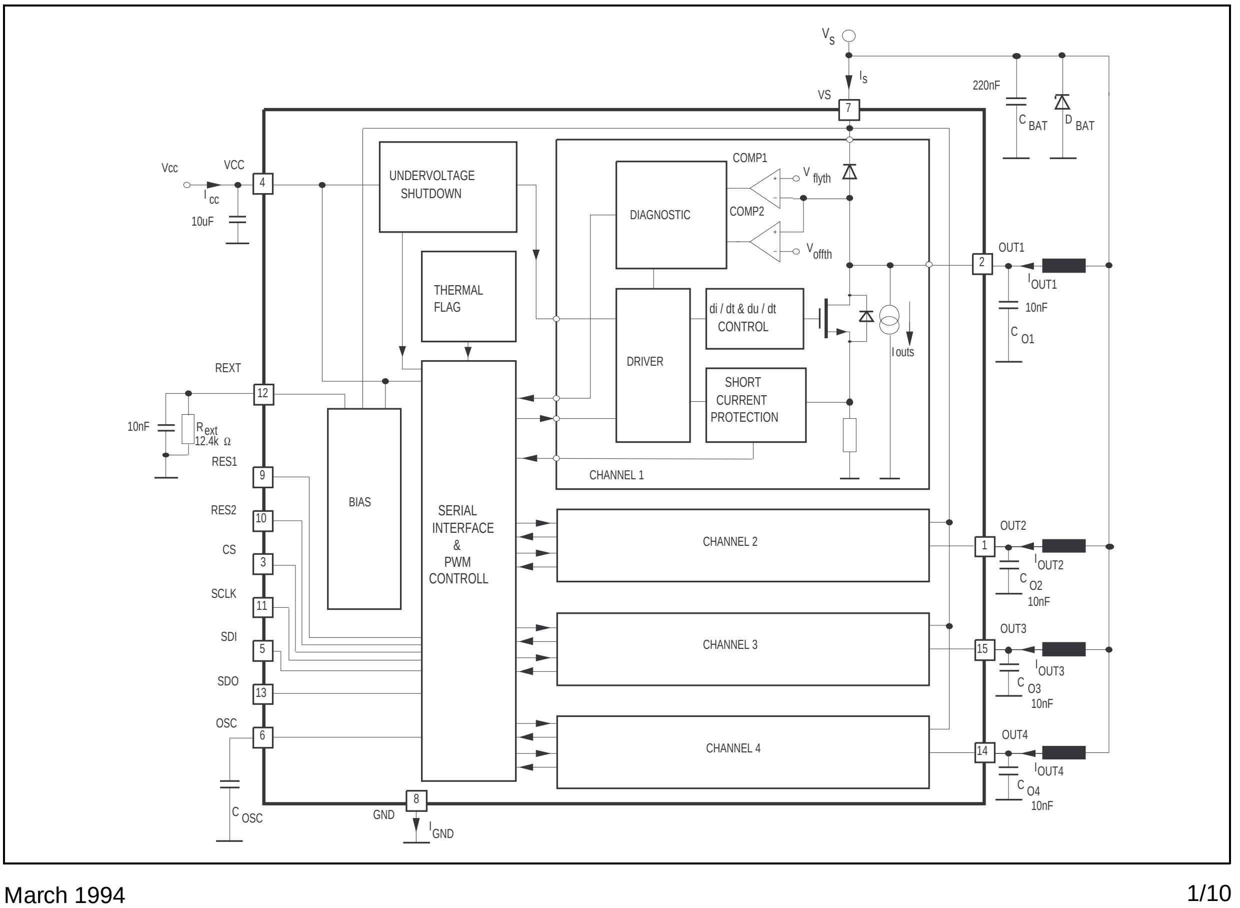
Multiwatt 15

ORDERING NUMBERS: L9341V
L9341H

DESCRIPTION

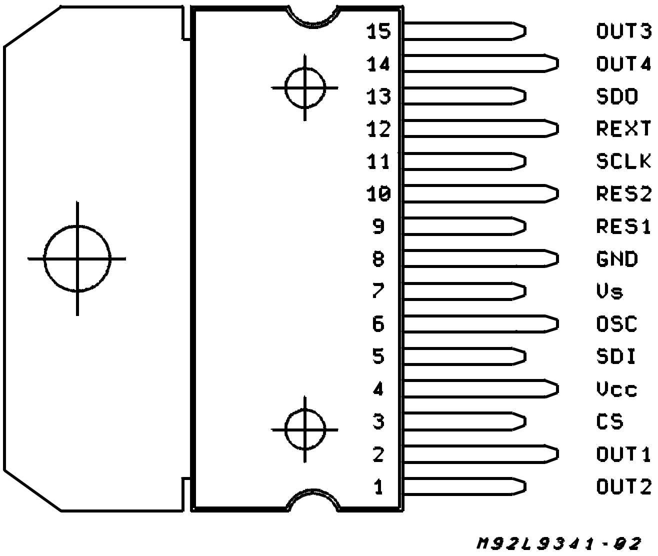
The L9341 is a monolithic integrated circuit realized in Multipower BCD-II mixed technology. The driver is intended for inductive loads in synchronous PWM applications, especially for valve drivers. The output voltage and current rise and fall slopes du/dt and di/dt are controlled.

BLOCK & APPLICATION DIAGRAM



This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

PIN CONNECTION (Top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	V_{CC} Voltage Range	-0.3 to 6	V
V_S	V_S Voltage Range	-0.3 to 24	V
V_{spmax}	VS Voltage Range for t ≤ 400ms	-2 to 40	V
V_{st}	Schaffner Transient Pulses on V_S	see note 1	V
Vin	Input Voltage Range for SDI; SCLK;CS;RES1;RES2	-0.3to V_{CC}+0.3	
V_{out}	Output Voltage Range for all Outputs: Negative Positive	 – 0.3 intern. clamped to V_S	 V V
I_{out}	Output Current for all Outputs: Negative Positive	 – 2 + 2	 A A
	for Transient with t < 10ms Negative Positive	 – 5 5	 A A
	Schaffner Transient Pulses on Output	see note 2	
V_{ESD}	ESD Voltage Capability (MIL 883 C)	1500	V

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance Junction to Case	3	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction to Ambient mounted on PC Board	35	°C/W
T_{sdh}	Thermal Hysteresis	20	°C
T_{sd}	Thermal Diagnostic	T_j > 150	°C

Notes:
1. Schaffner transient specification: DIN 40839 test waveforms of the following type: 1, 2, 3a, 3b, 5 and 6.
The pulses are applied to the application circuit according to fig. 3.

2. The maximum output current results from the Schaffner pulses specified in note 1.

ELECTRICAL CHARACTERISTICS (Unless otherwise specified: 8V ≤ V_S ≤ 24V; 4.7V ≤ V_{CC} ≤ 5.3V; –40 °C ≤ Tj ≤ 150°C; $\overline{I_O}$ ≤ 1A (note 3); I_O ≤ 1.5A; V_{sp} = V_S for t ≤ 400ms; V_{OUTP} = V_{OUT} for t ≤ 400ms; R_{ext} = 12.4KΩ ± 1%).

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{ccq}	V_{cc} Quiescent Current	All Outputs Off		1	3	mA
I_{sq}	V_s Quiescent Current	All Outputs Off		14	25	mA
V_{ccu}	V_{cc} Undervoltage Threshold	See Note 4	3	4	4.7	V
V_{ccr}	V_{cc} Range for RES1 and RES2 Operation		3			V
R_{on}	On Resistance	I_o = 1A T_j = 125°C T_j = 25°C			750 450	mΩ mΩ
$I_{o\ off}$	Off State Output Current	Outputs Off 1.4V ≤ V_o ≤ V_s V_{outp} = V_{sp} = 40V	 1 1	 2.5	 4 10	 mA mA
V_{outf}	Output Voltage During Flyback	I_o = 1A Output Off T_j = 25°C T_j = 125°C			 V_s +1.3 V_s +1.1	 V V
I_{gndf}	Current to GND during Flyback (see note 5)	I_o = 1A Output Off V_s = 24V V_{sp} = 40V		 17 20	 44 52	 mA mA
I_{outr}	Reverse Leakage Current	V_{sp} - V_o = 40V			500	µA
V_{inH}	High Input Level of SCLK, SDI, CS, RES1, RES2		0.7*V_{cc}		V_{cc}+0.3	V
V_{inL}	Low Input Level of SCLK, SDI, CS, RES1, RES2		– 0.3		0.3*Vcc	V
V_{REShys}	Hysteresis of Reset Inputs RES1, RES2		0.3		1	V
I_{inRESH}	Input Current on RES1,RES2	RES_i = H; -2V ≤ V_{sp} ≤ 8V RES_i = H; 8V ≤ V_{sp} ≤ 40V	– 10 5		10 10	µA µA
I_{in}	Input Current on SCLK,SDI,CS	– 2V ≤ Vsp ≤ 40V	– 10		10	µA
V_{SDOH}	High Level SDO Output Voltage	I_{SDO} = -1mA -2V ≤ V_{sp} ≤ 40V	0.9*V_{cc}		V_{cc}	V
V_{SDOL}	Low Level SDO Output Voltage	I_{SDO} = 1mA -2V ≤ V_{sp} ≤ 40V	0		0.4	V
I_{SDOZ}	SDO Tristate High-Z Leakage Current	0 ≤ V_{SDO} ≤ V_{cc} – 2V ≤ V_{sp} ≤ 40V	– 10		10	µA
PWM_{duty}	PWM Duty Cycle		1/16		15/16	
K_f	Frequency Accuracy Constant	See Note 6	0.93*K_{fn}	K_{fn}	1.07*K_{fn}	
V_{flyth}	Flyback Diagnostic Comparator Threshold	40 ≥ V_{sp} ≥ 8V V_s ≤ 8V	V_s – 1 1.5		V_s – 0.4	V V
V_{offth}	Off State Diagnostic Comparator Threshold		1.5		2	V
I_{outl}	Output Current Limitation Threshold	see Note 7	1.5		2.5	A
t_{dpo}	Delay Time PWM Signal to Out.		5		15	µs
S_{ov}	Output Voltage Rise and Fall Slope | du/dt |	(from 10 to 90% of V_o) Fig. 2	1.0		10	V/µs
S_{oc}	Output Current Rise and Fall Slope |di/dt|	0.1 ≤ Io ≤ 1.5A (from 10 to 90% of I_o)	25		125	mA/µs

Notes:

3. The mean value is $I_o = \frac{1}{T}\int_0^T I_o(t)\,dt$;

4. The outputs are switced off for Vcc ≤ Vccu. The logic is not reseted. For a reset, RES1 or RES2 must be used.

5. This current is measured in the GND - terminal when one single output is in flyback and consists of the supply current added to the value of the output current source and the leakage current of the flyback diode. This leakage current is less than 1% of the nominal flyback current.

6. The PWM frequency is defined by an external capacitor. The PWM oscillator frequency is: $f_{pwm} = \frac{f_{osc}}{32}$ with $f_{osc} = \frac{K_f}{C_{osc}} \cdot 1A/V$ and $k_{in} = 15 \cdot 10^{-6}$; the range is: 300Hz ≤ f_{pwm} ≤ 3000Hz. The OSC Pin can be alternatively driven by an external TTL / CMOS signal.

7. For $I_{out} \geq I_{outl}$ an internal comparator switches the corresponding output off for the current PWM cycle.

Figure 1: Logic Diagram of PWM Generation.

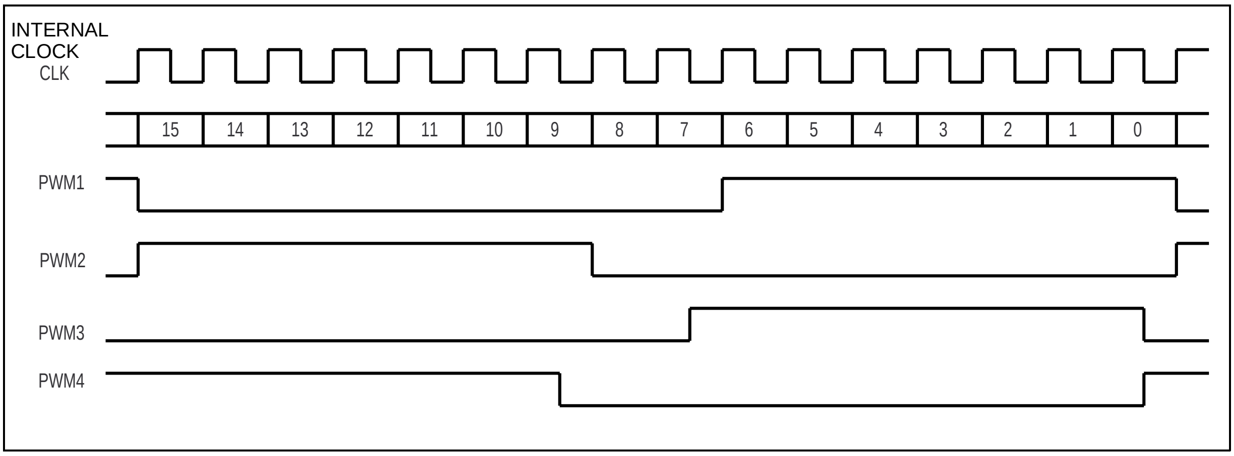


Figure 2: Output Switching Diagram.

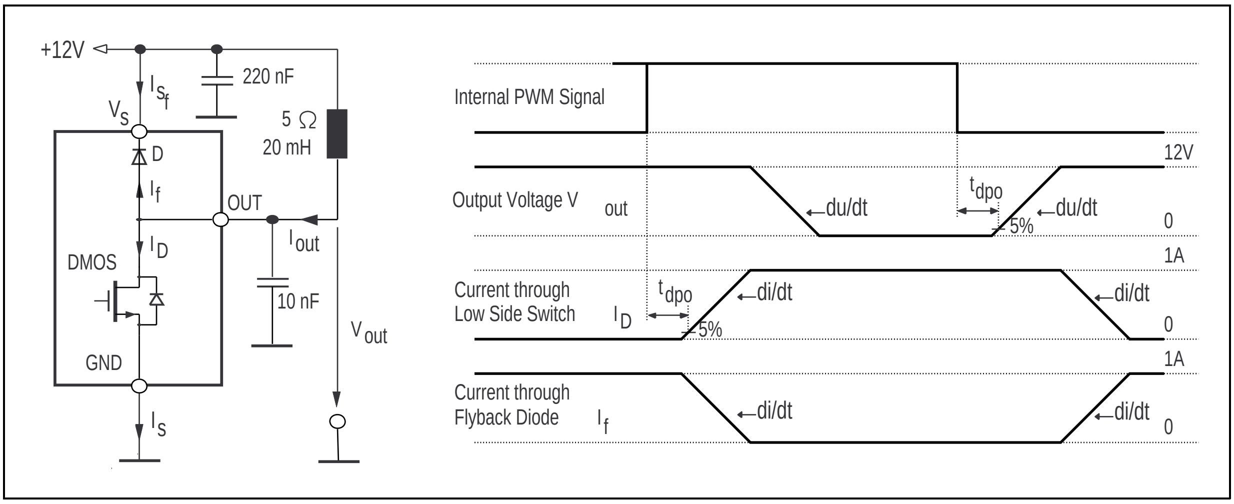


Figure 3: Test Circuit for Schaffner Pulses.

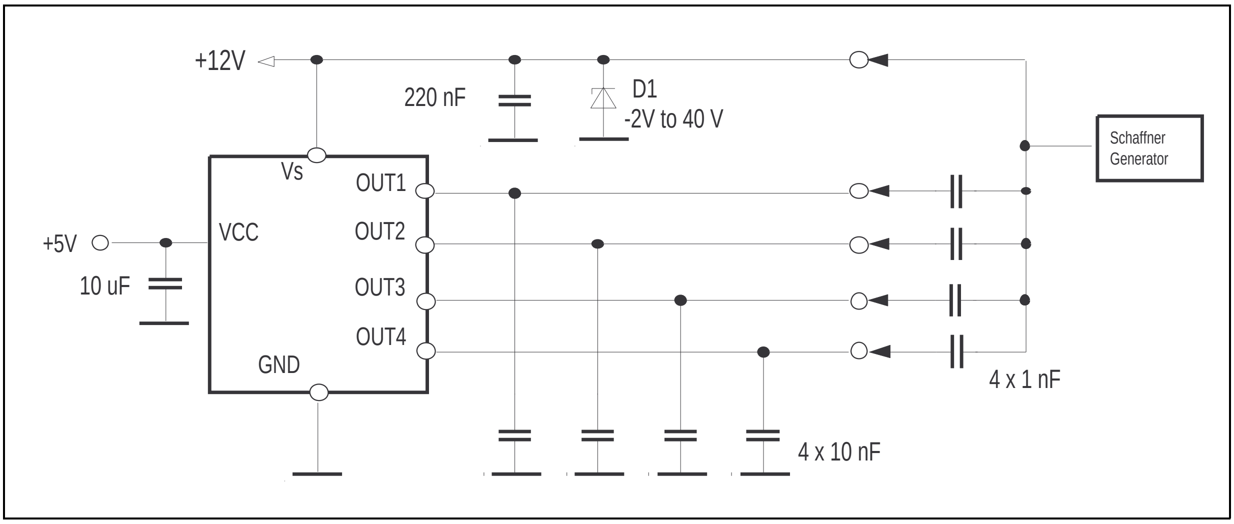
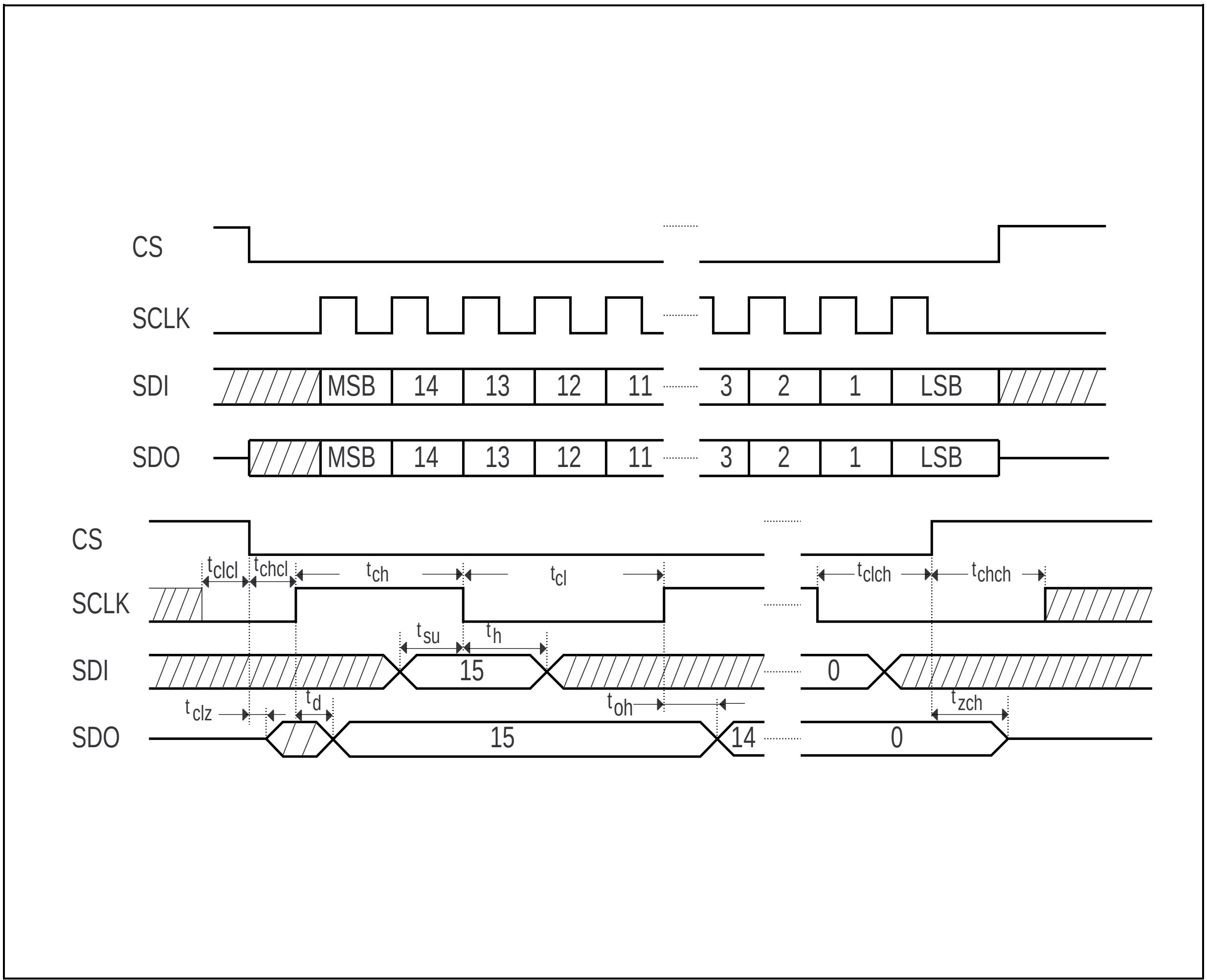


Figure 4: Synchronous Serial Interface Protocol.



f_{clock}	Clock Frequency	min. DC	max. 2MHz
t_{ch}	Width of Clock Input High Puls	min. 200ns	
t_{cl}	Widh of Clock Input Low Puls	min. 200ns	
t_{cicl}	Clock Low Before CS Low	min. 200ns	
t_{chcl}	Clock High After CS Low	min. 200ns	
t_{clch}	Clock Low Before CS High	min. 200ns	
t_{chch}	Clock High After CS High	min. 200ns	
t_{ciz}	SDO Low-Z CS Low	min. 0ns	max. 400ns
t_{zch}	SDO High-Z CS High		max. 400ns
t_{su}	SDI Input Setup Time	min. 80ns	
t_h	SDI Input Hold Time	min. 80ns	
t_d	SDO Output Delay Time (C_L = 50pF)		max. 100ns
t_{oh}	SDO Output Hold Time	min. 0ns	

Figure 5: PWM Generation Function Table.

Bit 3 - 0	PWM1	PWM2	PWM3	PWM4	OUTPUT
0000	15/16	15/16	15/16	15/16	OFF
0001	1/16	15/16	1/16	15/16	ON
0010	2/16	14/16	2/16	14/16	ON
0011	3/16	13/16	3/16	13/16	ON
0100	4/16	12/16	4/16	12/16	ON
0101	5/16	11/16	5/16	11/16	ON
0110	6/16	10/16	6/16	10/16	ON
0111	7/16	9/16	7/16	9/16	ON
1000	8/16	8/16	8/16	8/16	ON
1001	9/16	7/16	9/16	7/16	ON
1010	10/16	6/16	10/16	6/16	ON
1011	11/16	5/16	11/16	5/16	ON
1100	12/16	4/16	12/16	4/16	ON
1101	13/16	3/16	13/16	3/16	ON
1110	14/16	2/16	14/16	2/16	ON
1111	15/16	1/16	15/16	1/16	ON

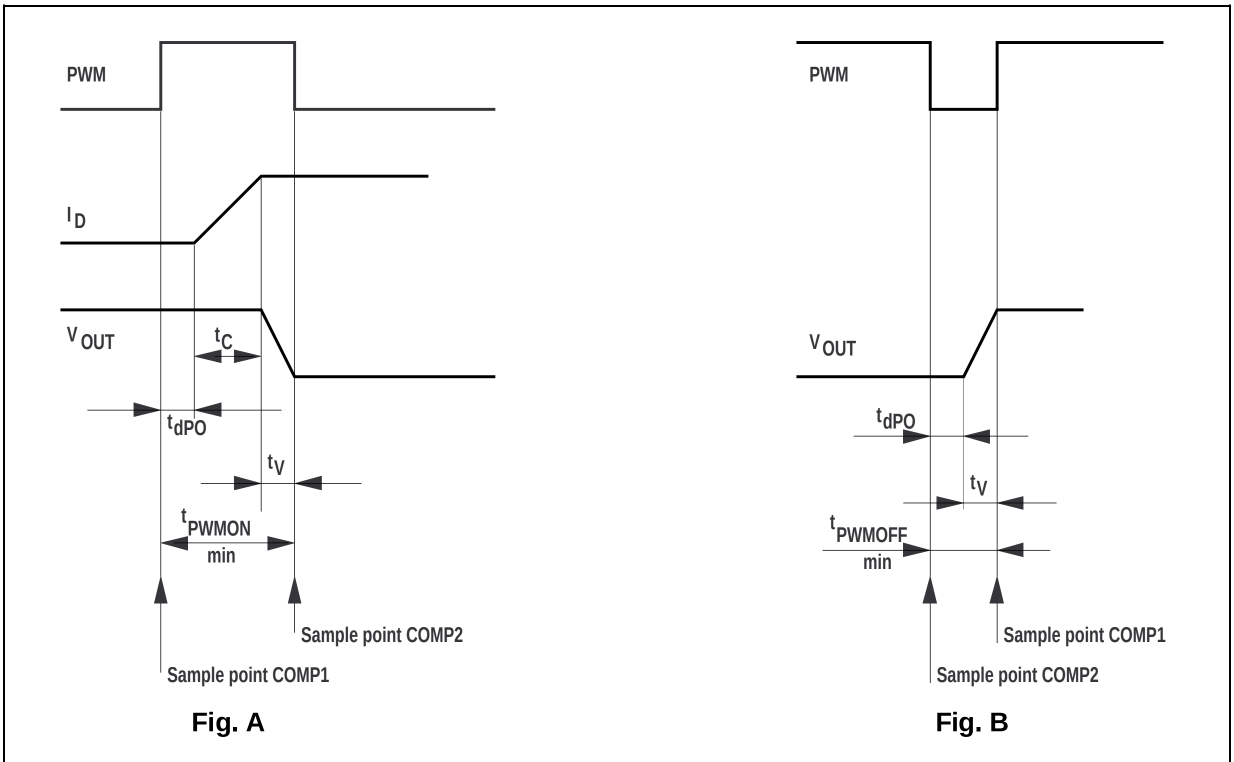
Figure 6: PWM Information From Microcontroller to QLSD.

Bit. Nr.	Name	Contents
0	P10	PWM Duty Cycle for Channel 1 / Bit 0: LSB
1	P11	PWM Duty Cycle for Channel 1 / Bit 1
2	P12	PWM Duty Cycle for Channel 1 / Bit 2
3	P13	PWM Duty Cycle for Channel 1 / Bit 3 : MSB
4	P20	PWM Duty Cycle for Channel 2 / Bit 0 : LSB
5	P21	PWM Duty Cycle for Channel 2 / Bit 1 :
6	P22	PWM Duty Cycle for Channel 2 / Bit 2 :
7	P23	PWM Duty Cycle for Channel 2 / Bit 3 : MSB
8	P30	PWM Duty Cycle for Channel 3 / Bit 0 : LSB
9	P31	PWM Duty Cycle for Channel 3 / Bit 1 :
10	P32	PWM Duty Cycle for Channel 3 / Bit 2 :
11	P33	PWM Duty Cycle for Channel 3 / Bit 3 : MSB
12	P40	PWM Duty Cycle for Channel 4 / Bit 0 : LSB
13	P41	PWM Duty Cycle for Channel 4 / Bit 1:
14	P42	PWM Duty Cycle for Channel 4 / Bit 2 :
15	P43	PWM Duty Cycle for Channel 4 / Bit 3 : MSB

Figure 7: Diagnostic Information from QLSD to Microcontroller.

Bit Nr.	Name	Contents
0	F11	COMP1 State at Positive Edge of PWM1 (0: $V_{out1} > V_{flyth}$; 1: $V_{out1} < V_{flyth}$)
1	F12	COMP2 State at Negative Edge of PWM1 (1: $V_{out1} > V_{offth}$; 0 : $V_{out1} < V_{ofth}$)
2	F21	COMP1 State at Positive Edge of PWM2 (0: $V_{out2} > V_{flyth}$; 1: $V_{out2} < V_{flyth}$)
3	F22	COMP2 State at Negative Edge of PWM2 (1: $V_{out2} > V_{ofth}$; 0 : $V_{out2} < V_{ofth}$)
4	F31	COMP1 State at Positive Edge of PWM3 (0: $V_{out3} > V_{flyth}$; 1: $V_{out3} < V_{flyth}$)
5	F32	COMP2 State at Negative Edge of PWM3 (1: $V_{out3} > V_{offth}$; 0 : $V_{out3} < V_{ofth}$)
6	F41	COMP1 State at Positive Edge of PWM4 (0: $V_{out4} > V_{flyth}$; 1: $V_{out4} < V_{flyth}$)
7	F42	COMP2 State at Negative Edge of PWM4 (1: $V_{out4} > V_{offth}$; 0 : $V_{out4} < V_{ofth}$)
8	RES1	Logic State of RES1 Input (0: RES1 = L ; 1: RES1 = H)
9	RES2	Logic State of RES2 Input (0: RES2 = L ; 1: RES2 = H)
10	TSDF	Thermal Diagnostic Flag (0: Overtemperature ; 1:Normal)
11	C1	Current at Negative Edge of PWM1 (0: $I_{out} > I_{outl}$; 1: $I_{out} < I_{outl}$)
12	C2	Current at Negative Edge of PWM2 (0: $I_{out} > I_{outl}$; 1: $I_{out} < I_{outl}$)
13	C3	Current at Negative Edge of PWM3 (0: $I_{out} > I_{outl}$; 1: $I_{out} < I_{outl}$)
14	C4	Current at Negative Edge of PWM4 (0: $I_{out} > I_{outl}$; 1: $I_{out} < I_{outl}$)
15	1	Framing Information (always 1)

Figure 8.



Note:
For safty diagnostic take notice of the following conditions:

$t_{PWMON} \geq t_{dPOMAX} + t_C + t_V$ (see Fig. A) $\qquad t_C = \frac{I_D}{S_{OCMIN}} \qquad t_V = \frac{V_{outfmax}}{S_{OVMIN}}$

$t_{PWMOFF} \geq t_{dPOMAX} + t_V$ (see Fig. B)

FUNCTIONAL DESCRIPTION

The U511 is a PWM quad low side driver for inductive loads. The duty cycle of the internal generated PWM signal is set by a microcontroller via a serial interface for each output. An output slope limitation for both dv/dt and di /dt is implemented to reduce RFI. The PWM generation is realized avoiding a simultaneous output switching. As a result, di/dt becomes smaller. Integrated flyback diodes clamp the output voltage during the flyback phase of the low side switches.

The driver is protected against short circuit. An undervoltage shutdown circuit switches off all outputs if V_{cc} is less then V_{ccu}. Below the shutdown voltage all outputs remain in off state regardless of the input state. After each malfunction which resets the driver, only the serial link interface can reactivate the normal function. In case of overcurrent ($I_{out} = I_{out1}$), an internal comparator switches the output off. The overcurrent information can be read via the serial link for each driver separately at the negative edge of the corresponding PWM signal.

The interface to the microcontroller is realized with a 16 bit synchronous serial peripheral interface (SPI). If CS is switched low, the serial link becomes active and SDO goes to low impedance. At the rising edge of the SCLK signal, one of the 16 bit of data stored in a shift register appear sequencely at SDO. These data contain the 8 error flags, the status of thermal diagnostic flag and the external reset sources RES1, RES2 and the overcurrent flgs c1...c4. The last bit is framing information (see fig. 7). At each falling edge of SCLK, one of the 16 bits of data sent by the microcontroller is transferred via the SDI input to the driver. These data contain the duty-cycle information for the internal PWM generation (4 times 4 bit).

On the rising edge of CS the previously stored information is transferred to the circuits. SDO become now high impedance and SDI is inactive. The serial interface of the QLSD is cascadable with the serial link interface of another QLSD, thus obtaining a 32 bit serial link information wich can control eight inductive loads. For a safety data transfer the takeover of data bits is only realized when the number of SCLK - clocks is n x 16 ($n \geq 1$).

The PWM duty cycle is set by 4 bit for each output independently via the serial link. If all four bits for an output are zero, the output is turned off, but the error diagnosis will work correctly (see fig. 5 and 6). The PWM frequency is defined by an external capacitor on the OSC pin. Rext defines through the reference current the output current slope, the diagnostic current sink and the internal oscillator frequency (together with C_{osc}).

For error diagnosis the voltage on the output is measured during the on and off state of the particular output driver. Upon the rising edge of the PWM signal (at this moment the power output is off and will be switched on) the status of COMP1 is stored into an internal latch. On the falling edge of the PWM signal (the power output is on and will be switched off) the status of COMP2 is stored into another internal latch. This information can be read via the serial link for each output driver separately (see fig. 7).

The thermal diagnostic switch the thermal flag to 0 in case of overtemperature $T \geq T_{sd}$. It will be switched to 1 with the hysteresis T_{sdth} in case of $T < T_{sd} - T_{sdh}$.

To avoid male functions due to extensive noise or spikes at the supply pins V_{CC}, V_S and R_{ext} must be blocked externally via capacitors.

MULTIWATT15 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			5			0.197
B			2.65			0.104
C			1.6			0.063
D		1			0.039	
E	0.49		0.55	0.019		0.022
F	0.66		0.75	0.026		0.030
G	1.02	1.27	1.52	0.040	0.050	0.060
G1	17.53	17.78	18.03	0.690	0.700	0.710
H1	19.6			0.772		
H2			20.2			0.795
L	21.9	22.2	22.5	0.862	0.874	0.886
L1	21.7	22.1	22.5	0.854	0.870	0.886
L2	17.65		18.1	0.695		0.713
L3	17.25	17.5	17.75	0.679	0.689	0.699
L4	10.3	10.7	10.9	0.406	0.421	0.429
L7	2.65		2.9	0.104		0.114
M	4.25	4.55	4.85	0.167	0.179	0.191
M1	4.63	5.08	5.53	0.182	0.200	0.218
S	1.9		2.6	0.075		0.102
S1	1.9		2.6	0.075		0.102
Dia1	3.65		3.85	0.144		0.152