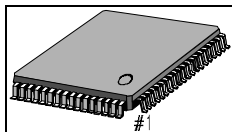
INTRODUCTION

100-QFP-1420D



S5L9231 is a CDP 1-chip LSI which includes the following components: CMOS RF, Digital Servo, CD-DSP, 1-bit DAC, and Audio Post-Filter. The RF signal from the pick-up is converted from current to voltage at the CMOS RF block. The RF signal, together with the Digital Servo block containing the built-in DSP core, carries out focus and tracking adjustments with H/W and S/W. The EFM signal from the CMOS RF block is made into a digital signal in the CD-DSP block, goes through the 1-bit DAC and Audio Post-Filter, then is output as a playback audio signal.

FEATURES

The S5L9231 has the following features:

- Digital Servo that interacts with both CD 1x and CD 2x
- Support to Read CD-RW (Rewritable) Disc
  - — Focus Servo
  - — Tracking Servo
  - — Sled Servo
  - — Spindle Servo
- Complete Automatic Adjustment
  - — Focus Offset Control
  - — Tracking Offset Control
  - — Focus Input Gain Control
  - — Tracking Input Gain Control
  - — Tracking Balance Control
  - — Focus Loop Gain Control
  - — Tracking Loop Gain Control
- Disc Detect (Focus Search)
- Drop Out and Shock countermeasure
- Built-in DSP
- Able to select the characteristics of various types of filters and internal coefficients by Micro Controller
- A digital filter for each servo loop resulting in a reduction of external parts
- A built-in 8/6-bit D/A Converter for Motor Drive and an 8-bit A/D Converter
- EFM Data Demodulation
- Built-in Frame Sync Detection, Protection, and Insertion circuits
- Subcode Data Serial output
- C1: 2 error correction, C2: 2 error, 4 erasure correction
- Interpolation
- CLV Servo Controller

- Built-in 16-bit Track Counter
- Micro Controller Interface
- Digital Audio Out
- ESP Interface
- Built-in Digital PLL
- Built-in 1-bit DAC & Audio Post-Filter
- 1x and 2x Play (L/R Channel output, Digital Output)
- CMOS RF
  - RF Summing Amplifier
  - Focus Error Amplifier
  - Tracking Error Amplifier
  - Automatic Focus Balance Adjustment
  - Automatic Tracking Balance Adjustment
  - Automatic Focus Gain Adjustment
  - Automatic Tracking Gain Adjustment
  - Envelope Detection Function
  - Defect Detection Function
  - Mirror Detection Function
  - Automatic Laser Diode Power Control Function
  - EFM Comparator Function
  - Anti-Shock Function
- 5V Single Power Supply

ORDERING INFORMATION

Device	Package	Operating Temperature
S5L9231	100-QFP-1420D	-20 °C — +75 °C

BLOCK DIAGRAM

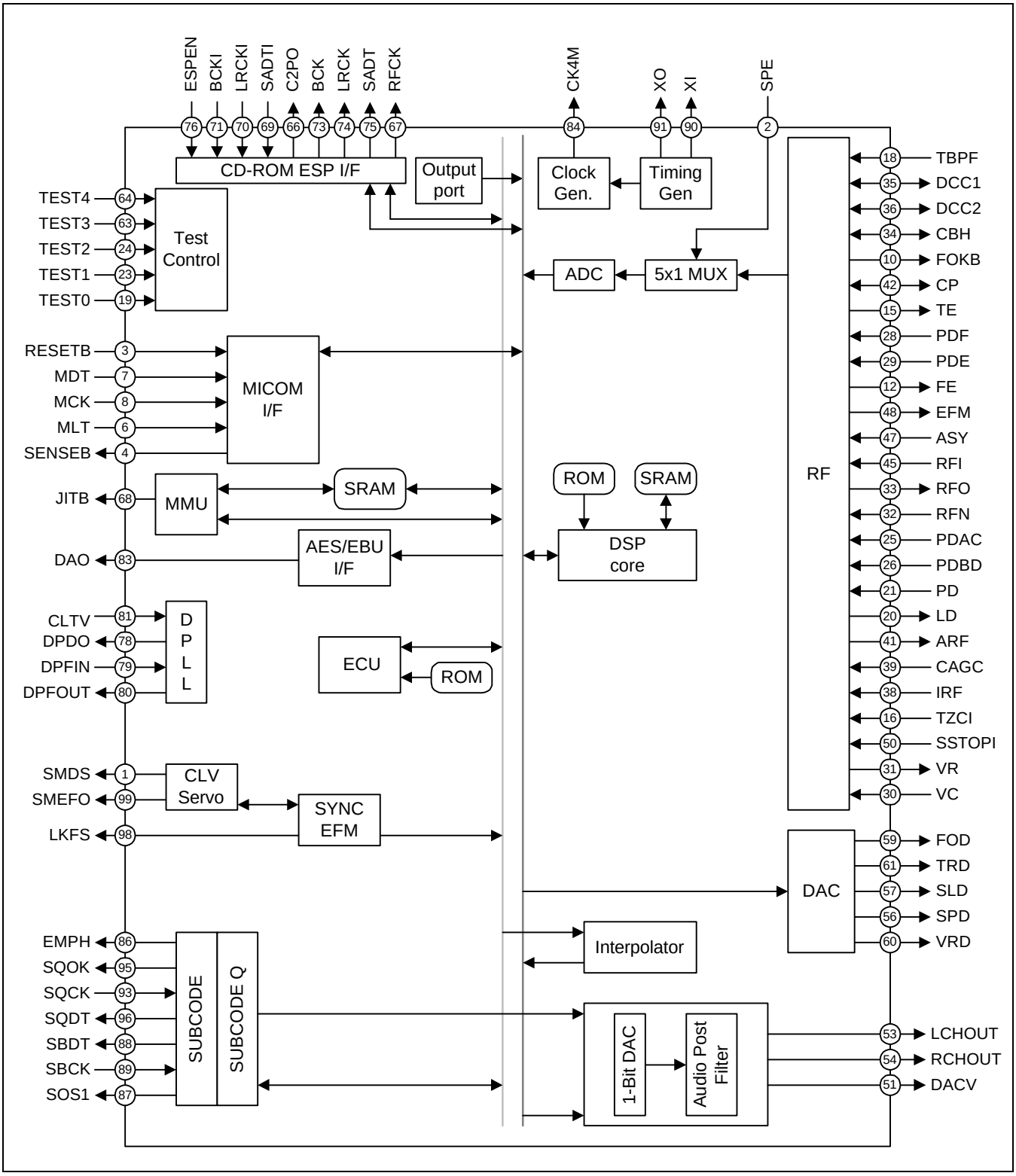


Figure 1. Block Diagram

PIN CONFIGURATION

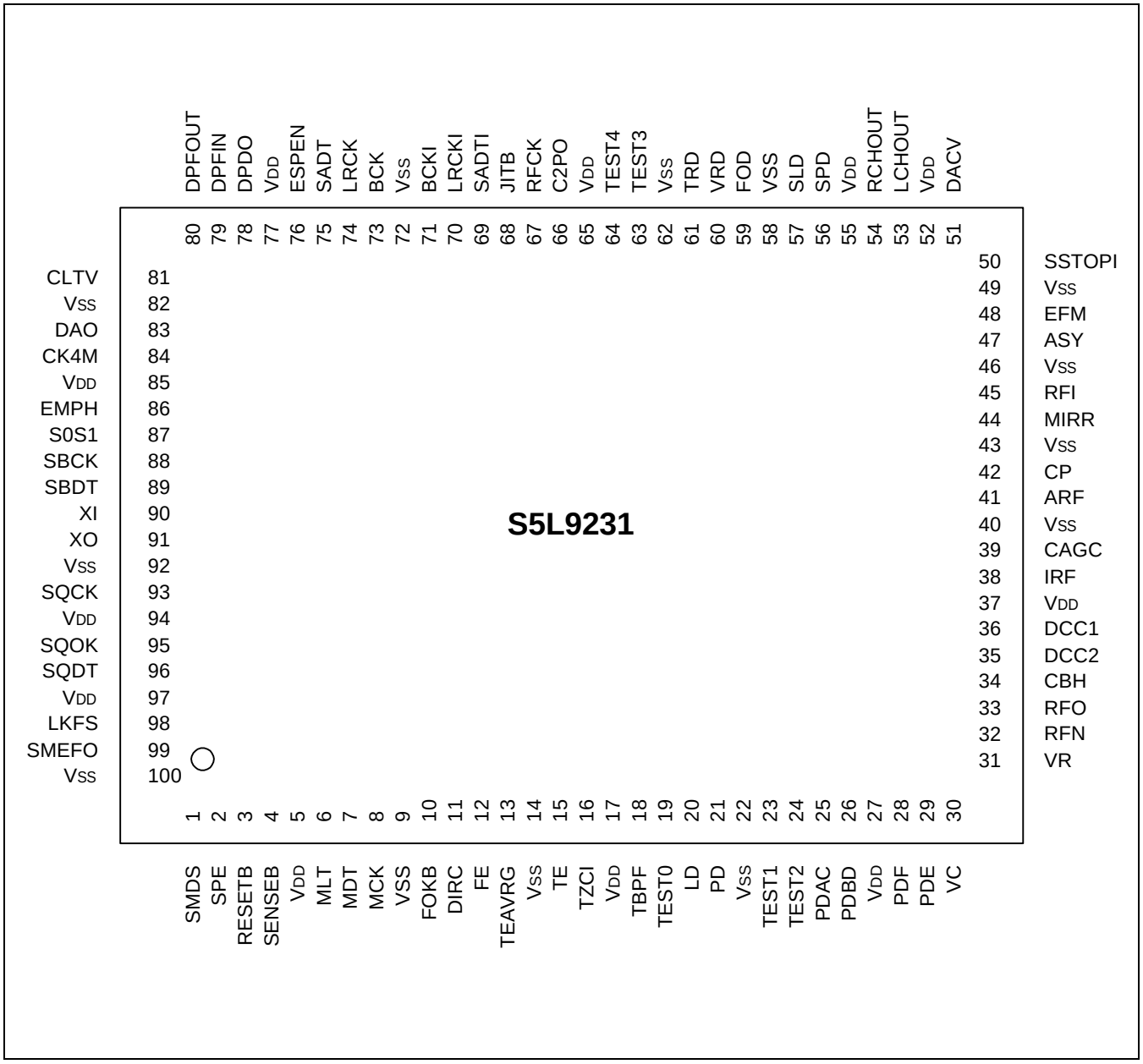


Figure 2. Pin Configuration

PIN DESCRIPTIONS

No	Pin Name	I/O	Descriptions
1	SMDS	O	Spindle motor velocity control in Phase Mode
2	SPE	I	Spindle error input
3	RESETB	I	Micro Controller reset (Active Low)
4	SENSEB	O	Internal status monitor (Active Low)
5	VDD	-	Digital VDD (Logic Power)
6	MLT	I	Micro Controller serial data latching signal input (Active Low)
7	MDT	I	Micro Controller data
8	MCK	I	Micro Controller clock signal input
9	VSS	-	Digital VSS (Logic Power)
10	FOKB	O	Focus OK output to Micro Controller (Active Low)
11	DIRC	I	Direct 1 track jump
12	FE	O	Focus error output
13	TEAVRG	I	LPF input for defect interruption
14	VSS	-	Digital VSS (Logic Power)
15	TE	O	Tracking error output
16	TZCI	I	Tracking zero cross input
17	VDD	-	Digital V_{DD} (I/O PAD Power)
18	TBPF	I	Anti-shock input from BPF
19	TEST0	I	Test mode selection 0
20	LD	O	APC output
21	PD	I	APC input
22	VSS	-	Analog V_{SS} (RF analog Power)
23	TEST1	I	Test mode selection 1
24	TEST2	I	Test mode selection 2
25	PDAC	I	RF I-V AMP 1 input from pick-up
26	PDBD	I	RF I-V AMP 2 input from pick-up
27	V_{DD}	-	Analog V_{DD} (RF analog Power)
28	PDF	I	F I-V AMP input from pick-up
29	PDE	I	E I-V AMP input from pick-up
30	VC	I	Center voltage input
31	VR	O	V_{CC}/2 DC voltage output
32	RFN	I	RF summing AMP (-) input
33	RFO	O	RF summing output
34	CBH	I/O	Defect bottom hold capacitor
35	DCC2	I/O	Defect bottom hold capacitor

PIN DESCRIPTIONS (Continued)

No	Pin Name	I/O	Descriptions
36	DCC1	I/O	Defect bottom hold capacitor
37	VDD	-	Analog VDD (ADC and DAC analog part Power)
38	IRF	I	Coupling capacitor of RFO
39	CAGC	I	AGC-EQ capacitor
40	VSS	-	Analog VSS (ADC and DAC analog part Power)
41	ARF	O	AGC-EQ output
42	CP	I/O	Mirror hold capacitor
43	VSS	-	VSS for bulk bias
44	MIRR	O	Mirror signal
45	RFI	I	EFM input
46	VSS	-	Digital VSS (Power for I/O pad)
47	ASY	I	EFM slicing LPF
48	EFM	O	EFM output
49	VSS	-	Analog VSS (Audio DAC analog part Power)
50	SSTOPI	I	SSTOP input
51	DACV	O	Analog voltage reference for 1-Bit DAC output
52	VDD	-	Analog VDD (Audio DAC analog part Power)
53	LCHOUT	O	Left-channel audio output through 1-Bit DAC
54	RCHOUT	O	Right-channel audio output through 1-Bit DAC
55	VDD	-	Digital VDD (Audio DAC/DAC logic part Power)
56	SPD	O	Spindle motor drive signal output
57	SLD	O	Sled motor drive signal output
58	VSS	-	Digital VSS (Audio DAC/DAC logic part Power)
59	FOD	O	Focus actuator drive signal output
60	VRD	O	Voltage reference drive signal output
61	TRD	O	Tracking actuator drive signal output
62	VSS	-	Digital VSS (Logic Power)
63	TEST3	I	Test mode selection 3
64	TEST4	I	Test mode selection 4
65	VDD	-	Digital VDD (Logic Power)
66	C2PO	O	C2 pointer for serial audio data
67	RFCK	O	Crystal-controlled read frame clock
68	JITB	O	Jitter margin flag (Active Low)
69	SADTI	I	Serial audio data input from ESP controller
70	LRCKI	I	Channel clock from ESP controller

PIN DESCRIPTIONS (Continued)

No	Pin Name	I/O	Descriptions
71	BCKI	I	Serial data bit clock from ESP controller
72	VSS	-	Digital VSS (Logic Power)
73	BCK	O	Serial audio data bit clock
74	LRCK	O	Channel clock
75	SADT	O	Serial audio data output
76	ESPEN	I	ESP enable (0: disable, 1: enable)
77	VDD	-	Digital VDD (Logic Power)
78	DPDO	O	Charge pump output for VCO
79	DPFIN	I	Filter input for VCO
80	DPFOUT	O	Filter output for VCO
81	CLTV	I	VCO control voltage
82	VSS	-	Digital VSS (Logic Power)
83	DAO	O	Digital audio output
84	CK4M	O	4.2336MHz clock output
85	VDD	-	Digital VDD (Logic Power)
86	EMPH	O	Emphasis/non-emphasis output ('H': emphasis)
87	S0S1	O	Subcode sync S0+S1 output to Micro Controller
88	SBCK	I	Subcode data bit clock
89	SBDT	O	Subcode data serial output
90	XI	I	System clock signal input (crystal input:16.9344MHz)
91	XO	O	System clock signal output
92	VSS	-	Digital VSS (IO PAD Power)
93	SQCK	I	Subcode-Q data bit clock
94	VDD	-	Digital VDD (IO PAD Power)
95	SQOK	O	Subcode-Q CRC check result signal
96	SQDT	O	Subcode-Q data serial output
97	VDD	-	Digital VDD (Logic Power)
98	LKFS	O	Lock status output of Frame Sync
99	SMEFO	O	CLV LPF connection
100	VSS	-	Digital VSS (Logic Power)

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Spec.	Unit
Supply Voltage	V_{DD}	-0.3 — 7.0	V
Input Voltage	V_I	-0.3 — V_{DD}+0.3	V
Output Voltage	V_O	-0.3 — 7.0	V
Operating Temperature	T_{OPR}	-20 — 75	°C
Storage Temperature	T_{STG}	-40 — 125	°C

ELECTRICAL CHARACTERISTICS

DC Characteristics : (V_{DD} = 5V, V_{SS} = 0V, Ta = 25°C)

ITEM	Symbol	Test Condition	MIN	TYP	MAX	Unit	Misc.
'H' Input Voltage1	$V_{IH(1)}$		3.5	-	-	V	note 1
'L' Input Voltage1	$V_{IL(1)}$		-	-	1.5	V	
'H' Input Voltage2	$V_{IH(2)}$		-	-	4.0	V	note 2
'L' Input Voltage2	$V_{IL(2)}$		1.0	-	-	V	
'H' Output Voltage1	$V_{OH(1)}$	I_{OH} = -2mA	2.4	-	-	V	note 3
'L' Output Voltage1	$V_{OL(1)}$	I_{OL} = 2mA	-	-	0.4	V	
Input Leak Current	I_{LKG}	V_I = 0 — V_D	-10	-	10	uA	
Three State Output Leak Current	$I_{O(LKG)}$	V_O = 0 — V_{DD}	-10	-	10	uA	note 4

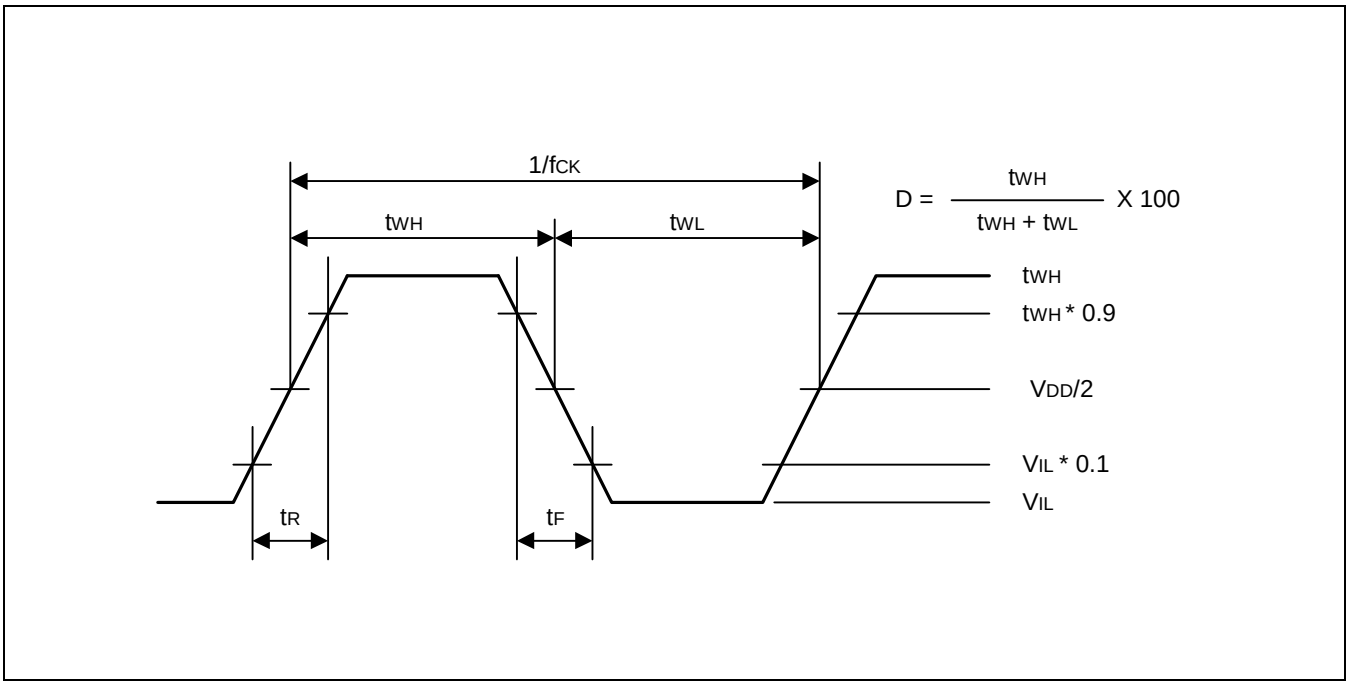
NOTES :

1. Related pins: CMOS interface.
2. Related pins: CMOS Schmitt trigger interface, (MLT, MCK, MDT pins).
3. Related pins: All output pins except #91(XO) and #80 (DPFOUT).
4. Related pins: SMEFO (#99), SMDS (#1), SENSEB (#4), C2PO (#66).

AC Characteristics :

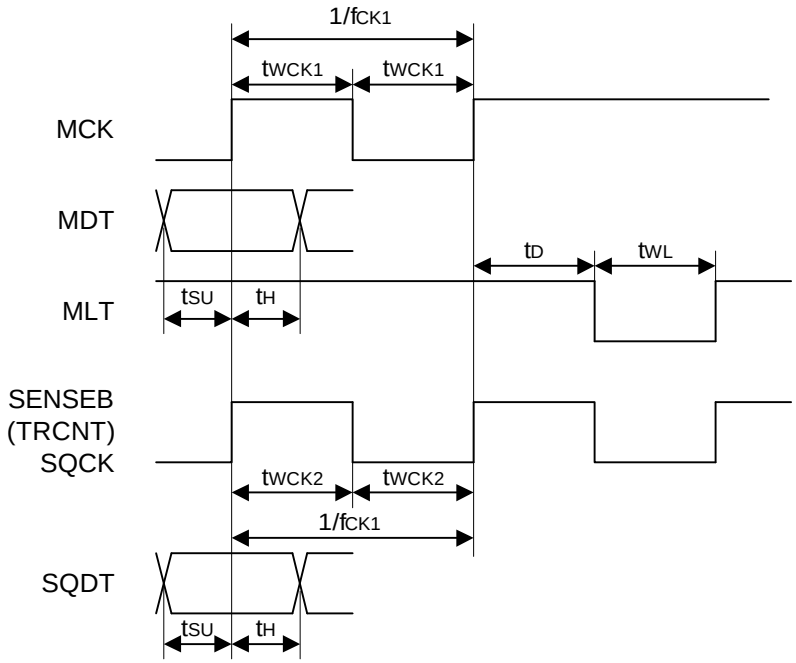
When a pulse is input into XI pin: (V_{DD} = 5V, V_{SS} = 0V, Ta = 25°C)

Item	Symbol	MIN	TYP	MAX	Unit
Clock Frequency	f_{CK}	-	16.9344	-	MHz
Clock Duty	D	-	50	-	%
Input "H' Level	V_{IH}	V_{DD}-1.0	-	-	V
Input 'L' Level	V_{IL}	-	-	0.8	V
Rising & Falling Time	t_R,t_F	-	-	8	ns



MCK, MDT, MLT (V_{DD} = 5V, V_{SS} = 0V, Ta = 25°C)

Item	Symbol	MIN	TYP	MAX	Unit
Clock Frequency	f_{CK1}	-	-	1	MHz
Clock Pulse Width	t_{WCK1}	500	-	-	ns
Setup Time	t_{SU}	300	-	-	ns
Hold Time	t_H	300	-	-	ns
Delay Time	t_D	300	-	-	ns
Latch Pulse Width	t_{WL}	500	-	-	ns
SENSEB (TRCNT), SQCK Frequency	f_{CK2}	-	-	1	MHz
SENSEB (TRCNT), SQCK Pulse Width	t_{WCK2}	500	-	-	ns



SIGMA-DELTA AUDIO DAC (V_{DD} = 5V, Ta = 25°C, Fs = 44.1kHz, Signal Frequency = 20 - 20kHz)

Item	MIN	TYP	MAX	Unit
Resolution		16		bits
SNR<1>		96		dB
THD<2>			.005	%
Reference Voltage Output		2.25		V
Frequency Response			± 0.5	dB
Analog Output				
Voltage Range		± 1.414		V
Load Impedance	5			kΩ

<1> 1kHz 0 dB Input, A-Weighted
<2> 1kHz 0 dB Input

FUNCTIONAL DESCRIPTIONS

MICRO CONTROLLER INTERFACE

Data input from Micro Controller is received in MDAT, and transmitted by MCK. This signal is stored in the Control Register by MLT. The Timing diagram for this process is shown in Figure 1. Each command is carried out by receiving data and commands (LSB first) from Micro Controller.

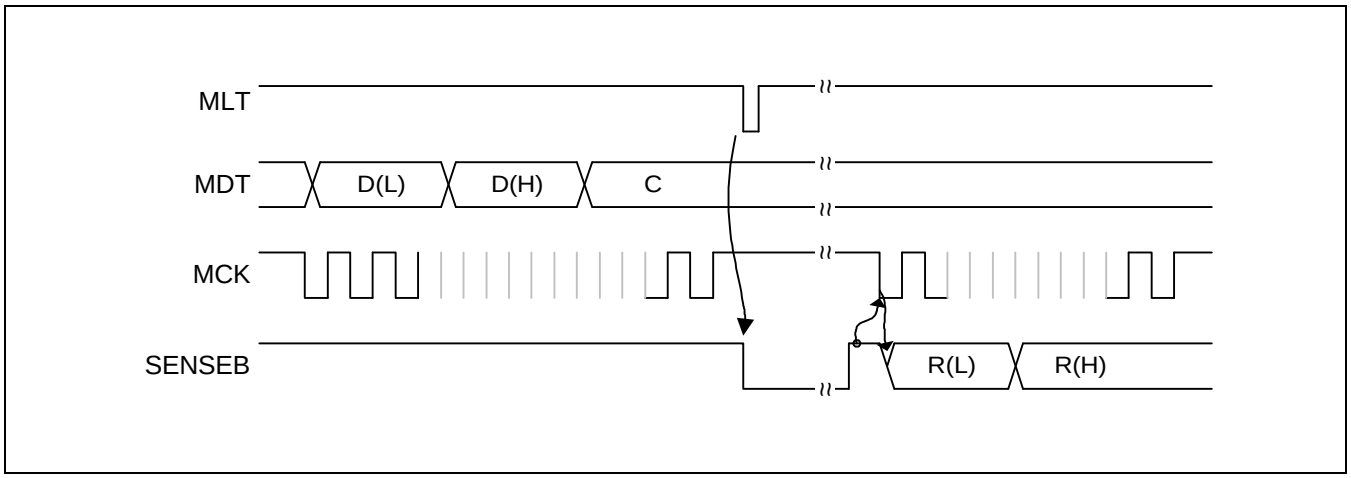


Figure 1. Micro Controller Interface Timing

For CD-DSP, the command and data length is 4 bits respectively. In the case of the Servo, the command length is fixed at 8 bits, but the data length is variable from 0 to16 bits. When Data is 16 bits and command is 8 bits, the input is made starting with the LSB in the following order: D(L) = D7 — D0, D(H) = D15 — D8, and C = C7 — C0. In the case of a command with no data, you only need to input the command byte. When data input is finished, a pulse at MLT is generated to indicate that the command transmission is finished. From then on, command is decoded and carried out. The SENSEB output shows READY (/BUSY) status at default. In other words, it is "L" when it receives a command, and "H" when the command is completed. In certain commands, SENSEB output has a meaning other than that of Ready. For example, it can show the "on/off" information of the limit switch or the presence of a disc.

The detailed input timing of S5L9231 is shown in Figure 2. Micro Controller sends MDT to MCK falling edge, in the order of LSB, Data, and Command. S5L9231 latches the data at MCK's rising edge. Micro Controller no longer sends MCK when the transmission of all MDT is finished. At this time, MLT becomes "L" to indicate that the transmission of command and data from Micro Controller to S5L9231 is complete.

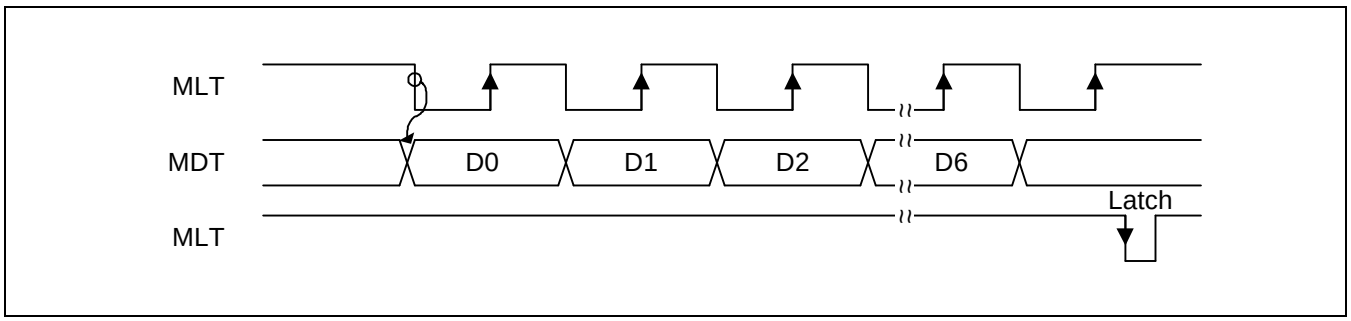


Figure 2. Micro Controller to S5L9231 Input Timing

The timing for sending data to Micro Controller is shown in Figure 3. In such a case the Digital Servo Signal Processor (DSSP) stores the data to be sent to Micro Controller after command has been carried out, in the output buffer. At the same time, it makes the SENSEB output "H" to indicate that the DSSP's command processing routine is finished. If Micro Controller needs to read the response data, only MCK is sent to S5L9231. S5L9231 then sends the output serially through SENSEB to Micro Controller, on MCK's falling edge. Since SENSEB's Ssel (Serial Data Select Signal) is "1", the data in the output buffer should be output. The output to SENSEB is carried out in units of byte, and in the order of R(L) = R7 — R0 and R(H) = R15 — R8, starting with LSB.

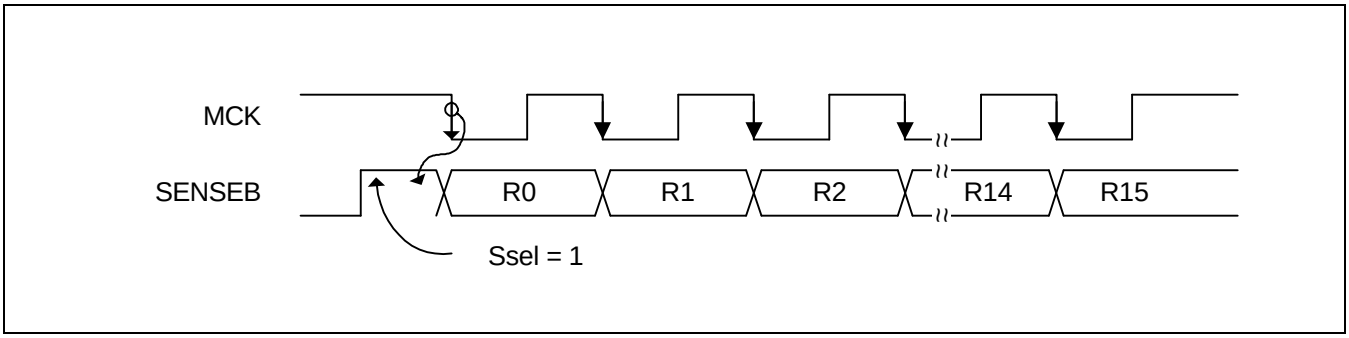


Figure 3. S5L9231 to Micro Controller Output Timing

S5L9231 generates one SENSEB signal that makes the CD-DSP and Servo into a single chip and goes through MUX to Micro Controller. Hence, Micro Controller can use SENSEB as a direct input signal.
As shown in Table 1 and Table 2, Micro Controller command can be divided into Micro Controller command for Digital Servo (00 — 5Fh), and Micro Controller command for CD-DSP (6Xh — FXh). CD-DSP Micro Controller is composed of upper 4 bits, and has a command from 6h to Fh.

Table 1. Digital Servo Micro Controller Command (00 ¾ 5Fh)

Command		DH1				DH0				DL	Remark
Name	code	DH7	DH6	DH5	DH4	DH3	DH2	DH1	DH0	DL7 - DL0	
STPcmd	00	STOP	ABRT	IDLE	LDX						
DDTcmd	01	*AUTO*	*UPDN*	*FIGA*	*FBAL*	RPT	FSP2	FSP1	FSP0		FSspd
FONcmd	02	LYRX	Fmthd	*FOPI*	FSPC	PIL3	PIL2	PIL1	PIL0		FONc
TONcmd	03	0	*SLSV*	*TRPI*	TOLB	MTLB	SFOG	STRG	DGs		TONc
SLDcmd	04	HOME	SMOV	SPLY							
JMPcmd	05	DIR	JPM1	JPM0	JIT2	JIT1	JIT0	JPD9	JPD8	JPD7 - JPD0	JMPc
-	06	Reserved for super of next generation									
EMEcmd	07	Test	SLST	DFavrg	upFv	dsAS	ASFO	ASTR	ASBR		EMEc
HDWcmd	08	PN	SSTOP	enASin		PCUP		SLbrk			HDWc
INIcmd	09	SLDO	JPCK	TKJM	JPEC	BJJM	BTS	enJaP	MHsel		iNic
MSCcmd	0A	MD11	MD10	MD9	MD8	MD7	MD6	MD5	MD4	MD3-MD0, MSS3-MSS0	BANK0 55
SPDcmd	0B	0	0	0	0	0	0	0	SPD		SPDc
TMScmd	0C	TD11	TD10	TD9	TD8	TD7	TD6	TD5	TD4	TD3-TD0, TMS3-TMS0	Bank0 41
OKScmd	0D	OD11	OD10	OD9	OD8	OD7	OD6	OD5	OD4	OD3-OD0, OKS3-OKS0	BANK1 B0
AJKcmd	0E	AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4	AD3-AD0, AJS3-AJS0	BANK0 24
LEScmd	0F	LD11	LD10	LD9	LD8	LD7	LD6	LD5	LD4	LD3-LD0, LES3-LES0	BANK1 C0
AARWcmd	10	AA11	AA10	AA9	AA8	AA7	AA6	AA5	AA4	AA3-AA0, AAS3-AAS0	BANK1
OFAcmd	11	FTS	LDoff								
FBAcmd	12										
TBAcmd	13	*TIGA*	*RPTB*								
FGAcmd	14										
TGAcmd	15										
-	16	Reserved									

Command		DH1				DH0				DL	Remark
Name	**code**	**DH7**	**DH6**	**DH5**	**DH4**	**DH3**	**DH2**	**DH1**	**DH0**	**DL7 ¾ DL0**	
-	17										
SQDTcmd	18							SQDT1	SQDT0		
SNScmd	19	0	0	0	0	0	SNS2	SNS1	SNS0	[0000 00:Ssel:0]	
FLGcmd	1A	stp	Fptmg		HOME	itvJ	TSV	SSV	enTJn	FLG7-0 (DECT...)	
SNSCcmd	1B			*NORM*	FTLK						
SPRWcmd	1C	DD11	DD10	DD9	DD8	DD7	DD6	DD5	DD4	DD3-0, ST6, DPS2-0	
FTSTcmd	1D				WTF				WFF		
RamRcmd	1E	NEXT	0	0	BANK	0	0	0	PAGE	RAM7 - RAM0	
RamWcmd	1F	RD15	RD14	RD13	RD12	RD11	RD10	RD9	RD8	RD7 - RD0	
Fxkcmd	2X	Fk15	Fk14	Fk13	Fk12	Fk11	Fk10	Fk9	Fk8	Fk7 - Fk0	
Fxkcmd	30-33	Fk15	Fk14	Fk13	Fk12	Fk11	k10	Fk9	Fk8	Fk7 - Fk0	
SPKcmd	34-38	Sk15	Sk14	Sk13	Sk12	Sk11	Sk10	Sk9	Sk8	Sk7 - Sk0	
SLKcmd	3A-3E	Sk15	Sk14	Sk13	Sk12	Sk11	Sk10	Sk9	Sk8	Sk7 - Sk0	
TxKcmd	4X	Tk15	Tk14	Tk13	Tk12	Tk11	Tk10	Tk9	Tk8	Tk7 - Tk0	
TxKcmd	50-53	Tk15	Tk14	Tk13	Tk12	Tk11	Tk10	Tk9	Tk8	Tk7 - Tk0	
ASKcmd	54-56	Lk15	Lk14	Lk13	Lk12	Lk11	Lk10	Lk9	Lk8	Lk7 - Lk0	
TTKcmd	57	Lk15	Lk14	Lk13	Lk12	Lk11	Lk10	Lk9	Lk8	Lk7 - Lk0	
Xgkcmd	58-5A	Bk15	Bk14	Bk13	Bk12	Bk11	Bk10	Bk9	Bk8	Bk7 - Bk0	
FTGcmd	5B	Fchg	DWN	Tchg	UP						
AVKcmd	5C	AV12	AV11	AV10	AV9	AV8	AV7	AV6	AV5	AV4 - AV0, AVS2 - AVS0	
ATTcmd	5D	0	0	AT5	AT4	AT3	AT2	AT1	AT0		
TRFcmd	5E	Gin4	Gin3	Gin2	Gin1	Gin0	Bal4	Bal3	Bal2	Bal1 - Bal0	TEST
TDACcmd	5F	DAC7	DAC6	DAC5	DAC4	DAC3	DAC2	DAC1	DAC0		TEST

NOTES:

1. S5L9231 supports only Micro Controller commands as LSB first scheme.
2. The words in ***Bold Italics*** in the table above signify active low, and the places designated "0" always need to be set to "0".
3. Empty spots signify "don't care".
4. MSC, SPD, OKS, AJK and LES commands store the data set in DH7-0 and DL7-4's 12 bits into the object set in DL3-0. When the 12 bits of data are all "1", or FFFh, it means reading the value of the object set in DL3-1. Other values mean write. Write data is set to the lower 12 bits of the designated RAM, and AJK and LES commands are set at the upper 12 bits. At this time, the 4 bits left over are written as "0".

Table 2. Micro Controller Command Code List for CD-DSP (6X to FXh)

Name	Address	Data				SENSEB	Remark
	D7- D4	D3	D2	D1	D0		(Default)
CNTL-6	6	ERAOFF	CDROM	-	-	Hi-Z	(0000)
CNTL-7	7	MUTE	-	-	SMDS_ OFFSET	Hi-Z	Audio Output Format (0000)
CNTL-8	8	-	CFS	PHASE_OFFSET[1:0]		Hi-Z	(0000)
CNTL-Z	9	ZCMT	-	NCLV	CRCQ	Hi-Z	(0011)
CNTL-S	A	GSEM	GSEL	WSEL	ATTM	Hi-Z	(1110)
CNTL-L	B	ADATEN	SPDIFEN	MCKEN	SUBDTEN	Hi-Z	(0110)
CNTL-U	C	-	ERA4OFF	-	-	Hi-Z	(0000)
CNTL-W	D	COM	WB	WP	GAIN	Hi-Z	(0001)
CNTL-C	E	CLV Mode Control				CLV_STATE	(0000)
CNTL-D	F	COM	LC	DS1	DS0	Hi-Z	(0000)

DIGITAL SERVO MICRO CONTROLLER COMMAND DESCRIPTIONS

The Digital Servo Signal Processor (DSSP) handles the optical pick-up system servo command for CD. DSSP's main goal is to simplify the external hardware by digital filtering, and to carry out automatic adjustment features. When DSSP receives a command from Micro Controller, SENSEB = "L". If the command job ends, it is inverted to SENSEB = "H". Also, the SENSEB output has the designation /BUSY(READY) as default, but some commands have other designations for SENSEB. If there is no special note, consider SENSEB to be /BUSY. Commands can be divided into those that actually carry out processes, and the select/refer commands which do not carry out processes. The former includes Action Commands that carry out those that are directly related to the Servo, and Automatic Adjustment commands. The latter includes filter coefficient set/refer commands and initialization commands, and system constant/time set/refer commands. The action command is a command with less than 05 of command codes, and no matter which one is carried out, Repeat Jump is cancelled. In addition, there are commands whose function changes according to which command comes before it, so when a command is received, the previous command is saved. The execution of the 1-bit DAC's attenuation command is carried out by the 1-bit DAC block, but command address is included in the servo part.
Command's data, or the coefficient data length varies from 0 — 16 bits according to each command. Please refer to each command.

- **STPcmd (Address 00H)**

The STPcmd stops the JMPcmd (05H) or auto adjustment-related servo actions, or changes them to STOP mode. Furthermore, it lowers the speed of the DSP core to lower power usage, carries out Laser Diode on/off, and can also clear the adjust/measure data. The following 4 bits of constant data are used to explain the above.

Command		DH1				DH0				DL
Name	**code**	**DH7**	**DH6**	**DH5**	**DH4**	**DH3**	**DH2**	**DH1**	**DH0**	**DL7 - DL0**
STPcmd	00	STOP	ABRT	IDLE	LDX					

.STOP: Goes to STOP mode. This bit can be used in any mode. This command acts as a reservation for STOP, executing it after the MON signal is turned Off. If already in the STOP mode and STOPcmd (0080H) is sent again, STOP is carried out without concern to the MON signal.
L : Do not carry out anything but the bit check below.
H : Reserve STOP mode.

.ABRT: Aborts Track search and automatic adjustment function, and returns to previous state.
L : Do not carry out anything but the bit check below.
H : Abort Jump or Adjustment and return to previous state.

.IDLE: Selects IDLE (Power Save Mode). RAM Data remains.
L : Go from IDLE mode to Normal mode.
H : Select IDLE mode.

.LDX: Turns the Laser Diode On/Off.
L : Laser Diode Off
H : Laser Diode On

The order of priority for the bits is STOP, then ABORT, followed by IDLE and LDX, which have equal priority. If a higher priority bit is "1", then the IDLE and LDX bit are not checked.
Except, if STOP = ABRT = 1, all RAM clear is carried out. RAM clear is carried out during regular STPcmd as well. In that case, Servo On is possible in the next Play without readjusting, but the automatically adjusted value and measurements are not clear. When a Disc has been exchanged, these values should be cleared and initialized. Thus the adjustment values should be cleared as well by the STLPcmd's main option.
When in IDLE mode, the DSP core's processing speed is 1/256, a low power consumption mode. Also, IDLE and LDX bit can only be received during Servo Off status.

· **DDTcmd (Address 01H)**

This command determines the presence of a disc and outputs the result. It also measures the offset at the same time. Focus error input gain adjustment and focus balance adjustment is possible as well. Before Focus search, the Laser Diode is automatically turned On. The Focus search has the following two modes- Auto mode which automatically searches using delta waves, and Manual mode carried out by Micro Controller. For any mode, the speed is determined by FPS2 — 0. To determine the presence of a disc, the Focus actuator searches at a faster speed than that during Focus Pull-in. (Focus Pull-in is not carried out.) It can also read the data that shows the disc type and presence.

Command		DH1				DH0				DL
Name	**code**	**DH7**	**DH6**	**DH5**	**DH4**	**DH3**	**DH2**	**DH1**	**DH0**	**DL7 - DL0**
DDTcmd	01	*AUTO*	*UPDN*	*FIGA*	*FBAL*	RPT	FSP2	FSP1	FSP0	

./AUTO./UPDN: Focus search mode select
0 0 : Auto mode. SENSEB output means Busy(L)/Ready(H).
0 1 : Auto mode. Automatically carries out DDTcmds from search to focus pull-in.
1 0 : Manual up mode (actuator up). Actuator signal (FZC) is output through SENSEB.
1 1 : Manual down mode (actuator down). Actuator signal (FZC) is output through SENSEB.

./FIGA : Changes the Focus input gain by the FE Peak level. Since the Input gain's standard is changed for each adjustment, the adjustment should be finished at one try.
L : Carry out adjustment.
H : Do not carry out adjustment (maintain previous gain).

./FBAL : Adjust F-BAL so that the absolute value of the minimum and maximum value of the focus S-curve during DDTcmd are the same.
L : Carry out adjustment.
H : Do not carry out adjustment (maintain previous balance).

.RPT: Adjust the number of the Actuator's Up/Down search (when delta waves for search are generated).
L : Search once.
H : Repeat search (continue until the next command input. However, SENSEB goes to "H" after just one time.)

.FSP<2:0> : Bit that controls the actuator speed (slope) during DDTcmd and focus pull-in.
0 0 0 : 2Hz (Fast) at clock = 34MHz
0 0 1 : 1Hz
0 1 1 : 1/2Hz
1 1 1 : 1/3Hz (Slow) * Values other than these cannot be selected.

<Focus input gain control>

There are two methods, manual and auto. Manual setting is recommended because FEpeak signal is very unstable due to PU characteristics. If auto input gain control is chosen, FEpk measured during disc detect can be adjusted according to the look-up table as FEpk is about 80% (64 - 70h) of ADC's full range value (7Fh). In case manual adjustment is set by direct port write command, 1Ccmd:DPRWcmd. For tracking, TEpk is detected when it is in off track state, and adjusted as focus is done.

<Focus search>
FOD = (FScnt+FSval) × (FSpk)
where (FScnt)n = (FScnt)n-1 ± K (Fixed K = 3 for DDTcmd) at every M determined by FSP2 — 0.
If M = 2^m (m = Number of 1 of FSP bits), $f_{SRCH} = f_S/(2 \times 2^{16} \times M \times K^{-1})$

where 2×2^{16} is doubling the value since FScnt for 1 search cycle changes 0000h → 7FFFh → 0000h → 8000h → 0000h.

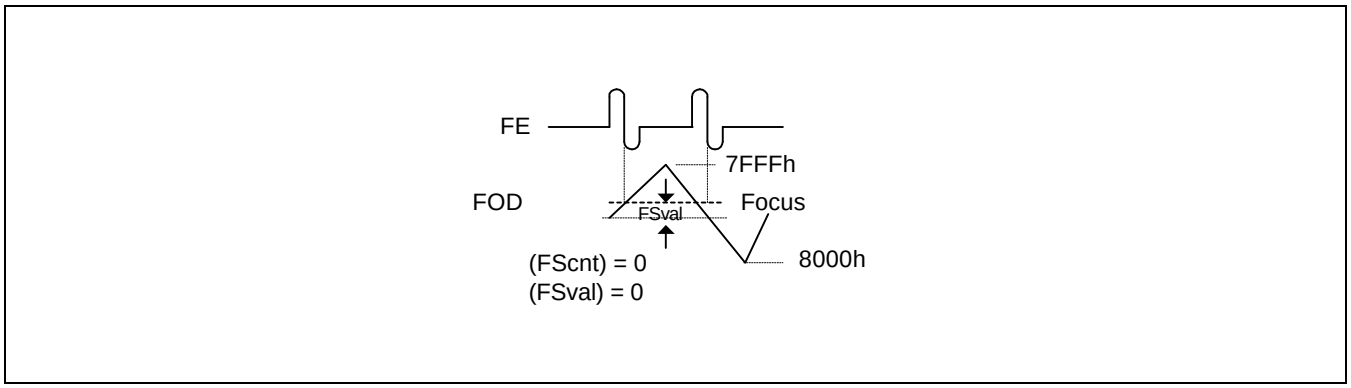


Figure 4. Focus Search Cycle

Register	Address	Function	Default	Value
FSpk	0055h	Output adjustment coefficient (% of full swing) when F-srch pull in	4000h	50%
unBal	004Eh	Percentage of S-curve unbalance detection criterion	2003h	4-Jan
DDT_J	10C8h	Disc detection level	1800h	468mVp
NZlvl	10CCh	Noise level criterion	0800h	156mVp
FBk	0030h	Feedback gain of focus balance control error at DDT	7FFFh	100%
FODbias	1090h	Bias level of FOD output(= FSpk × FSval)	0000h	-

*** DDT(Disc detect) Command Response format**

15 ~ 8	7	6	5	4	3	2	1	0
FE PEAK LEVEL	0	0	0	0	0	0	DIN	X

. FE PEAK LEVEL : S-curve peak level
. DIN : DISC Detect
"0" : No disc
"1" : Presence
. X : Don't care

- **FONcmd (Address 02H)**

This command turns off the focus pull-in and tracking servo. The laser diode is automatically turned on, and many different types of pull-in methods are selected by the command's data. If this command is received when focus is already on, no actions take place. Also, if FONcmd is received after TONcmd (03H), only the tracking servo is turned off.

When AUTO bit of DDTcmd (01H) is "1", focus loop filter is turned on.

Command		DH1				DH0				DL
Name	**code**	**DH7**	**DH6**	**DH5**	**DH4**	**DH3**	**DH2**	**DH1**	**DH0**	**DL7 - DL0**
FONcmd	02	LYRX	Fmthd	*FOPI*	FSPC	PIL3	PIL2	PIL1	PIL0	

.LYRX: Sets the direction of focus search (pull-in).
L : Start pull-in from the bottom.
H : Start pull-in from the top.

.Fmthd: Sets the focus pull-in method.
L : Pull-in from S-curve's both top and bottom directions.
H : Pull-in from one of the S-curve's top or bottom directions.

./FOPI: sets whether retrying of pull-in is within the search level (FSrng), during focus drop.
L : Auto mode (DSSP automatically retries pull-in during Focus drop).
H : Does not. Micro Controller retries pull-in through FON command.

.FSPC : Automatic speed control select bit during focus pull-in (feature that lowers the search speed as it gets closer to the pull-in location).
L : Does not automatically control the speed (during Search).
H : Automatically controls the speed (feature that reduces the search speed by half according to the S-curve).

.PIL3, PIL2, PIL1, PIL0 : S-curve recognition level : pull-in level

x	x	1	1	:	FEpk/2	:	FEpk/4
x	x	0	1	:	FEpk/2	:	FEpk/8
x	1	1	0	:	FEpk/4	:	FEpk/8
x	0	1	0	:	FEpk/4	:	FEpk/16
1	x	0	0	:	FEpk/8	:	FEpk/16
0	x	0	0	:	FEpk/8	:	FEpk/32

The HDWcmd''s PCUP bit is also related to the focus pull-in method. If PCUP is "0", the pick-up is searched close to the pull-in point, and if it is "1", it will fall. The returning points are each made FOK, and FSrng. If Fmthd = "1", pull-in action is carried out only when searching towards the pull-in point, and pull-in action is not carried out when it fails to search. Therefore, for pick-ups that are easily oscillated, make Fmthd = "1" as well as PCUP.

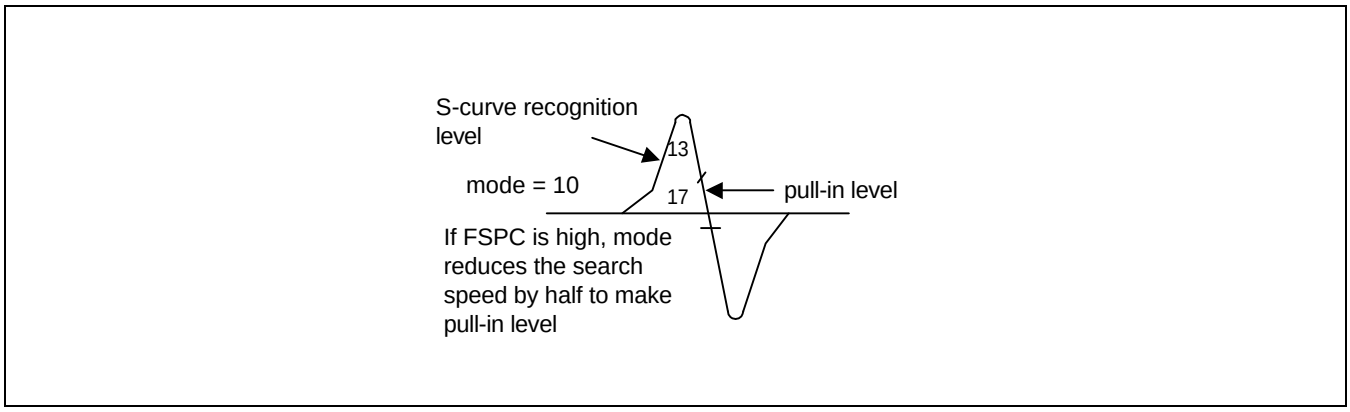


Figure 5. S-Curve Recognition and Pull-up Level

Register	Address	Function	Default	Value
FSpk	0055h	Output adjustment coefficient (% of full swing) when F-srch pull in	4000h	50%
FLoff	10ACh	FLKB (Focus lock) off time	0172h	4.4ms
FLon	10ADh	FLKB (Focus lock) on time	000Ah	113us
Fsrng	10C6h	Search range when retrying focus pull-in search	3000h	936mV
FSspd	0038h	Focus search speed register	00xxh	-

- **TONcmd (Address 03H)**

This is a tracking pull-in command which selects the gain of the lens brake and track search. If tracking is already on in this command, no actions are taken.

Command		DH1				DH0				DL
Name	**code**	**DH7**	**DH6**	**DH5**	**DH4**	**DH3**	**DH2**	**DH1**	**DH0**	**DL7 - DL0**
TONcmd	03	0	*SLSV*	*TRPI*	TOLB	MTLB	SFOG	STRG	DGs	

./SLSV : Sled Servo on select.
L : Sled servo turned on at the same time as tracking servo.
H : Sled servo is not turned on (turn on in sled command).

./TRPI : Tracking pull-in method select.
L : Use the tracking kick pulse during pull-in (auto mode).
H : Do not use the tracking kick pulse during pull-in (manual mode).

.TOLB : Lens brake select when tracking servo is on.
L : Do not activate Lens brake.
H : Activate Lens brake until the MIRR signal is no longer generated.

.MTLB : Manual tracking's lens brake.
L : Do not activate Lens brake.
H : Activate Lens brake (lens brake on when MIRR/TZC signal is generated).

.SFOG : Focus gain select during Search.
L : Do not change Gain (Manual).
H : Automatically change gain (Down: changes to temporary gain).

.STRG : Tracking gain select at search end.
L : Do not change gain (manual).
H : Automatically change gain (Up: changes to temporary gain).

.DGs : Tracking gain select during tDFCT period when defect is detected.
L : STRG valid (Gain is decided by STRG).
H : STRG invalid (Tracking gain is always normal without concern with STRG selection).

When there is a defect, apart from the Timer when deciding the defect period (DFCTpd), defect timer (tDFCT) is selected for DGs = 1, and controlled so that the tracking gain is not up. If the tDFCT timer without defects overflows, the STRG bits selection is valid even when DGs = 1.
For a disc with many defects, DGs = 1 makes the selection valid.

Register	Address	Function	Default	Value
GuT	10A5h	Track gain up time after jump (Track pull-in)	00A9h	1.9ms
dlyTG	10A7h	TGup delay time after completion of GuT	0060h	1.04ms
TLoff	10AEh	TLKB off delay time	0001h	11.3us
TLon	10AFh	TLKB on delay time	0100h	2.9ms

· **SLDcmd (Address 04H)**

This command controls the sled motor, and carries out bit check starting with the HOME bit. It also carries out the Sled Servo's On/Off and the pick-up's inner/outer circumference movement. During playback, the Micro Controller controls the sled movement, and manual sled move is also possible. Home location detect feature is also available.

Command		DH1				DH0				DL
Name	code	DH7	DH6	DH5	DH4	DH3	DH2	DH1	DH0	DL7 - DL0
SLDcmd	04	HOME	SMOV	SPLY						

.HOME : Sled HOME_IN mode select MSB (Most Significant Bit).
L : Off (checks the bits below).
H : After return to HOME, moves to outer circumference during the setting time (tHFwd).
SENSEB = BUSY/READY

.SMOV .SPLY : Sled Servo On/Off and Sled move control bit.
0 0 : Sled Servo off/move off.
0 1 : Sled Servo on.
1 0 : Sled forward move (to outer circumference), Kick level set to LEScmd's SKCKd.
1 1 : Sled backward move (to inner circumference), Kick level set to LEScmd's SKCKd.

.DH4 - 0 : Don't care.

During SENSEB output, focus off outputs limit switch information for sled inner/outer circumference move. It is "L" when arrived at the innermost circumference, and "H" at all other times (sled output is Off). Except, when HOME = "1", BUSY/READY is output to SENSEB. On the other hand, for focus on, manual sled move is activated. If OKScmd's count is 0, the TZC signal is output to SENSEB, and if not, the track count is output instead. Therefore, it is possible to carry out the sled move by Micro Controller counting these signals. First, the Count is selected by OKScmd, turning the tracking off by FONcmd, and accelerated using the SLDcmd. When the SENSEB signal count approaches the goal, set the brake using SLDcmd at the same time. If the SENSEB signal intervals are sufficiently far apart, the sled looks stopped. Then turn the brake pulse off using the SLDcmd. After a standby period for stability, send track on command: TONcmd, then turn on tracking and both sled servos to return to playback.

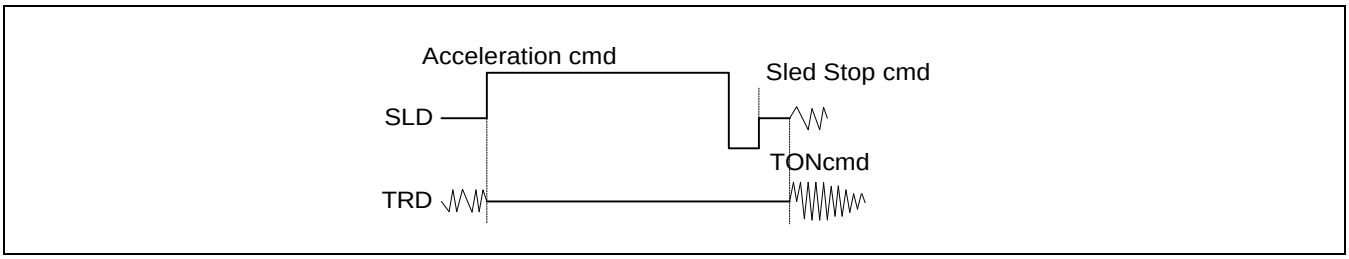


Figure 6.

Register	Address	Function	Default	Value
SKCKd	10C1h	SLED kick level (with respect to Vref)	6000h	46.2ms
tHBwd	0056h	Backward move time after home-in	1833h	70ms
tHFwd	10A9h	Fwd move time after home-in	0FF0h	46ms

· **JMPcmd (Address 05H)**

This command carries out Track search. There are two types of search methods, including track jump and sled move. Track jump has a Manual mode as well. Repeat search is also possible.

Command		DH1				DH0				DL
Name	code	DH7	DH6	DH5	DH4	DH3	DH2	DH1	DH0	DL7 - DL0
JMPcmd	05	DIR	JPM1	JPM0	JIT2	JIT1	JIT0	JPD9	JPD8	JPD7 - JPD0

.DIR : Jump direction select.
L : Forward (to outer circumference) jump.
H : Reverse (to inner circumference) jump.

.JPM1 - 0 : Bit that selects jump type.
0 0 : Automatically decides whether to carry out tracking jump or sled jump, according to the number of jump tracks. The decision depends on the boundary set by OKScmd.
0 1 : Tracking jump.
1 0 : Sled move.
1 1 : Tracking jump is repeated for intervals set by JIT2 - 0 (Interval Jump).

.JIT2 - 0 : Bit that sets the Repeat track jump time interval. This period spans from the initial point of one jump to the next.

JIT2 ¾ 0	Time Interval (repeat freq.)
0 0 0	Manual jump mode (1 track jump)
0 0 1	2.7Hz
0 1 0	5.4Hz
0 1 1	8.1Hz
1 0 0	13.5Hz
1 0 1	21.6Hz
1 1 0	29.7Hz
1 1 1	40.5Hz

¡Ø In Manual jump mode, if the number of jump tracks (JD7-0) = 0, TZC signal is output to SENSEB. The signal can be counted to make the jump using the Micro Controller's inversion signal: DiRC possible.

.JPD9 — 8 : If the following conditions are fulfilled in Manual jump mode, then stop and make the SENSEB "H". Tracking jump is repeated for intervals set by JIT2 - 0 (Interval Jump).
0 0 : Reserved.
0 1 : Preset track: COUNT (preset track number: for acceleration).
1 0 : MIRR interval: Tstp (MIRR interval: for deceleration).
1 1 : COUNT or Tstp (for deceleration).

.JPD12 — 0 : When JPM1 — 0 bit is selected to anything other than 11, JIT2 — 0 becomes JD12 — 10. When JPM1 — 0 bit is set to 10, the number of jump tracks are JD12 — 0, the product of the track number and 8.

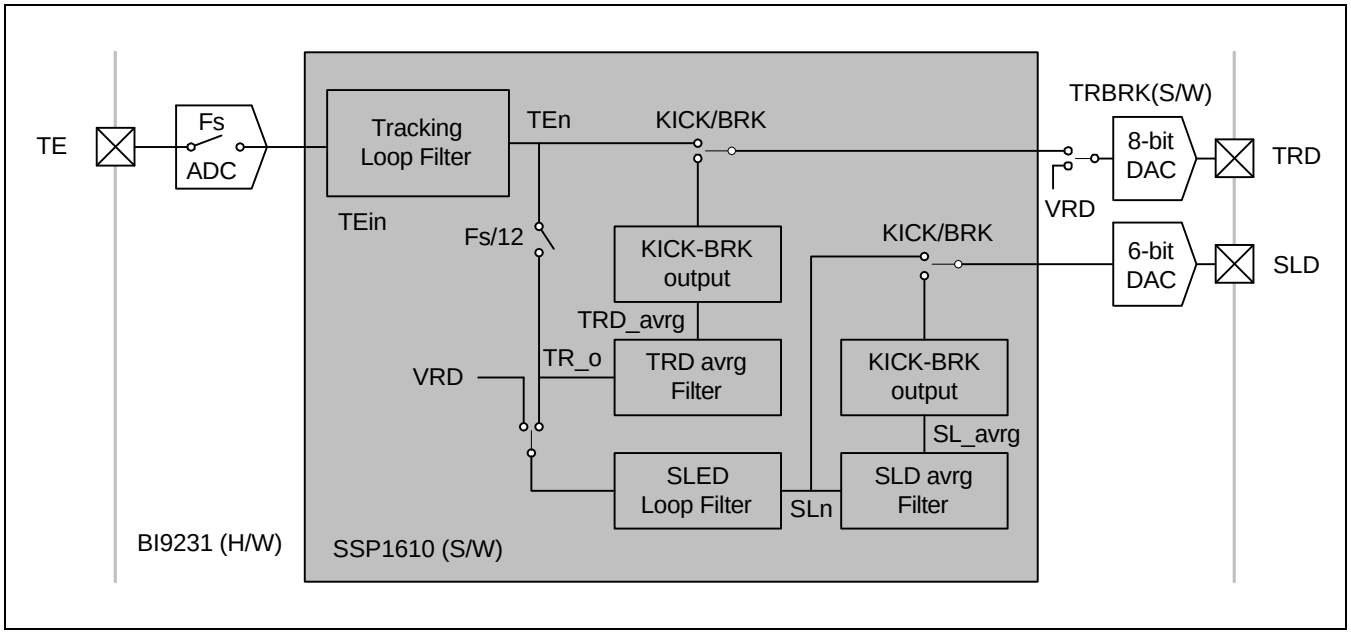


Figure 7.

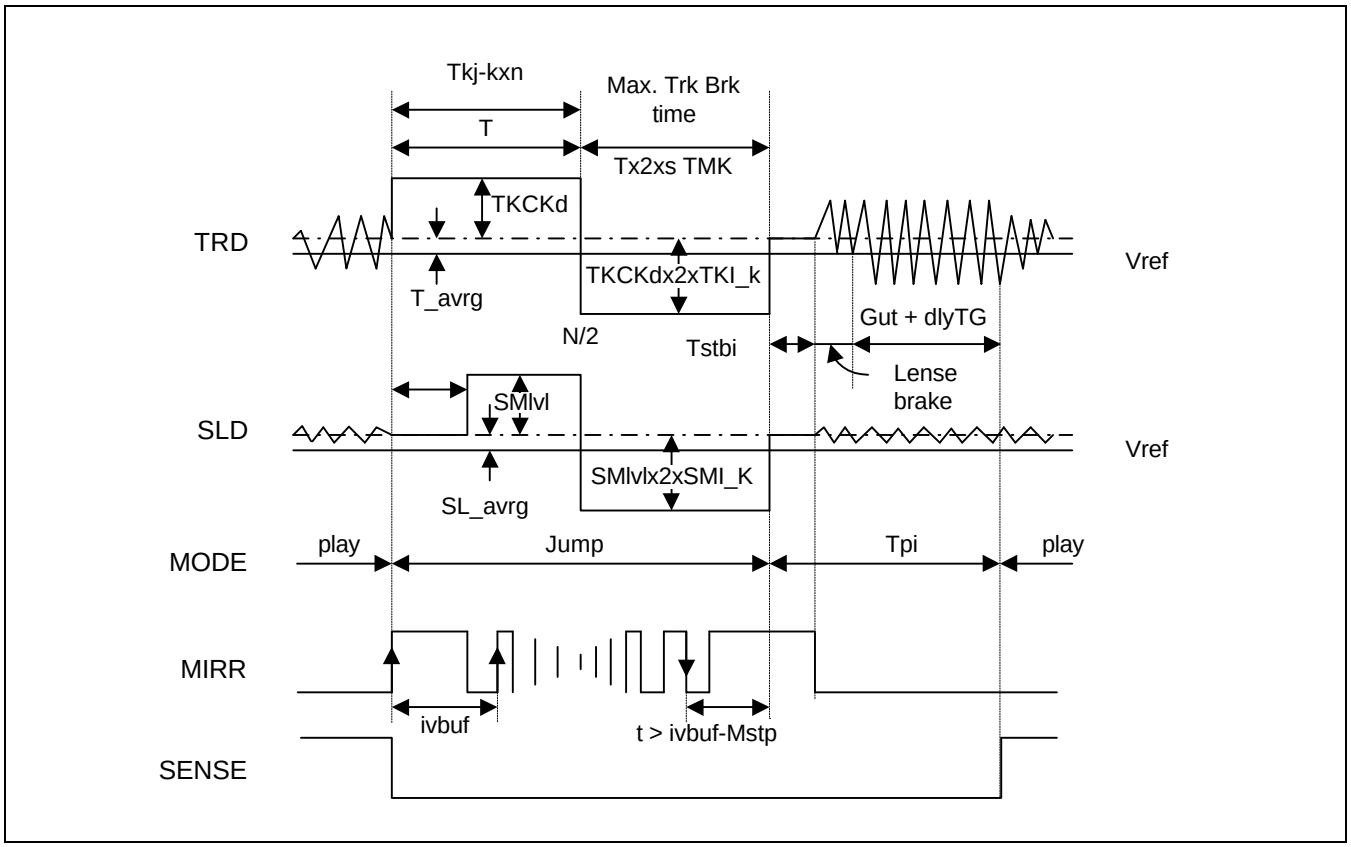


Figure 8.

If the track counter (H.CT) has a reverse count value (GSkbf), results from the number of jump trk(n)×TKj_k, trk kick pulse which is TRD output after TRD average before jump (TRD_avrg), are added to the kick level (TKCKd), changed to brake, and its level becomes as much as TKCKd×2×TKl_k times.
During brake period, if the mirror period is less than the trk completion condition at mirror edge, tracking reverses again. Then tracking goes back to where it was, and makes pull-in unstable because of excessive brake period. Therefore, if maximum brake time is limited as kick time (T) ×2×sTMK, the extreme energy difference between acceleration and brake cannot occur.
If the number of moving tracks by track kick reaches SMcnt, SL_avrg (the average value of SLED output before jump) is accumulated to the SMlvl (sled move level)'s kick, sled is changed to brake at the same time that track kick is changed to brake, and its level is determined by SMlvl×2×SMl_k.
The limit of kick/brake period is shared with the tracking setting condition. However, SMcnt doesn't make the sled move if the number of track jump is small, but sets the number of tracks to jump only by lens. After the stabilization time, the track pull-in (Tpi_int) routine starts. If Tstbl is carried out, GuT is set and then tracking gain up (in case of STRG = H) is done, but if there is a lens brake (MIRR), GuT is re-loaded continuously. Therefore, focus gain down (when SFOG = H) from starting jump should be returned to normal after the period from the completion of lens brake to GuT. After that, if dlyTG is passed, tracking gain should also be returned to normal, then go to normal play mode. The reason for the time difference is that dlyTG, between converting time of focus gain and that of tracking gain, prevents the system from emergency situations such as tracking oscillation and focus drop result from tracking gain converting under the unstable focusing on converting, or right after transition characteristics for focus gain.
The maximum brake window (T×2×sTMk) is the maximum brake time. It is used for preventing returning to an excessive brake or an unstable state unless the brake is finished by the condition t < ivbuf-Mstp.

Register	Address	Function	Default	Value
TKCKd	10C0h	Initial kick level	0A00h	195mV
SMlvl	10C3h	Sled move level during track jump	5000h	1.56V
Tkj_k	0025h	Kick/brk duty setting coefficient	3D00h	47.70%
TKl_k	002Ah	Trk brake level adjustment coefficient	4000h	50%×2
SMl_k	002Bh	Sled brake level adjustment coefficient	C000h	-50%×2
SMbrkl	002Ch	Brake level adjustment coefficient during sled move	0008h	0.00%
fsTjN	00BAh	Number of track for forced completion of Brk	0003h	3 trk
sTMk	00DAh	Trk brake window time note 1)	5000h	62.5%×2
LbT	10A0h	Lens brake start time	0018h	271ms
Tstbl	10A2h	Stabilization time after Trk jump	0000h	0us
Twin	10A3h	MIRR/TZC blind time	000Ah	113us
Mstp	10A4h	Compensation time during jump	0003h	33.9us
GuT	10A5h	Tgup delay time after jump	00A9h	1.9ms
Jstp	10A6h	Stop when Tracking jump's stop timer < MIRR period	0018h	271ms
dlyTG	10A7h	Delay time after GuT	0060h	1.04ms
tJap	10A8h	Jump assist procedure time (at this time, enMH=SLST=0)	024Ch	79.7ms
Cchg	10B8h	# of track for Cout (up/dn) and TZC/MIRR (up) selection	0080h	128 trk
Bound	10B9h	# of boundary track for Trk jump and sled move	0080h	128 trk
SMcnt	10BBh	# of track from Trk kick to sled move start	0001h	1 trk
SScnt	10BCh	Brake if remaining # of tracks is less than SScnt during sled move	0200h	512 trk
Sbrk	005Bh	Bbrake max time when sled move	2380h	103 ms

NOTE: max. trk brk time = T × 2 × sTMk (T = kick time)

The completion condition of jump is ivbuf-Mstp if BTS (INIcmd) is 'L', and Jstp-Mstp if BTS is 'H'. TM1, the down counter for jump stop frequency (MIRR ↓ to ↓) detection before Twin is Jstp, but is replaced by either ivbuf or Jstp according to BTS after Twin.

· **EMEcmd (Address 07H)**

This command orders the emergency handling of defects and shocks.

Command		DH1				DH0				DL
Name	**code**	**DH7**	**DH6**	**DH5**	**DH4**	**DH3**	**DH2**	**DH1**	**DH0**	**DL7 - DL0**
EMEcmd	07	Teset	SLST	DFavrg	upFv	dsAS	ASFO	ASTR	ASBR	

.Test : Filter test mode select (set at FTSTcmd).
L : Normal mode.
H : Filter test mode.

.SLST : Bit that decides whether or not the LOCK signal should stop the sled when off.
L : Do not stop.
H : Stop.

.DFavrg : FE/TE average filter hold selection according to DFCT/ATSC/FOK/MIRR.
L : Hold.
H : Do not hold (performs average filter function).

.upFv : Orders focus output offset: FSval adjustment during focus pull-in.
L : Do not adjust (during the value measured by focus search).
H : Adjust.

.dsAS : Decides whether or not to carry out Anti-shock handling.
L : Enable.
H : Disable. ¡Ø Features are selected in conjunction with TONcmds /TRPI bit.

/TRPI	dsAS	Function
0	0	Carry out track pull-in only during ATSC period using kick pulse.
0	1	When MIRR is detected, carry out tracking pull-in using the kick pulse apart from the defect period.
1	0	Make the ASFO, ASTR, and ASBR features valid.
1	1	Leave it to Servo and do not proceed (Anti-shock and kick pulse using tracking pull-in are prohibited).

.ASFO : Bit that decides whether or not to down the focus gain in case of Shock.
L : Maintain focus gain at normal.
H : Down the focus gain.

.ASTR : Bit that decides whether or not to up the tracking gain in case of shock.
L : Maintain tracking gain at normal.
H : Up the tracking gain.

.ASBR : Bt that decides whether or not to activate the lens brake during the anti-shock period.
L : Do not activate.
H : Activate.

Register	Address	Function	Default	Value
tDFCT	0057h	TGup hold time for LOCK off when DFCT	0800h	277ms
DFCTpd	10AAh	Set DFCT handling time after DFCT	0040h	723us
ATSCd	10ABh	Set ATSC handling time after ATSC	0400h	11.6ms
AS_J	10CBh	Shock detection acceptance level	1800h	468mV

- **HDWcmd (Address 08H)**

Carries out the initialization of the DSSP core. This command is generated by the first command after reset removal. It is impossible to generate this command at a status other than STBY.

Command		DH1				DH0				DL
Name	**code**	**DH7**	**DH6**	**DH5**	**DH4**	**DH3**	**DH2**	**DH1**	**DH0**	**DL7 - DL0**
HDWcmd	08	PN	SSTOP	enASin		PCUP		SLbrk		

.PN : Factor that is sent to RF. Value that sets the Laser Diodes P-sub/N-sub type.
L : P-sub.
H : N-sub.

.SSTOP : Can be selected since the limit switch's active H/L is different according to Mecha.
L : High active.
H : Low active.

.DH4, DH2, DH0 : Don't care.

.enASin : Shock detection signal (Anti-shock filter) selection.
L : Shock is detected by calculation of the built-in filter.
H : Shock is detected by a filter outside and a comparator-using signal: ATSC.

.PCUP : Pick-up type.
L : Pick-up which is robust against shock.
H : Pick-up which is not robust against shock.

.SLbrk : Choose either 0 or a non-zero value according to TRD output as zero for SLE during lens brake.
L : Do not consider lens brake.
H : Zero input to SLE during lens brake.

· **INIcmd (Address 09H)**

This command sets the initial values.

Command		DH1				DH0				DL
Name	**code**	**DH7**	**DH6**	**DH5**	**DH4**	**DH3**	**DH2**	**DH1**	**DH0**	**DL7 - DL0**
INIcmd	09	SLDO	JPCK	TKJM	JPEC	BJJM	BTS	enJaP	MHsel	

.SLDO : Sled drive output select during speed control track jump.
L : Output as is.
H : Output through sled filter.

.JPCK : Signal used for track search/count during sled move select.
L : TZC.
H : MIRR.

.TKJM : Tracking jump method select.
L : No speed control (kick/brake).
H : Speed control.

.JPEC : Decides whether or not the errors in speed control during search should be adjusted.
L : Do not adjust search.
H : Adjust search.

.BJJM : Selects whether to change the remaining track number to track jump after track search.
L : Continue sled move.
H : Carry out sled move + track jump.

✻ After carrying out sled move using TZC/MIRR, if the remaining track number is less than the Bound selected by OKScmd, it is changed to track jump.

.BTS :
L : Stop if the TZC period that decides the point for stop during tracking kick/jump is the same as the MIRR period at kick start.
H : Stop if the TZC period that decides the point for stop during tracking kick/jump is the same as Jstp selected by TMScmd (0CH).

.enJap :
L : Do not make enMH = 0 and SLST = 0 during tJaP after Track search.
H : Make enMH = 0 and SLST = 0 during tJaP after Track search.

.MHsel : Selects interruption flag.
L : MIRR (below 11 MHz).
H : CPEAK from EFM.

- **MSCcmd (Address 0AH)**

This is a command that can select and read things related to automatic adjustment, and system parameters as well.

Command		DH1				DH0				DL
Name	code	DH7	DH6	DH5	DH4	DH3	DH2	DH1	DH0	DL7 - DL0
MSCcmd	0A	MD11	MD10	MD9	MD8	MD7	MD6	MD5	MD4	MD3-MD0, MSS3-MSS0

.MSS3 - MSS0 : Select bit for RAM (Object) to be selected.

.MD11 - MD0 : Data to Write (FFFh is not written; instead, it becomes read).
Data read method : Set all 12 data bits (MD11-MD0) to "1".
Example) If you send 0AFFF3, 16-bit data tOFa is read.
Data write method : Select all data except when MD11-MD0's are all "1", then select the location to write to MSS3 - 0.
Example) If you send 0A0402, data 0400 is written in tDFCT.
The object decides whether the data during write is written in the upper 12 bits of the target RAM or the lower 12 bits (Refer to the table below).

MSS3-0	Name	Contents	Default	Area	RAM Addr.
0000	FSpk	Peak level during focus search/kick (jump)	4000	upper	0055
0001	tHBwd	SSTOP is on if in an inward jump, then sets backward move time	1833	upper	0056
0010	tDFCT	Tracking gain up holding time during DFCT	0800	upper	0057
0011	tOFa	Offset adjustment time	0FF0	upper	0058
0100	FBpd	Focus balance adjust repeat period	0172	upper	0059
0101	TBwt	Tracking balance adjust repeat standby time	1000	upper	005A
0110	Sbrk	Break max time for sled move using MIRR/TRZ (at tc_int)	2380	upper	005B
0111	FGmax	Focus gain control: output gain maximum value	7000	upper	005C
1000	FGmin	Focus gain control: output gain minimum value	0800	upper	005D
1001	TGmax	Tracking gain control: output gain maximum value	7000	upper	005E
1010	TGmin	Tracking gain control: output gain minimum value	0800	upper	005F
1011	tTpi	Pull-in confirmation time when carrying out track pull-in using kick pulse	0030	lower	0060
1100	nTbal	Number of average track number (cycle number) when controlling tracking balance	0010	lower	0061
1101	-	-			0062
1110	Ffrq	Focus auto gain control 0 dB frequency	0008	lower	0043
1111	Tfrq	Track auto gain control 0 dB frequency	000B	lower	0047

NOTE: Select time = (interrupt frequency) × (select value) = 11.3 usec × (select value)
Except, tDFCT, FBpd are 12x = 136 usec × (select value)

- **SPDcmd (Address 0BH)**

This command selects the playback speed. One of two types of filter coefficients is chosen by this command. Since this command can be generated at any time, the speed can be changed at any time as well.

Command		DH1				DH0				DL
Name	code	DH7	DH6	DH5	DH4	DH3	DH2	DH1	DH0	DL7 - DL0
SPDcmd	0B	0	0	0	0	0	0	0	SPD	

.DH7 - 1 : Reserved. Must set to L.

.SPD : Playback speed select bit.
0 : 1x (RAM address pointer = 8X - BX)
1 : 2x (RAM address pointer = CX - FX)

This command only carries out the selection of the filter coefficient set that is actually used, and the rotation speed is set at the CD-DSP block.

· **TMScmd (Address 0CH)**

This command selects and refers to the timer used in the system.

Command		DH1				DH0				DL
Name	**code**	**DH7**	**DH6**	**DH5**	**DH4**	**DH3**	**DH2**	**DH1**	**DH0**	**DL7 - DL0**
TMScmd	0C	TD11	TD10	TD9	TD8	TD7	TD6	TD5	TD4	TD3-TD0, TMS3-TMS0

.TMS3 - 0 : RAM (Object) select bit.

.TD11 - TD0 : Lower 12 bit data to be written (FFFh is not written, but read).
Data read method: Set TD11 - TD0 to "1".
Example) If 0CFFF3 is sent, 16-bit data Twin is read
Data write method: Select all data apart from when TD11-TD0 are all "1", and select TMS3 — 0 as the place to write.
Example) If 0C0023 is sent, data 0002 is written in Twin.

TMS3-0	Name	Contents	Default	Area	RAM Addr.
0000	LbT	Lens brake time	0030	lower	10A0
0001	tFpi	Delay time from focus pull-in to tracking pull-in	0014	lower	10A1
0010	Tstbl	Stabilization time for track jump	0000	lower	10A2
0011	Twin	TZC blind time select during track jump	000A	lower	10A3
0100	Mstp	Stop when stop timer of tracking jump is less than MIRR period	0003	lower	10A4
0101	GuT	Track gain up time after jump	00A9	lower	10A5
0110	Jstp	Stop timer of tracking jump. Stop at MIRR period	0018	lower	10A6
0111	dlyTG	Delay time from focus gain to tracking gain normal	0060	lower	10A7
1000	tJap	Jump assist procedure time (at this time, enMH=SLST=0)	024C	lower	10A8
1001	tHFwd	Forward move time select after Home in	0FF0	lower	10A9
1010	DFCTpd	DFCT repeat handling time select after DFCT	0040	lower	10AA
1011	ATSCd	ATSC repeat handling time select after ATSC	0400	lower	10AB
1100	FLoff	FLKB off delay time select	0172	lower	10AC
1101	FLon	FLKB on delay time select	000A	lower	10AD
1110	TLoff	TLKB off delay time select	0001	lower	10AE
1111	TLon	TLKB on delay time select	0100	lower	10AF

NOTE: Setting time = (interrupt period) × (select value) = (select value) × 11.3 us
(In the case of tJaP = (select value) × 136 us)

During DFCTed (= DFCT+DFCTpd), functions such as track pull-in in case of track off, retrying focus pull-in when FOK = L, ATSC process, and TE hold in case of MIRR do not have to be performed like a case of DFCT.

· **OKScmd (Address 0DH)**

This command selects and refers to the allowance and boundary values of an automatic adjustment.

Command		DH1				DH0				DL
Name	**code**	**DH7**	**DH6**	**DH5**	**DH4**	**DH3**	**DH2**	**DH1**	**DH0**	**DL7 - DL0**
OKScmd	0D	0D11	0D10	0D9	0D8	0D7	0D6	0D5	0D4	0D3—0D0, 0KS3—0KS0

. 0KS3 - 0: RAM (Object) select bit.

. 0D11 - 0D0: Lower 12-bit data to write (FFFh is not written, but becomes read).
Data read method: Set 0D11-0D0s data 12 bits to 1.
Example) If 0CFFF3 is sent, 16 bit data TGok is read.
Data write method: Select all data apart from when 0D11 — 0D0s data 12 bits are all 1, and select 0KS3 — 0 as the place to write.
Example) If you send 0D0023, data 0002 is written in Tgok.

OKS3-0	Name	Contents	Default	Area	RAM Addr.
0000	FBok	Focus balance OK level	0800	lower	10B0
0001	TBok	Tracking balance OK level	0200	lower	10B1
0010	FGok	Focus gain OK level	0080	lower	10B2
0011	TGok	Tracking gain OK level	0080	lower	10B3
0100	-	-	-		10B4
0101	FSjspd	Focus search MAX and MIN speed control: lower 3 bits. Speed tables track number/step assignment: upper 13 bits.	2003	lower upper	10B5
0110	TSjspd	Track search MAX and MIN speed control: lower 3 bits. Speed tables track number/step assignment: upper 13 bits.	2003	lower upper	10B6
0111	-	-	-		10B7
1000	Cchg	H/W track counters input/feature track number. Noise free/up down < Cchg < TZC/MIRR direct up count.	0080	lower	10B8
1001	bound	Boundary track number between track jump and fine search	0080	lower	10B9
1010	-	-	-		10BA
1011	SMcnt	Time from after track kick to sled move	0001	lower	10BB
1100	SScnt	Sled stop count: When using MIRR/TZC and when the number of remaining tracks in sled move becomes less than SScnt, brake is activated.	0200	lower	10BC
1101	Cout	Track count divisor if in manual sled move	0000	lower	10BD
1110	-	-	-	lower	10BE
1111	-	-	-	lower	10BF

NOTE: Cout is only n power of 2 where n = 0, 1, 2, ...
FSjspd and TSjspds track number/step are in powers of 2 (decrease 1 from number of 0)

· **AJKcmd (Address 0EH)**

This command sets and refers to the system coefficients that decide the kick level.

Command		DH1				DH0				DL
Name	**code**	**DH7**	**DH6**	**DH5**	**DH4**	**DH3**	**DH2**	**DH1**	**DH0**	**DL7 - DL0**
AJKcmd	0E	AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4	AD3 - AD0, AJS3 - AJS0

.AJS3 - 0 : Select bit for RAM (Object) to be set.

.AD11 - 0 : Lower 12 bit data to write (FFFh is not written but read) lower 4 bit = "0".
Data read method: Set AD11 - AD0s data 12 bits to 1.
Example) If 0CFFF3 is sent, 16 bit data TSj_k is read
Data write method: Select all data apart from when AD11 — AD0s data 12 bits are all "1", and select AJS3 - 0 as the place to write.
Example) If you send 0E3003, data 3000 is written in TSj_k.

AJS3-0	Name	Contents	Default	Area	RAM Addr.
0000	-	-	-		0024
0001	TKj_k	Track kicks acceleration period coefficient: Accelerate until count = N×TKj_k.	3D00	upper	0025
0010	FSj_k	Speed control fine searches: Speed difference return gain coefficient.	1800	upper	0026
0011	TSj_k	Gain adjustment coefficient in tracking speed control jump.	1800	upper	0027
0100	-	-	-		0028
0101	SL_k	Sled move acceleration period coefficient: Accelerate until Count = N×SL.	5000	upper	0029
0110	TKl_k	Tracking brake level coefficient: 2×TKl_k times the kick level.	4000	upper	002A
0111	SMl_k	Sled brake level count number during track jump: 2×smL_Kx. Speed control track jumps filtered sled output coefficient: 32×SMl_k.	C000	upper	002B
1000	SMbrkl	Sled brake level coefficient	0008	upper	002C
1001	-	-	-		002D
1010	-	-	-		002E
1011	dXbuf	Fbal lowered value's initial value at focus balance adjustment	0800	upper	002F
1100	FBk	Focus balance adjustment error return gain coefficient at DDT	7FFF	upper	0030
1101	TBk	Track balance adjustment error return gain coefficient	0A00	upper	0031
1110	Kcf	Focus gain adjustment error return gain coefficient	4000	upper	0032
1111	Kct	track gain adjustment error return gain coefficient	4000	upper	0033

· **LEScmd (Address 0FH)**

This command sets and refers to the different levels and decision values.

Command		DH1				DH0				DL
Name	**code**	**DH7**	**DH6**	**DH5**	**DH4**	**DH3**	**DH2**	**DH1**	**DH0**	**DL7 - DL0**
LEScmd	0F	LD11	LD10	LD9	LD8	LD7	LD6	LD5	LD4	LD3 - LD0, LES3 - LES0

.LES3 - 0 : RAM (Object) select bit.

.LD11 - 0 : Lower 12 bit data to write (FFFh is not written but read). Lower 4 bits = 0.
Data read method: Set LD11 — LD0s data 12 bits to 1.
Example) If 0FFF3 is sent, 16 bit data SMlvl is read.
Data write method: Select all data apart from when LD11-LD0s data 12 bits are all 1, and select LES3 — 0 as the place to write.
Example) If you send 0F4003, data 4000 is written in SMlvl.

LES3-0	Name	Contents	Default	Area	RAM Addr.
0000	TKCKd	Track jump and track pull-in: Tpi's track kick level	0A00	upper	10C0
0001	SKCKd	Sled move and sled pull-in: Spi's sled kick level	6000	upper	10C1
0010	TKlvl	Track kick level at speed control l track jump	7000	upper	10C2
0011	SMlvl	Sled kick level during track jump Sled kick level during sled move	5000	upper	10C3
0100	xGwt	Loop gain adjust: Repeat delay time (cycle number-1)	0018	upper	10C4
0101	xGcnt	Loop gain adjust: Measuring time (cycle number)	000A	upper	10C5
0110	FSrng	Search range for focus pull-in	3000	upper	10C6
0111	-	-			10C7
1000	DDT_J	Disc presence detect level	1800	upper	10C8
1001	-	-			10C9
1010	-	-			10CA
1011	AS_J	Shock detect decision level	1800	upper	10CB
1100	NZlvl	Level seen as noise during focus search	0800	upper	10CC
1101	-	-	-		10CD
1110	-	-	-		10CE
1111	FZCofs	Focus zero cross offset level	0A00	upper	10CF

· **AARWcmd (Address 10H)**

This command can refer to and change the values that have been adjusted and measured by Auto adjustment.

Command		DH1				DH0				DL
Name	code	DH7	DH6	DH5	DH4	DH3	DH2	DH1	DH0	DL7 - DL0
AARWcmd	10	AA11	AA10	AA9	AA8	AA7	AA6	AA5	AA4	AA3 - AA0, AAS3 - AAS0

.AAS3 - 0 : RAM (Object) select bit.

.AA11 - 0 : Data to write (FFFh is not written but read). Lower 4 bits = "0".
Data read method: Set AA11-AA0s data 12 bits to "1".
Example) If 10FFF3 is sent, 16 bit data Tofst is read.
Data write method: Select all data apart from when AA11 - AA0s data 12 bits are all "1", and select AAS3 — 0 as the place to write.
Example) If you send 104003, data 4000 is written in Tofst.

AAS3 - 0	Name	Contents	Default	Area	RAM Addr.
0000	Fin_G	Focus input gain	0000	upper	1008
0001	Tin_G	Tracking input gain	0000	upper	1009
0010	Fofst	Focus offset	0000	upper	1083
0011	Tofst	Tracking offset	0000	upper	1085
0100	Fbal	Focus balance	0000	upper	1086
0101	Tbal	Tracking balance	0000	upper	1087
0110	Fbias	Focus bias	0000	upper	1088
0111	Tbias	Tracking bias	0000	upper	1089
1000	FODbias	Focus output bias	0000	upper	1090
1001	TRavrg	Tracking output average	0000	upper	10F3
1010	SLavrg	Sled output average	0000	upper	1095
1011	SPin	Spindle error input	0000	upper	10FA
1100	GND	Vref level offset for POT	0000	upper	1081
1101	-				108D
1110	RF_env	RF envelope average result	0000	upper	1093
1111	DDTdt	Response data after disc detect	0000	lower	100A

· **OFAcmd (Address 11H)**

This command adjusts the focus/tracking offset. This command can be received only in focus off status. This command turns the laser diode "on", and in that state, it measures the t0Fa, the time average value of the Focus Error/Tracking Error including the electric offset. The difference between the error input and the value found above should be designated as the error.
Even after the adjustment is finished, STANDBY mode is maintained while the Laser Diode is on.
Some time is needed until the laser output is stabilized, after the Laser Diode is turned on. First adjust the tracking offset, then adjust the focus offset.
While tracking offset adjust measures mostly electrical offset, the focus offset adjust measures the error level of the off focus, since the DDTcmd to be carried out next uses that value.

Command		DH1				DH0				DL
Name	**code**	**DH7**	**DH6**	**DH5**	**DH4**	**DH3**	**DH2**	**DH1**	**DH0**	**DL7 - DL0**
OFAcmd	11	FTS	LDoff							

.FTS : Focus or Tracking offset adjust select.
L : Focus offset adjust.
H : Tracking offset adjust.

.LDoff : Select offset measurement in case of LD on/off state.
L : LD on.
H : LD off.

.DH6 - 0 : Don't care.

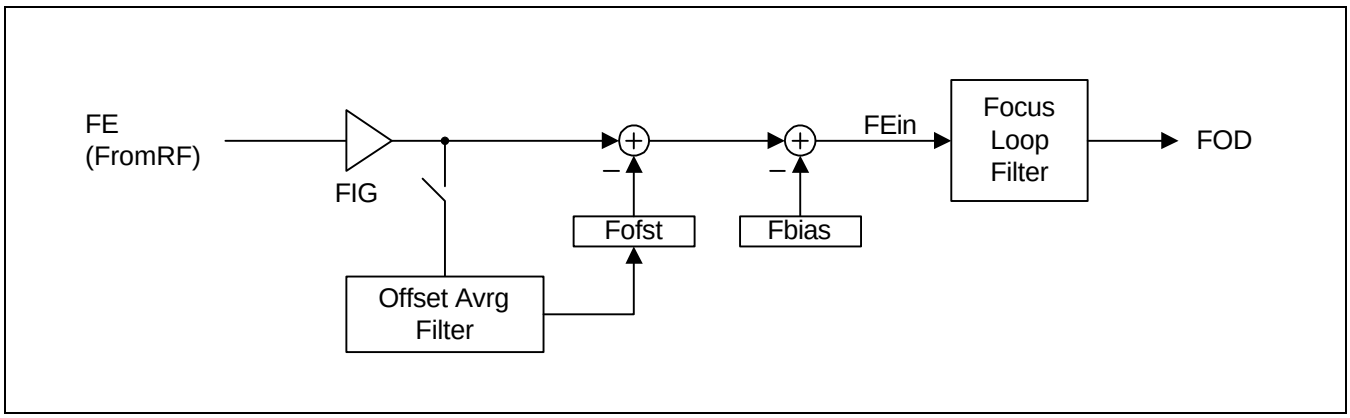


Figure 9.

Register	Address	Function	Default	Value
ofst K0	003Dh	New data gain (K0 = 1-K) for offset average filter	0050h	-
ofst K	003Ch	Old data gain for offset average filter	7FA0h	-
tOFa	0058h	Offset measure time (average measure time)	0FF0h	46.2 ms

· **FBAcmd (Address 12H)**

This command adjusts the focus balance. It receives and executes in playback status.

Disc Detect: Even in DDTcmd, the balance adjust is carried out so that the peak and bottom sizes are the same, but the method supported by this command makes the following adjustments so that the peak level shown in the RF signal's envelope is at its maximum.
Focus balance: Adjusts Fbal output voltage (Fbmthd = 0).
Focus bias: Adjusts focus pull-in point according to Fbias (Fbmthd = 1).

Command		DH1				DH0				DL
Name	code	DH7	DH6	DH5	DH4	DH3	DH2	DH1	DH0	DL7 - DL0
FBAcmd	12									

Selecting method is chosen by the focus balance method (Fbmthd bit) of the flag command (FLGcmd). In any case, the relationship between FBpd (Measure frequency at RF amp) and the cutoff frequency of the RF envelope average filter should be proper.
The figure below shows the flow when bias control is selected.

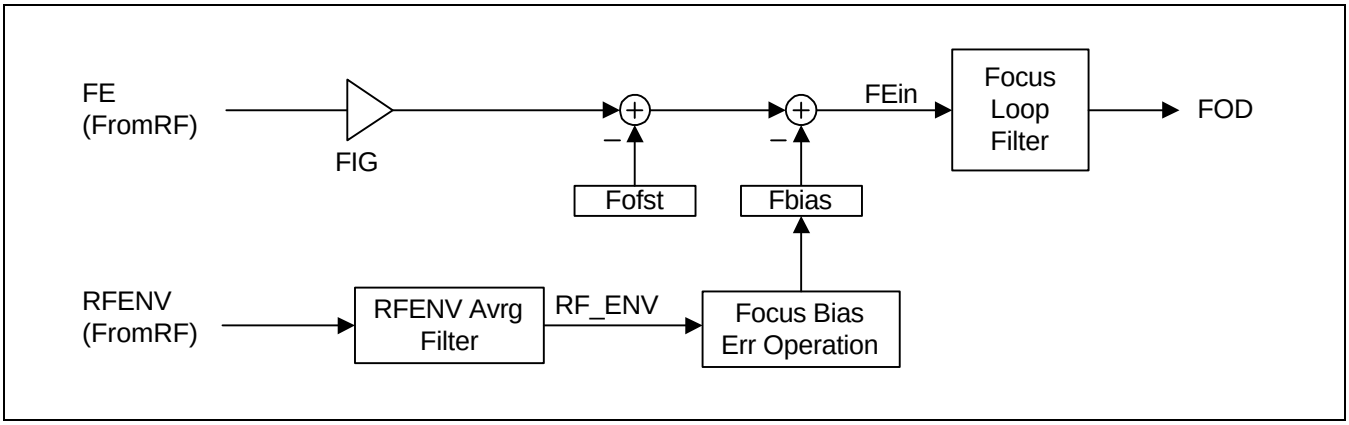


Figure 10.

Register	Address	Function	Default	Value
FBpd	0059h	RFENV measure frequency for focus bias control	0172h	50 ms
FBok	10B0h	Focus bias OK level	0800h	-
dXbuf	002Fh	Initial dX setting level	0800h	-

¨ **Manual focus balance control :**

While FBAcmd can enable automatic focus balance control by holding RF envelope peak during tracking on, the RF envelope level can be read out (AARWcmd AAS = "E") during play, making manual focus balance control possible.

· **TBAcmd (Address 13H)**

This command adjusts the tracking balance. It is received and executed while focus is on. The following adjustments are made so that within a specific frequency range, the average value of a peak and bottom size nTbal cycle and a tracking error signal during off-track are the same.

Track balance: Adjusts the Tbal output (repeat: RPTB = 0).

Track bias: Selects Tbias and subtracts it from TE input (Tbmthd = 1).

Track balance: To change and adjust the Tbal output, an RF AMP that can interact with it is necessary. On the other hand, the method subtracting the bias does not select an RF AMP.
Flag command (FLGcmd)'s tracking balance method (Tbmthd) bit decides which method to use. In the case of the bias method, adjustment is finished after measuring once.

Command		DH1				DH0				DL
Name	**code**	**DH7**	**DH6**	**DH5**	**DH4**	**DH3**	**DH2**	**DH1**	**DH0**	**DL7 - DL0**
TBAcmd	13	*TIGA*	*RPTB*							

./TIGA :
L : Tracking input gain adjust according to the TE signal peak value level.
H : Do not adjust tracking input gain.

./RPTB : Decides if the tracking balance adjustment will be repeated.
L : Repeat is carried out from after the stable period (TBwt). Wait until the error falls beneath the value allowed (TBok).
H : Do not repeat.

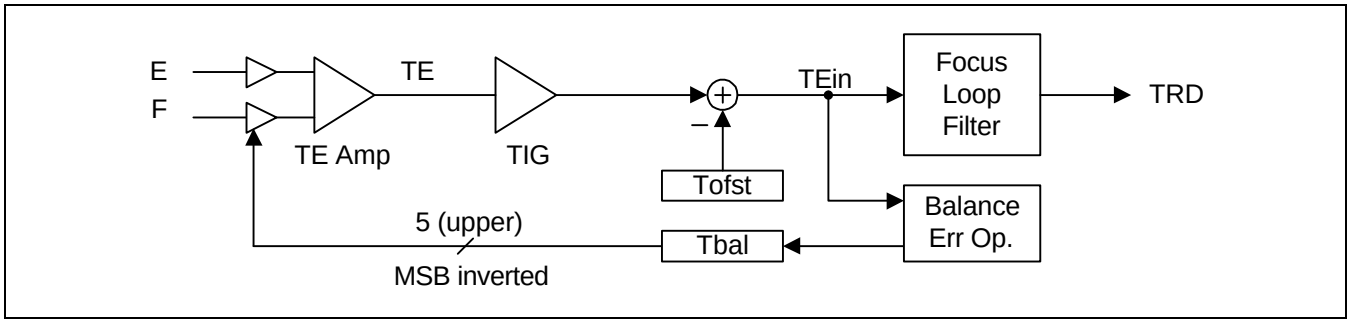


Figure 11.

Register	Address	Function	Default	Value
nTbal	0061h	TZC cycle number for one time balance err detection	0010h	16 trk
TBwt	005Ah	Wait time from Tbal change to re-measurement	1000h	46.4ms
TBok	10B1h	T_bal ok level (allowance error)	0200h	± 40mV
TBk	0031h	Trk balance control sensitivity coefficient	0A00h	125%
Tengh	004Fh	Minimum limit of TZC	1000h	312mV
fmin	0009h	Minimum frequency for TZC detection	00F6h	359Hz
fmax	000Ah	Maximum frequency for TZC detection	0018h	3.68kHz

✻ nTbal should be 2^n

- **FGAcmd (Address 14H)**

This command adjusts the auto focus gain. It is transmitted and carried out during playback.
The frequency amplitude in the servo loop's (Kf) measured wave (Kf×sin(Fwave)) is overlapped. After stabilizing the FGwt cycle, the detected signals phase errors are accumulated during the FGcnt cycle. Until the result of the accumulation falls below the allowed value (FGok), the product of the return gain count number (Kcf) to the phase error and the output gain are calculated to the gain. This is repeated until the loop gain becomes Ffrg frequency 0 dB.

Command		DH1				DH0				DL
Name	code	DH7	DH6	DH5	DH4	DH3	DH2	DH1	DH0	DL7 ~ DL0
FGAcmd	14									

Block diagram of Loop gain control is as follows (same for both focus and tracking).

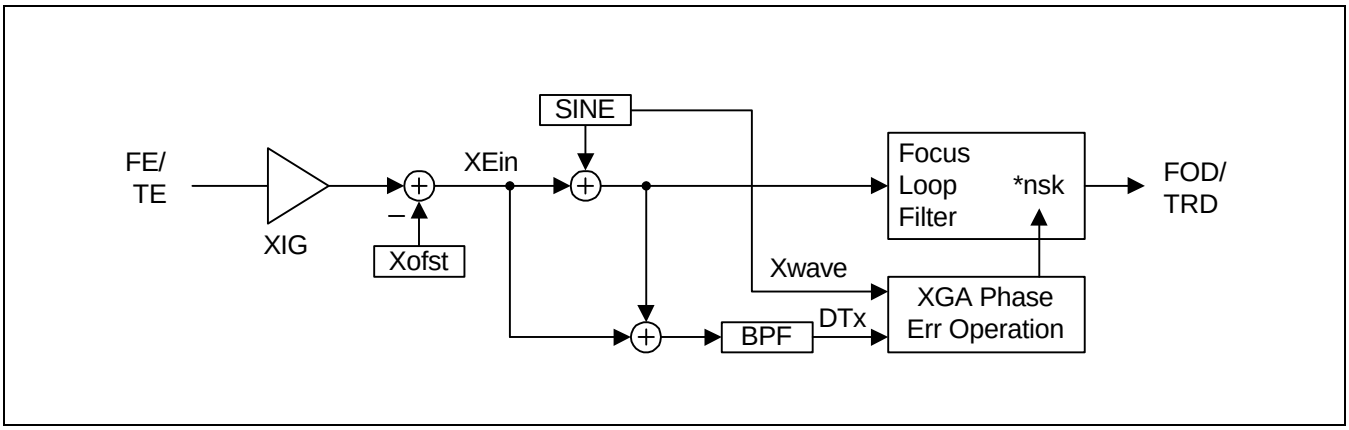


Figure 12.

Register	Address	Function	Default	Value
xGcnt	10C5h	Measuring frequency	000Ah	10 times
xGwt	10C4h	Wait time	0018h	24 times
Ffrq	0043h	Focus loop bandwidth (sine frequency)	000Ah	997.7Hz
Kf	0045h	F_gain (sine)disturbance level	1000h	625mVpp
Kcf	0032h	F_gain control sensitivity coefficient	4000h	0.5
FGok	10B2	F_gain control OK level	0080h	
FGmax	005Ch	Upper limit of F_gain control	7000h	nsk
FGmin	005Dh	Lower limit of F_gain control	0800h	nsk

NOTE: Perform 10 times of one cycle of a sine table.

- **TGAcmd (Address 15H)**

This command adjusts the auto tracking gain. It is transmitted and carried out during playback.
The frequency amplitude in the servo loop's (Kt) measured wave (Kt×sin(Twave)) is overlapped. After stabilizing the TGwt cycle, the detected signals phase errors are accumulated during the TGcnt cycle. Until the result of the accumulation falls below the allowed value (TGok), the product of the return gain count number (Kct) to the phase error and the output gain are calculated to the gain. This is repeated until the loop gain becomes Tfrq frequency 0 dB.

Command		DH1				DH0				DL
Name	**code**	**DH7**	**DH6**	**DH5**	**DH4**	**DH3**	**DH2**	**DH1**	**DH0**	**DL7 - DL0**
TGAcmd	15									

- **SQDTcmd (Address 18H)**

This command can select the signal that is output to the SQDT pin. Therefore signals SQDT, FOKB, and LKFS can be selected according to the request of Micro Controller.

Command		DH1				DH0				DL
Name	**code**	**DH7**	**DH6**	**DH5**	**DH4**	**DH3**	**DH2**	**DH1**	**DH0**	**DL7 - DL0**
SQDTcmd	18							SQDT1	SQDT0	

.SQDT1 - 0: The output of SQDT pin is determined by SQDT1 - 0 as follows.

SQDT1 - 0	SENSE Output
00	SQDT
01	FOKB
10	LKFS
11	SQDT

FOKB and LKFS selected by this command can be monitored by SNScmd (address19H) through the SENSEB pin. After jump command, MICRO CONTROLLER must monitor the SENSEB pin steadily to check whether a jump is finished or not. So during that time, FOKB and LKFS cannot be monitored through the SENSEB pin. Using this command, Micro Controller can check the status of focus drop and LOCK off without using the ports FOKB and LKFS.

- **SNScmd (Address 19H)**

This command can select the signal that is output to the SENSEB pin. Therefore the signals Cout, FOKB, LKFS, S0S1, and TLKB can be selected according to the request of Micro Controller.

Command		DH1				DH0				DL
Name	code	DH7	DH6	DH5	DH4	DH3	DH2	DH1	DH0	DL7 - DL0
SNScmd	19	0	0	0	0	0	SNS2	SNS1	SNS0	[0000 00:Ssel:0]

.SNS2 - 0, Ssel: The output of the SENSEB pin is determined by the combination of SNS2 — 0 and Ssel.

SENSE Output	SNS2 - 0 (SNSsel)	Ssel
ST5	000	0
Sout	001	0
Cout	010	0
Sout	011	0
FOKB	100	0
LKFS	101	0
S0S1	110	0
TLKB	111	0
Serial	XXX	1

When this command is used, the other bits should be set to zero.

· **FLGcmd (Address 1AH)**

This command refers to and changes the flags within the DSSP system.

Command		DHH				DHL			
Name	**code**	**DH7**	**DH6**	**DH5**	**DH4**	**DH3**	**DH2**	**DH1**	**DH0**
FLGcmd	**1A**	stp	Fptmg		HOME	itvJ	TSV	SSV	enTJn
		DL							
		DL7	**DL6**	**DL5**	**DL4**	**DL3**	**DL2**	**DL1**	**DL0**
		DFCTed	ATSCed	Tbmthd	Fbmthd	enMH	FSend		enLOCK

♦ If the spindle motor is off (MON = "L"), turn each output Off and wait in STBY mode.
At this time, pull-in is impossible.

.Stp : Stop reservation flag.
L : Do not Stop.
H : Stop reservation.

.Fptmg : Select focus pull-in timing.
L : Pull-in again when out of FLK.
H : Pull-in again when out of FOK.

.HOME : Home location processing flag.
L : Home location process not active.
H : Home location process active.

.itvj : Interval jump flag.
L : Not in interval jump.
H : In interval jump.

.TSV : Track Servo flag.
L : Off
H : On

.SSV : Sled Servo flag.
L : Off
H : On

.enTJn : When jumping a set number of tracks.
L : Do not stop.
H : Stop.

.DFCTed : Defect period flag.
L : Not in Defect period.
H : In Defect period.

.ATSCed : Anti-shock period flag.
L : Not in Anti-shock period.
H : In anti-shock period.

.Tbmthd : Tracking balance adjustment method.
L : RF AMPs balance is controlled by the Tracking balance (Tbal).
H : Tracking error balance is corrected by subtracting the bias value.

.Fbmthd : Focus balance adjustment method.
L : RF AMPs balance is controlled by the focus balance (Fbal) output.
H : S-curves pull-in point is moved by subtracting the Bias value, in order to select the optimum spot.

.enMH : MIRR detection handling when tracking gain is normal in Playback (in case of Interruptions).
L : No Operation.
H : Hold the tracking error input at average value if MIRR is generated.

.FSend : Focus search end location select.
L : Vref (processing current = 0 location).
H : pull-in range (below FSrng) from the focus point.

.enLOCK : The tracking gain when the LOCK is dropped.
L : Normal.
H : Up.

- **SNSCcmd (Address 1BH)**

This command can select the signal that is output to the SENSEB pin, or monitor the DSSP internal data, which is not an output pin. Also, it can return the SENSEB output that was converted to jump SENSEB to its previous position in order to carry out non-DSSP commands after activating JMPcmd. In other words, it returns to jumps BUSY/READY.
The monitored data is analog output to sled output (SLD) through DAC, so real time observation is possible through an oscilloscope.
Using the monitor output gain command (TTKcmd = 57), monitoring not only the upper byte of the 16-bit data, but the lower byte as well (if Gain = 0040h, upper byte, and if 4000h, lower byte is output).
If you monitor using this command, the sled output (SLD) is used as monitor output. Therefore, when returning to the original sled output, you should use this command with the BANK & MOD7-0 all at "0", and at the same time, RWB = 0 (select SENSEB output only). Monitoring at address 000 is impossible, so after using this command, 1B00H must be entered.

Command		DH1				DH0				DL
Name	**code**	**DH7**	**DH6**	**DH5**	**DH4**	**DH3**	**DH2**	**DH1**	**DH0**	**DL7 - DL0**
SNSCcmd	1B	RWB		*NORM*	FTLK				BANK	MOD7-MOD0

.RWB : Input/output select of the RAM address you wish to monitor.
L : Write
H : Read

./NORM.FTLK : SENSEB pin's output control bit.
0 0 : Normal SENSEB output (READY/BUSY).
0 1 : Returns SENSEB to jump's /BUSY after carrying out non-DSSP commands such as jump.
1 0 : FLKB output.
1 1 : TLKB output.

.BANK : RAM bank with the data that you want to monitor.

.MOD7 - MOD0 : Address of the RAM bank with the data that you want to monitor.

Only thing that can be monitored is the internal RAM's PAGE0. PAGE1 only has invariable data such as coefficient data, so there is no need for monitoring.

- **DPRWcmd (Address 1CH)**

This command directly reads and writes at the DSSP input/output port. The functions for supporting R/W disc are included. That is, converting gain for RF and TE are performed by this command.

Command		DH1				DH0				DL
Name	code	DH7	DH6	DH5	DH4	DH3	DH2	DH1	DH0	DL7 - DL0
DPRWcmd	1C	DD11	DD10	DD9	DD8	DD7	DD6	DD5	DD4	DD3-0, ST6, DPS2-0

.ST6, DPS2 - 0 : Selection of output port.

.DD11-0 : Data to be input (No write for FFFh: perform read operation).

.Data input method : Set 1 for all DD11- 0 data 12bit. No relationship with ST6.
Example : Read after sending "1CFFF3". External status input can be read.

.ST6, DPS2-0
"X 0 0 0" : Read AD converted digital data of Analog input.
"X 0 0 1" : Read interrupt vector of free running counter.
"X 0 1 0" : -
"X 0 1 1" : Read external status.
"X 1 0 0" : Read count value of Hardware track counter HCT.
"X 1 0 1" : Read Micro Controller data.
"X 1 1 0" : Read Micro Controller command.
"X 1 1 1" : Reserved.

.Data output method : Set DD11 - 0 as anything except all "1", and select output to ST6, DPS2-0.
Example : If "1C100B" is sent, control register of DSSP is written as "0100", then laser is on.

.ST6, DPS2-0
"0 0 0 0" : Output upper 8 bits (DD11-4) of DD data to Focus drive (FOD).
"0 0 0 1" : Output upper 8 bits of DD data to Tracking drive (TRD).
"0 0 1 0" : Output upper 6 bits (DD11-6) of DD data to Sled drive (SLD).
"0 0 1 1" : Output upper 6 bits of DD data to Spindle drive (SPD).
"0 1 0 0" : Output upper 8 bits of DD data to Focus gain selection register (FIG) and Fin_G.
"0 1 0 1" : Output upper 8 bits of DD data to Tracking gain selection register (TIG) and Tin_G.
"0 1 1 0" : Output upper 8 bits as signals for RF function support.

RF[15] : AGC skip selection.
"L" : AGC skip.
"H" : Use AGC (default).

RF[14:13] : Determine TE block gain for RW disc support.
"0 0" : Normal, 1 time (default).
"0 1" : 2.5 times
"1 0" : 3.5 times
"1 1" : 5 times

RF[12:11] : Determine RF gain for RW disc support.

"0 0"	: Normal, 1 time (default).
"0 1"	: 2.5 times
"1 0"	: 3.5 times
"1 1"	: 5 times
"X 1 1 1"	: Reserved.
"1 0 0 0"	: Output lower 9 bits of DD data (DD8 - 0) to Analog selection register (Asel).
"1 0 0 1"	: Output lower 8 bits of DD data (DD7 - 0) to Interrupt vector register (VCT).
"1 0 1 0"	: Reserved
"1 0 1 1"	: Output upper 4 bits of both DSSP control output and CNTbuf as all zero, and DD11 - 0 to their lower 12 bits.
"1 1 0 0"	: Clear Hardware track counter H.CT as "0000H".
"1 1 0 1"	: Output DD11 - 0 for 12 bits of register to Micro Controller, and "D" for lower 4 bits of it.
"1 1 1 0"	: Output DD11 - 4 to Tracking balance output (TBAL), and DD3 - 0*16+ "1110" to depth compensation output (DPctl) (exist on B/B only).

· **FTSTcmd (Address 1DH)**

This command is for measuring the DSSP's internal digital filter characteristics. To place each filter in processing mode, the internal mode is forcefully put to PLAY, or the filter's input is changed to usual input. When the pick-up or the motor are connected to the DSSP output, this command is not used. The sled filter's input is used in common with the TE input.

Command		DH1				DH0				DL
Name	**code**	**DH7**	**DH6**	**DH5**	**DH4**	**DH3**	**DH2**	**DH1**	**DH0**	**DL7 - DL0**
FTSTcmd	1D				WTF				WFF	

.WTF : Tracking filter's measurement gain select.
L : Tracking filter normal test.
H : Tracking filter up test.

.WFF : Focus filter's measurement gain select.
L : Focus filter normal test.
H : Focus filter down test.

· **RamRcmd (Address 1EH)**

This command refers to the DSSP internal RAM's contents. Continuous read is possible as well.

Command		DH1				DH0				DL
Name	**code**	**DH7**	**DH6**	**DH5**	**DH4**	**DH3**	**DH2**	**DH1**	**DH0**	**DL7 - DL0**
RamRcmd	1E	NEXT	0	0	BANK	0	0	0	PAGE	RAM7 - RAM0

.NEXT : Address selection method.
L : Set the RAM address in BANK, PAGE, and RAM7-RAM0.
H : Add 1 to the previous RAM address to make the current RAM address.

.DH6 - 5, 3 - 1 : Reserved. Must be set to L.

.BANK : BANK 0, 1 select

.PAGE : PAGE 0, 1 select

RAM7 - RAM0 : Internal SRAM address select. SRAM, according to PAGE 0, 1, is made up of a total of 512 words, BANK0, 256 words and BANK1, 256 words

- **RamWcmd (Address 1FH)**

This command writes 16-bit data in the DSSP's internal RAM. Continuous write is possible

Command		DH1				DH0				DL
Name	code	DH7	DH6	DH5	DH4	DH3	DH2	DH1	DH0	DL7 - DL0
RamWcmd	1F	RD15	RD14	RD13	RD12	RD11	RD10	RD9	RD8	RD7 - RD0

.RD15 -RD0: Data to write.

The write address should be set to RamRcmd beforehand. If you wish to write on consecutive addresses, issue this command continuously. If the previous command is RamWcmd, the DSSP adds 1 to the previous address to make the current address, then writes the current data there. If you add 1 to all the addresses of RamRcmd/RamWcmd, it is 00 and automatically adds 1 to the page.

- **FxKcmd (Address 20H - 33H)**

This command refers to and changes the focus filter coefficient.

2XFFFF : Read the (X+1) count number.
.2X<count number> : Write the count number on the (X+1) address.

.20 - 26 :	Focus normal coefficient select command.	K0 - K6
.27 :	Focus normal coefficient select command	nsk
.28 - 2E :	Focus down coefficient select command.	K0 - K6
.2F :	Focus down coefficient select command.	Nsk
.30 :	Reserved	
.31 :	Reserved	
.32 :	Reserved	
.33:	Reserved	

- **SPKcmd (Address 34H - 38H)**

This command refers to and changes the spindle filter coefficient.

.34 - 37 : Spindle coefficient select command.	Ka, K1, Kb, K2
.38 : Spindle output gain select	nsk
.39 : Reserved	

- **SLKcmd (Address 3AH - 3EH)**

This command refers to and changes the sled filter coefficient.

.3A - 3D : Sled coefficient select command.	Ka, K1, Kb, K2
.3E : Sled output gain select	nsk
.3E : Reserved	

- **TxKcmd (Address 40H - 53H)**

This command refers to and changes the tracking filter coefficient.

.40 - 46 : Tracking normal coefficient select command	K0 - K6
.47 : Tracking normal coefficient select command	nsk
.48 - 4E : Tracking up coefficient select command	K0 - K6
.4F : Tracking up coefficient select command	nsk
.50 : Tracking gain normal input attenuation. Setting/read command	k0
.51 : Tracking gain normal output gain. Setting/read command	nsk
.52 : Tracking gain up input attenuation. setting/read command	k0
.53 : Tracking gain up output gain. Setting/read command	nsk

- **ASKcmd (Address 54H - 56H)**

This command refers to and changes the anti-shock filter coefficient.

.54 - 55 : ATSC filter coefficient select (input gain)	K0, K1
.56 : ATSC filter coefficient select (Output gain)	Kout

- **TTKcmd (Address 57H)**

This command refers to and changes the output gain when WNSCcmd monitors the internal RAM.

.57: Monitor output gain coefficient nsk

- **xGKcmd (Address 58 - 5AH)**

Command		DH1				DH0				DL
Name	**code**	**DH7**	**DH6**	**DH5**	**DH4**	**DH3**	**DH2**	**DH1**	**DH0**	**DL7 - DL0**
xGKicmd	5j	Bk15	Bk14	Bk13	Bk12	Bk11	Bk10	Bk9	Bk8	Bk7 - Bk0

I = 0,1,2 j = i+8h

.58 - 5A: Band pass filter coefficient K1, K2, K0.

This command refers to and changes the gain-adjusting band pass filter's coefficient. In the AVKcmds AVS = 111b which will be explained later, all of K0, K1 and K2 can be set at the same time, but the lower 3 bits become 0. Compared to that, this command is able to set 16 bits with K0, K1 and K2, all separately.
This command is not included in the filter coefficient setting/referring command's common articles, but the setting/referring method is the same. (Refer to the data at "FFFf". The rest is set as follows.)

· **FTGcmd (Address 5BH)**

This command manually changes the focus/tracking gain.

Command		DH1				DH0				DL
Name	**code**	**DH7**	**DH6**	**DH5**	**DH4**	**DH3**	**DH2**	**DH1**	**DH0**	**DL7 - DL0**
FTGcmd	5B	Fchg	DWN	Tchg	UP					

.Fchg : Focus gain change
L: off
H: on

.DWN : Focus gain
L: normal
H: down

.Tchg : Tracking gain change
L: off
H: on

.UP : Tracking gain
L: normal
H: up

· **AVKcmd (Address 5CH)**

This command refers to and changes various average filter coefficients. In the case of AVS = 111b, it is possible to write AV data above the gain-adjusting band pass filter coefficients K1, K2, and (1-k1) at K0 at the same time, and also to refer to K1. This command is not included in the filter coefficient setting/referring command's common articles. The average value filter coefficient is different from the other filter coefficient sets. Thus, even if you change the coefficient set by SPdcmd, it does not change. If you wish to change it along with playback speed, you should issue this command along with SPDcmd.

Command		DH1				DH0				DL
Name	**code**	**DH7**	**DH6**	**DH5**	**DH4**	**DH3**	**DH2**	**DH1**	**DH0**	**DL7 - DL0**
AVKcmd	5C	AD12	AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4-AD0, AVS2-AVS0

.AVS2 - 0 : RAM select bit to be set.

.AD12 - 0 : Data when in write (if in data read, all "1").
0 0 0 : Focus tracking offset average filter count number.
0 0 1 : Tracking output average filter count number.
0 1 0 : Focus input average filter count number.
0 1 1 : Tracking input average filter count number.
1 0 0 : Sled output average filter count number.
1 0 1 : RF envelope input average filter count number.
1 1 0 : Reference input average filter count number.
1 1 1 : Band pass filters K1 and K2 (K0 = 1-K1).

- **ATTcmd (Address 5DH)**

This command sets the audio level. It sets the AT6-AT0s attenuation ratio.

Command		DH1				DH0				DL
Name	**code**	**DH7**	**DH6**	**DH5**	**DH4**	**DH3**	**DH2**	**DH1**	**DH0**	**DL7 - DL0**
ATTcmd	5D	0	(AT6)	AT5	AT4	AT3	AT2	AT1	AT0	

Audio level ratio = {0.5 (AT)} × 2

.AT5 - AT0 : Shows the attenuation level.

- **TRFcmd (Address 5EH)**

This command is for CMOS RF block testing. It can set the focus/tracking input gain and focus/tracking balance values in test mode.

Command		DH1				DH0				DL
Name	**code**	**DH7**	**DH6**	**DH5**	**DH4**	**DH3**	**DH2**	**DH1**	**DH0**	**DL7 - DL0**
TRFcmd	5E	Gin4	Gin3	Gin2	Gin1	Gin0	Bal4	Bal3	Bal2	Bal1-Bal0

.Gin4 - Gin0 : Focus/tracking input gain select value.

.Bal4 - Bal0 : Focus/tracking balance value select.

- **TDACcmd (Address 5FH)**

This command is for testing the DAC part in Servo test mode. It can set the 8-bit digital input value as a MICRO CONTROLLER command.

Command		DH1				DH0				DL
Name	**code**	**DH7**	**DH6**	**DH5**	**DH4**	**DH3**	**DH2**	**DH1**	**DH0**	**DL7 - DL0**
TDACcmd	5F	DAC7	DAC6	DAC5	DAC4	DAC3	DAC2	DAC1	DAC0	

.DAC7 - DAC0 : DAC's 8-bit input value select.
The selected DAC7 — 0 are transmitted in the servo test mode as FOD, TRD, SLD, and SPD's DAC.

CD-DSP MICRO CONTROLLER COMMAND

- **CNTL-6 Register (Address : 6H, DATA : {ERAOFF, CDROM, -, - })**

This register is ERAOFF, and can select Erasure correction for ECCs testing.

.ERAOFF : Erasure correction function On/Off during ECC (H: Erasure Off, L: Erasure On).
.CDROM : CDROM mode function On/Off (H: CDROM mode On, L: CDROM mode Off).
When CDROM mode is On, the ECC data is output as 16 bits without carrying out the interpolation process.

- **CNTL-7 Register (Address : 7H, DATA : {MUTE, -, smds_offset})**

.MUTE : Selects the mute function through Micro Controller (H: Mute On, L: Mute Off).
.SMDS_OFFSET : When calculating SMDS's pulse width, offset adjust.
(H: (THW-278T) × 32, L: (THW-279T) × 32)

- **CNTL-8 Register (Address : 8H, DATA : {NSI, CFS, Phase_Offset[1:0]})**

.CFS : Compensated Fsync detect On/Off signal (H: enable, L: precise frame sync detect).
.Phase_Offset : Decides the frequency of wbfck and rbfck.
.00 or 11 : 7.35kHz / 4, .01 : 7.35kHz/2 .10 : 7.35kHz/8

- **CNTL-Z Register (Address : 9H, DATA : {ZCMT, DEEPHEN, NCLV, CRCQ})**

This register controls the audio's zero cross mute, internal De-emphasis enable signal and the Phase servo's control signal. It also controls whether or not to include the CRCF data in SQDT.

Table 3. CNTL-Z Register

	Data	Data = 0	Data = 1
ZCMT	D3	Zero cross mute is OFF	Zero cross mute is ON
NCLV	D1	Phase Servo is activated by Frame Sync	Phase Servo is controlled by base counter
CRCQ	D0	SQDT outputs except for SQOK	SQDT = CRCF when S0S1 = 'H'

NOTE: The default value currently used in MICRO CONTROLLER programming is xx11.

- **CNTL-S Register (Address : AH, DATA : {GSEM, GSEL, WSEL, ATTM})**

This register controls the Frame Sync protect, Frame Sync insert and attenuation. In S5L9231, NWSEL (New WSEL) is added to the CNTL-D Register, to define Window Size along with WSEL.

Table 4. CNTL-S + CNTL-D Register

GSEM	GSEL	# of Frame Sync Insertion
0	0	2
0	1	4
1	0	8
1	1	13

NWSEL	WSEL	Window Size
0	0	± 3 T
0	1	± 7 T
1	0	± 13 T
1	1	± 26 T

ATTM	MUTE	dB
0	0	0
0	1	-∞
1	0	-12
1	1	-12

- **CNTL-L Register (Address : BH, DATA : {ADATEN, SPDIFEN, MICKEN, SUBDTEN})**

.ADTATEN: ESP interface enable/disable. Same function as the ESPEN pin.
H: ESP I/F On L: ESP I/F Off

.SPDIFEN : Digital audio output enable/disable (H: Enable, L: Disable).

.MICKEN : MICRO CONTROLLER clock (4.2336MHz) enable/disable (H: Enable, L: Disable).

.SUBDTEN : Subcode data output On/Off (H: enable, L: disable).

- **CNTL-U Register (Address : CH, DATA : {PDON, -, -, -})**

.PDON : MDP disable On/Off (H: MDP disable On, L: MDP disable Off)

.ERA4OFF : 4 Erasure Off. Perform 3 Erasure. (H: 4 Erasure Off, L: 4 Erasure On)

- **CNTL-W Register (Address : DH, DATA : {COM, WB, WP, GAIN})**

This register controls the CLV-Servo.

Table 5. CNTL-W Register

	Data = 0	Data = 1	Comments
COM	RFCK/4 and WFCK/4		Phase comparison frequency control during Phase mode
WB	RFCK/32	RFCK/16	Bottom hold period control during Speed mode
WP	RFCK/4	RFCK/2	Peak hold period control during Speed mode
GAIN	-12 dB	0 dB	SMDP gain control during Speed mode

- **CNTL-C Register (Address : EH, DATA : {CLV_MODE[3:0]})**

Table 6. CNTL-C Register

Mode		D7-D4	D3 D0	SMDP	SMDS	SMEF	SMON	Function
KICK	Forward	1 1 1 0	1 0 0 0	H	Hi-Z	L	H	Spindle motor forward mode
BRAKE	Reverse		1 0 1 0	L	Hi-Z	L	H	Spindle motor reverse mode
CLV-S	Speed		1 1 1 0	Speed	Hi-Z	L	H	Rough servo mode at start up
CLV-P	Phase		1 1 1 1	Phase	Phase	Hi-Z	H	PLL servo mode
CLV-A	XPHSP		0 1 1 0	Speed	Hi-Z	L	H	Normal play mode (If LOCK ='
				Phase	Phase	Hi-Z		H', CLV-P, otherwise, CLV-S)
CLV-A'	VPHSP		0 1 0 1	Speed'	Hi-Z	L	H	Automatic servo mode (If
				Phase	Phase	Hi-Z		LOCK = 'H' or GFS = 'H', CLV-P, otherwise CLV-S)
STOP	Stop		0 0 0 0	L	Hi-Z	L	L	Spindle motor stop mode

NOTE: HSPEED Mode is eliminated.

- **CNTL-D Register (Address : FH, DATA : {NWSEL, LC, DS[1:0]})**

.NWSEL : New WSEL. It is mentioned in the CNTL-S Register section.

.LC: Lock Control Signal.

.{[DS1,DS0]}:
"00" -> Normal Speed,
"11" -> Double Speed,
"01" or "10" -> Normal speed if ESPEN (or ADATEN in Micro Controller command) = L
Double speed if ESPEN (or ADATEN in Micro Controller command) = H

DIGITAL SERVO

- **Focus Servo**

The figure below is the functional block diagram of the Focus Servo.

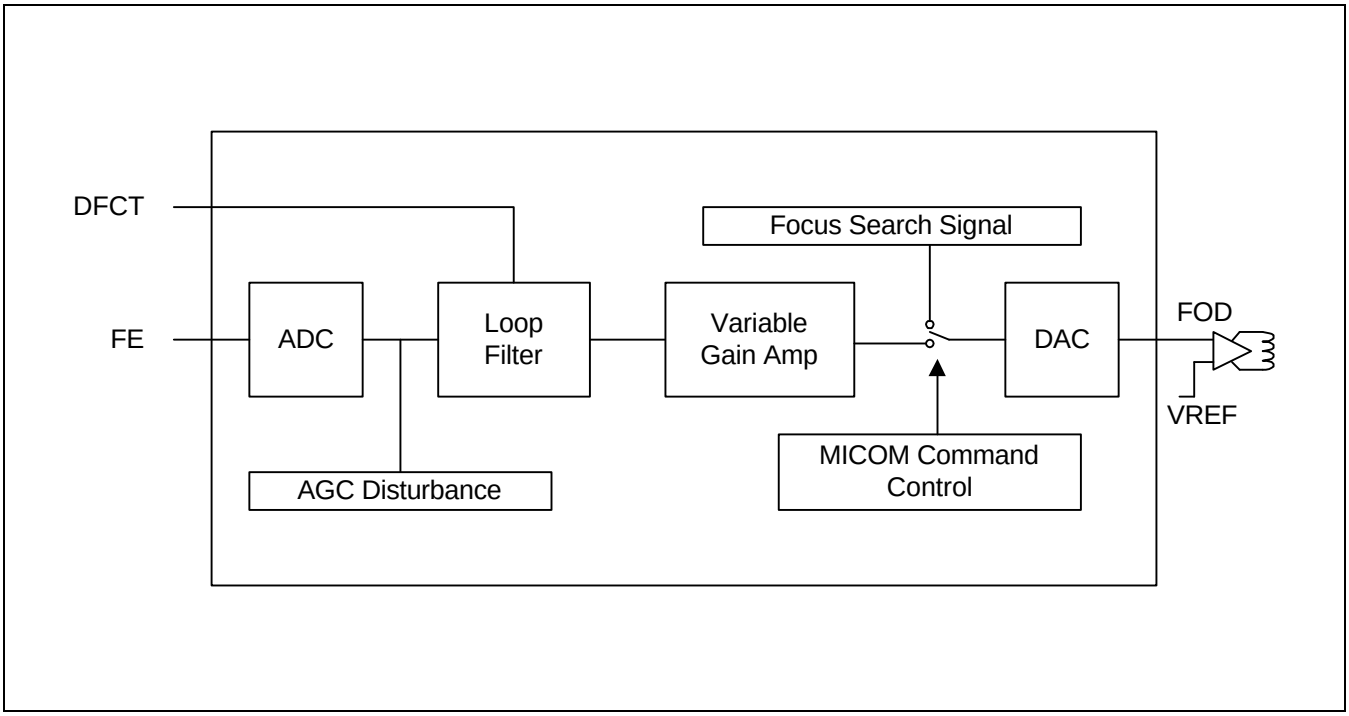


Figure 13. Focus Servo Functional Block Diagram

The focus error signal input into the FE pin goes through the input gain adjustment AMP to achieve a regular level. The signal goes through the ADC, Loop filter, and output AMP, then is output to the FOD pin through the DAC. It activates the focus coil through the drive AMP. For Drop out solution, it holds the loop filters output if a DFCT signal is generated by the RF. If it receives the disc detect command (DDT) or focus on command (FON), it generates delta waves from inside the digital servo, which activates the focus coil to move the pick up perpendicular to the disc. The output always passes through the noise shaping filter, improving output resolution. When FONcmd is input from Micro Controller, FOD generates focus actuator drive voltage to monitor the FE signal, which carries out focus pull-in.
Focus-related jobs are divided into Disc detection and focus pull-in. These are activated by DDT command and FON commands command routine.

· TRACKING SERVO

The figure below is the Tracking Servo's function block diagram.

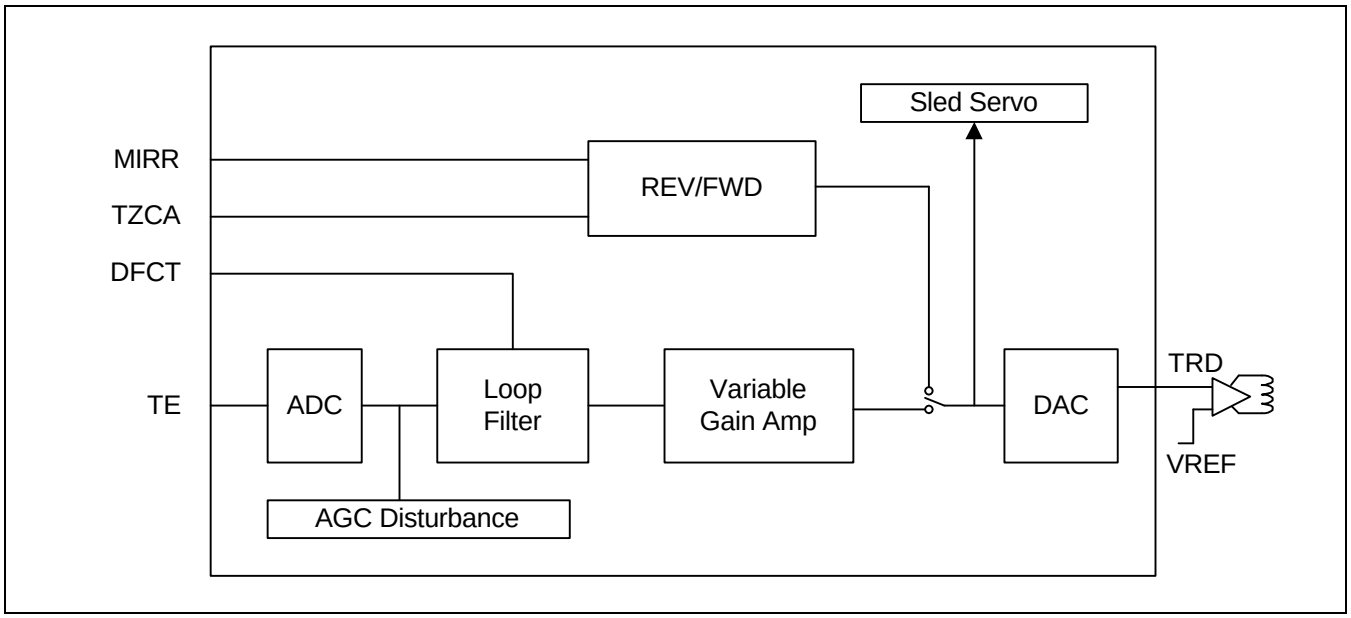


Figure 14. Tracking Servo Block Diagram

After A/D, the TE signal goes through the compensation filter and variable gain AMP. It is then D/A converted, then output to the TRD block (Variable gain AMP is automatically selected during auto gain adjustment). As Drop out solution, it holds the loop filter output for DFCT signal.
When TONcmd is input from Micro Controller, the TRD generates tracking actuator drive voltage, monitors MIRR and TZCA signals, and carries out pull-in of the closest track. Like the Focus Servo, the Tracking Servo also outputs through the noise-shaping filter.

- Automatic Adjustment

The following adjustments are included in Automatic Adjustments: Offset adjustment by OfAcmd, focus balance adjustment by FBAcmd, tracking balance adjustment by TBAcmd, and loop gain adjustment by FGAcmd and TGAcmd. The automatically adjusted features in order are as follows.

- Input Gain Adjustment

This function is to measure the input error signal's peak level, then to adjust the input AMP's gain to make the peak level about 80% of the A/D s maximum input. The Focus measures the S-curves, while the Tracking measures the peak level from the error signal during off-track.

- Offset Adjustment

The Focus offset is the focus error during defocus, or the focus error level in the S-curves . The tracking offset is electrical offset, which signifies the tracking error level during defocus.
The tracking offset can be explained as the tracking error signal when there is no input (TE's electrical offset). Tracking offset measurement is carried out during Laser Diode Off status, so it is appropriate to issue the system select command after reset cancellation at the end (before LD On).
When TONcmd is received, the Laser Diode (LD) is turned Off, and the timer is set so that the TE output is stabilized. Since LD is turned on at the end of this command, the TOA is sent out multiple times for accuracy. After the time delay when the TE output is stable, the measurement time is set to the timer. Between those times, the TE is read every 88.2kHz, and the average of the average values is taken up until then.

- Balance Adjustment

Two types of algorithms are used in this Digital Servo as focus balance adjustment methods. The first is the already explained method of making the S-curve's amplitude peak and bottom the same using the Disc Detect Command (DDTcmd). The second is the method in which the RF signal's envelope level becomes peak, supported by the FBA command.
The former is a rather temporary method which adjusts the balance as well as the DDTcmd search. The latter is a more active method which uses the following characteristic. If the balance is bad, the focus does not match exactly in the pit, and the envelope level becomes lower, whereas when the focus is exact, the envelope level goes to peak.
In addition, for each method, there are a total of 4 different methods which can be chosen or used together, including the way of controlling the Focus Balance output, Fbal, and two ways of changing the Focus Bias, Fbias. Please refer to the flag select/read Command, FLGcmd. You must choose if you wish to adjust the balance or the bias using Micro Controller COMMAND. When you are in balance adjust, the gain should be adjusted through the Fbal/Tbal output, and when you are in bias adjust, it should be adjusted through the TOD/TRD.

- Loop Gain Adjustment

The goal of this function is to make the gain of an entire Loop at a specific frequency f0 to 1, or 0 dB. Gain adjustment is accomplished by overlapping the measurement signal X within the Servo loop during Servo On status, and measuring the phase difference between X and Y, the detected signal. If you overlap the measurement signal with the sinusoidal wave of the frequency, the loop gain you want is 0 dB, and you can use the following characteristic. When the phase difference between the detected signal and the measurement signal is 90 degrees, the loop gain at that frequency is 0dB.

Example of Automatic Control Flow

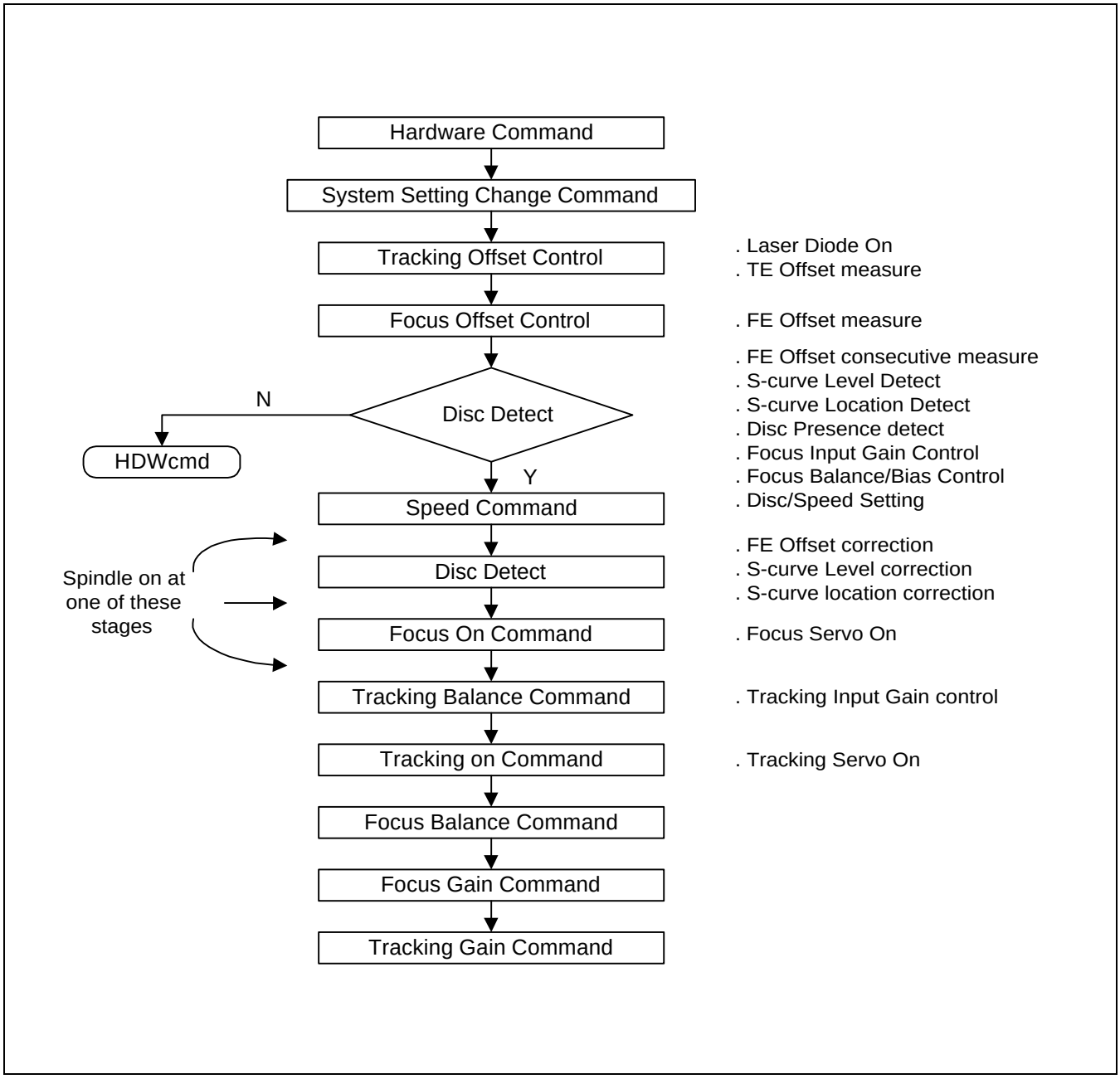


Figure 15. Example of Automatic Control Flow

- **DRIVE INTERFACE**

The digitally handled Focus, Tracking, Sled, and Spindle Servo output go through DAC, then are output as analog values. Here, the Focus and Tracking drive output uses the 8-bit DAC, and the Sled and Spindle, the 6-bit DAC.

CD-DSP

- **EFM Demodulator**

This block demodulates EFM signals read from the CD. EFM Demodulator block-related command registers and data are shown in the table below.

Table 6. Command Register and Data

Control Register	Comments	Address D7-D4	Data D3	Data D2	Data D1	Data D0	/CLV_STATE
CNTL_S	Frame SYNC Protection, Attenuation Control	1010	GSEM	GSEL	WSEL	ATTM	Hi-Z
CNTL_D	Double Speed	1111	NWSEL	LC	DS1	DS0	Hi-Z

- **EFM Phase Detection (Phase Comparison)**

The NRZ type EFM input signal from the CD is made into a syn_efm_nrz signal, whose phase is matched to plck4M (2x: 8.6436MHz, 1x: 4.3218MHz), and NRZI type syn_efm_nrzi signal. As shown in Figure 6, the syn_efm_nrzi signal, from syn_efm_nrz signal, outputs "H" from the transition point, and "L" from the rest.

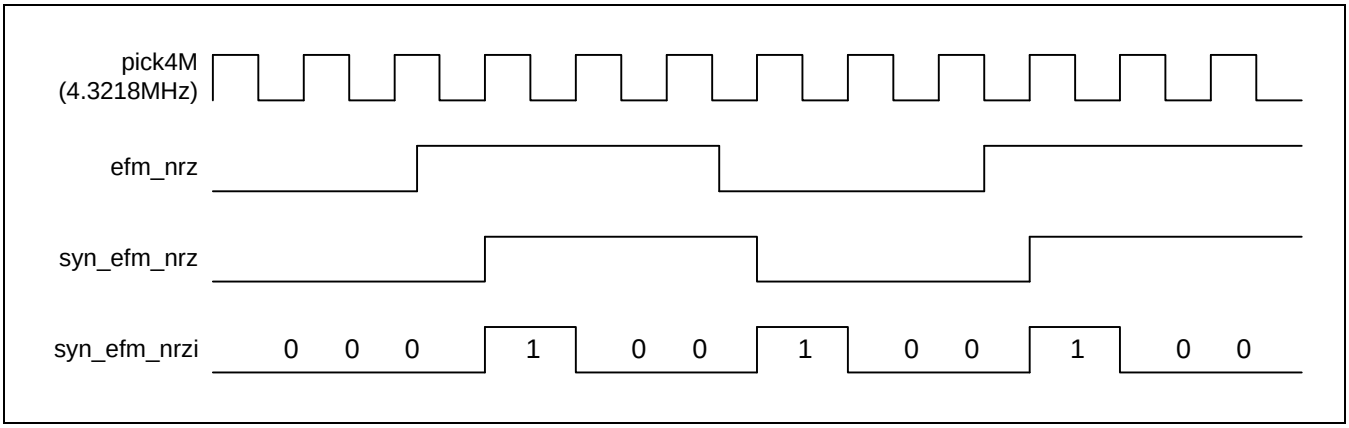


Figure 16. Timing Diagram

- **SUBCODE S0S1 Generation**

The subcode sync patterns S0 (00100000000001) and S1 (00000000010010) are detected by this circuit. If either one of S0 or S1 is detected, S0S1 is set to H.

- **SUBCODE Block**

The Subcode block receives 8-bit subcode data with the period of 7.35kHz from the EFM block (synchronized with the write frame clock), and transmits to the digital audio out block from the EFM block. Out of the 8-bit data (channel P — channel W), P and Q data are handled, then sent to Micro Controller. The subcode data is data for CDP control or display (one subcode block is composed of 98 symbols (8-bit)). Channel P data bit shows the start of the track. If it is "0", it is in the middle of a track, and if it is "1", it is the starting of a track. Channel Q data is mainly timing data information, and each frame has 16 bits of CRC data. If the CRC result is "0", this data is transmitted to Micro Controller, and if "1", "L" is output. The other channel R, S, T, U, V, W data are not used in S5L9231.

· **CLKGEN**

The CLKGEN block makes all the clocks used in the CD-DSP and reset-related signals for each block. All clocks used in the CD-DSP are made using a crystal-generated 16.9344MHz signal.

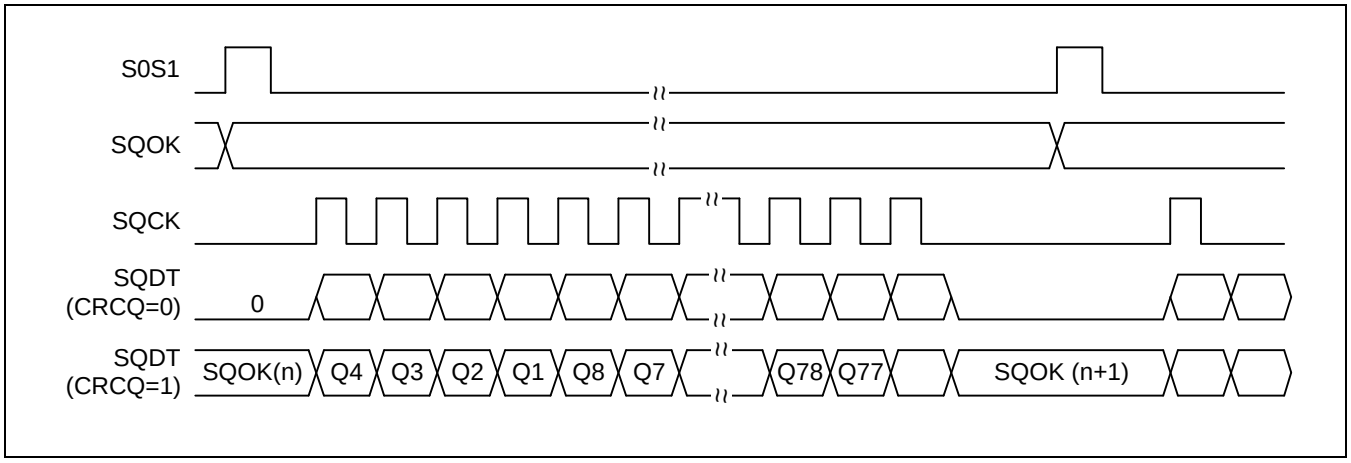
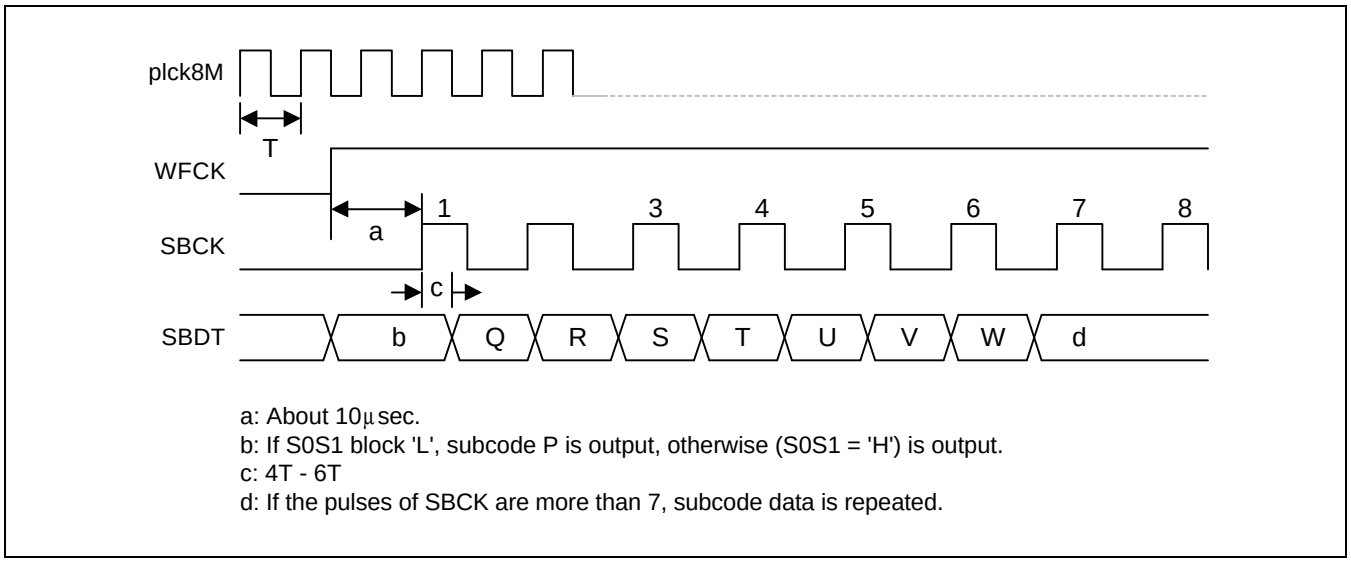


Figure 17. Subcode Block Signal Timing Diagram



a: About 10μsec.
b: If S0S1 block 'L', subcode P is output, otherwise (S0S1 = 'H') is output.
c: 4T - 6T
d: If the pulses of SBCK are more than 7, subcode data is repeated.

Figure 9. plck8M, WFCK, SBCK, SBDT Timing Diagram

· **ECU / MMU**

- ECU (Error Correction Unit)

The ECU block is a microprocessor specifically for ECC, and thus makes error corrections during decoding according to the Error Correction Code (ECC) algorithm.

- MMU (Memory Management Unit)

The MMU block manages the 16 Kb memory that is used within S5L9231 for EFM data storage, and reads/writes memory according to EFM data priority.

- **Interpolation**

The Interpolation block interpolates the audio data that may have errors. Whether the audio data has the potential to have errors or not is decided when the c2p data from the ECU block is decoded. If it is decided that there are errors in the audio data, a new audio data value is found using the most recent error-less data before the current one, and the error-less data which follows. The handling of audio data with possibility of errors brings the error concealment effect. This is under the assumption that the continuing audio data value is similar to nearby values. If there are no errors in the audio data, the said data is output as is.

-Interpolation : The interpolation algorithm used in CDP is linear interpolation. In other words, when carrying out interpolation, the average of the error-less previous and following two values are used as the output value, and if erroneous data is continually input, the most recent error-less audio data value is maintained.

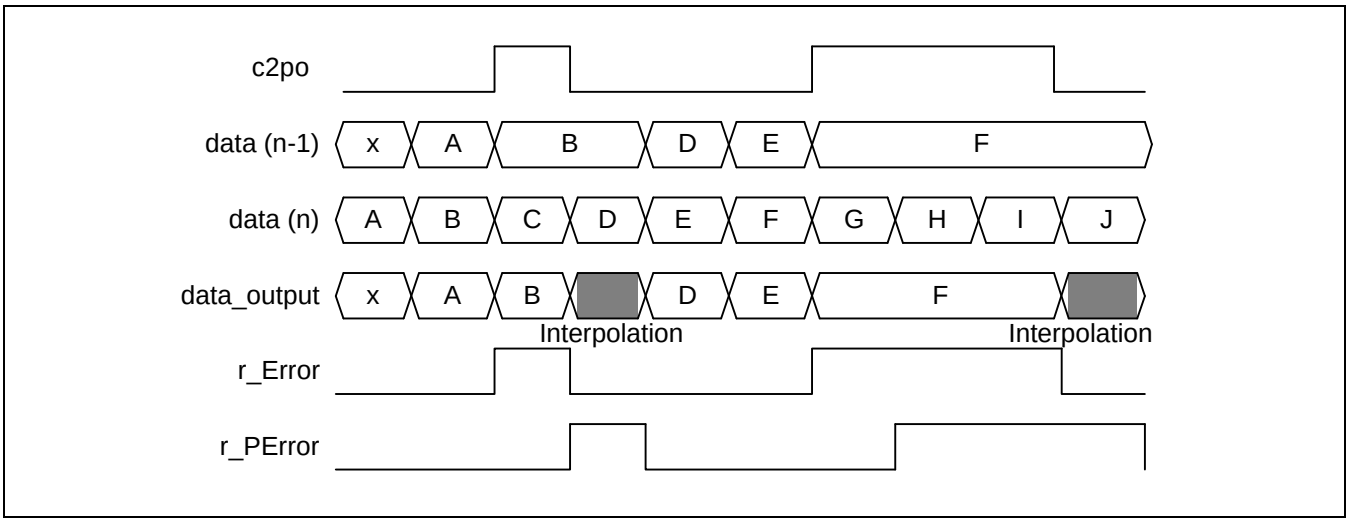


Figure 19. Interpolation

- **AUDOUT**

The AUDOUT block transforms the 16-bit parallel data input from the INTERPOLATION block according to audio mode format. The audio format supported by S5L9231 is shown in Figures 11.

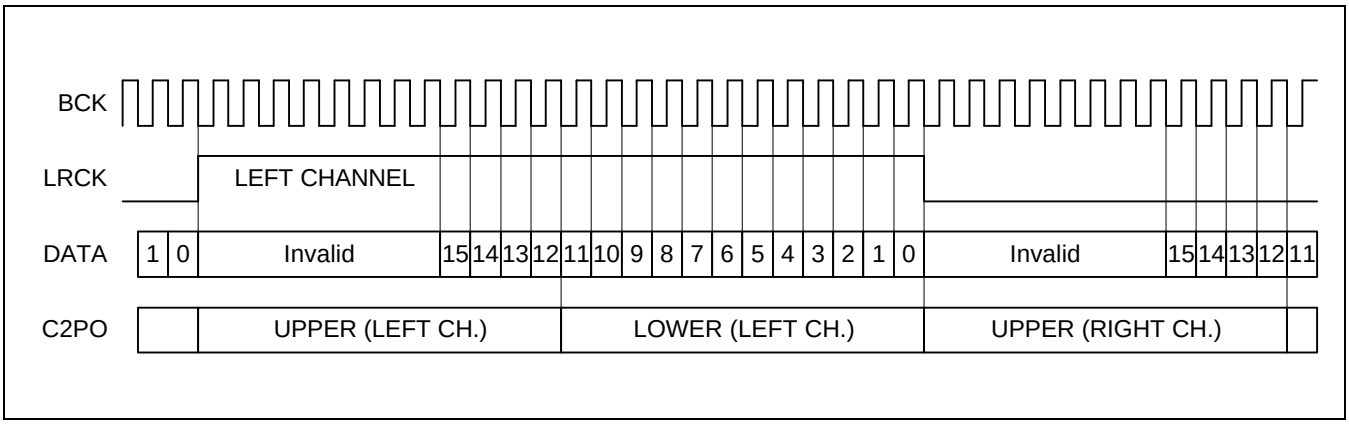


Figure 20. Audio Output Protocol for CD-DSP
(24-bit clock, MSB first, Right channel low, c2po MSB first, data latch timing negative edge)

- **Digital Audio Out**

The Digital Audio Interface block serially transmits the information recorded in the CD to nearby parts. This interface method has the advantage of communicating using only one pin, and does not need other pins such as clocks. Because of this advantage, it is used not only in audio systems designed for home use, but also those for professional use. This interface is used only in normal speed.

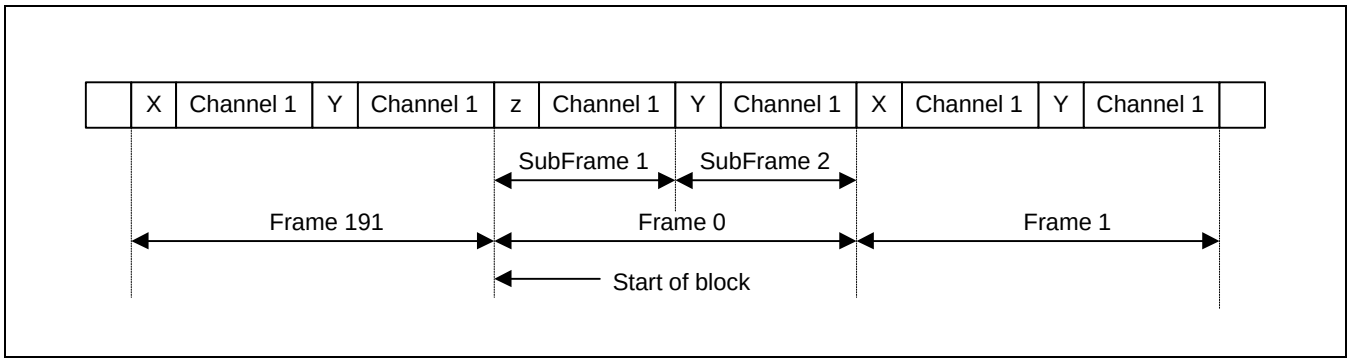


Figure 21. Digital Audio Out

- SPDIF (Sony-Philips Digital audio Interface)

Because the Digital Audio Interface method for CDs was originally suggested by Sony and Philips, it is called SPDIF, and its stipulations are listed in the AES (Audio Engineering Society). Data is transmitted serially and is sensitive to background noise. To overcome this, the digital out data is transmitted after being demodulated to bi-phase condition. This is accomplished as follows: Phase0 is set as a different value from the previous data's phase1 value, and if the source data of phase1 is "0", the same value as that of phase 0 is set. If the source data is "1", a different value from phase 0 is set.

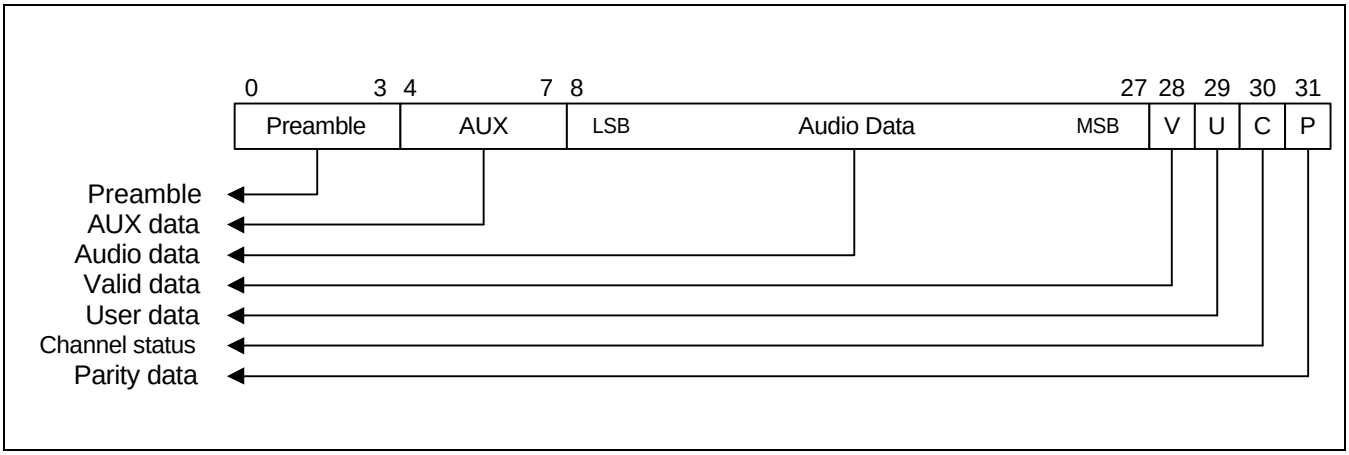


Figure 22. SPDIF

- Structure of Format

Each subframe is made of 32 time slots, and the subframe includes audio data. Two subframes make one frame, and it has Left and Right stereo signal components. 192 frames make 1 block, which is the information unit of a control bit.

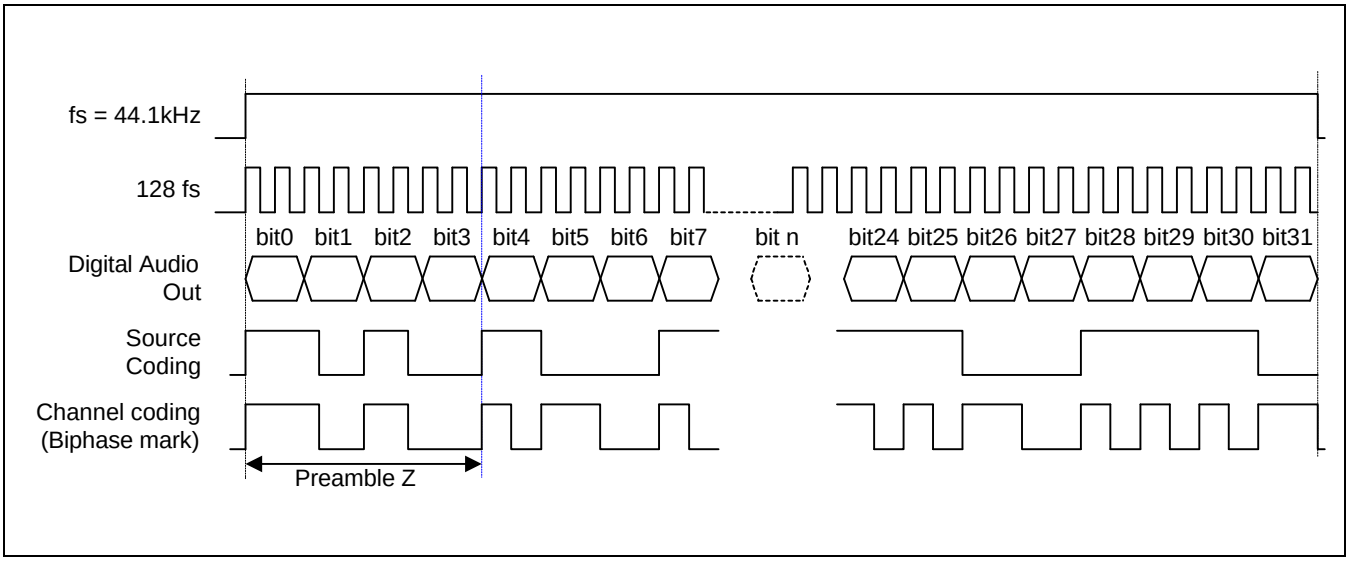


Figure 23. Subframe Format

- Subframe Format

Preamble (4-bit): The preamble has the sync information of each subframe and block, and to maintain the original characteristics of sync data, the preamble data is not changed into a biphase signal. Instead, it is started as the opposite value from the previous symbol's phase1 value. The preamble needs three patterns to distinguish left and right, and to show the start of the block. The patterns are as follows.

Preceding State	0	1	
	Channel Coding		
"X"	11100010	00011101	Subframe 1
"Y"	11100100	00011011	Subframe 2
"Z"	11101000	00010111	Subframe 1 and block start

Preamble X is channel 1's sync, and preamble Y is channel 2's sync. To show the start sync of a block, preamble Z is used. The reason why there are two sync patterns for each preamble is that the value is reversed according to the previous data's phase.

- AUX (4-bit) : Auxiliary data area.

Audio Data (20-bit) : The resolution of the audio data transmitted to digital out is basically 16-bit for CD, but you can expand to 20-bit, or even 24-bit by expanding the audio data area to the AUX area. This area is LSB first.

Validity Bit (1-bit) : If the audio sample word can be changed into analog audio signal, the validity bit is set to "1", and if not, it is set to "0". For CDs, it is set to "0". User data (1-bit) : For CDs, subcode data is transmitted using this area.

Control Status Data (1-bit) : Information is input for each subframe, and you need 192 subframes to make one control status data. This area has the consumer mode and professional mode, and the S5L9231 supports the consumer mode. For CDs, the control status data has the following meaning.

Bit	Control Status Data
0	0 : Consumer use, 1 : Professional use
1	0 : Normal Audio, 1 : Non-audio Mode
2	0 : Copy Prohibit, 1 : Copy Permit
3	0 : No Preemphasis, 1 : Preemphasis
4	Reserved (= 0)
5	0 : 2-channel, 1 : 4-channel
6 - 7	00 : Mode 0, Reserved
8 - 15	10000000 : 2-channel CD player User bit channel = CD Subcode V bit optional
16 - 19	Source number (= 0000)
20 - 23	Channel number (= 0000)
24 - 27	Sampling frequency : 44.1kHz = 0000
28 - 29	Clock accuracy 00 : Normal accuracy 10 : High accuracy 01 : Variable speed
30 - 191	Don't care (all zero)

- **ESPIF (ESP Interface)**

The ESPIF block handles the interface between the external ESP controller and CDDSP. The MSB signal, like in the AUDOUT block, decides the audio output format, and if MSB is "L", data is made using the 24-bit clock for each half cycle. If MSB is "H", data is made using the 32-bit clock.
The ESPEN signal is an external ESP controller enable signal, input from the exterior through a pin. If the ESPEN signal is "L", the external ESP controller is not used, and the serial data input from the AUDOUT block goes through the serial to parallel register, then is output to the DIGOUT block and DSP core as parallel 16-bit. If the ESPEN signal is "H", the audio data output from the ESPIF block is input to the external ESP controller at a 2x data rate, and the data input to the ESPIF block from the ESP controller is input in normal speed. So, the parts excepting the DPLL and DIGOUT block are designed to operate at 2x if the ESPEN signal is "H". In the ESPIF block, the output part to the DIGOUT block and the DSP core uses a 16-bit serial to parallel converter for parallel output. The operation carried out next in the ESPIF block is the audio data mute control. The mute control functions supported in S5L9231 are zero-cross muting, muting, and attenuation.
Attenuation : Attenuation of audio signal according to the CNTL-S register's ATTM signal and MUTE signal.

Table 7. Attenuation

ATTM	MUTE	Degree of Attenuation
0	0	0 dB
0	1	- ∞ dB
1	0	-12 dB
1	1	-12 dB

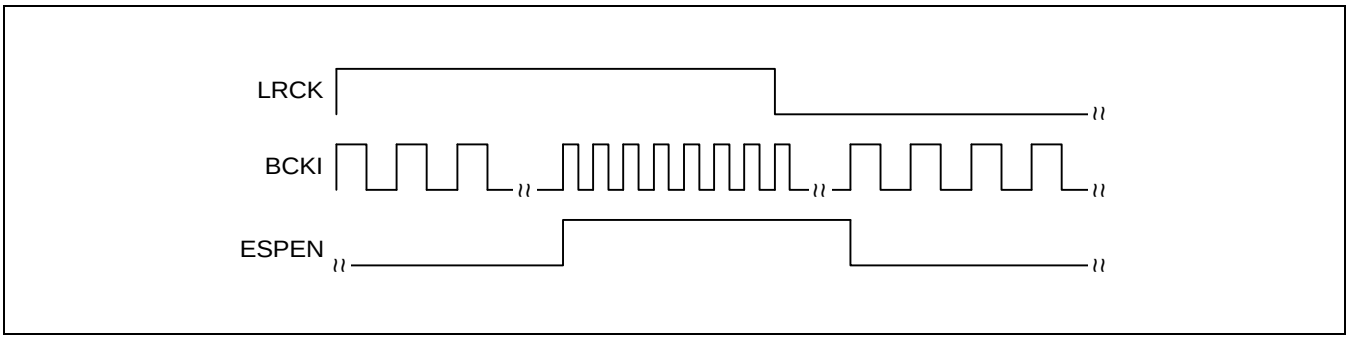


Figure 24. ESPIF Timing Diagram

The external input formats from the ESP controller are limited to Figures 10 and 11.

NOTE: Micro Controller command ADATAEN (BCh) carries out the same function as the ESPEN pin.

· **CLV SERVO**

The command register and data related to the CLV block are shown in the table below.

Table 8. Command Register and Data

Control Register	Comments	Address D7-D4	Data				/CLV_STATE
			D3	D2	D1	D0	
CNTL-Z	Data Control	1 0 0 1	ZCMT	-	NCLV	CRCQ	Hi-Z
CNTL-S	Frame Sync Protection Attenuation Control	1 0 1 0	GSEM	GSEL	WSEL	ATTM	Hi-Z
CNTL-W	CLV Control	1 1 0 1	COM	WB	WP	GAIN	Hi-Z
CNTL-C	CLV mode	1 1 1 0	CLV Mode				/(Pw ≥ 64)
CNTL-D	Double Speed	1 1 1 1	NWSEL	LC	DS1	DS0	Hi-Z

• CLV Servo Mode

The CNTL-C register receives the signal to control the CLV (Constant Linear Velocity) Servo from Micro Controller.

- **KICK Mode (Forward Mode**)
  SMDP outputs "H" (accelerate), SMDS outputs "Hi-Z", SMEF outputs "L", and SMON outputs "H".

- **BRAKE Mode (Reverse Mode)**
  SMDP outputs "L" (decelerate), SMDS outputs "Hi-Z", SMEF outputs "L", and SMON outputs "H".

- **CLV-S Mode (Speed Mode)**

When Track jump of EFM phase is unlocked, speed mode roughly controls the spindle motor.
The frame sync signal's pulse width from the NRZ type's EFM signal is exactly 22T (assuming the period of plck8M is T). It can exceed 22T because of noise, and in that case, the correct frame sync cannot be detected. If the maximum pulse width of the NRZ type EFM signal is smaller than 21T, SMDP outputs "L". If the pulse is 22T, it outputs "Hi-Z", and if larger than 23T, it outputs "H". If the CNTL-W register's gain is "L", SMDP's output is sent after attenuation (-12 dB), and if "H", it is output without attenuation. SMDS outputs "Hi-Z", SMEF outputs "L", and SMON outputs "H".

Table 9. Peak Hold Clock and Bottom Hold Clock's Frequency

Peak hold clock frequency		Bottom hold clock frequency	
WP = 0	WP = 1	WB = 0	WB = 1
RFCK/4	RFCK/2	RFCK/32	RFCK/16

Table 10. SMDP Output

Max. pulse width of Frame Sync	SMDP	Þ if CNTL-W register GAIN is 'L',
≤ 21T	L	SMDP output is attenuated as -12dB. If 'H', no attenuation is performed.
= 22T	Hi-Z	
≥ 23T	H	

- CLV-P Mode (Phase Mode)

This mode is for controlling the EFM phase. When CNTL-Z register's NCLV is "L", the phase difference between P2WFCK/4 and RBFCK(P2RFCK/4) is detected and output to SMDP. When it is "H", the phase difference between RBFCK (Read Base Counter/4, P2RFCK/4) and WBFCK (Write Base Counter/4) is detected and output to SMDP. SMEF outputs "Hi-Z" and SMON outputs "H".

P2RFCK (=7.35kHz) : Crystal-generated Read Frame Clocks output
P2WFCK (≅ 7.35kHz) : EFM-generated Write Frame Clocks output

If in normal speed, the period of 4.2335MHz is T. The width where WFCK is "H" is tHW. SMDS outputs "H" for (tHW-278T)×32 at WFCKs falling edge, and then outputs "L" until the next falling edge.

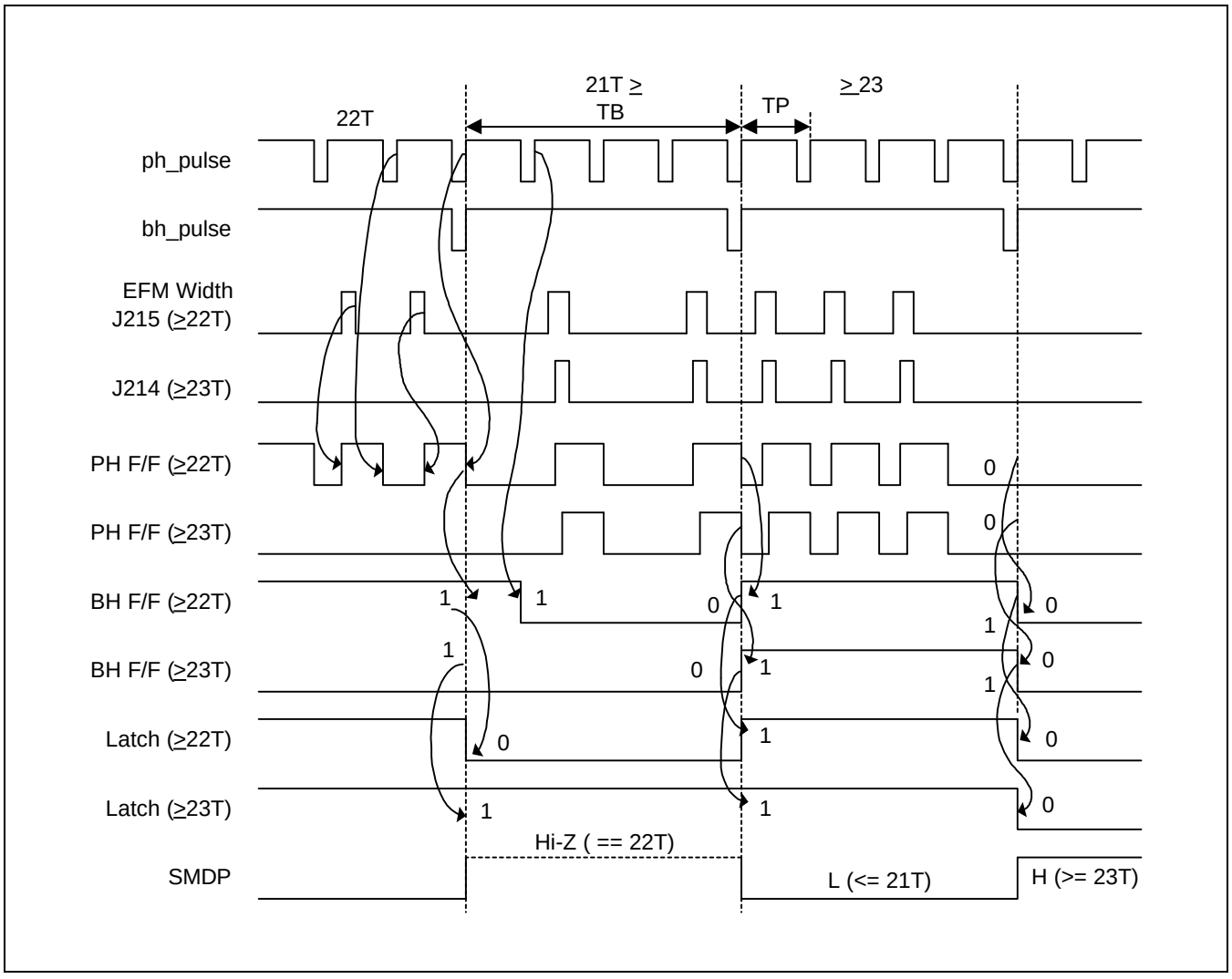


Figure 25. In CLV-S Mode, SMDP Output when GAIN is 'H'

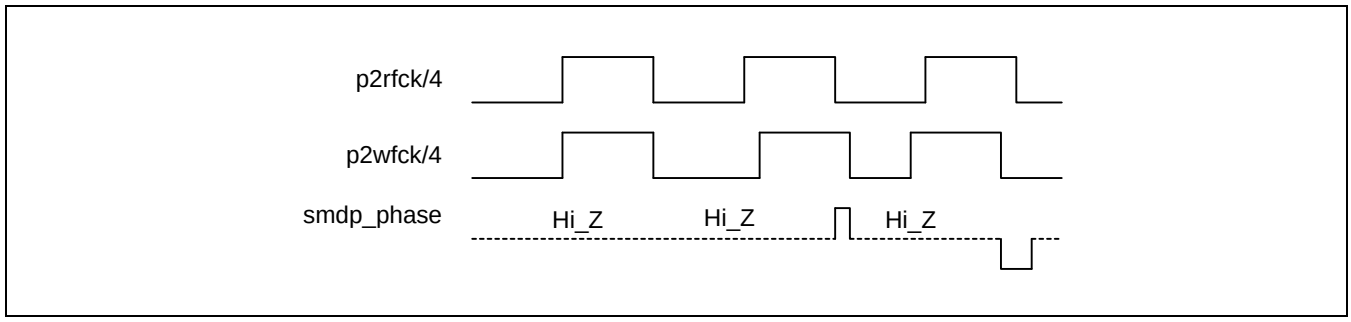


Figure 26. SMDP Output in CLV-P Mode

- CLV-A Mode (XPHSD Mode)

This mode is for normal action. The GFS generated in the EFM block is sampled at WFCK/16 period. If GFS is sampled as "H", the CLV-P mode (phase mode) is carried out, and if it is sampled 8 consecutive times as "L", it automatically carries out the CLV mode (Speed mode). At this time, the CNTL-W register decides the peak hold cycle in phase mode, and the bottom hold cycle and gain in the speed mode.

When PLL is locked, (LOCK = 1) SMEF is "Hi-Z", and SMDS operates like SLV-P mode.

When PLL is unlocked, (LOCK = 0) SMEF is "L", and SMDS is "Hi-Z".

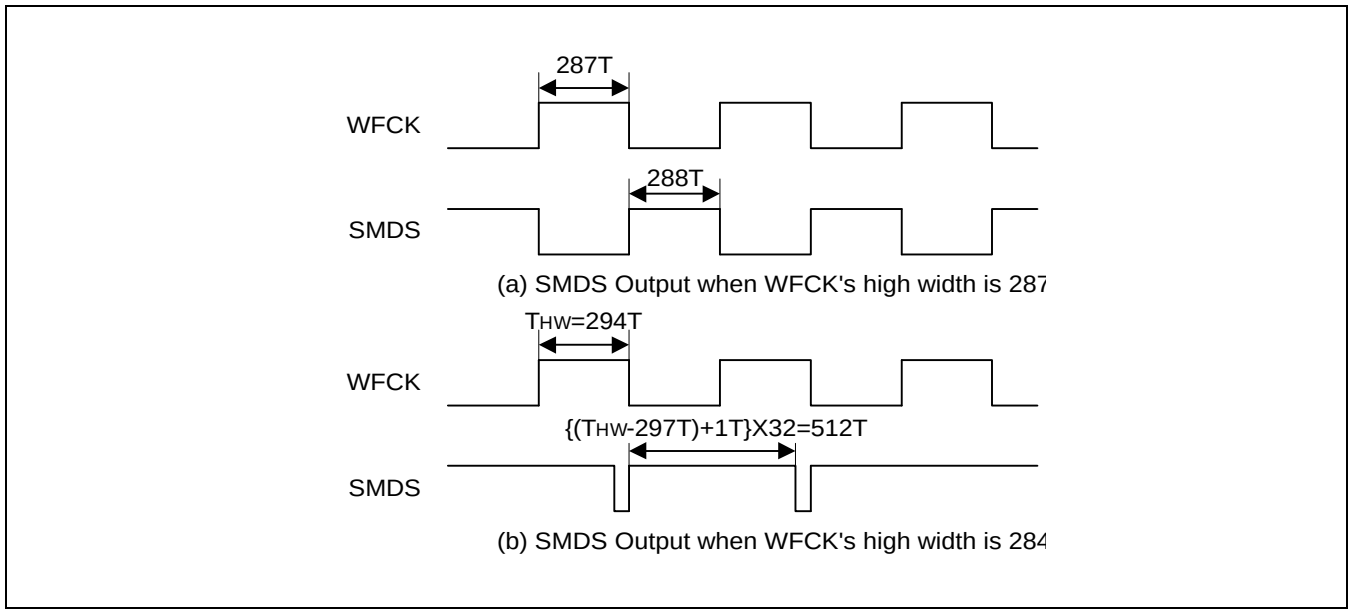


Figure 27. SMDS Output in CLV-P Mode (T: one frequency of 4.2336 MHz, WFCK¡Ö7.35 kHz)

- CLV-A Mode (VPHSP Mode)

This mode is for Rough Servo control.
To test the EFM pattern, use PLL-generated plck8M instead of Xtal.
When 0 dB, (ATTM = 0&&MUTE = 0) it operates like CLV-A mode. If it is not 0 dB (ATTM = 1 // MUTE = 1), GFS is 1, SMEF is "Hi-Z", and SMDS operates like CLV-P Mode.
When GFS is 0, SMEF is "L", and SMDS is "Hi-Z".

- **STOP Mode**

This mode is to stop the spindle motor. The SMDP outputs "L", SMDS outputs "Hi-Z", SMEF outputs "L", and SMON outputs "L"-Spindle Motor Off.

- LOCK Generation

This the period of WFCK (1x: 7.35 kHz, 2x: 7.35 × 2kHz). According to the Micro Controller command LC, LOCK is generated as shown in the table below. In other words, it is generated after GFS becomes "L", whether it is 1x or 2x.

Lock status is maintained for 127 frames. Since LOCK is synchronized to WFCK, GFS default action takes place when LC is "0".

Table 11. Lock Control (T: Frequency of WFCK)

	Normal	Double
LC = 0	127T	127*2T
LC = 1	127T	127T

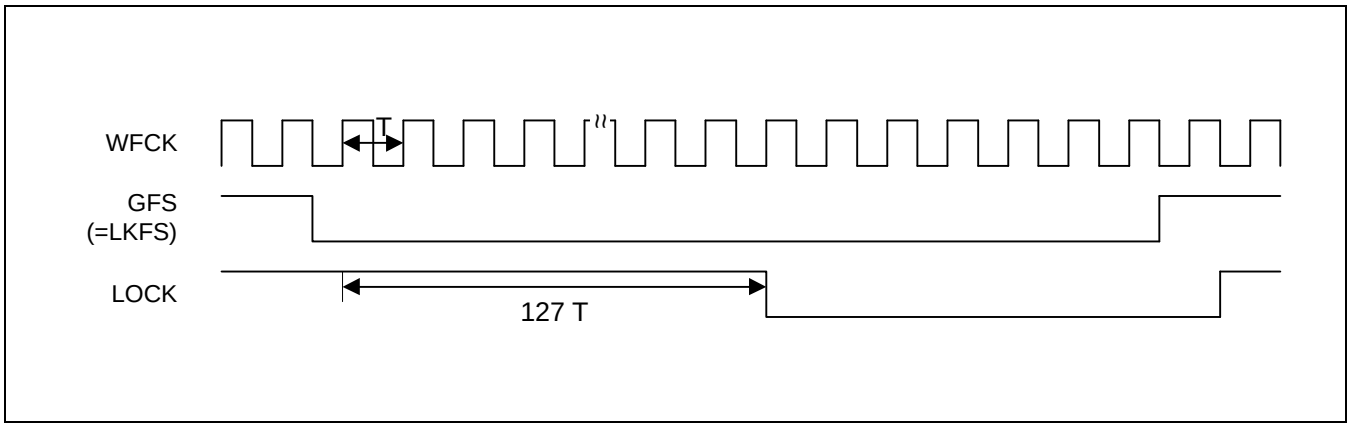


Figure 28. LOCK Generation (LC = '1')

- **Digital PLL**

The purpose of the DPLL block is to generate the bit clock plck4M from the EFM signal, which is input for EFM signals. As seen in Figure 20, DPLL can be divided into the DPLL main block (DPLLF) and the Frequency synthesizing block (HICK).

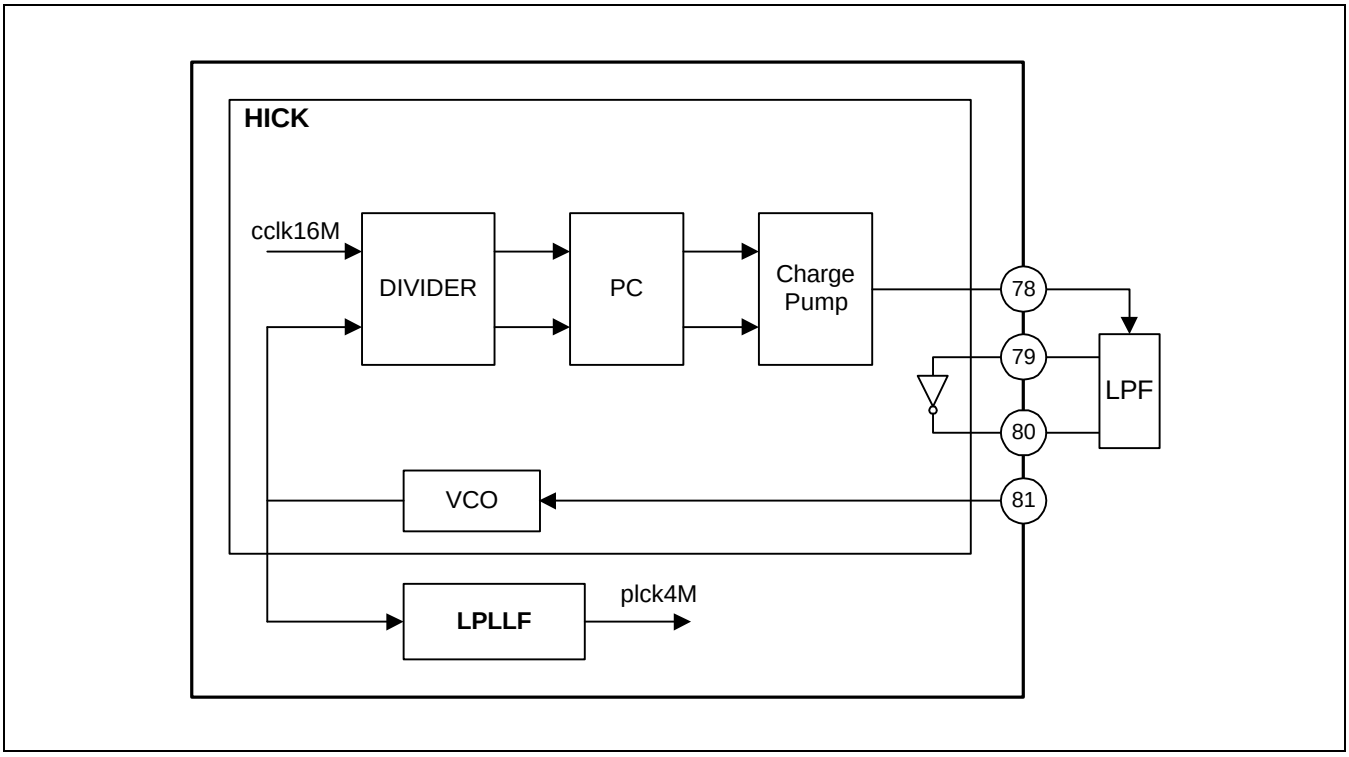


Figure 29. DPLL's Block Diagram

HICK Block (High Frequency Synthesizer)

The HICK block is composed of the divider, phase comparator, charge pump, loop filter, and the VCO. In the high frequency synthesizer, the VCO output frequency can be found using the formula cclk16M*M/N. Figure 21 shows the VCO's characteristic curve.

Where N: Division of 16 MHz clock, M: Division of VCO

The Phase comparator uses the PFD (Phase Frequency Detector) type, and as shown in Figure 21, the output conditions of the Charge Pump are "H", "L", and "Hi-Z". The UP signal is "L", only when the reference clock is "L" before the compared clock. Inversely, the Down signal is "H" only when it the reference clock is "L" later than the compared clock.

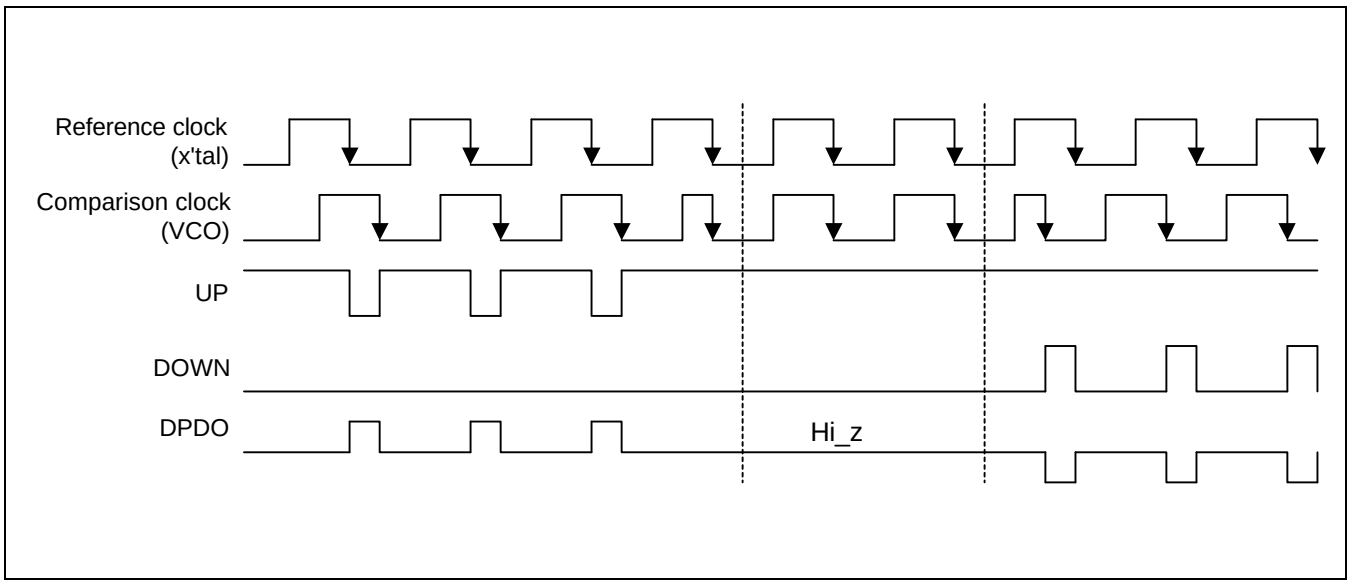


Figure 30. Timing Chart for Phase Comparator and Charge Pump

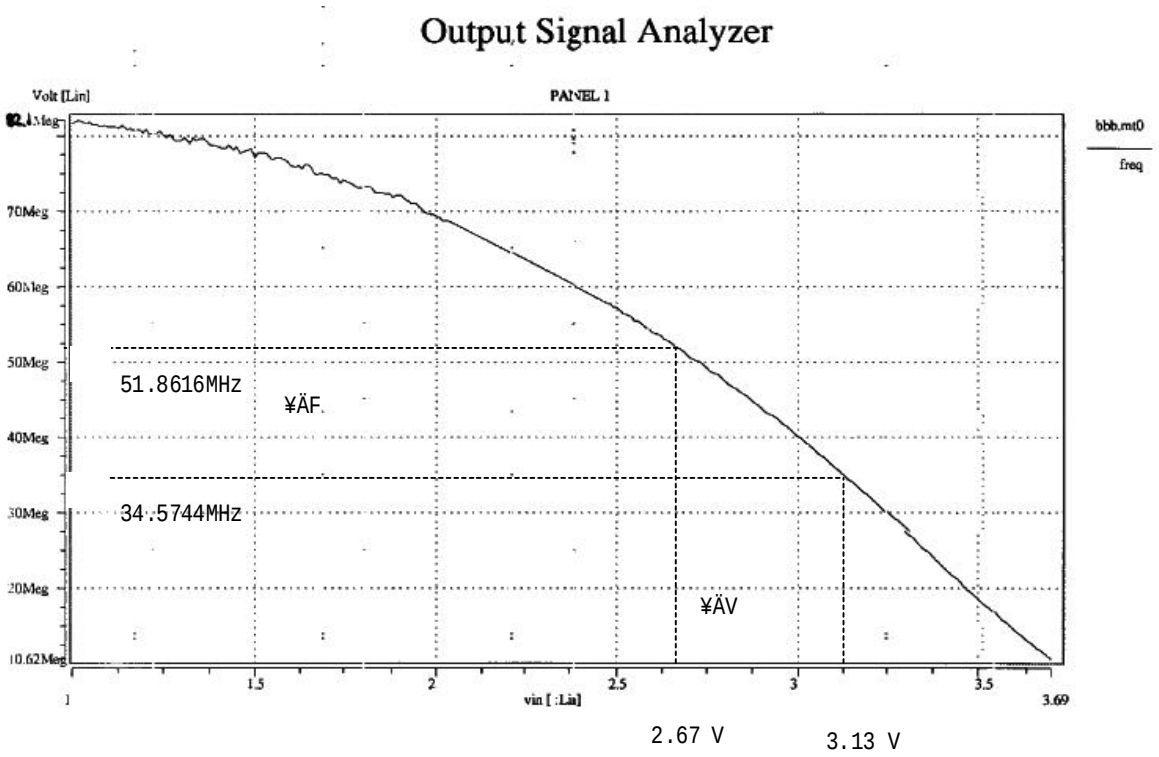


Figure 31. VCO Characteristics

Figure 32 shows an external Loop Filter, which is a PI (Proportional Integral) type Active Low Pass Loop Filter. The inverter is used instead of the OP AMP, and gets the Active loop filter's frequency characteristics just like the OP AMP. The Loop Filter filters the phase comparator's error output signal and outputs VCO control signals.

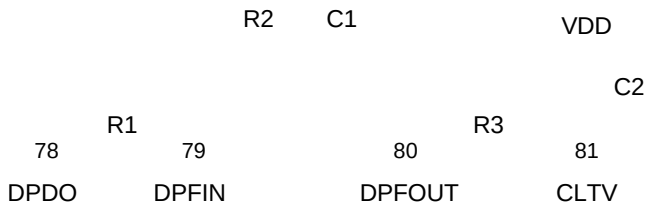


Figure 32. External Low Pass Filter

DPLLF Block

The DPLLF block generates the bit recovery clock plck4M from the EFM signal. It uses the VCO clock (1x: 34.5744MHz, 2x: 51.8616 MHz) to count the EFM signal and detect errors, carry out frequency adjustment, and make the phase-compensated plck4M.

· **1-BIT DAC**

The 1-bit DAC is a Digital-To-Analog Converter which uses sigma delta modulation. It is composed of Digital Attenuation, De-emphasis, H1 Filter and H2 Filter, Sync Filter, Analog Post-Filter, and AIF (Anti-Image-Filter). The normal input/output characteristics have more than 100 dB SNR (Signal to Noise Ratio) over the 20kHz band.

FEATURES

- 16-bit Sigma-Delta Digital-to-Analog Converter
- On-Chip Analog Post-Filter
- Filtered Line-Level Outputs, Linear Phase Filtering
- SNR 100dB over
- Sampling Rate: 44.1kHz
- Input Rate 1Fs or 2Fs by Normal/Double Mode Selection (Not Included H1 in Interpolation)
- On-Chip Voltage Reference
- Digital De-emphasis
- Low Clock Jitter Sensitivity
- Digital Attenuation function

DAC

The DAC used in S5L9231 is used to supply the signal that runs the pick-up's motor driver. It changes the digital signal from the motor driver to an analog signal at the DSP core. Focus and Tracking motor activating signal is 8-bit, while the sled and spindle motor activating signal is 6-bit.

FEATURES

- Maximum Conversion Rate: 0.5 MSPS
- DLE: ± 1.0 LSB
- ILE: ± 1.0 LSB
- Full Scale Output: 0 - 5 V

TIMING DIAGRAM

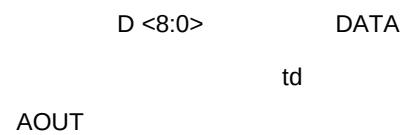


Figure 33. Timing Diagram

- Output delay measured from the 50% point of the rising edge of DATA to the full scale transition.

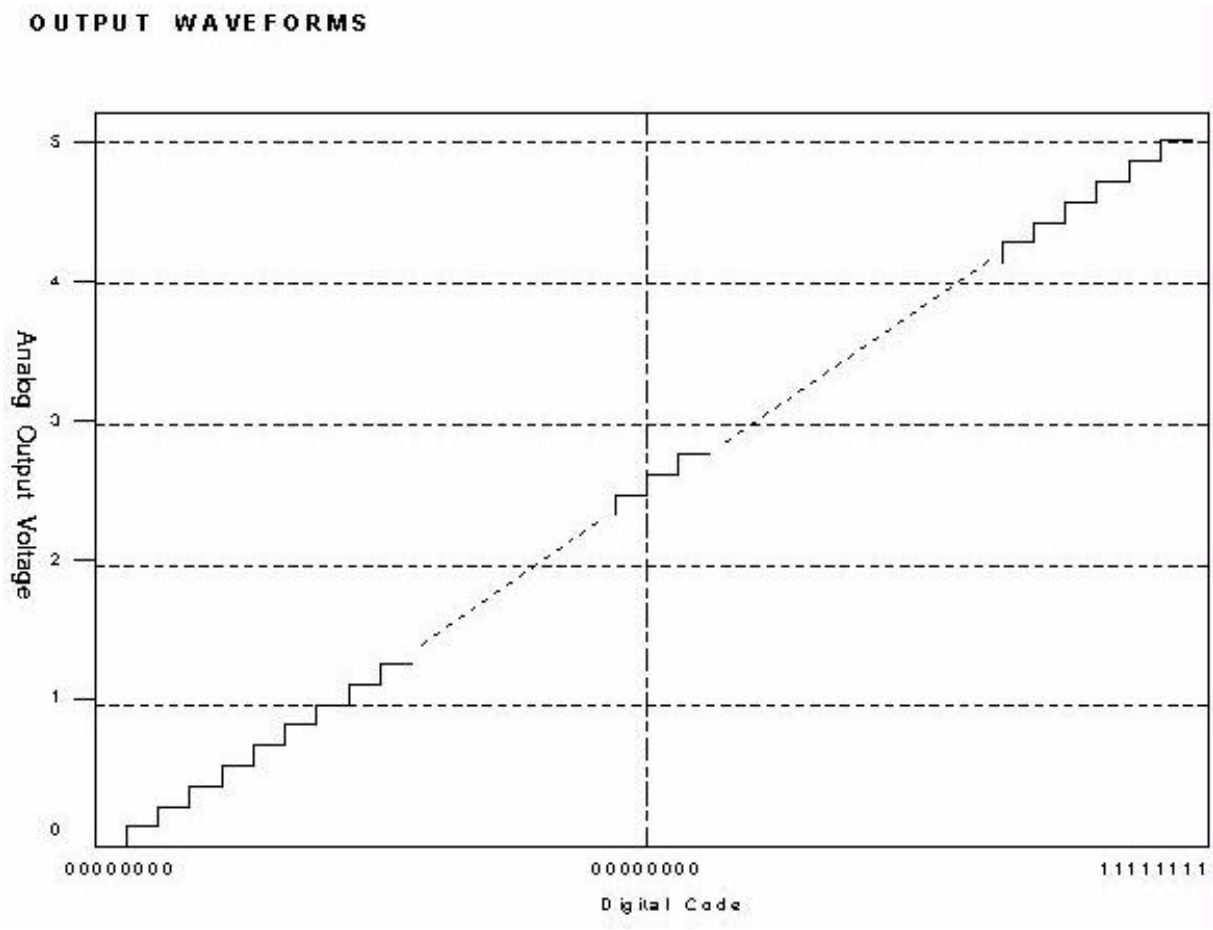


Figure 34. Output Waveforms

CMOS RF

The CMOS RF is the S5L9231's analog block, and it fulfills the function of receiving (from pick-up) and handling EFM, focusing/tracking RF signals, and sending them to servo.

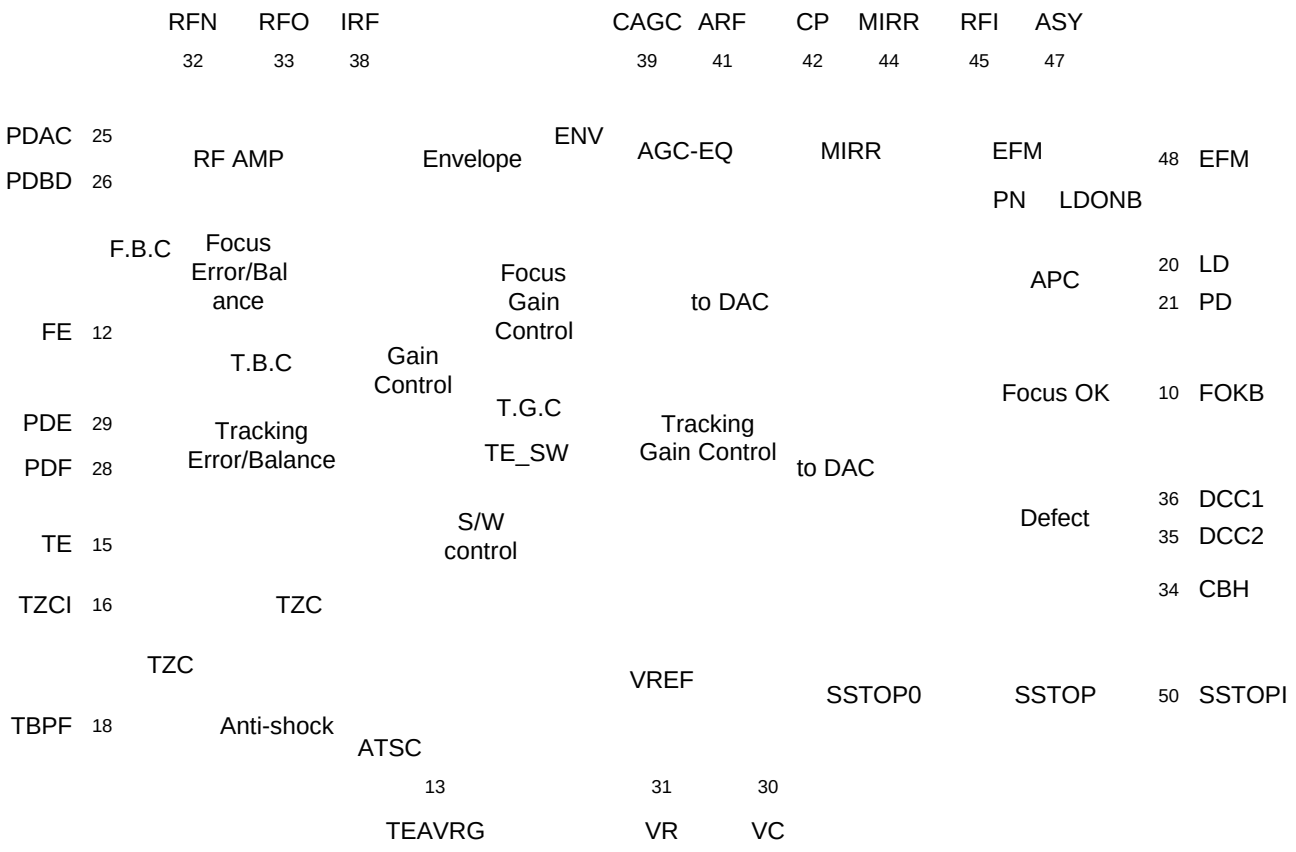


Figure 35. RF Block Diagram

· **RF Amplifier**

The Photo Diode's current input into the input pins PDAC and PDBD are transformed from current to voltage in the RF I/V AMP. The Photo Diode (A+B+C+D)'s transformed voltage value is output to the RFO block. Also, this RF Amplifier Block supports CD-RW Disc format. There are 4 modes (1X, 2X, 3X, 4X) according to the values of R1 and R2 which are set by Micro Controller command.

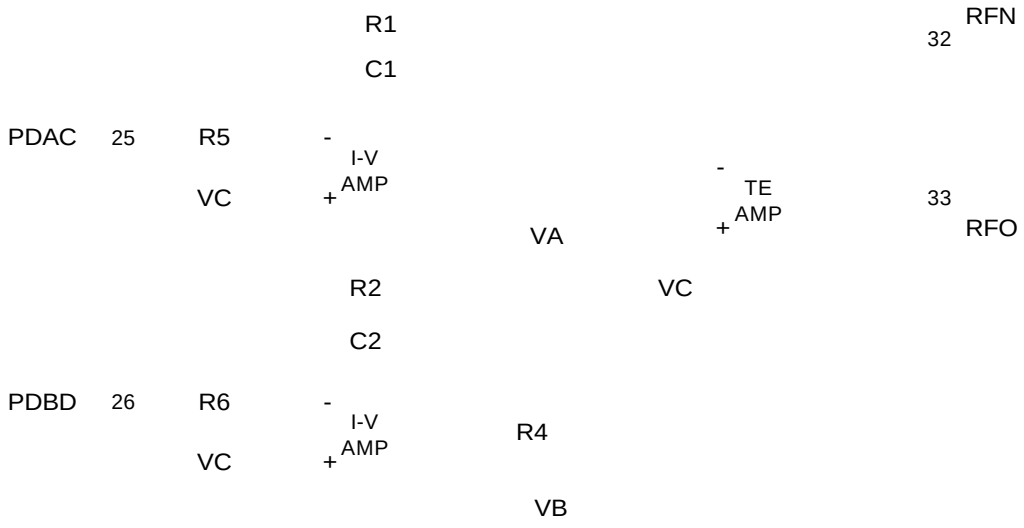


Figure 36. RF Amplifier Circuit

· **Tracking Error and Balance Block**

The Side Spot Photo Diode current, input into PDE and PDF blocks, goes through the I-V AMP and is converted into voltage. The difference is gotten from the Tracking Error AMP. The Micro Controller programming carries out the balance adjustments by adjusting the PDE block's gain. Also, this RF Amplifier Block supports CD-RW Disc format. There are 4 modes (1X, 2X, 3X, 4X) according to the values of R3 and R4 which are set by Micro Controller command.

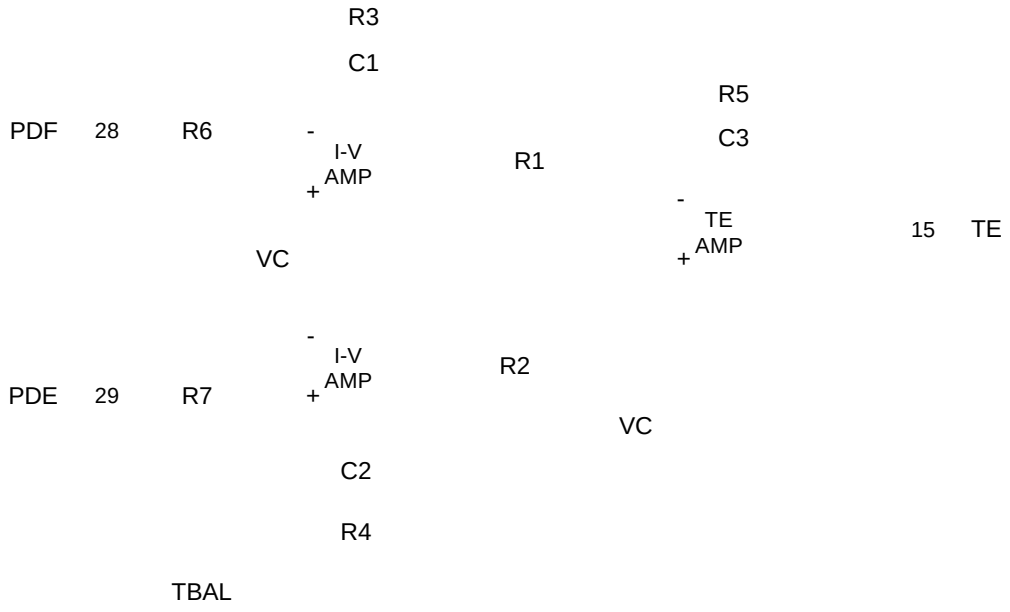


Figure 37. Tracking Error and Balance Circuit

· **Tracking Zero Cross**

The TZC carries out the function of changing the TE signal to digital. It receives TE input from the RF, passes it through the voltage follower, then compares it to the standard voltage. The TZCI connects a capacitor to the input to receive the TE signal as input, and is buffered to send out digital output as TZC. TZC is applied when phase compensating within the tracking servo. TZC is applied to activate the pick-up by sending the compensated value to the tracking activation block.

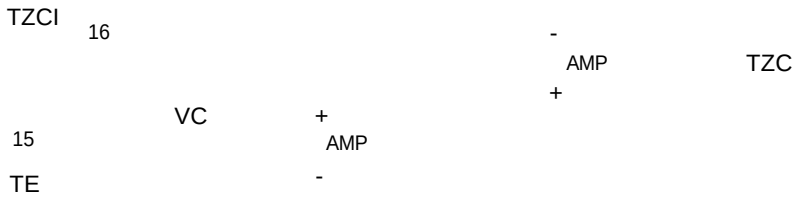


Figure 38. Tracking Error Cross Circuit

- **FOCUS ERROR AMP AND BALANCE BLOCK**

This block takes the difference between the RF I-V AMP output VA and the RF I-V output VB, and outputs the Photo Diode ((A+C)-(B+D))'s I-V transformed voltage. This block is Micro Controller programmed so that the VB block can automatically adjust the gain to adjust the balance.

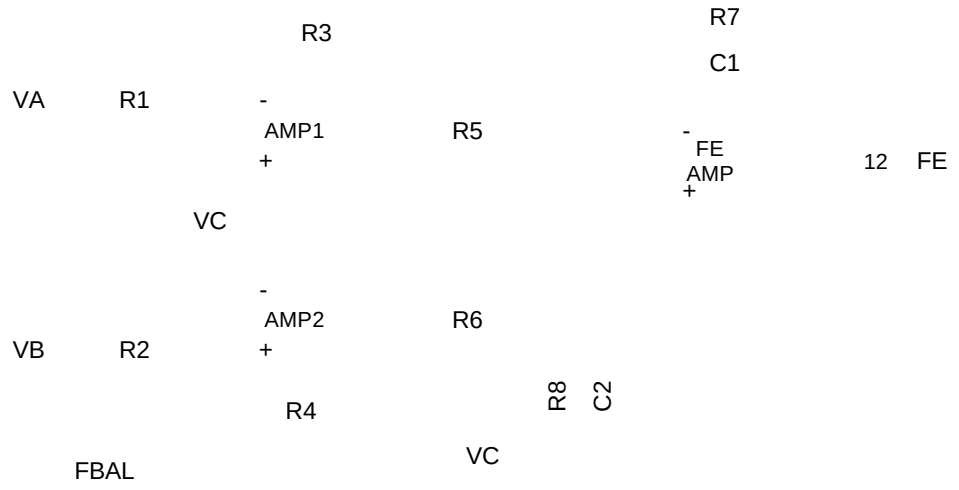


Figure 39. Focus Error Amplifier and Balance Circuit

- **Focus OK**

RFI and RFO blocks' DC components are extracted and compared with the standard DC values. If the RF level is above standard, FOK is output to make the timing window, which carries out focus "on" while in focus search status by the Focus OK circuit.

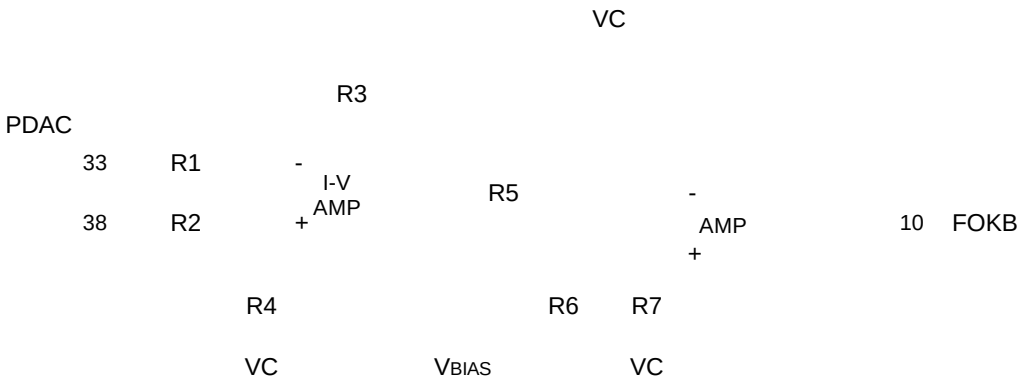


Figure 40. Focus OK Circuit

· **Mirror**

The IRF signal is amplified and then carries out the peak and bottom hold. Peak hold can follow up to 100kHz traverse, and bottom hold can follow the envelope changes of the radiation frequency. Mirror output above 1kHz on the disc's track is "L", and between tracks is "H". If a defect above 1.4 ms is detected, it is also "H".

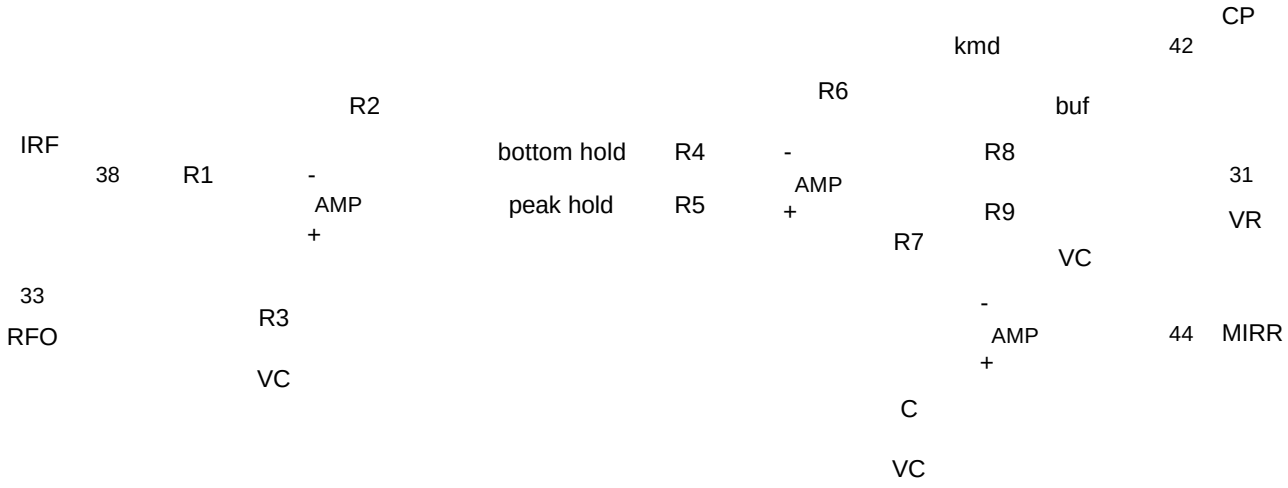


Figure 41. Mirror Circuit

· **EFM Slicer**

The EFM comparator changes the RF signal to a binary signal. Asymmetry generated during disc production cannot be eliminated by the AC coupling, but it can be by adjusting the EFM comparator's standard voltage.

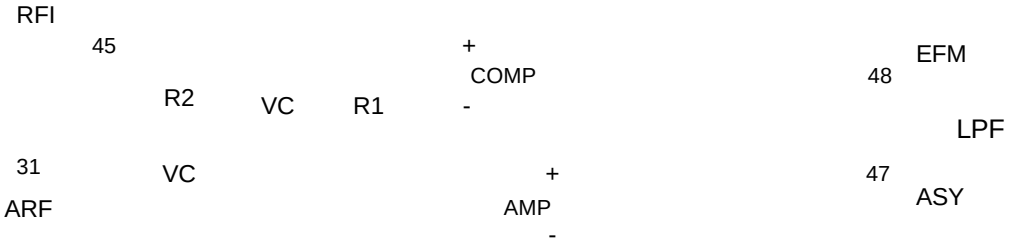


Figure 42. EFM Comparator and Asymmetry Circuit

· **Defect Detection Function**

After inverting the RFO signal, bottom hold is carried out by 2 kinds of the time constants which are long and short. The bottom hold of the time constants holds the defect level just before the defect. The level is differentiated by coupling, then level shifted to compare the signals of both directions to generate the defect detection signal.

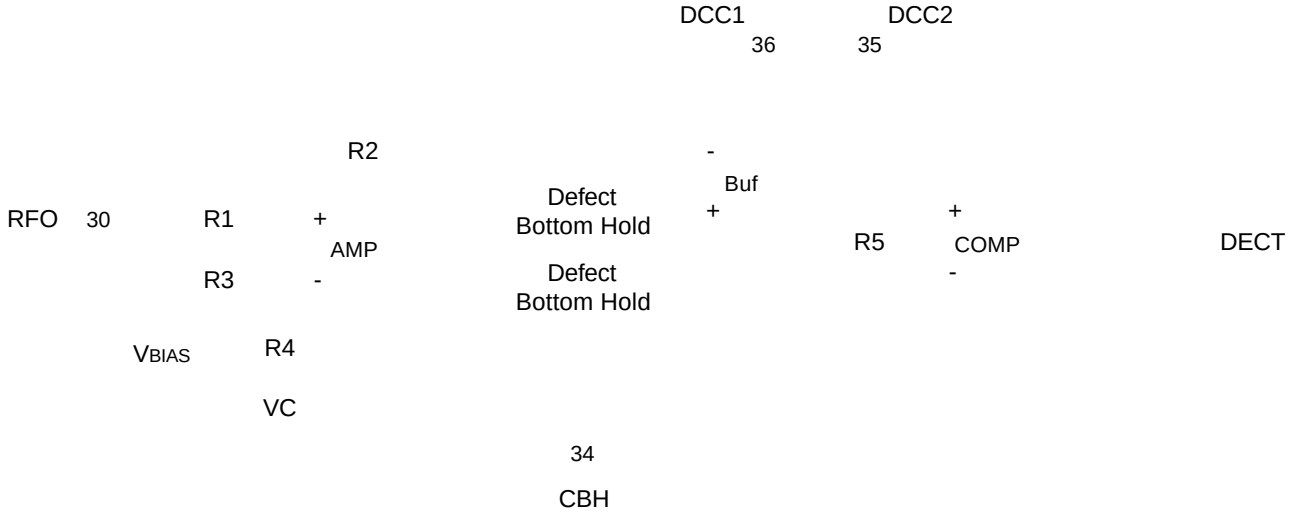


Figure 43. Defect Circuit

· **Automatic Power Control Function**

If you use it in the constant current state, the laser diode has a negative temperature characteristic with a large optical output, and this function controls the monitor photo diode's output so that it is regular.

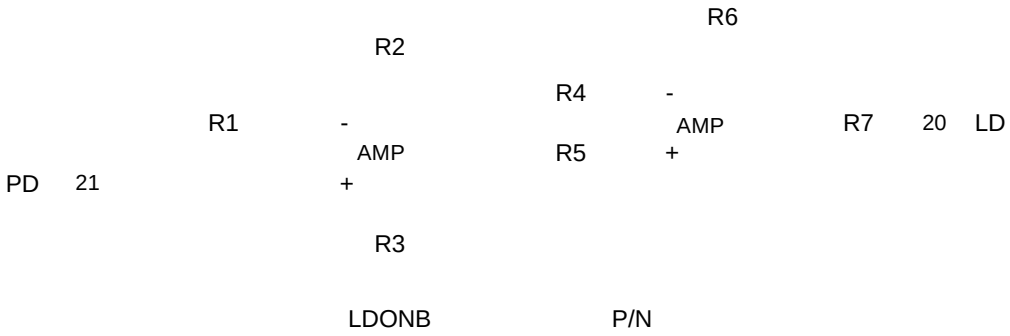


Figure 44. APC Circuit

- **ANTI-Shock Function**

A defect circuit for tracking gain improvement against shock is configured as a window comparator. This circuit detects physical shock from external factors during disc playback. Regular tracking error signal has a very small value, but for external shock, the error value is very large. So, if the width of change is large in the TE's level, "H" is output.

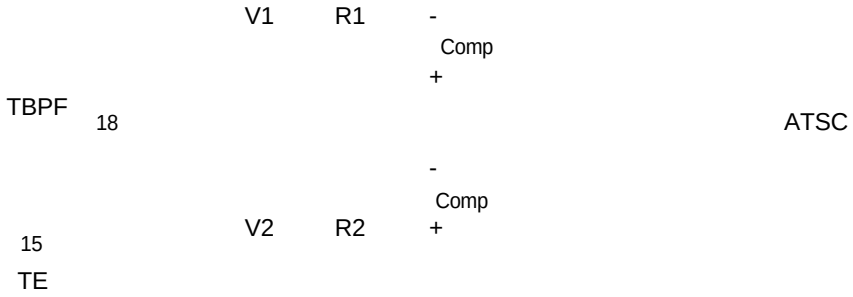


Figure 45. Anti-Shock Circuit

- **Automatic Gain Control Function**

The AGC block, which has a 3T gain boost feature, maintains the RF peak to peak level at a certain level. The block detects the RF envelope, compares it to the standard voltage, then adjusts the gain. It also receives RF output, stabilizes the RF level to 1Vpp, and applies this output as EFM slice input.

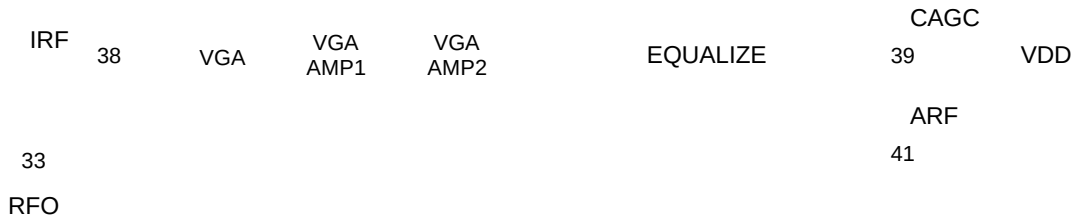


Figure 46. AGC Block

· **Envelope Function**

This circuit detects the amplitude level of the eye patterns which is the RF signal. The envelope's voltage changes according to the IRF's amplitude level. The voltage which is charged at the capacitor connected outside is output through the Buffer AMP after IRF. The DC-removed signal from RFO is rectified.

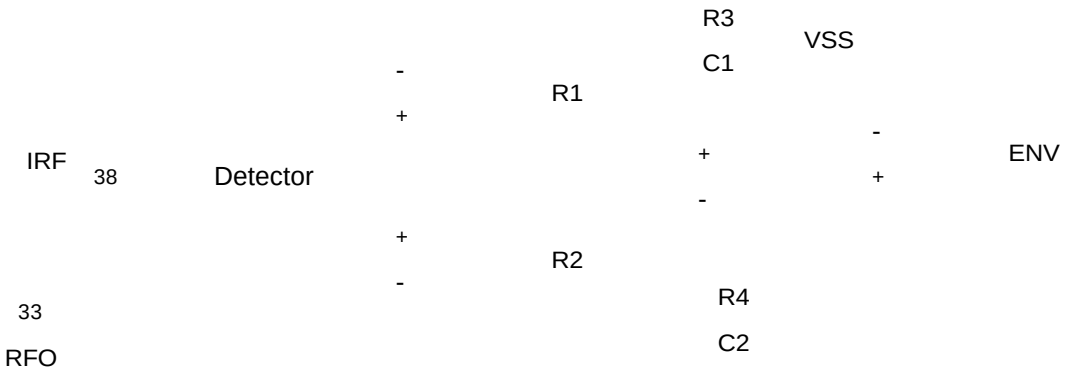


Figure 47. Envelope Detection Circuit

· **Reference Voltage Generator**

This generator makes reference voltage using the resistance divider. VC is the center voltage's input, and it uses external reference voltage or VR.

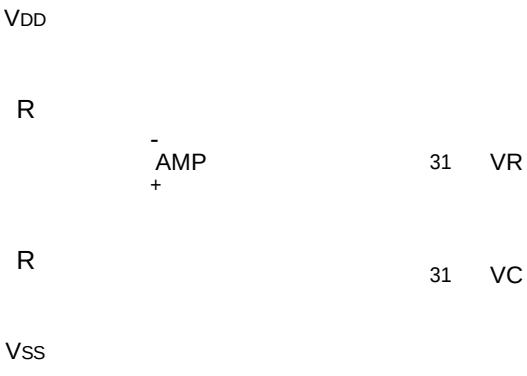


Figure 48. Reference Voltage Generation Circuit

- **SSTOP Block**

When the pick-up is at the innermost circumference of the disc, the SSTOP block generates the stop signal.

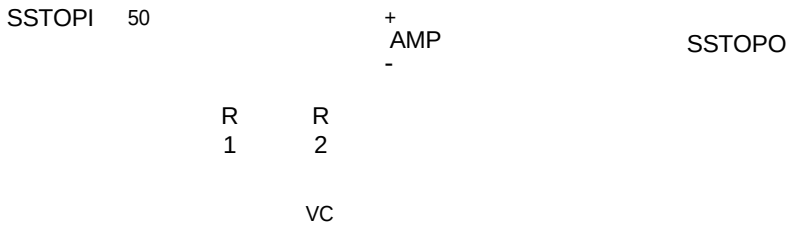


Figure 49. SSTOP Circuit

- **Interruption Function**

To prevent the collapse of the RF signal caused by interruptions such as scratches, the following measures are taken. Using the mirror signal, the tracking servo's defect switch route is taken, sending the error caused by the interruption through the low pass filter, thus lowering the error level.

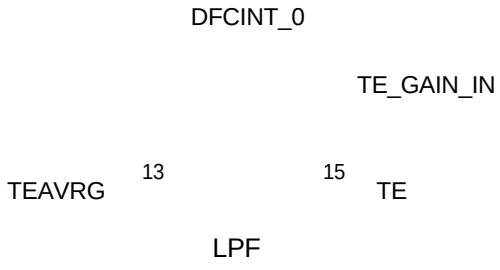
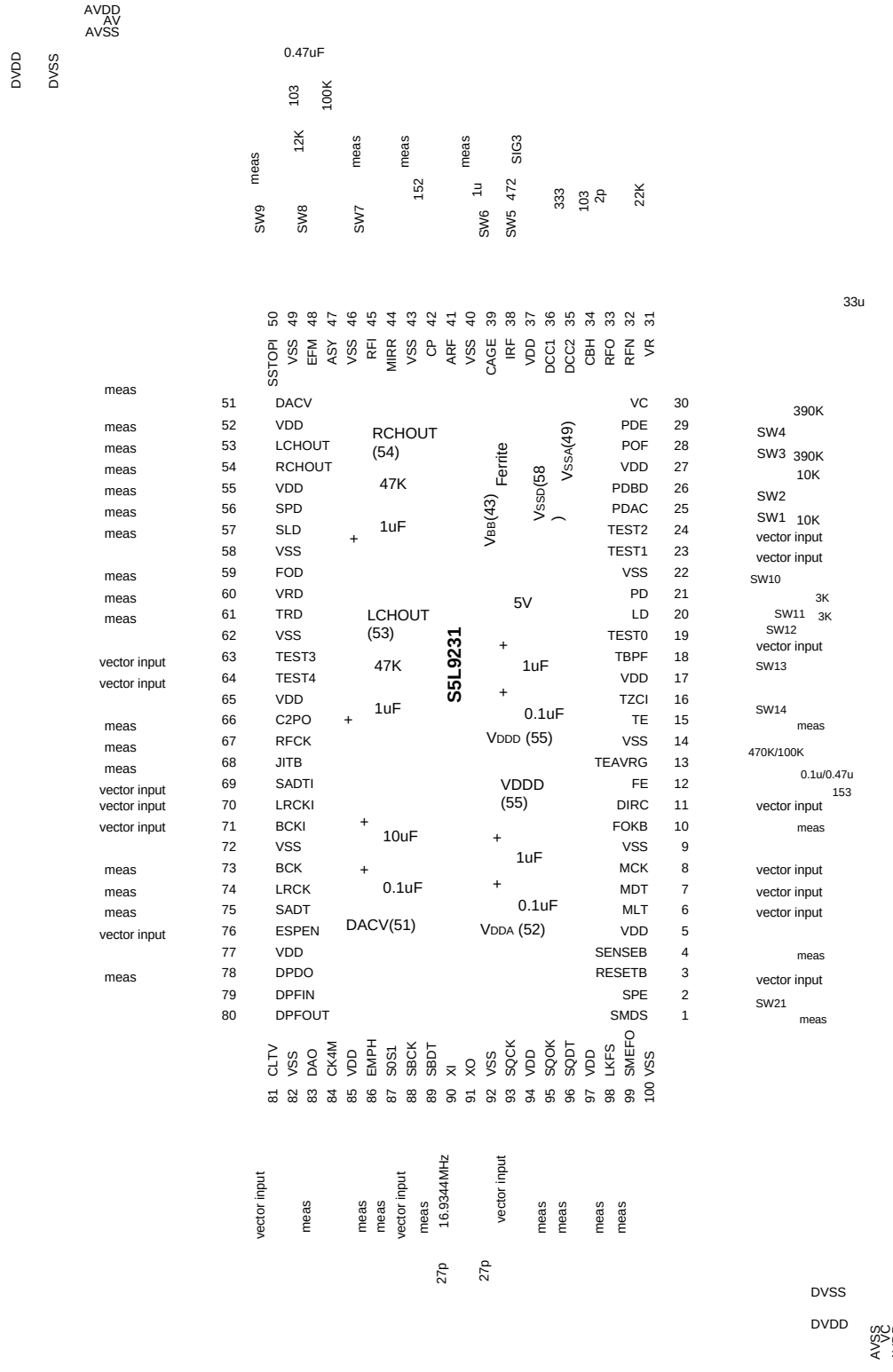


Figure 50.

TEST CIRCUIT



APPLICATION CIRCUIT

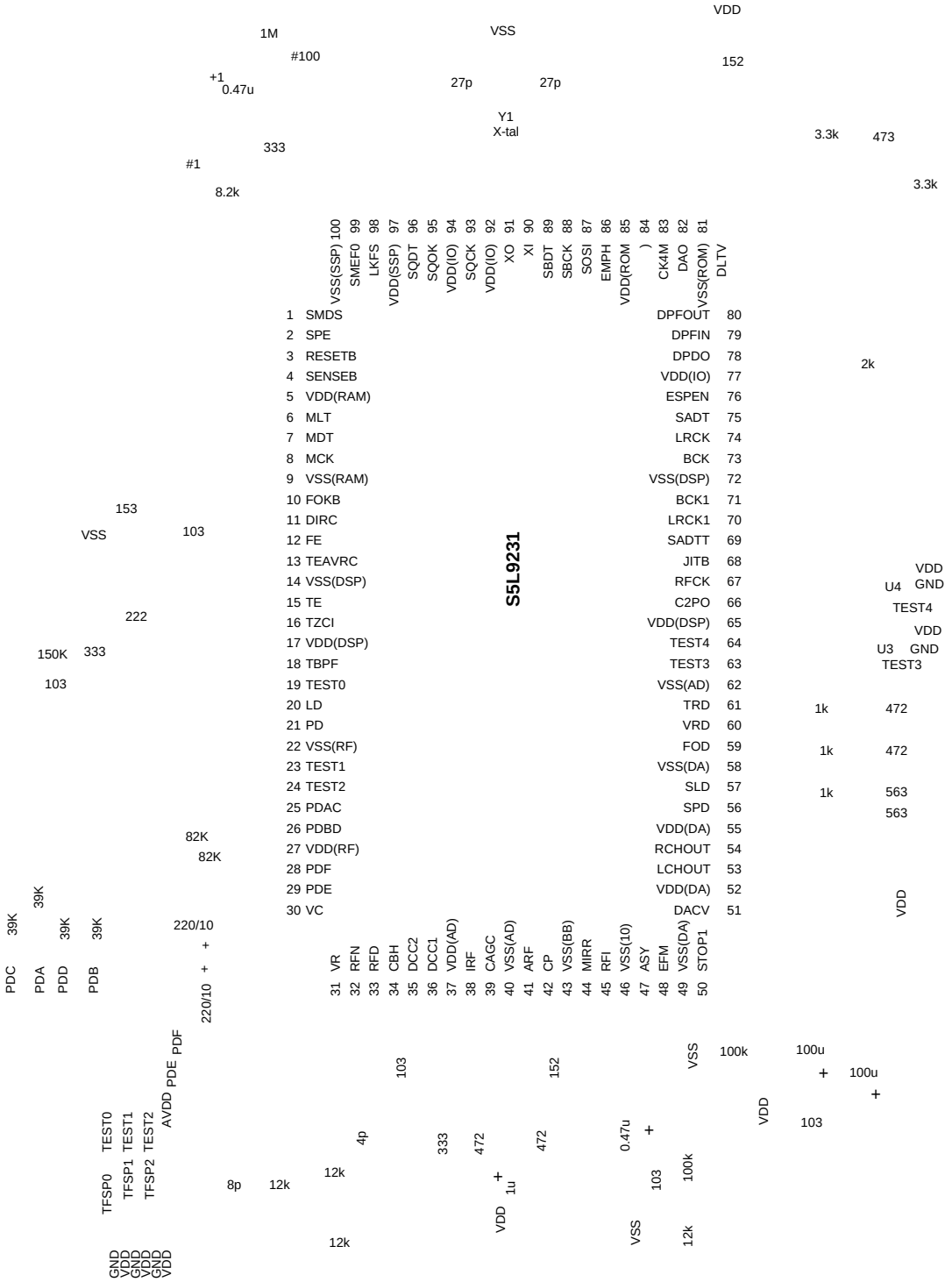


Figure 52. Application Circuit