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SAMSUNG 386SX PC/AT SINGLE CHIP
KS82C388

OVERVIEW

The SAMSUNG KS82C388, 386SX PC/AT single chip, is a controller for high performance PC-ATs with the 80386SX or the Cx486SLC CPU. Major features of the KS82C388 include:

· Two modes of operation
- MODE1 for cache systems (DRAM banks reside on MD bus)
  Zero wait state cache read hit operation up to 40MHz
- MODE2 for non-cache systems (DRAM banks reside on D bus)
  Zero wait state DRAM page read hit operation up to 33MHz

· High performance cache controller for 25, 33 and 40MHz systems (MODE1 only)
- Direct mapped cache organization
- Buffered posted write-through DRAM updating scheme
- Supports I6KB, 32KB and 64KB of data cache
- Non-cacheable region that can range from 1KB to 1MB
- Uses external TAG RAM and internal TAG comparator

· High performance DRAM controller
- Supports the full 16MB physical address space
- Supports 256Kb/IMb/4Mb DRAM
- Page mode operation with programmable wait states and RAS/CAS timing
- 384K memory relocation option
- System and Video BIOS shadow RAM function
- Zero wait state page read hit operation up to 33MHz (MODE2 only).

· On-chip Integrated Peripheral Controller (82C206)
- 7 DMA channels
- 13 Interrupt request channels
- 2 Timer/Counter
- Real Time Clock with 114 bytes of CMOS RAM

· Supports 80387SX Coprocessor

· Supports 8-Bit / 16-Bit ROM

· Synchronous PC-AT bus clock with programmable frequency

· Provides local bus VGA graphics support

· Fast Gate A20 and Fast Reset for OS/2 optimization

· 100% IBM PC/AT compatible

· 208 Pin PQFP (Plastic Quad Flat Package)

The KS82C388 has two modes of operaion (MODE1 for cache based systems, MODE2 for systems without cache). With these two modes, two types of PC-AT system can be implemeted. The resulting system organization is illustrated in Figure 0-1.

The KS82C388 generates and synchronizes all control signals for busses and manages the interfaces of all function blocks inside the chip, e.g. Reset/Shutdown logic, CPU/Local Memory/AT/Cache state machines, arbitration and refresh logic, DRAM and cache controller (refer to Figure 0-2a.). The internal cache controller supports direct mapped cache organization with data cache sizes of 16KB, 32KB or 64KB. It implements a posted write-through DRAM updating scheme.

By integrating the cache controller along with the DRAM controller, the KS82C388 can further enhance system performance by time-sharing cache and DRAM cycles. For example, when a read cycle starts, cache access and DRAM access are performed in parallel and DRAM cycles can continue and/or be terminated depending on the outcome of the cache hit/miss signal from the TAG RAM directory. The KS82C388 thus can achieve a faster cache line fill during a cache miss cycle.

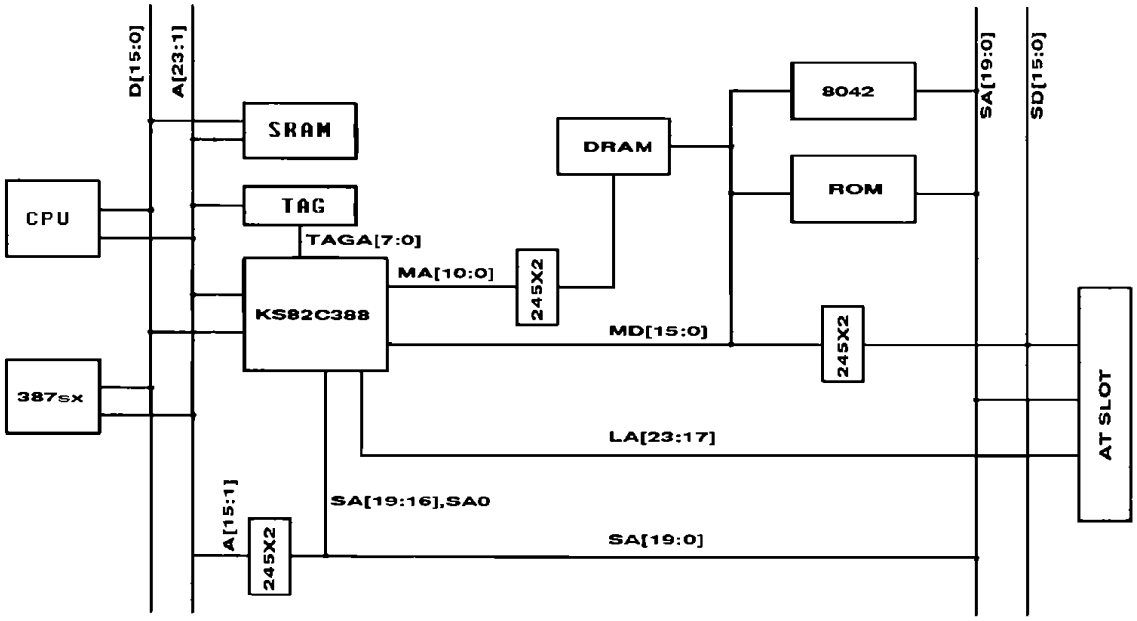


Figure 0-1a. Desktop System Block Diagram - MODE1 (DRAM on MD bus mode for CACHE based systems)

The KS82C388 also contains the control logic to manage the interface between the CPU data bus, local main memory data bus, local system bus, PC-AT bus, ROM, and on board peripherals (refer to Figure 0-2b). It also implements the byte alignment and byte swapping logic for data transfer where source and target are of different bus widths. The parity logic embedded in the chip generates and writes the parity bits into the DRAM array during main memory write cycles. It also latches the data parity for each byte during memory read cycle. The parity handler and associated NMI logic is designed to assure data integrity throughout the system operation. The built-in coprocessor detection/interface circuitry supports the 80387SX Math Coprocessor without additional discrete logic.

The AT peripherals - 8237 DMA, 8254 Timer and the 8259 Interrupt controller as well as the Real Time Clock and the associated CMOS memory are included on the KS82C388. This results in an AT system with very few external logic devices.

The KS82C388 is available in 208 Pin PQFP (Plastic Quad Flat Package)

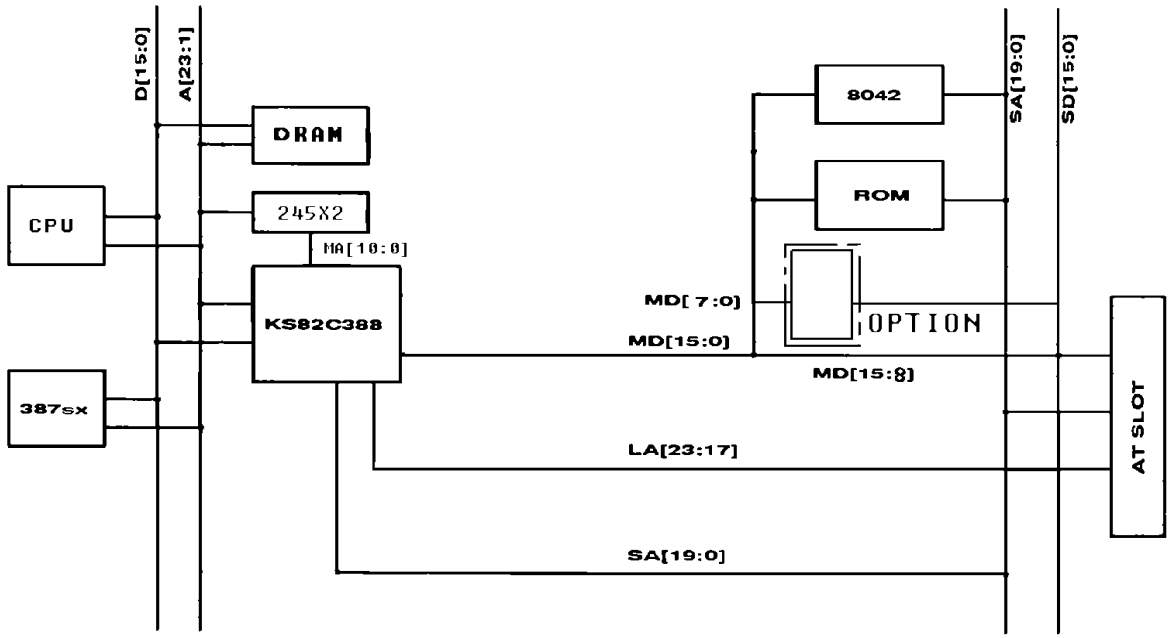


Figure 0-1a. Desktop System Block Diagram - MODE2 (DRAM on MD bus mode for CACHE based systems)

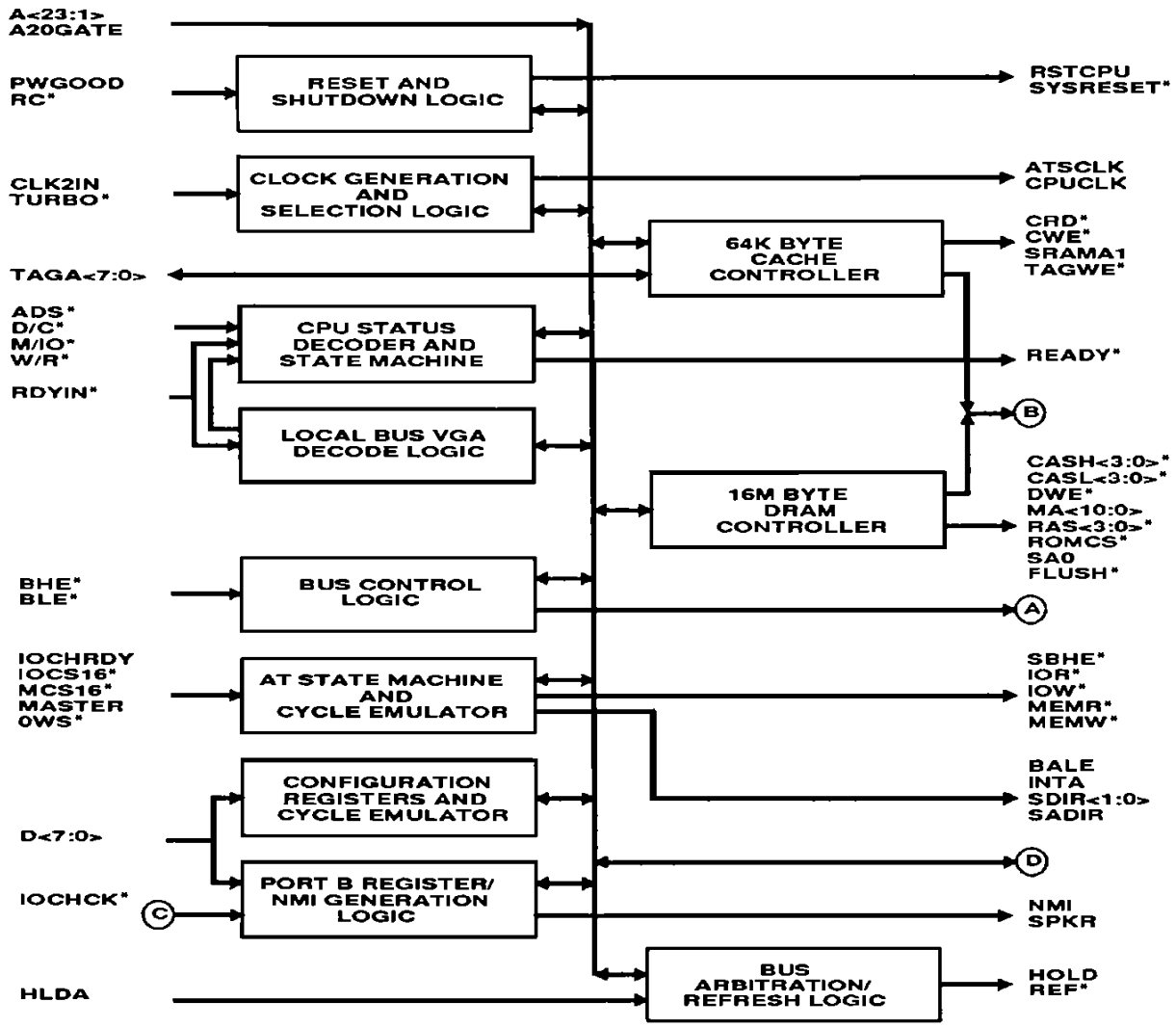


Figure 0-2a. KS82C388 Block Diagram

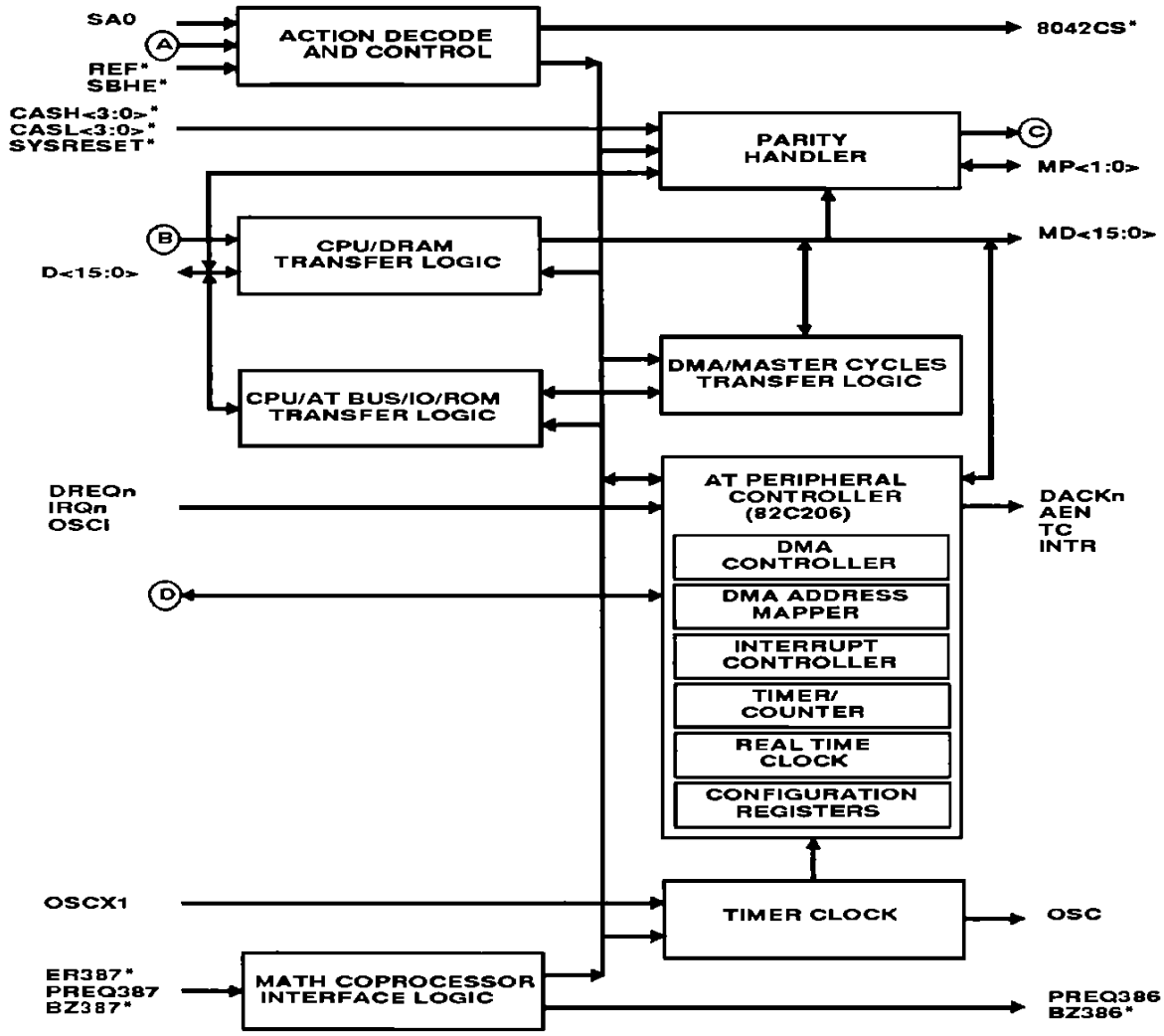


Figure 0-2b. KS82C388 Block Diagram (Cont.)

1. KS82C388 FUNCTIONAL DESCRIPTION

1.1 Reset and Shutdown Logic

The KS82C388 takes PWGOOD and RC* inputs and generates the signals RSTCPU and SYSRESET* that trigger both warm and cold reset. PWGOOD is the Power Good signal and originates at the power supply. When PWGOOD is low, the KS82C388 will assert RSTCPU and SYSRESET* thereby initiating a cold reset of the complete system. If RC* is asserted by the keyboard controller (8042 or 8742) a system warm reset is generated, the KS82C388 asserts RSTCPU to reset the CPU. RSTCPU is also asserted by the KS82C388 when a shutdown bus cycle is detected.

Both RSTCPU and SYSRESET* last for at least 80 CPUCLK cycles. The HIGH to LOW transition of RSTCPU and the LOW to HIGH transition of SYSRESET* signal is synchronous with the CLK2 input signal of the CPU. This guarantees that the phase of the internal clock of the KS82C388 state machine is the same as the phase of the internal clock of the CPU.

1.2 Clock Generation and Selection Logic

The KS82C388 receives three clock inputs: CLK2IN, OSCX1 and OSCI. It generates various clock signals to drive the CPU, the coprocessor, DRAM/Cache/AT state machines and the AT bus system. CLK2IN is derived from a crystal oscillator running at twice the rated frequency of the CPU.

The KS82C388 generates two clock output signals: CPUCLK and ATSCLK. The processor clock CPUCLK drives the CLK2 inputs of the CPU and the coprocessor. It is also used to drive KS82C388 internal DRAM/Cache state machines. ATSCLK is the AT bus system clock.

CPUCLK is derived from CLK2IN to allow the CPU to operate at the maximum speed. ATSCLK is a subdivision of CLK2IN. The ATSCLK frequency can be programmed to be CLK2IN/4, CLK2IN/6, CLK2IN/8 or CLK2IN/10 by setting bits <7:6> of configuration register 11h.

1.3 Port B Register and NMI generation logic

The KS82C388 provides access to the Port B defined for PC/AT system level function control. The port can be accessed through any odd I/O port address between 61h and 6Fh. Table 1-1 shows the register definition:

Table 1-1. Port B register Definition

BITS	READ/WRITE	DEFINITION	
7	READ ONLY	PCK	Memory Parity Check
6	READ ONLY	IO CH CK	IO Channel Check
5	READ ONLY	OUT 2	Timer 2 (8254) Out
4	READ ONLY	REF DET	Refresh Detect
3	READ/WRITE	ENA IO CK__	Enable IO Channel Check
2	READ/WRITE	ENA RAM PCK__	Enable RAM Parity Check
1	READ/WRITE	SPKR DATA	Speaker Data
0	READ/WRITE	T2GATE SPK	Timer 2 Gate Speaker

The master enable for NMI (non-maskable interrupt) is programmed through bit 7 of system I/O port 70h inside the KS82C388. If this bit is set to 1, NMI generation is disabled and if set to 0, it is enabled. After bit 7 of system I/O port 70h is set to 0 and the corresponding NMIs are enabled in Port B, a non-maskable interrupt is generated to the CPU and the source of the NMI is latched in Port B. Bits <7:6> indicate a memory parity error (PCK) or an I/O Channel Check error (IOCHCK).

1.4 Action Mode Codes Generation

This logic performs data buffer action mode codes generation for CPU accesses to devices on the CPU (D) bus, system (SD) bus, or memory (MD) bus. The AT bus conversions are performed for 16-bit and 8-bit read or write operations. 16-bit transfers to and from the CPU are broken into 16- or 8- bit AT bus cycles. The KS82C388 generates action mode codes for internal use. These codes control the buffers in the KS82C388 for byte alignment, direction control and data conversion between the D, MD and SD data buses. Data buffer action mode codes are also used by the KS82C388 to generate encoded Chip Select (CS*) signals for on-board I/O ports.

1.5 CPU State Machine, Local Memory State Machines, Cache State Machine, AT Bus State Machine

In the original IBM AT architecture, the CPU and AT bus run at the same speed. In order to maintain AT compatibility and to achieve the highest system performance, the CPU, the local DRAM and cache memory are driven by CPUCLK while the AT bus is driven by ATSCLK. This allows the CPU and memories to operate at much higher frequencies, whereas the AT bus runs at an AT compatible 8 MHz speed. For synchronization, the KS82C388 contains several state machines to control all the accesses initiated by the CPU, DMA/AT Bus Master or Refresh Request Timer.

The CPU state machine, DRAM and Cache state machines control all the accesses to the local bus (DRAM, Cache SRAM or coprocessor cycles). These state machines support only 16-bit data transfers between the CPU and the system memory; therefore no bus conversions are required.

The AT bus state machine is responsible for all non-local bus accesses and controls the AT bus for proper bus conversions.

1.5.1 CPU State Machine

In the KS82C388, the CPU state machine provides the interface to the CPU. The CPU state machine monitors and decodes the bus status lines, ADS*, W/R*, M/IO*, D/C* and establishes the type of bus cycle to be performed. The CPU state machine begins its cycle upon assertion of ADS* and terminates the cycle upon generation of READY* at completion of the access.

For each new CPU cycle, the CPU state machine generates an internal signal CYCSTART (cycle start). It is sent to other state machines to indicate the beginning of a CPU cycle. Another internal signal LMEM16* is generated by the memory controller module to distinguish a local memory access (DRAM or SRAM) from a non-local memory access. After generation of CYCSTART, the CPU state machine samples the LMEM16* signal. If LMEM16* is active, it is a local memory cycle and control passes to the local DRAM and Cache state machines. DRAM or cache state machine generates the READY* to terminate the CPU cycle. However, if LMEM16* is inactive, the control is passed to the AT state machine. The CPU state machine then waits for the generation of the READY* signal from the AT state machine to terminate the cycle.

1.5.2 Local Memory State Machines

The DRAM array can be accessed by three different sources - CPU memory cycles, DMA/MASTER to local DRAMs, and refresh requests from the internal timer output. These different accesses are controlled by three different state machines in the KS82C388 DRAM module.

The KS82C388 DRAM controller can support one, two, three or four banks of local DRAMs. Each RAS* line drives one DRAM bank, and each CAS* line drives one byte of memory data. The DRAM row and column addresses are output on the MA<10:0> address pins.

When a memory location is decoded to be within the local DRAM range (LMEMI6* active) and a cache miss/or a write hit cycle is detected, the CPU and Cache state machines pass control to the local DRAM state machine. The local DRAM state machine generates RAS<3:0>*, CASH<3:0>*, CASL<3:0>*, DWE*, and row/column address signals. The DRAM state machine also generates CWE* to update the data cache during the cache read miss cycle. During a read miss the local DRAM state machine initiates two DRAM accesses with inverted and non-inverted A1 address for each cycle respectively.

The KS82C388 provides configuration registers to store memory system information for page mode, DRAM wait states, and shadow DRAM. For a "page hit" cycle, RAS* stays asserted after the previous accesses. For a "page miss" the DRAM cycle starts by first de-asserting the RAS* corresponding to the accessed bank. The local DRAM state machine also inserts programmed wait states into the DRAM cycle.

Local DRAMs can also be accessed by a DMA controller or an AT bus master. DMA/MASTER local DRAM access is initiated by asserting HLDA1(internal signal). The MEMR* and MEMW* determine if it is a read or write memory access per DMA/Master bus cycle. Local memory refreshes are controlled by a separate refresh state machine.

1.5.3 Cache State Machine

The main function of the cache state machine in the KS82C388 is to manage the external tag directory and external cache memory through various CPU and DMA/Bus Master cycles. The KS82C388 runs in non-pipelined mode with zero or one wait state. For data coherency between the data SRAM and main memory, the cache state machine has to monitor the system bus used by the DMA controller or AT Bus Master. During a DMA/MASTER write hit cycle, when the other master overwrites DRAM contents of which the SRAM also has a copy, the cache state machine will update the data in the cache memory.
In zero wait state mode, a CPU cache read hit cycle completes the access in two T states. The cache state machine generates the READY* signal back to CPU a quarter way into the second T state to terminate the cycle.
For one wait state, a CPU cache read hit cycle takes three T states to complete the access. The cache state machine generates a READY* signal to the CPU at the beginning of the third T state.

For CPU memory cycles that are not cache read hits, the cache state machine passes control over to the DRAM or the AT state machine. This occurs at the middle of the second T state after ADS* is active. One of the state machines generates the READY* signal to the CPU and terminate the cycle. For the DRAM state machine, the number of T states between ADS* and READY* depends on whether RAS* is active or inactive, page hit or miss, and the number of DRAM wait states programmed. Writing to cache SRAM is controlled by the cache state machine for cache write hit cycles. For read misses or cache line fill, the DRAM state machine controls the write operation to cache SRAM.

1.5.4 AT Bus State Machine

The AT bus state machine is invoked when CYCSTART is generated and LMEM16* is inactive. The AT state machine is driven by ATCLK2, which runs twice the frequency of the AT bus clock (ATSCLK). The AT bus cycle is initiated by asserting the BALE signal and is terminated by asserting READY*. The KS82C388 supports 8-bit or 16-bit transfers between the processor and 8-bit or 16-bit peripherals located on the AT bus. MCS16* and IOCS16* are sampled during the AT cycle to determine the bus size conversion and necessary byte alignment. For the AT memory cycle, MCS16* is sampled at the falling edge of BALE. For the AT I/O cycle, IOCS16* is sampled one-half of the ATSCLK after the falling edge of BALE to accommodate some slower I/O cards. If none of these 16-bit status signals are asserted, 8-bit transfers are assumed and the request is converted into 1 or 2 AT cycles based on BHE* and BLE*.
After BALE goes inactive, the AT state machine enters the command cycle. The command signals for the memory or I/O access remain active until the programmed number of wait states are executed. Bits <3:0> of register 11h control the AT Bus wait state generation for 8- and 16-bit accesses. Bits <5:4> provide the option to ensure enough recovery time for back to back I/O commands. The second I/O command is activated only after the programmed recovery time is satisfied.

After the programmed number of wait states are executed, IOCHRDY is sampled. If IOCHRDY is active (ready), the command becomes inactive after the next ATSCLK cycle. If IOCHRDY is not active (not ready), the commands are extended for an additional cycle (i.e., one ATSCLK) and IOCHRDY is sampled again. This process continues until IOCHRDY becomes active.

1.6 Bus Arbitration

The KS82C388 provides bus arbitration between CPU, DMA, AT bus Master and AT style refresh logic. HRQ, a level triggered signal from the on-chip 82C206, is active when a DMA or a Master is requesting a bus cycle. REFREQ, an edge triggered signal, initiates a DRAM refresh request from the refresh interval timer. The KS82C388 arbitrates between HRQ and REFREQ by sending a hold request (HOLD) to the CPU. The CPU responds to hold request (HOLD) by issuing HLDA to KS82C388 and relinquishes the CPU bus. The KS82C388 then issues HLDA1(internal signal) or REF* depending on which device prevailed during arbitration.

During a normal DMA cycle, the DMA controller has control of the bus until HRQ becomes inactive. During a refresh cycle, the refresh logic has control of the bus until REF* goes inactive and will generate separate control signals for local DRAM as well as AT bus memory.

1.7 Coprocessor Support

The KS82C388 supports the interface logic for the 80387SX math coprocessor. Bus cycle generation is handled by the KS82C388. Interface signals consist of the input signal ER387*, BZ387*, PREQ387, and output signals BZ386* and PREQ386.
At reset, the state of the ER387* signal is sampled to detect the presence of the 80387SX coprocessor. The state is latched into bit 3 of register 12h.
The 80387SX asserts ER387* after an operation resulting in an error not masked by the coprocessor's control register. The KS82C388 uses the ER387* input to generate IRQ13.

During 80387SX operations, the CPU generates one or more I/O cycles to addresses 8000F8h through 8000FCh. The KS82C388 executes a local (non-AT) cycle and no DRAM or AT commands will be activated. When present, the 80387SX generates 387RDY* at the end of the coprocessor cycle. In the absence of 80387SX, the KS82C388 will generate a ready signal (READY*) to terminate the cycle.

1.8 Cache Controller

The memory system in a PC/AT design is usually implemented with inexpensive, slow dynamic DRAMs. A cache memory is a small, high speed unit that resides between the CPU and the main memory. It increases the effective speed of the main memory by providing access to a copy of the most frequently used code or data from the main memory. When the CPU tries to read data from main memory, the high speed cache memory will respond first if the data resides in the cache memory (Hit cycle). Otherwise (miss cycle), a normal main memory cycle will take place.

A cache system can further enhance system performance by time-sharing cache and DRAM cycles. During write cycles, the data is held in a temporary buffer inside the KS82C388. Before the write cycle to main memory is completed, the CPU can access cache memory during a read hit cycle. However, if another read miss cycle or write cycle is performed, it has to wait until the previous write cycle is completed.

The KS82C388 integrates the cache controller and the DRAM controller into a single chip. When a read cycle starts, cache access and DRAM access are performed in parallel. In the case of a cache hit, DRAM commands to main memory are terminated and cache memory provides the data to the CPU. In the case of a miss, a DRAM cycle will be completed. The integrated cache controller reduces the time penalty during a miss cycle because it does not have to wait for a HIT/MISS signal from the external cache tag RAM to start a DRAM operation.

1.8.1 Cache Performance

A cache reduces the average memory access time if it holds the most frequently requested code and data. The effectiveness of the cache is determined by the data cache size, line size, cache mapping scheme, cache replacement algorithm, and type of program execution.

The cache miss rate decreases with increasing data cache size. The gain is marginal, however, if the cache is 64KB or larger. The cache controller moves data from main memory to the cache during a miss cycle. A block is the basic unit of memory in that process. A typical block size (line size) is 4 bytes. A large line size increases the hit rate if the CPU is accessing consecutive addresses or repeating a short loop. On the other hand, a large line size takes longer to transfer and increases the likelihood of unneeded data being placed in the cache. In the KS82C388 direct mapped cache, each block holds one set of memory locations. The index field addresses are used to select one entry in the tag directory. The tag field addresses are compared with the contents of the tag directory to determine whether the access is a hit or a miss.

1.8.2 KS82C388 Cache Organization

The KS82C388 supports 16KB/32KB/64KB data cache options. The cache controller is a direct mapped organization.
Table 1-2 outlines direct mapped cache organization for the 16KB, 32KB and 64KB cache. It lists the physical address assignments of line select, set select, and tag field for all cache options supported by the KS82C388.

Table 1-2 Direct Mapped Cache Organization for 16KB, 32KB, and 64KB Data Cache

CACHE DATA SIZE	16KB	32KB	64KB
Line Size(Byte per line)	4	4	4
Set #	4K	8K	16K
Line Select	A1	A1	A1
Set Select	A2-A13	A2-A14	A2-A15
Tag Field	A14-A21	A15-A22	A16-A23

1.8.3 General Operations

In this section the following operations are illustrated in detail:

Read hit cycle
Read miss cycle
Write cycle
DMA/Master cycle

1.8.3.1 Read Hit Cycle

When the CPU starts a read cycle, the block (index) field of physical addresses selects a line from the cache directory. The tag bits stored in that location are compared with the CPU address inputs; a hit cycle is indicated when there is a match. The KS82C388 generates CRD* to transfer data from cache memory to the CPU. A ready signal (READY*) is sent to the CPU to terminate the cycle.

After power up, the tag directory is flushed by the BIOS. (During this time, the KS82C388 forces all local memory accesses to be DRAM cycles.)

1.8.3.2 Read Miss Cycle

In a read miss cycle, the DRAM memory provides the data to the CPU and writes the same data to cache memory. The cache controller then updates the tag entry. The next time the same address is accessed, it will result in a hit cycle.

There are 4 bytes for each line. For each read miss cycle, two words are moved into the cache memory. Two DRAM accesses have to be completed before the current cycle can be terminated.

During the first data move-in and DRAM access, SRAMA1 drives inverted A1 address to data cache RAM and A1 is inverted to drive the DRAM address output. During the second data move-in and DRAM access, SRAMA1 returns to non-inverted A1 state and that same A1 drives the DRAM address output. At the end of the second DRAM access (non-inverted A1 access), the requested data is available on the CPU data bus and the ready signal, READY* is generated to terminate the cycle.

1.8.3.3 Write Cycle

During a write miss cycle, no cache write or tag updates are performed. The CPU writes the data to the DRAM array without any interaction with cache memory. In the case of a hit access, CPU data is written to cache memory as well as to the DRAM array. This will ensure that cache memory maintains the same copy of data as the main memory so that no "stale data" problem occurs. Since a SRAM write is much faster than a DRAM write, additional wait states will be needed before the CPU data is copied into DRAM. In order to enhance system performance, the KS82C388 incorporates a "posted write" scheme. If the next cycle does not require DRAM accesses (cache hit, AT, I/O cycles), the write cycle is running an equivalent of a zero wait state to the CPU. However, if the following cycle requires another DRAM access while the DRAM is busy with the first write cycle, additional wait states will be asserted until the DRAM has completed its previous cycle.

1.8.3.4 DMA/MASTER Cycle

In an AT system, bus masters other than the CPU can access the main memory and alter its contents. When a cache hit access occurs within a master write cycle, data coherence between DRAM and cache memory must be maintained. The KS82C388 will update the cache for that tag location with the same data written into the DRAM. Subsequent CPU memory access to the same memory location will be a cache hit. For local memory read cycles initiated by another master or DMA controller, only local DRAM accesses will be activated.

1.8.4 Other Issues in Cache System Design

1.8.4.1 Non-Cacheable Regions

The KS82C388 provides one non-cacheable region to allow the user to set aside one blocks (size ranges from 1KB to 1MB) of address space as non-cacheable. The starting address of any non-cacheable region has to be on a boundary of that region's size. This region can then be used as ROM area, memory-mapped I/O space, shared memory accessed by multiple masters, or any other memory areas that should not be cacheable. Once the region is defined as non-cacheable, the memory operation can be re-directed to either local DRAM access or AT memory access via bits <7:6> in index register 50h. Non-cacheable features are defined through index registers 50h to 52h.

1.8.4.2 Direct SRAM and Tag RAM access

For diagnostic purposes, the contents of data cache and TAG RAM can be directly accessed by the CPU. Direct SRAM access is defined in index register 60h. If this feature is enabled, then the cache data RAM will be treated as an extension of main memory with 16KB/32KB/64KB block size at starting address 040000h. These features make system debugging and initialization easier, i.e., line invalidation, tag RAM, or data caches RAM purge.

1.9 DRAM Controller

1.9.1 DRAM Operation

The KS82C388 supports page mode of memory access. The BIOS, following reset, provides automatic detection of the number of banks of DRAM present and the DRAM type present within each bank. If different types of DRAM are used, the largest type of DRAM must be in the first bank.
For normal DRAM access, both RAS* and CAS* have to be activated. The memory access time is determined by the Row Address Access time (Trac) rather than the much faster Column Address Access time (Tcac). Page mode DRAMs allow a number of locations within an area of memory (page) to be accessed without repeating the entire address. After providing the row address and asserting RAS*, the column address can be changed a number of times to access a series of locations. Each time a new column address is strobed by CAS*, RAS* must be kept asserted throughout the process. The number of cycles that can be performed is limited by the maximum length of the RAS* active pulse width. The effectiveness of the page-mode DRAM subsystem is determined by the page size and the locality of the program being executed. The page size can be increased by using higher density DRAMs. Table 1-3 illustrates the effective page size for different types of DRAM.

Table 1-3 Effective Page Size for DRAMs

DRAM type	Each bank
256Kb x N	1 KBytes
1Mb x N	2 KBytes
4Mb x N	4 KBytes

1.9.2 Refresh Logic

The KS82C388 provides the following refresh schemes:

- AT refresh
- Slow refresh option

1.9.2.1 AT Refresh

In an AT refresh scheme, the KS82C388 arbitrates the bus after receiving the REFREQ from the internal refresh interval timer and generates HOLD request to the CPU. The CPU relinquishes the bus by issuing the HLDA. The KS82C388 in turn will respond with the REF* and starts the AT refresh cycle. The local DRAM will be refreshed with RAS* active for all banks at the same time the AT bus is refreshed. For refresh, the internal refresh counters provide refresh addresses onto the MA<10:0> and the SA<10:0> and MEMR* and all RAS* lines are asserted.

1.9.2.2 Slow Refresh

Slow refresh is an option provided for local DRAM refresh, not for an AT refresh. Instead of generating refresh request at a rate of 256 per 4ms, the Refresh control register (index 47H, bit 1 & 0) of the KS82C388 can be set to allow slower refresh rate, e.g., 128 per 4ms, 64 per 4ms or 32 per 4ms. The ability to run slow refresh option depends on the local DRAM used. This option is usually applicable when Low power DRAMs are used for local memory.

The KS82C388 refresh logic also provides a special mechanism to reduce system noise during simultaneous refreshing of each DRAM bank. RAS2* and RAS3* are delayed, after RAS0* and RAS1* are generated, to allow the refresh cycle for bank 2 and bank 3 to be performed immediately after refresh of bank 0 and bank 1. This "staggered Refresh" scheme results in a reduction of system level noise when multi-bank local DRAMs are installed.

1.9.3 Shadow RAM

It is preferable to execute codes through the faster local memory (DRAM or Cache RAM) than through the slower EPROMs. System performance can be enhanced by having the BIOS codes reside in local memory, rather than in EPROMs. This is especially true for applications with extensive BIOS calls. The KS82C388 provides a SHADOW RAM feature that, when enabled, allows the BIOS codes stored in the EPROMs to be executed (shadowed) from the local RAM area. However, these BIOS codes need to be transferred from EPROMs into local RAMs prior to use of the SHADOW RAM feature. A the KS82C388 implementation, this transfer is accomplished at system initialization by means of the following procedure:

1) Set register bits in configuration register 41h-44h for different memory access method

2) Copy ROM block to Shadow DRAM block

3) Set Corresponding bits in configuration register 41h-44h for blocks that are write protected.

The KS82C388 can shadow any DRAM block with an address from 0C0000H to 0FFFFFH (i.e., the C, D, E and F block) in 16KByte granularity. In another word, 256KBytes of total DRAM at 16KByte per chunk can be selectively activated for shadowing. With the cache option turned on, the shadow RAM region is then cacheable after the BIOS or other codes are copied into local DRAM. Special attention needs to be made to prevent any write operation onto the shadowed area. This is accomplished by setting write protection bits in procedure 3.

1.9.4 Memory Remapping

The KS82C388 memory remapping logic is able to remap physical memory locations between 640KB to 1MB (address 0A0000 to 0FFFFFH) in 64KByte chunks to the top of total system memory, provided that no portion of the 64KByte is shadowed. This feature is designed not to be limited by the amount of populated system DRAM.
A 64KByte block is not remappable even if only one 16KByte chunk is shadowed.

Special consideration has been given to the remapping logic so that the KS82C388 not only provides up to 384KBytes of remapping capability, but also assures all remapped memory to be contiguous on top of the total system memory.

The 384KByte reserved area at memory locations between 0A0000h and 0FFFFFH can be subdivided into A, B, C, D, E and F blocks, each with 64 KBytes. The KS82C388 supports the following remapping schemes:

1) No remap
2) A,B
3) A,B,D
4) A,B,D,E
5) A,B,D,E,C
6) A,B,D,E,C,F

While block A, B are remapped on top of the system memory, block "X" is remappable if no shadowed area exists within the block. Block "X" will be remapped by the KS82C388 if and only if:

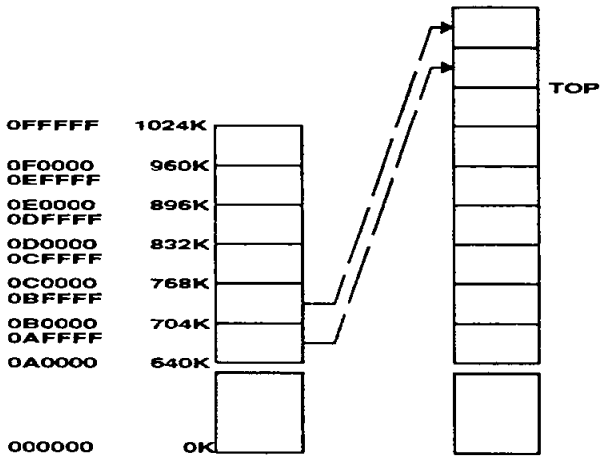
i) It is remappable and
ii) corresponding remap control bit in index register 45h is set to 1;
iii) Other block(s) to the left of block "X" is also remapped,
based on the series of combination stated above.

Refer to Remapping Scheme Figure on the next page for detailed remap implementation.

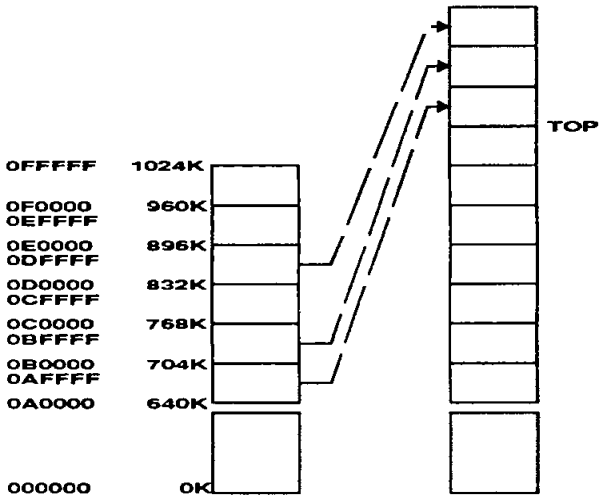
1.9.5 EPROM Control Logic

The KS82C388 provides control logic to generate the ROMCS* signal for an EPROM access. The AT bus state machine generates the READY* for this cycle. ROMCS* is connected to the EPROM chip enable (CE*) input. Since the KS82C388 supports both 8 and 16 bits of ROM, it needs to generate appropriate action codes indicating 8 bits or 16 bits ROM access. These action codes are used within the KS82C388 to transfer ROM data to the CPU data bus.
8 or 16 bits ROM selection is done by strapping DACK7 pin during system reset and the state of the DACK7 pin is latched into the bit 2 of register 40h.

1. The system always remaps 640K to 768K to top of physical memory, if remap is enabled



2. From 832K to 896K area is remapped to top of 640K to 768K area.



3. From 832K to 960K area is remapped to top of 640K to 768K area.

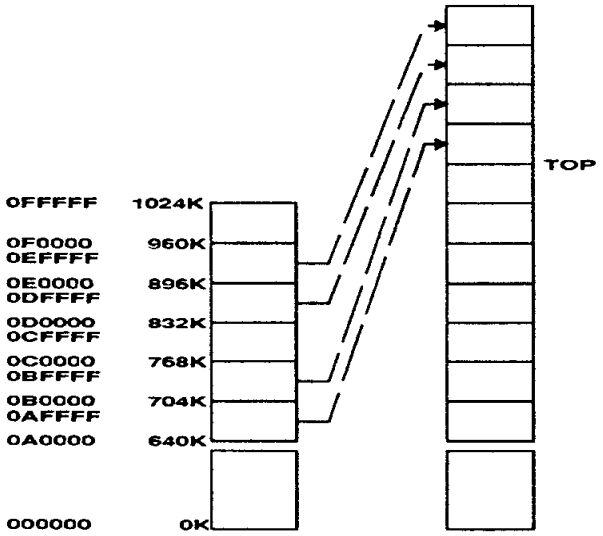


Figure 1-1. KS82C388 Remapping Scheme

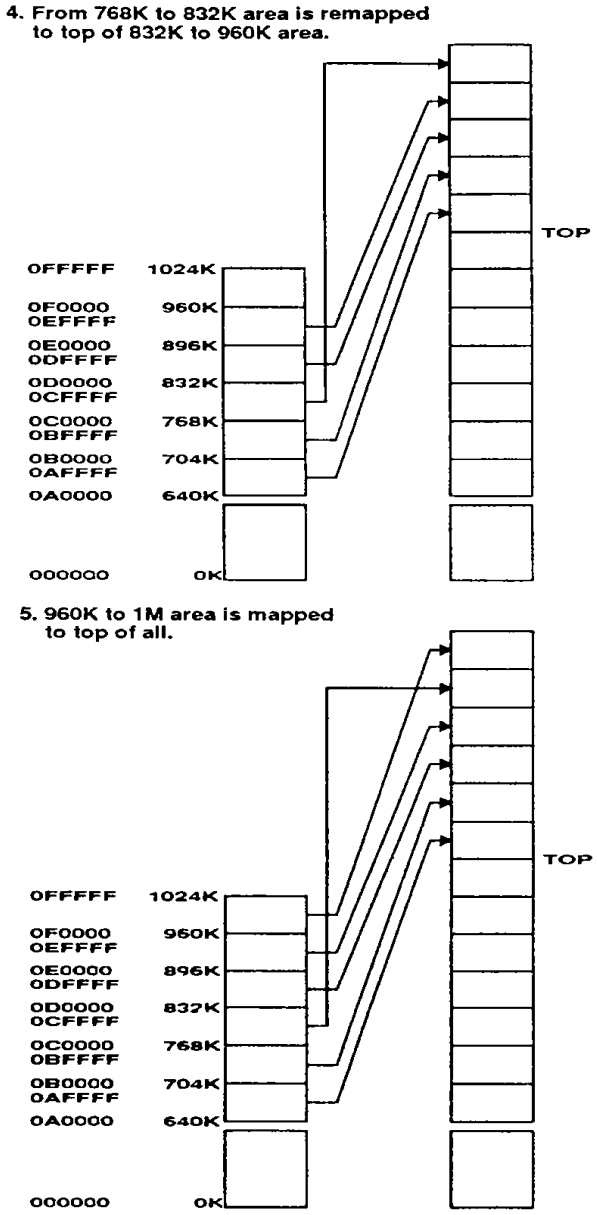


Figure 1-2. KS82C388 Remapping Scheme (Continued)

1.9.6 OS/2 Optimization

The KS82C388 provides two specific features that are further enhancements to the original IBM AT design:

- Fast Gate A20 (bit 1 of port 92h)
- Fast Reset CPU (bit 0 of port 92h)

The OS/2 operating system developed by IBM and Microsoft has two operating mode. The OS/2 mode operates on CPU protected address region while DOS mode operates on CPU real address region. In the OS/2 mode, the operating system can make many function calls in DOS mode. The CPU needs to switch from Protected Mode to Real mode before the DOS call could be executed. A CPU reset (RSTCPU) is one way to make the mode change without executing a cold reset (Power Down/On). The address A20 must be switched low before the CPU changes to Real mode. This is necessary to assure downward compatibility with the 8086.

Both functions in the original PC/AT design were handled through the keyboard controller (8042). The interface between the CPU and the keyboard controller is very slow. To switch from Protected to Real mode, the CPU needs to set A20 low and reset the CPU. For each operation, the CPU checks the keyboard controller ready status and issues commands to the keyboard controller. The KS82C388 provides both functions through much faster I/O operations.

In the KS82C388 implementation, Fast Gate A20 is a read/write bit controlling internal address bit A20. This bit is set to 1 during system reset allowing CPUA20 from the 80386SX to pass onto address A20. Writing a 0 into this bit will force the address A20 to be low.

The Fast Reset CPU read/write bit (Bit 0 of port 92h) is set to 0 during system reset (cold reset). To generate Fast Reset CPU during normal operation, the CPU only needs to execute two I/O write cycles for this bit to make 0 to 1 transition. The RSTCPU pin is pulled high after a 2μs delay or until a HALT state is detected(if the bit 2 of the register 1Bh), whichever is earlier.

1.9.7 Memory Subsystem Design Specification

The following table describes the SRAM, DRAM speed required for a certain performance level as related to the CPU clock frequency.

Table 1-4. CPU/SRAM/DRAM Speed vs. Wait States (MODE1 only)

CPU Clock Freq.	SRAM Tag / Cache Addr. Access	DRAM (Cache based) tRAC	Cache Read Hit
16 MHz	45 ns / 55 ns	120 ns	0 w.s.
20 MHz	35 ns / 45 ns	100 ns	0 w.s.
25 MHz	25 ns / 35 ns	80 ns	0 w.s.
33 MHz	20 ns / 25 ns	70 ns	0 w.s.
40 MHz	15 ns / 20 ns	60 ns	0 w.s.

Table 1-5. CPU/DRAM Speed vs. Wait States (MODE2 only)

CPU Clock Freq.	DRAM tRAC	DRAM Read Page Hit
16 MHz	120 ns	0 w.s.
20 MHz	100 ns	0 w.s.
25 MHz	80 ns	0 w.s.
33 MHz	70 ns	0 w.s.

1.10 Action Decode and Control

The activities within the KS82C388 are initiated by internally generated action codes that originate in the Action Mode Generation Logic (see Figure 0-2a). The action codes determine what the current bus cycle is and prompt the Action Decode and Control logic (see Figure 0-2b) to control the direction of data flow by decoding these codes together with REF*, SA0, and SBHE*.

1.11 Data Transfer Modules

As shown in the block diagram (Figure 0-2b), there are 4 data transfer modules. Each of these is controlled by the internal control signals generated by the Action Decode and Control module. Figure 1-3 demonstrates the memory and bus organization in a cached systems.

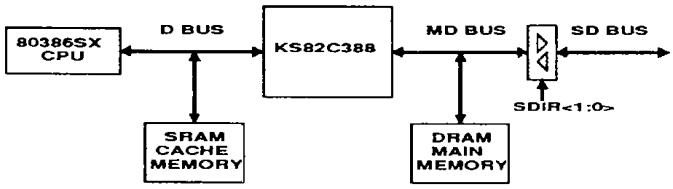


Figure 1-3. Memory and Data Bus Organization

The description and function of each of the data transfer modules, as they operate within a cached system, are given below.

1.11.1 CPU/DRAM Data Transfer Module

The CPU/DRAM Data Transfer Module controls the data flow between the CPU and the main memory. During memory write, CPU data is latched by WDLE and driven onto the MD bus. During memory read, the memory data is latched by DLE and driven onto the D bus. The data flow involved is shown in Figure 1-4.

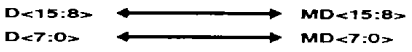


Figure 1-4. CPU/DRAM Data Transfer

1.11.2 CPU/AT/IO/ROM Data Transfer Module

The CPU/AT-BUS/IO/ROM Data Transfer Module controls data flow between the CPU and the AT Bus, peripherals and system BIOS ROM. The data flows for 16-bit transfers are shown in Figure I-5a.

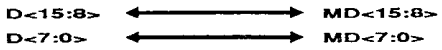


Figure 1-5a. CPU/AT/IO/ROM 16-bit Data Transfer

The data flows for 8-bit transfers are shown in Figure 1-5b.

Figure 1-5b. CPU/AT/IO/ROM 8-bit Data Transfer

1.11.3 DMA Cycles Transfer Module

The DMA Cycles Transfer Module, via the use of SDIR<1:0>, limits its control of 8-bit/8-bit and 16-bit/16-bit DMA transfers to data flow direction between the main memory MD bus and the AT SD bus. The data transfer between an 8-bit AT SD bus I/O and 16-bit AT SD bus memory is accomplished through a byte-swap mechanism as shown in Figure 1-6.

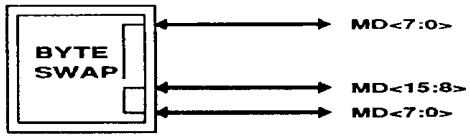


Figure 1-6. 16-bit AT Memory / 8-bit AT I/O DMA Memory Cycles Transfer

1.11.4 MASTER Cycles Transfer Module

In a cached system, the MASTER Cycles Transfer Module limits its control to data flow direction, vias the use of SDIR<1:0>, between the AT SD bus and the main memory MD bus.

1.12 Parity Handler

In order to maintain data integrity, the KS82C388 generates a parity bit for each byte of data written to local memory and also provides parity check to detect any mismatch whenever data is read from local memory.

During the local memory write cycle, source data (CPU, DMA or Master) is passed to the MD bus as well as to the parity generation logic. The parity generator generates one parity bit for each byte of write data and passes this bit to the memory parity outputs MP<1:0>. The memory write data (MD<15:0>) together with the parity bits (MP<1:0>) are written into the DRAM when the proper row address and/or column address strobes are issued by KS82C388.

During the local memory read cycle, memory data MD<15:0> and memory parity bits MP<1:0> are latched into the KS82C388. The MD data is redirected to the proper destinations (CPU, DMA or Master) as well as to the parity check logic. The parity check logic will regenerate new parity bits from the memory read data, one bit per byte, and compare them with the read memory parity bits.

The byte parity error bits are OR'ed together and latched to generate an internal parity error signal. The KS82C388 then generates an NMI (if it is enabled) to the CPU. Upon completion of error diagnosis, the parity error bit must be reset.

1.13 Timer Clock

The KS82C388 uses the OSCX1 (14.31818 MHz) oscillator input to derive the OSC119 internal clock signal by dividing OSCX1 by 12. This clock signal is used by the on-chip 82C206 Timer/Counter to perform the following functions under software control: timer, rate generator, pulse or square wave generators, and strobe signal. It is also used in the KS82C388 for refresh counters.

1.14 Local Bus Support

The KS82C388 provides hardware support to permit a peripheral controller to reside on the local or CPU bus. This results in faster data transfer rates between the CPU and the controller, whose data rates on the PC/AT bus would otherwise be restricted by that bus's bandwidth. A peripheral controller on the local bus can operate at the same frequency as the CPU.

1.14.1 Local Bus Hardware Support

The LOCAL* and the RDYIN* pins permit peripheral controllers to share the local bus with the KS82C388. These might include VGA graphics controllers. Data on the Local or CPU bus can be transferred as the CPU clock rate instead of the more restrictive 8 MHz rate associated with the PC/AT bus.

When a local peripheral wants access to the Local bus, it must assert the LOCAL* input to the KS82C388. The KS82C388 samples the LOCAL* input at the end of the T2 state. If it is detected LOW, the KS82C388 releases control of and ceases futher access to the Local or CPU bus. The current cycle execution is suspended.

At the end of the cycle, the local peripheral controller must generate a RDYIN* signal to terminate the cycle. This ready signal (RDYIN*) is sampled by the KS82C388 to detect when to resume cycle execution. If Bit 6 of configuration register 3Ah is set to zero, RDYIN* is internally directly connected or passed through to become READY* as the READY to the CPU. If Bit 6 is set to one, the RDYIN* is first synchronized with the CPU clock, then output to READY*. (If no RDYIN* is detected within 3.4μs to 6.8μs from the LOCAL* input, the KS82C388 generates READY* to terminate the cycle.)

1.15 Pins used for internal configuration

At system reset, DACK[7:5] pins are used to configure the KS82C388 operation modes. They shoud be strapped according to the following descriptions.

1.15.1 8 Bit / 16 Bit ROM selection

8 or 16 bit ROM selection can be accomplished by strapping the DACK7 pin.
0 : 8 Bit ROM, 1 : 16 Bit ROM
At system reset, the state of the DACK7 is inverted and latched into the bit 2 of the register 40h.

1.15.2 Mode selection

The KS82C388 can be configured into two different modes of operation by strapping the DACK6 pin according to the following table:

MODE	DACK6	DESCRIPTION
1	0	Cache mode. DRAM banks reside on MD bus and the cache controller is enabled.
2	1	Non-cache mode. DRAM banks reside on D bus and the cache controller is disabled.

At system reset, the state of the DACK6 pin is latched into the bit 1 of the register 40h.
The following is the description of the pins that are multiplexed for the two different operating modes:

NAME	TYPE	DESCRIPTION	
TAGA[7:0] \ SA[8:1]	I/O I/O	Mode 1: Mode 2:	TAG Address bits 7 - 0. System Address bus bits 8 - 1.
TAGWE* \ SA9	O I/O	Mode 1: Mode 2:	TAG Write Enable. System Address bus bit 9.
SRAMA1 \ SA10	O I/O	Mode 1: Mode 2:	SRAM Address bit 1. System Address bus bit 10.
CBS[1:0] \ SA[12:11]	O I/O	Mode 1: Mode 2:	Cache Byte Select bits 1, 0. System Address bus bits 12,11.
CWE* \ SA13	O I/O	Mode 1: Mode 2:	Cache Write Enable. System Address bus bit 13.
CRD* \ SA14	O I/O	Mode 1: Mode 2:	Cache Read enable. System Address bus bit 14.
SADIR \ SA15	O I/O	Mode 1: Mode 2:	SA bus Direction control. System Address bus bit 15.

Note : DACK5 pin is used for the internal mode setting. It shoud always be strapped to low..

1.16 AT peripheral controller (On-chip 82C206)

The KS82C388 provides on-chip AT peripheral controller, which is functionally equivalent to 82C206. The AT peripheral controller logic consists of two 8237 DMA controllers, two 8259 Interrupt controllers, one 8254 Timer/Counter, one Real Time Clock and 74LS612 memory mapper.

1.16.1 Clock and Wait State Control

The Clock and Wait State Control logic controls the DMA command width, the CPU Read/Write cycle length and selection of the DMA clock rate. Theses functions are programmable by writing to the Configuration Register described below. Reading and writing to this register is accomplished by first writing a 01H to I/O location 22H and then read or write to I/O location 23H.

Clock and Wait State Control Register **Default=1100,0000** **Index: 01H**

Bit 7	6	5	4	3	2	1	0
RW1	RW0	16W1	16W0	8W1	8W0	EMR	CLK

Bits	Value	
7:6		Control wait states when the CPU accesses the internal 82C206 registers. Wait states are in increments of one ATSCLK cycle and not affected by the DMA clock divider.
	00:	Read/Write Cycle Wait States = 1.
	01:	Read/Write Cycle Wait States = 2.
	10:	Read/Write Cycle Wait States = 3.
	11:	Read/Write Cycle Wait States = 4; Default.
5:4		16-Bit DMA Wait States Control.
	00:	1 wait state; Default.
	01:	2 wait states.
	10:	3 wait states.
	11:	4 wait states.
3:2		8-Bit DMA Wait States Control.
	00:	1 wait state; Default.
	01:	2 wait states.
	10:	3 wait states.
	11:	4 wait states.
1		Extended MEMR* function control.
	0:	MEMR* is delayed 1 clock cycle later than IOR*; Default.
	1:	MEMR* is asserted at the same time as IOR*.
0		DMA Clock Selection
	0:	DMA Clock = ATSCLK/2; Default.
	1:	DMA Clock = ATSCLK.

1.16.2 DMA Controller

The DMA control logic has two 8237A compatible DMA controllers and 74LS612 memory mappers. Each controller has four DMA channels and will generate the memory addresses and control signals necessary to transfer information between an I/O channel and memory.

The two DMA controllers are internally cascaded to provide four DMA channels for transfers to 8-bit peripherals (DMA1), and three channels for transfers to 16-bit peripherals (DMA2). DMA2 channel 0 provides the cascade interconnection of the two DMA controllers.

1.16.2.1 DMA Registers

The two DMA controllers can be programmed any time HLDA is inactive. Table 1-7 lists the register address assignment. An internal flip-flop is used to supplement the addressing of the Count and Address registers. This bit is used to select between the high and low bytes of these registers. The flip-flop will toggle each time a read or write occurs to any of the Word Count or Address registers in the DMA. This internal flip-flop will be cleared by hardware reset, or a Master Clear command and may be set or cleared by the CPU issuing the appropriate command.

The internal 82C206 will enable programming whenever HLDA has been inactive for one DMA clock cycle. Erratic operation can occur if a request for service occurs on an unmasked channel which is being programmed.

1.16.2.2 Address Generation

At the beginning of a DMA operation (during state S1), the intermediate addresses are output on the internal data lines XD0-XD7. These 8-bit addresses are latched by the internal address bit latches and used to drive the system address bus. Since DMA1 is used to transfer 8-bit data and DMA2 is used to transfer 16-bit data, an one bit skew occurs in the intermediate address fields. DMA1 will therefore output addresses A8-A15 on the data bus whereas DMA2 will output A9-A16.

During 8-bit DMA cycles, the lower address bits are output on A0-A7. The intermediate 8-bits of address are internally latched and output on A8-A15. A16-A23 are generated from a DMA Page Register.

During 16-bit DMA cycles, the lower address bits are output on A1-A8. The intermediate addresses are internally latched and output on A8-A15. The DMA Page Register now generates A17-A23.

ADDRESS		OPERATION		Flip-Flop	Register Function
DMA1	DMA2	IOR*	IOW*		
000h	0C0h	0	1	0	Read Channel 0 Current Address Low Byte
		0	1	1	Read Channel 0 Current Address High Byte
		1	0	0	Write Channel 0 Base and Current Address Low Byte
		1	0	1	Write Channel 0 Base and Current Address High Byte
001h	0C2h	0	1	0	Read Channel 0 Current Word Count Low Byte
		0	1	1	Read Channel 0 Current Word Count High Byte
		1	0	0	Write Channel 0 Base and Current Word Count Low Byte
		1	0	1	Write Channel 0 Base and Current Word Count High Byte
002h	0C4h	0	1	0	Read Channel 1 Current Address Low Byte
		0	1	1	Read Channel 1 Current Address High Byte
		1	0	0	Write Channel 1 Base and Current Address Low Byte
		1	0	1	Write Channel 1 Base and Current Address High Byte
003h	0C6h	0	1	0	Read Channel 1 Current Word Count Low Byte
		0	1	1	Read Channel 1 Current Word Count High Byte
		1	0	0	Write Channel 1 Base and Current Word Count Low Byte
		1	0	1	Write Channel 1 Base and Current Word Count High Byte
004h	0C8h	0	1	0	Read Channel 2 Current Address Low Byte
		0	1	1	Read Channel 2 Current Address High Byte
		1	0	0	Write Channel 2 Base and Current Address Low Byte
		1	0	1	Write Channel 2 Base and Current Address High Byte
005h	0CAh	0	1	0	Read Channel 2 Current Word Count Low Byte
		0	1	1	Read Channel 2 Current Word Count High Byte
		1	0	0	Write Channel 2 Base and Current Word Count Low Byte
		1	0	1	Write Channel 2 Base and Current Word Count High Byte
006h	0CCh	0	1	0	Read Channel 3 Current Address Low Byte
		0	1	1	Read Channel 3 Current Address High Byte
		1	0	0	Write Channel 3 Base and Current Address Low Byte
		1	0	1	Write Channel 3 Base and Current Address High Byte
007h	0CEh	0	1	0	Read Channel 3 Current Word Count Low Byte
		0	1	1	Read Channel 3 Current Word Count High Byte
		1	0	0	Write Channel 3 Base and Current Word Count Low Byte
		1	0	1	Write Channel 3 Base and Current Word Count High Byte
008h	0D0h	0	1	X	Read Status Register
		1	0	X	Write Command Register
009h	0D2h	0	1	X	Read DMA Request Register
		1	0	X	Write DMA Request Register
00Ah	0D4h	0	1	X	Read Command Register
		1	0	X	Write Single Bit DMA Request Mask Register
00Bh	0D6h	0	1	X	Read Mode Register
		1	0	X	Write Mode Register
00Ch	0D8h	0	1	X	Set Byte Pointer Flip-Flop
		1	0	X	Clear Byte Pointer Flip-Flop
00Dh	0DAh	0	1	X	Read Temporary Register
		1	0	X	Master Clear
00Eh	0DCh	0	1	X	Clear Mode Register Counter
		1	0	X	Clear All DMA Request Mask Register Bits
00Fh	0DEh	0	1	X	Read All DMA Request Mask Register Bits
		1	0	X	Write All DMA Request Mask Register Bits

Table 1-6. DMA Registers

The DMA Page Register is a set of 16 8-bit registers which are used to generate the high order addresses during DMA cycles. Each DMA channel has a register associated with it. Assignment of each of these registers is shown in the table below.

Address	Register Function
080h	Unused
081h	8-Bit DMA Channel 2 (DACK2)
082h	8-Bit DMA Channel 3 (DACK3)
083h	8-Bit DMA Channel 1 (DACK1)
084h	Unused
085h	Unused
086h	Unused
087h	8-Bit DMA Channel 0 (DACK0)
088h	Unused
089h	16-Bit DMA Channel 2 (DACK6)
08Ah	16-Bit DMA Channel 3 (DACK7)
08Bh	16-Bit DMA Channel 1 (DACK5)
08Ch	Unused
08Dh	Unused
08Eh	Unused
08Fh	Refresh Cycle

Table 1-7. DMA Address Extension Register Map

1.16.3 Interrupt Controller

The programmable interrupt controllers accept requests from peripherals, resolve priority on pending interrupts and interrupts in service, issue an interrupt request to the CPU, and provide a vector which is used as an index by the CPU to determine which interrupt service routine to execute.

Two interrupt controllers, INTC1 and INTC2, are included in the internal 82C206. Each of the interrupt controllers is equivalent to an 8259A. The two controllers are cascaded internally and must be programmed to operate in Cascade Mode for porper operation of all 16 interrupt channels. INTC1 is located at addresses 020H-021H and INTC2 is located at address 0AH-0A1H. The interrupt request output signal from INTC2 is is internally connected to the interrupt request input channel2 of INTC1. Table 1-8 lists the 16 interrupt channels and their interrupt request source.

Controller No.	Channel Name	INT Request Source
INTC1	IR0	Counter/Timer Output 0
INTC1	IR1	IRQ1 Input Pin
INTC1	IR2	INTC2 Cascade INT
INTC1	IR3	IRQ3 Input Pin
INTC1	IR4	IRQ4 Input Pin
INTC1	IR5	IRQ5 Input Pin
INTC1	IR6	IRQ6 Input Pin
INTC1	IR7	IRQ7 Input Pin
INTC2	IR0	Real Time Clock IRQ
INTC2	IR1	IRQ9 Input Pin
INTC2	IR2	IRQ10 Input Pin
INTC2	IR3	IRQ11 Input Pin
INTC2	IR4	IRQ12 Input Pin
INTC2	IR5	IRQ13 (NPX Error IRQ)
INTC2	IR6	IRQ14 Input Pin
INTC2	IR7	IRQ15 Input Pin

Table 1-8. Interrupt Request Source

1.16.4 Counter/Timer

The Counter/Timer (CTC) contains 3 16-bit counters (Counter 0-3) which can be programmed to count in binary or binary coded decimal (BCD). Each counter operates independently of the other two and can be programmed for operation as a timer or a counter. All three counters are driven from a common clock signal which is the 14.318Mhz oscillator input divided by 12.

Counter 0's output is connedted to the IRQ0 input of Interrupt Controller 1. Counter 1's output is used by the KS82C388 as a refresh request source. Counter 2's output is ANDed together with bit 1 of the Port B Register to drive the speaker.

The GATE inputs of Counter 0 and Counter 1 are not externally accessable. The GATE input of Counter 2 is connected to bit 0 of the Port B Register.

After power-up each counter must be programmed before it can be used. Counters are programmed by writing a Control Word and then an initial count. The Control Register of a counter is written by writing to the Control Word address.

Address	Function
040h	Counter 0 Read/Write
041h	Counter 1 Read/Write
042h	Counter 2 Read/Write
043h	Contro Word Register Write Only

Table 1-9. Counter/Timer Address Map

1.16.5 Real Time Clock

The KS82C388 contains a complete time-of-day clock with alarm, one hundred year calendar, a programmable periodic interrupt and 114 bytes of SRAM.

1.16.5.1 Register Access

Reading and writing to the 128 locations in the Real Time Clock is accomplished by first writing an index to I/O location 70H and then read or write to I/O location 71H.

Index	Function
00h	Seconds
01h	Seconds Alarm
02h	Minutes
03h	Minutes Alarm
04h	Hours
05h	Hours Alarm
06h	Day of Week
07h	Date of Month
08h	Month
09h	Year
0Ah	Register A
0Bh	Register B
0Ch	Register C
0Dh	Register D
0Eh - 7Fh	User RAM

Table 1-10. RTC Address Map

1.16.5.2 Time Calendar and Alarm Bytes

The processor program obtains time and calendar information by reading the appropriate locations in the Real Time Clock. The program may initialize the time, calendar, and alarm by writing to these RAM locations. The contents of the 10 time, calendar, and alarm bytes may be either binary or binary-coded decimal (BCD).

Before initializing the internal registers, the SET bit in Register B should be set to a "1" to prevent time/calendar updates from occurring. The program then initializes the 10 locations in BCD format. The SET bit should then be cleared to allow updates. Once initialized and enabled, the Real Time Clock will perform Clock/Calendar updates at a 1 Hz rate.

Address	Function	BCD Range
0	Seconds	00-59
1	Seconds Alarm	00-59
2	Minutes	00-59
3	Minutes Alarm	00-59
4	Hours (12 hour mode)	01-12 (AM) 81-92 (PM)
	Hours (24 hour mode)	00-23
5	Hours Alarm (12 hour mode)	01-12 (AM) 81-92 (PM)
	Hours Alarm (24 hour mode)	00-23
6	Day of Week	01-07
7	Day of Month	01-31
8	Month	01-12
9	Year	00-99

Table 1-11. Data Format

Table 1-11 shows the BCD format for the 10 time, calendar and alarm locations. The 24/12 bit in Register B establishes whether the hour locations represent 1-12 or 0-23 format. The 24/12 bit cannot be changed without reinitializing the hour locations. When the 12-hour format is selected the high-order bit of the hours byte represents PM when it is a "1".

The time, calendar and alarm bytes are not always accessable by the processor program. Once-per-second the 10 bytes are switched to the update logic to be advanced by one second and to check for an alarm condition. If any of the 10 bytes are read at this time, the data outputs are undefined. The update lockout time is 1948μs for the 32.768kHz time base.

The three alarm bytes may be used in two ways. First, when the program inserts an alarm time in the appropriate hours, minutes and seconds alarm locations, the alarm interrupt is initiated at the specified time each day if the alarm enable bit is high. The second usage is to insert a "don't care" state in one or more of three alarm bytes. The "don't care" code is any byte from 0C0H to 0FFH. An alarm interrupt each hour is created with a "don't care" code in the hours alarm location. Similary, an alarm is generated every minute with "don't care" codes in the hours and minutes alarm bytes. The "don't care" codes in all three alarm bytes create an interrupt every second.

1.16.5.3 Control and Status Registers

The internal 82C206 contains four registers used to control the operation and monitor the status of the Real Time Clock. These bytes are located at Index Address 0AH-0DH and are accessable by the CPU at all times.

REGISTER A **Index: 0AH**

Bit 7	6	5	4	3	2	1	0
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0

Bits Value

7 Update In Progress flag. Read Only. The UIP bit is not affected by Reset. A "1" indicates that an update cycle is taking place or is imminent. UIP will go active (High) 244µs prior to the start of an update cycle and will remain active for an additional 2ms while the update is taking place. Writing a "1" to the SET bit in Register B will clear the UIP status bit.

6:4 Control the Divider/Prescaler on the Real Time Clock.
- 010: Operation Mode, 32.768KHz.
- 11X: Reset Divider.

3:0 Control the Periodic Interrupt rate.
- 0000: None
- 0001: 3.90526 ms
- 0010: 7.8125 ms
- 0011: 122.070 µs
- 0100: 244.141 µs
- 0101: 488.281 µs
- 0110: 976.562 µs
- 0111: 1.953125 ms
- 1000: 3.90625 ms
- 1001: 7.8125 ms
- 1010: 15.625 ms
- 1011: 31.25 ms
- 1100: 62.5 ms
- 1101: 125 ms
- 1110: 250 ms
- 1111: 500 ms

REGISTER B **Index: 0BH**

Bit 7	6	5	4	3	2	1	0
SET	PIE	AIE	UIE	0	DM2	24/12	DSE

Bits Value

7 0: Update cycle enable.
1: Update cycle inhibited and any cycle in progress is aborted.

6 0: Periodic interrupt disable.
1: Periodic interrupt enable. Cleared by reset.

5 0: Alarm interrupt disable.
1: Alarm interrupt enable. Cleared by reset.

4 0: Update-End interrupt disable.
1: Update-End interrupt enable.

2 Data Mode. CMOS time and date format.
0: BCD
1: Binary

1 Format of the Hours and Hours Alarm bytes.
0: 12 hour mode.
1: 24 hour mode.

0 0: Daylight savings disable.
1: Daylight savings enable.

REGISTER C (Read Only) **Index: 0CH**

Bit 7	6	5	4	3	2	1	0
IRQF	PF	AF	UF	0	0	0	0

Bits Value

7 interrupt request flag.
IRQF = PF & PIE + AF & AIE + UF & UIE
Cleard by reading register or by activating the PSRSTB* input pin.

6 Periodic interrupt flag.
5 Alarm interrupt flag.
4 Update-End interrupt flag.

REGISTER D (Read Only) **Index: 0DH**

Bit 7	6	5	4	3	2	1	0
VRT	0	0	0	0	0	0	0

Bits Value

7 Valid RAM and Tims Bit. This bit is cleared whenever the PSRSTB* input pin is LOW.
0: Invalid RAM and Time.
1: Valid RAM and Time.

2. CONFIGURATION REGISTERS

2.1 Summary of Configuration Registers

Signature Register (Read only) — Default=0000,0001 — Index: 10H

Identification	Version	Revision

Lock Register (Write only) — Default=XXXX,XXX0 — Index: 10H

-	-	-	-	-	-	-	LOCK

AT Bus Clock/Recover Time/Wait State — Default=1000,0110 — Index: 11H

ATCKM1	ATCKM0	CMDRC1	CMDRC0	WT16B1	WT16B0	WT8B1	WT8B0

System Control Register — Default=0000,X000 — Index: 12H

SLOWCLK	GA20INTC	RST2INTC	EROMWR	CO387	LOCALPE	GA20OUT	REF206

Miscellaneous Control Register — Default=0000,1000 — Index: 1BH

-	RASTCAS	-	-	RMPWT	ENHALT	-	-

DRAM Bank 0 Configuration — Default=0111,XX1X — Index: 30H

B0DTY1	B0DTY0	B0RDWT	B0WRWT	-	-	B0RPRC	-

DRAM Bank 1 Configuration — Default=00XX,XXXX — Index: 32H

B1DTY1	B1DTY0	B1RDWT	B1WRWT	-	-	B1RPRC	-

DRAM Bank 2 Configuration — Default=00XX,XXXX — Index: 34H

B2DTY1	B2DTY0	B2RDWT	B2WRWT	-	-	B2RPRC	-

DRAM Bank 3 Configuration — Default=00XX,XXXX — Index: 36H

B3DTY1	B3DTY0	B3RDWT	B3WRWT	-	-	B3RPRC	-

Miscellaneous Register — Default=0000,0100 — Index: 3AH

-	SYNC387	-	-	ENLODEC	-	-	DISPAR

Local VGA decode control register (Write only) — Default=0XXX,XXXX — Index: 3BH

-	LVGA6	LVGA5	LVGA4	LVGA3	LVGA2	LVGA1	LVGA0

Memory Control Register — Default=0100,0XXX — Index: 40H

SHADMR	ENMROM	DSLOCM	DSBUSM	-	ROM8	RAMOND	-

System ROM/Shadow RAM Control Register C — Default=0000,0000 — Index: 41H

SHADC3	ENROMC3	SHADC2	ENROMC2	SHADC1	ENROMC1	SHADC0	ENROMC0

System ROM/Shadow RAM Control Register D — Default=0000,0000 — Index: 42H

SHADD3	ENROMD3	SHADD2	ENROMD2	SHADD1	ENROMD1	SHADD0	ENROMD0

System ROM/Shadow RAM Control Register E — Default=0101,0101 — Index: 43H

SHADE3	ENROME3	SHADE2	ENROME2	SHADE1	ENROME1	SHADE0	ENROME0

System ROM/Shadow RAM Control Register F — Default=0101,0101 — Index: 44H

SHADF3	ENROMF3	SHADF2	ENROMF2	SHADF1	ENROMF1	SHADF0	ENROMF0

Remapping Control Register — Default=0XXX,XXXX — Index: 45H

ENREMAP	-	-	-	REMAPC	REMAPD	REMAPE	REMAPF

Remap Base Address — Default=XXXX,XXXX — Index: 46H

-	-	-	RMPA23	RMPA22	RMPA21	RMPA20	RMPA19

Refresh Control Register — Default=0011,0000 — Index: 47H

-	STGREF	REFPU1	REFPU0	-	-	SLWREF1	SLWREF0

Non-Cache/Non-Local DRAM Block 0 Register 1 — Default=00XX,XXXX — Index: 50H

DSDRAM0	NCDRAM0	-	-	NC0SZ3	NC0SZ2	NC0SZ1	NC0SZ0

Non-Cache/Non-Local DRAM Block 0 Register 2 — Default=XXXX,XXXX — Index: 51H

-	-	NC0A23	NC0A22	NC0A21	NC0A20	NC0A19	NC0A18

Non-Cache/Non-Local DRAM Block 0 Register 3 — Default=XXXX,XXXX — Index: 52H

NC0A17	NC0A16	NC0A15	NC0A14	NC0A13	NC0A12	NC0A11	NC0A10

Cache Control Register — Default=0000,1X10 — Index: 60H

ENCAH	FCRDMS	SRMSZ1	SRMSZ0	NCA2F	-	SRMWT	EDASRAM

2.2 Configuration Registers - Full Description

Signature Register (Read only) **Default=0000,0001** **Index: 10H**

Bit 7	6	5	4	3	2	1	0
Identification				Version		Revision	

Bits Value

7:4 KS82C388 Identification number.

3:2 Chip Version Number.

1:0 Chip Revision Number.

Lock Register (Write only) **Default=XXXX,XXX0** **Index: 10H**

Bit 7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	LOCK

Bits Value

7:1 Reserved.

0 Disable write Configuration Registers. Once set, all configuration registers except register 10H and register 41H become READ ONLY. This bit is cleard by RSTCPU.
0: Configuration Registers are READ/WRITE; Default.
1: Configuration Registers are READ ONLY.

AT Bus Clock/Recover Time/Wait State **Default=1000,0110** **Index: 11H**

Bit 7	6	5	4	3	2	1	0
ATCKM1	ATCKM0	CMDRC1	CMDRC0	WT16B1	WT16B0	WT8B1	WT8B0

Bits Value

7:6
00: ATSCLK = CLK2IN/10.
01: ATSCLK = CLK2IN/4.
10: ATSCLK = CLK2IN/6; Default.
11: ATSCLK = CLK2IN/8.

5:4
00: I/O command cycle RECOVER TIME = 1 ATSCLK; Default.
01: I/O command cycle RECOVER TIME = 2 ATSCLK, (250ns when ATSCLK=8MHz).
10: I/O command cycle RECOVER TIME = 3 ATSCLK, (375ns when ATSCLK=8MHz).
11: I/O command cycle RECOVER TIME = 4 ATSCLK, (500ns when ATSCLK=8MHz).

3:2
00: 16-Bit AT BUS wait state = 0 wait state.
01: 16-Bit AT BUS wait state = 1 wait state; Default.
10: 16-Bit AT BUS wait state = 2 wait states.
11: 16-Bit AT BUS wait state = 3 wait states.

1:0
00: 8-Bit AT BUS wait state = 2 wait states.
01: 8-Bit AT BUS wait state = 3 wait states.
10: 8-Bit AT BUS wait state = 4 wait states; Default.
11: 8-Bit AT BUS wait state = 5 wait states.

System Control Register **Default=0000,X000** **Index: 12H**

Bit 7	6	5	4	3	2	1	0
SLOWCLK	GA20INTC	RST2INTC	EROMWR	CO387	LOCALPE	GA20OUT	REF206

Bits	Value	
7		Select CPUCLK source between CLK2IN and ATCLK2. This bit works only when the TURBO* pin is set to low (active).
	0:	CPUCLK = CLK2IN; Default. (Turbo mode)
	1:	CPUCLK = 2 x ATSCLK. (Deturbo mode)
6		Intercept write to the keyboard controller output port bit 1 (GATEA20).
5		Intercept keyboard controller reset command.
4		Enable ROM write. (ROMCS* will be generated for a local ROM write cycle)
3	0:	387SX does not exist.
	1:	387SX exists. Note - Status of this bit relies on power on 387SX detection mechanism. (Read Only)
2	0:	LOCAL* pin input disable; Default.
	1:	LOCAL* pin input enable. Local VGA address decoding function (register 3BH) is disabled. This bit is valid when the bit 3 of register 3AH (ENLODEC) is set.
1		When this bit is set, the A20GATE pin becomes output for the Cx486SLC A20M* pin.
0		Refresh request source select.
	0:	Internal counter (13.4μs); Default.
	1:	On-chip 206 OUT1 signal (15.6μs).

Miscellaneous Control Register **Default=0000,1000** **Index: 1BH**

Bit 7	6	5	4	3	2	1	0
-	RASTCAS	-	-	RMPWT	ENHALT	-	-

Bits	Value	
7		Reserved.
6		RAS to CAS programmable delay.
	0:	RAS to CAS delay = 4 CPUCLK; Default
	1:	RAS to CAS delay = 2 CPUCLK.
5:4		Reserved.
3		Remap Wait.
	0:	No extra wait state added to DRAM cycle when Remap is enabled.
	1:	One extra wait state added to DRAM when Remap is enabled and CPU address falls within the range; Default.
2		Enable HALT Detection.
	0:	Function disabled, Default.
	1:	Execute fast reset only after the bit 0 of 92H is set and CPU has issued HALT bus cycle.
1:0		Reserved.

DRAM Bank 0 Configuration **Default=0111,XX1X** **Index: 30H**

Bit 7	6	5	4	3	2	1	0
B0DTY1	B0DTY0	B0RDWT	B0WRWT	-	-	B0RPRC	-

Bits	Value	
7:6	00:	DRAM not exist.
	01:	256Kx1, 256Kx4 DRAM; Default.
	10:	1Mx1, 1Mx4 DRAM.
	11:	4Mx1, 4Mx4 DRAM.
5	0:	0 wait state READ when DRAM PAGE HIT.
	1:	1 wait state READ when DRAM PAGE HIT; Default.
4	0:	0 wait state WRITE when DRAM PAGE HIT.
	1:	1 wait state WRITE when DRAM PAGE HIT; Default.
3:2		Reserved.
2	0:	RAS precharge time = 4 CPUCLK period.
	1:	RAS precharge time = 6 CPUCLK period; Default.
0		Reserved.

DRAM Bank 1 Configuration **Default=00XX,XXXX** **Index: 32H**

Bit 7	6	5	4	3	2	1	0
B1DTY1	B1DTY0	B1RDWT	B1WRWT	-	-	B1RPRC	-

Bits	Value	
7:6	00:	DRAM not exist; Default.
	01:	256Kx1, 256Kx4 DRAM.
	10:	1Mx1, 1Mx4 DRAM.
	11:	4Mx1, 4Mx4 DRAM.
5	0:	0 wait state READ when DRAM PAGE HIT.
	1:	1 wait state READ when DRAM PAGE HIT.
4	0:	0 wait state WRITE when DRAM PAGE HIT.
	1:	1 wait state WRITE when DRAM PAGE HIT.
3:2		Reserved.
2	0:	RAS precharge time = 4 CPUCLK period.
	1:	RAS precharge time = 6 CPUCLK period.
0		Reserved.

DRAM Bank 2 Configuration **Default=00XX,XXXX** **Index: 34H**

Bit 7	6	5	4	3	2	1	0
B2DTY1	B2DTY0	B2RDWT	B2WRWT	-	-	B2RPRC	-

Bits	Value	
7:6	00:	DRAM not exist; Default.
	01:	256Kx1, 256Kx4 DRAM.
	10:	1Mx1, 1Mx4 DRAM.
	11:	4Mx1, 4Mx4 DRAM.
5	0:	0 wait state READ when DRAM PAGE HIT.
	1:	1 wait state READ when DRAM PAGE HIT.
4	0:	0 wait state WRITE when DRAM PAGE HIT.
	1:	1 wait state WRITE when DRAM PAGE HIT.
3:2		Reserved.
2	0:	RAS precharge time = 4 CPUCLK period.
	1:	RAS precharge time = 6 CPUCLK period.
0		Reserved.

DRAM Bank 3 Configuration **Default=00XX,XXXX** **Index: 36H**

Bit 7	6	5	4	3	2	1	0
B3DTY1	B3DTY0	B3RDWT	B3WRWT	-	-	B3RPRC	-

Bits	Value	
7:6	00:	DRAM not exist; Default.
	01:	256Kx1, 256Kx4 DRAM.
	10:	1Mx1, 1Mx4 DRAM.
	11:	4Mx1, 4Mx4 DRAM.
5	0:	0 wait state READ when DRAM PAGE HIT.
	1:	1 wait state READ when DRAM PAGE HIT.
4	0:	0 wait state WRITE when DRAM PAGE HIT.
	1:	1 wait state WRITE when DRAM PAGE HIT.
3:2		Reserved.
2	0:	RAS precharge time = 4 CPUCLK period.
	1:	RAS precharge time = 6 CPUCLK period.
0		Reserved.

Miscellaneous Register **Default=0000,0100** **Index: 3AH**

Bit 7	6	5	4	3	2	1	0
-	SYNC387	-	-	ENLODEC	-	-	DISPAR

Bits	Value
7	Reserved.
6	Synchronize RDYIN* with CPU clock.
5:4	Reserved.
3	Local bus device enable. When this bit is set to low, the function of the LOCAL* pin and the register 3BH are disabled.
2:1	Reserved.
0	Disable parity check.

Local VGA decode control register (Write only) **Default=0XXX,XXXX** **Index: 3BH**

Bit 7	6	5	4	3	2	1	0
-	LVGA6	LVGA5	LVGA4	LVGA3	LVGA2	LVGA1	LVGA0

Bits	Value
7	Reserved.
6	Enable local VGA memory block at 0A0000H - 0AFFFFH.
5	Enable local VGA memory block at 0B0000H - 0B7FFFH.
4	Enable local VGA memory block at 0B8000H - 0BFFFFH.
3	Enable local VGA I/O block at 3C0H - 3CFH.
2	Enable local VGA I/O block at 3D0H - 3DFH.
1	Enable local VGA I/O block at 3B0H - 3BBH.
0	Enable local VGA I/O block at 4600H - 46FFH.

To enable Local VGA address decoding function,
Set ENLODEC (bit 3 of 3AH) = 1, LOCALPE (bit 2 of 12H) = 0.

Memory Control Register **Default=0100,0XXX** **Index: 40H**

Bit 7	6	5	4	3	2	1	0
SHADMR	ENMROM	DSLOCM	DSBUSM	-	ROM8	RAMOND	-

Bits Value

7 Enable Shadow RAM at FE0000 - FFFFFFH.
6 Enable Local ROM at FE0000 - FFFFFFH.

SHADMR/ENMROM/EROMWR(register 12H bit 4) Bits

Value
000: Read AT BUS, Write RAM (Local or AT BUS).
001: Read AT BUS, Write AT BUS.
010: Read Local ROM, Write RAM (Local or AT BUS); Default.
011: Read Local ROM, Write Local ROM.
10X: Read RAM (Local or AT BUS), Write Protect.
11X: Read RAM (Local or AT BUS), Write RAM (Local or AT BUS).

5 Disable local memory access.
Once set, all memory access, except the access to the LOCAL ROM (ROMCS* will be generated), will be directed to AT BUS. This is used to check the existence of AT BUS memory.
0: Enable local memory access; Default.
1: Disable local memory access.

4 Disable all AT BUS memory access.
Once set, all memory access will be treated as local memory access; for those existing DRAM locations, RAS*, CAS*, READY* will be generated; for those non-existing DRAM locations, only READY* will be generated. This is used to check existence and type of local DRAM.
0: Enable AT BUS memory access; Default.
1: Disable AT BUS memory access.

3 Reserved.

2 Local ROM size. (Read only)
0: Local ROM is 16 bit.
1: Local ROM is 8 bit.

1 RAM on D Bus. (Read only)
0: Local DRAM is on MD bus. (MODE1)
1: Local DRAM is on CPU D bus. (MODE2)

0 Reserved.

System ROM/Shadow RAM Control Register C **Default=0000,0000** **Index: 41H**

Bit 7	6	5	4	3	2	1	0
SHADC3	ENROMC3	SHADC2	ENROMC2	SHADC1	ENROMC1	SHADC0	ENROMC0

Bits Value

7 Enable Shadow RAM at 0CC000H - 0CFFFFH.
6 Enable Local ROM at 0CC000H - 0CFFFFH.

5 Enable Shadow RAM at 0C8000H - 0CBFFFH.
4 Enable Local ROM at 0C8000H - 0CBFFFH.

3 Enable Shadow RAM at 0C4000H - 0C7FFFH.
2 Enable Local ROM at 0C4000H - 0C7FFFH.

1 Enable Shadow RAM at 0C0000H - 0C3FFFH.
0 Enable Local ROM at 0C0000H - 0C3FFFH.

NOTE: The following SHAD/ENROM/EROMWR bit definitions apply to registers 41H, 42H, 43H & 44H.

SHAD/ENROM/EROMWR(register 12H bit 4) Bits

Value		
000:	Read AT BUS,	Write RAM (Local or AT BUS).
001:	Read AT BUS,	Write AT BUS.
010:	Read Local ROM,	Write RAM (Local or AT BUS).
011:	Read Local ROM,	Write Local ROM.
10X:	Read RAM (Local or AT BUS),	Write Protect.
11X:	Read RAM (Local or AT BUS),	Write RAM (Local or AT BUS).

NOTE: Procedure to turn on SHADOW RAM:

1. Set EROMWR (register 12H bit 4) = 0.
   Set corresponding SHAD = 0, ENROM = 1 for LOCAL ROM.
   Set corresponding SHAD = 0, ENROM = 0 for AT BUS ROM.

2. Repeat "Read then write to the same address" for the entire ROM block.

3. After finishing ROM copy, set corresponding SHAD=1, ENROM=0.

System ROM/Shadow RAM Control Register D **Default=0000,0000** **Index: 42H**

Bit 7	6	5	4	3	2	1	0
SHADD3	ENROMD3	SHADD2	ENROMD2	SHADD1	ENROMD1	SHADD0	ENROMD0

Bits	Value
7	Enable Shadow RAM at 0DC000H - 0DFFFFH.
6	Enable Local ROM at 0DC000H - 0DFFFFH.
5	Enable Shadow RAM at 0D8000H - 0DBFFFH.
4	Enable Local ROM at 0D8000H - 0DBFFFH.
3	Enable Shadow RAM at 0D4000H - 0D7FFFH.
2	Enable Local ROM at 0D4000H - 0D7FFFH.
1	Enable Shadow RAM at 0D0000H - 0D3FFFH.
0	Enable Local ROM at 0D0000H - 0D3FFFH.

System ROM/Shadow RAM Control Register E **Default=0101,0101** **Index: 43H**

Bit 7	6	5	4	3	2	1	0
SHADE3	ENROME3	SHADE2	ENROME2	SHADE1	ENROME1	SHADE0	ENROME0

Bits	Value
7	Enable Shadow RAM at 0EC000H - 0EFFFFH.
6	Enable Local ROM at 0EC000H - 0EFFFFH.
5	Enable Shadow RAM at 0E8000H - 0EBFFFH.
4	Enable Local ROM at 0E8000H - 0EBFFFH.
3	Enable Shadow RAM at 0E4000H - 0E7FFFH.
2	Enable Local ROM at 0E4000H - 0E7FFFH.
1	Enable Shadow RAM at 0E0000H - 0E3FFFH.
0	Enable Local ROM at 0E0000H - 0E3FFFH.

System ROM/Shadow RAM Control Register F **Default=0101,0101** **Index: 44H**

Bit 7	6	5	4	3	2	1	0
SHADF3	ENROMF3	SHADF2	ENROMF2	SHADF1	ENROMF1	SHADF0	ENROMF0

Bits	Value
7	Enable Shadow RAM at 0FC000H - 0FFFFFH.
6	Enable Local ROM at 0FC000H - 0FFFFFH.
5	Enable Shadow RAM at 0F8000H - 0FBFFFH.
4	Enable Local ROM at 0F8000H - 0FBFFFH.
3	Enable Shadow RAM at 0F4000H - 0F7FFFH.
2	Enable Local ROM at 0F4000H - 0F7FFFH.
1	Enable Shadow RAM at 0F0000H - 0F3FFFH.
0	Enable Local ROM at 0F0000H - 0F3FFFH.

Remapping Control Register **Default=0XXX,XXXX** **Index: 45H**

Bit 7	6	5	4	3	2	1	0
ENREMAP	-	-	-	REMAPC	REMAPD	REMAPE	REMAPF

Bits Value

7 0: Disable Remap function; Default.
1: Enable Remap function.

6:4 Reserved.

3:0 Remap memory block to above the Remap Base Address specified by register 46H.
0000: Remap memory at 0A0000 - 0BFFFFH.
0100: Remap memory at 0A0000 - 0BFFFFH and 0D0000 - 0DFFFFH.
0110: Remap memory at 0A0000 - 0BFFFFH and 0D0000 - 0EFFFFH.
1110: Remap memory at 0A0000 - 0EFFFFH.
1111: Remap memory at 0A0000 - 0FFFFFH.
else: Reserved.

Remap Base Address **Default=XXXX,XXXX** **Index: 46H**

Bit 7	6	5	4	3	2	1	0
-	-	-	RMPA23	RMPA22	RMPA21	RMPA20	RMPA19

Bits Value

7:5 Reserved.

4:0 Remapping Base Address A23 - A19.

Refresh Control Register **Default=0011,0000** **Index: 47H**

Bit 7	6	5	4	3	2	1	0
-	STGREF	REFPU1	REFPU0	-	-	SLWREF1	SLWREF0

Bits Value

7 Reserved.

6 0: Staggered refresh disabled; Default.
1: Staggered refresh enabled.

5:4 RAS pulse width during refresh.
00: 4 CPUCLK.
01: 5 CPUCLK.
10: 6 CPUCLK.
11: 6 CPUCLK; Default.

3:2 Reserved.

1:0 00: Refresh rate = 256 ROWs/4 ms; Default.
01: Refresh rate = 128 ROWs/4ms.
10: Refresh rate = 64 ROWs/4ms.
11: Refresh rate = 32 ROWs/4ms.

Non-Cache/Non-Local DRAM Block 0 Register 1 **Default=00XX,XXXX** **Index: 50H**

Bit 7	6	5	4	3	2	1	0
DSDRAM0	NCDRAM0	-	-	NC0SZ3	NC0SZ2	NC0SZ1	NC0SZ0

Bits Value

7:6 Non-Cache/Disable DRAM Block 0 control.
- 00: Function disabled; Default.
- 01: Non-Cache the DRAM block specified by 50 - 52H.
- 10: Reserved. (Local device decode)
- 11: Non-Local DRAM block specified by 50 - 52H. All memory access will be directed to AT BUS, and will not be cached.

5:4 Reserved.

3:0 Non-Cache/Non-Local DRAM Block 0 Size.
- 0000: IK.
- 0001: 2K.
- 0010: 4K.
- 0011: 8K.
- 0100: 16K.
- 0101: 32K.
- 0110: 64K.
- 0111: 128K.
- 1000: 256K.
- 1001: 512K.
- 1010: IM.

Non-Cache/Non-Local DRAM Block 0 Register 2 **Default=XXXX,XXXX** **Index: 51H**

Bit 7	6	5	4	3	2	1	0
-	-	NC0A23	NC0A22	NC0A21	NC0A20	NC0A19	NC0A18

Bits Value

7:5 Reserved.

4:0 Non-cache/Non-Local DRAM Block 0 base address bits A23 - A18. (The starting address of any non-cacheable region must be on a boundary of that region's size.)

Non-Cache/Non-Local DRAM Block 0 Register 3 **Default=XXXX,XXXX** **Index: 52H**

Bit 7	6	5	4	3	2	1	0
NC0A17	NC0A16	NC0A15	NC0A14	NC0A13	NC0A12	NC0A11	NC0A10

Bits Value

7:0 Non-cache/Non-Local DRAM Block 0 base address bits A17 - A10.

Cache Control Register **Default=0000,1X10** **Index: 60H**

Bit 7	6	5	4	3	2	1	0
ENCAH	FCRDMS	SRMSZ1	SRMSZ0	NCA2F	-	SRMWT	EDASRAM

Bits Value

7 Enable CACHE.
0: CACHE disabled; Default.
1: CACHE enabled.

6 Force Cache Read Miss
0: CPU cache read hit or miss is decided by TAG compare; Default.
1: Any CPU read is forced to a cache read miss.

5:4 CACHE Size selection.
00: 16K; Default.
01: 32K.
10: 64K.
11: Reserved.

3 Enable the Non-cacheability of memory space between 0A0000H to 0FFFFFH.
0: Disable 0A0000H to 0FFFFFH noncacheable.
1: Enable 0A0000H to 0FFFFFH noncacheable; Default.

2 Reserved.

1 SRAM Wait state selection.
0: 0 wait state.
1: 1 wait state; Default.

0 Enable Direct Access to SRAM. Once enabled, SRAM can be directly accessed starting at location 040000H up to cache size.
0: Disable SRAM direct access; Default.
1: Enable SRAM direct access.

16K : 040000 - 041FFFH 042000 - 043FFFH
32K : 040000 - 043FFFH 044000 - 047FFFH
64K : 040000 - 047FFFH 048000 - 04FFFFH

2.3 How To Program the Configuration Registers

All registers except the 4 non-indexed I/O ports can be accessed by the CPU through the system I/O ports, 22H and 23H. To access a register, first write the index number of the register being programmed on the system I/O port 22H then write/read data through I/O port 23H to/from this register. The KS82C388 chip set also provides a special feature: lock or unlock the chip set registers. The registers need to be unlocked before any write operation and normally are locked after all write operations are completed. This, however, is not necessary for read operations. In order to avoid an I/O timing problem, a delay is needed between the consecutive I/O access unless bits 5 & 4 of register 11H are properly programmed. Here is an example of an assembler program which programs the register 11H with value 04H:

```
        MOV AL,10H          ; LOCK/UNLOCK REGISTER INDEX
        OUT 22H,AL          ; LATCH REGISTER INDEX
        JMP $+2             ; GIVE I/O DEVICE RECOVERY TIME
        JMP $+2             ; GIVE MORE I/O DEVICE RECOVERY TIME
        MOV AL,0            ; REGISTER BIT 0 = 0
        OUT 23H,AL          ; UNLOCK REGISTERS
        JMP $+2             ; GIVE I/O DEVICE RECOVERY TIME
        JMP $+2             ; GIVE MORE I/O DEVICE RECOVERY TIME
P0:     MOV AL,11H          ; REGISTER INDEX 11H
        OUT 22H,AL          ; LATCH REGISTER INDEX
        JMP $+2             ; GIVE I/O DEVICE RECOVERY TIME
        JMP $+2             ; GIVE MORE I/O DEVICE RECOVERY TIME
        MOV AL,04H          ; VALUE TO BE WRITTEN TO REGISTER
        OUT 23H,AL          ; WRITE TO REGISTERS
        JMP $+2             ; GIVE I/O DEVICE RECOVERY TIME
P1:     JMP $+2             ; GIVE MORE I/O DEVICE RECOVERY TIME
        MOV AL,10H          ; LOCK/UNLOCK REGISTER INDEX
        OUT 22H,AL          ; LATCH REGISTER INDEX
        JMP $+2             ; GIVE I/O DEVICE RECOVERY TIME
        JMP $+2             ; GIVE MORE I/O DEVICE RECOVERY TIME
        MOV AL,1            ; REGISTER BIT 0 = 1
        OUT 23H,AL          ; LOCK REGISTERS
```

An assembler program example which reads the value of register 11H back is provided as follows.

```
P0:   MOV AL,11H      ; REGISTER INDEX 11H
      OUT 22H,AL      ; LATCH REGISTER INDEX
      JMP $+2         ; GIVE I/O DEVICE RECOVERY TIME
      JMP $+2         ; GIVE MORE I/O DEVICE RECOVERY TIME
      IN  AL,23H      ; READ DATA FROM PORT 23H
      JMP $+2         ; GIVE I/O DEVICE RECOVERY TIME
P1:   JMP $+2         ; GIVE MORE I/O DEVICE RECOVERY TIME
```

If more registers are to be read/written, the steps between P0 and P1 mentioned above should be repeated with an individual index number and value.

Note: Care must be taken to guarantee the integrity of the registers that contain reserved bits with default values. Those bits **should NOT be changed** when the values of the other bits within those registers are modified.

3. KS82C388 PIN DESCRIPTION

3.1 KS82C388 Pin Diagram

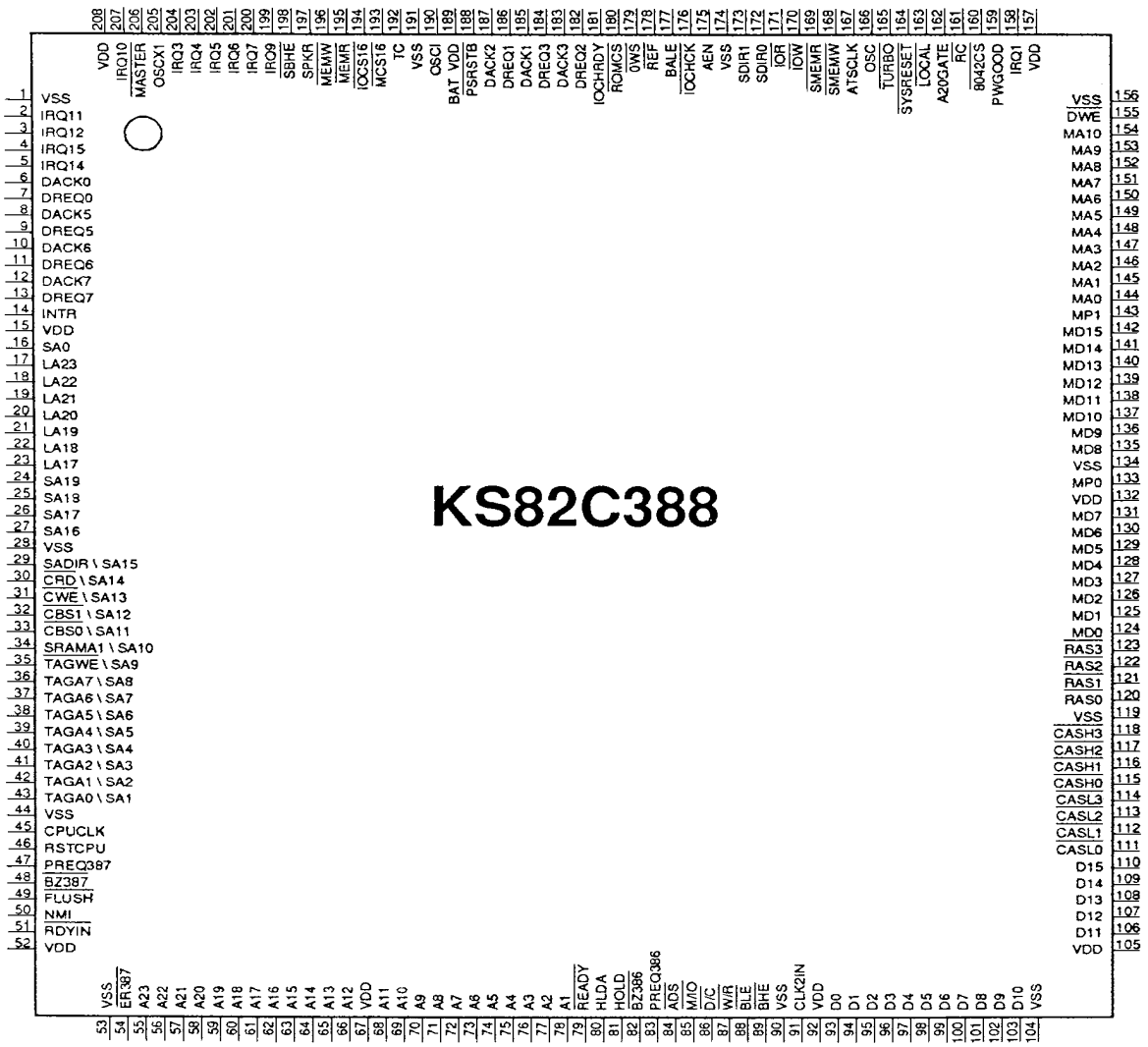


Figure 3-1. KS82C388 Pin Diagram (MODE1 \ MODE2)

3.2 KS82C388 Pin List

Pin No.	NAME	TYPE	DESCRIPTION
			CLOCK & OSCILLATOR SIGNALS
167	**ATSCLK**	O	AT bus System Clock is a clock output to the AT bus. Its frequency is programmable as CLK2IN/4, CLK2IN/6, CLK2IN/8 or CLK2IN/10.
45	**CPUCLK**	O	Output to the CLK2 of the CPU and the coprocessor. It is driven by CLK2IN with a 50% duty cycle.
91	**CLK2IN**	I	CLK2 input from an oscillator running at twice the rated frequency of the CPU.
205	**OSCX1**	I	14.318 MHz Clock input from a crystal oscillator.
166	**OSC**	O	14.318 MHz Clock output to the AT bus.
190	**OSCI**	I	32.768 KHz Clock input used by the internal Real Time Clock.
			RESET SIGNALS
159	**PWGOOD**	I	Input generated from the power supply PWRGOOD signal or pushbutton for cold reset. This signal causes a system level reset, setting all programmable registers to their default values. It has a Schmitt Trigger input buffer.
161	**RC***	I	A pulse signal input from the 8042 Keyboard Controller for a warm reset. It resets the CPU and the coprocessor.
46	**RSTCPU**	O	An output signal to reset the CPU and the coprocessor. It is activated by PWGOOD, RC*, shutdown or Fast Reset. It lasts for at least 80 CLK2 cycles so that the CPU can perform a Self Test. The phase relationship to CLK2 is maintained to reset the CPU properly.
164	**SYSRESET***	O	Activated by PWGOOD to reset on-board peripherals. It also drives the RESDRV to reset the AT I/O channel. The duration of the active period is the same as RSTCPU.
			CPU INTERFACE SIGNALS
55-61	**A[23:17]**	I/O	Local Address input signals from the CPU. Outputs during DMA/Master cycle, floated during Refresh cycle.
62-66 68-78	**A[16:1]**	I/O	Local Address input signals from the CPU. Outputs during Refresh, DMA/Master cycle.
84	**ADS***	I	Address Strobe is an active low input signal from the CPU indicating a valid bus cycle. A 10K pullup resistor on this pin is recommended.
88 89	**BLE*,** **BHE***	I/O	Byte Enable inputs, BLE* and BHE* are active low input signals from the CPU. These input pins indicate the 2 bytes of the 16-bit data bus involved with the current CPU cycle. BLE* controls the least significant byte and BHE* controls the most significant byte. For DMA/Master cycles, BHE* and BLE* are outputs.
82	**BZ386***	O	An active low output connected to the BUSY* input of the CPU.

Pin No.	NAME	TYPE	DESCRIPTION
110-106 103-93	**D[15:0]**	I/O	CPU data bus bits 15 to 0
86	**D/C***	I	Data/Code command status is an input signal from the CPU. It indicates a data cycle when high and a command(code) cycle when low. A 10K pullup resistor is recommended.
80	**HLDA**	I	Hold Acknowledge is an active high input from the CPU. When high, it indicates that the CPU has relinquished the system bus in response to a HOLD request.
81	**HOLD**	O	HOLD Request is an active high signal output to the CPU HOLD input. When active, this signal requests that CPU relinquish local bus control to another master (DMA, Master, or AT Refresh Controller).
14	**INTR**	O	An active high interrupt request output to the CPU.
85	**M/IO***	I	Memory or I/O command status is an input signal from the CPU. It indicates a memory cycle when high and an I/O cycle when low. A 10K pullup resistor on this pin is recommended.
50	**NMI**	O	An active high Non-Maskable Interrupt output connected to the NMI input of the CPU. in the KS82C388, an NMI can be generated when an I/O error, a DRAM parity error.
83	**PREQ386**	O	An active high output connected to the PEREQ input of the CPU.
79	**READY***	O	An active low READY signal to the CPU.
87	**W/R***	I	Write/Read command status is an input signal from the CPU. It indicates a write cycle when high and a read cycle when low. A 10K pullup resistor is recommended.
80387SX COPROCESSOR INTERFACE SIGNALS			
48	**BZ387***	I	80387SX BUSY* signal. It indicates that the 80387SX is currently executing an instruction
54	**ER387***	I	80387SX ERROR* signal.
47	**PREQ387**	I	80387SX PEREQ signal. When active, it indicates that the coprocessor has data to be transferred by the CPU.

Pin No.	NAME	TYPE	DESCRIPTION
			MISCELLANEOUS SIGNALS
162	**A20GATE \ A20M***	I/O	Gate A20 is an active high input signal from the keyboard controller. When high, the KS82C388 drives A20 (from the CPU) onto the internal logical address, A20. When low, it forces A20 to be low, regardless of the A20 pin state. When in output mode, A20GATE acts as an A20M* signal for the Cx486SLC.
49	**FLUSH***	O	An active low output to Cx486SLC FLUSH* signal. It is active during DMA/Master write cycle.
163	**LOCAL***	I	If this signal is detected low, the KS82C388 releases control of the CPU bus.
51	**RDYIN***	I	This signal is the active low READY input signal from the local bus VGA controller and math coprocessor.
180	**ROMCS***	O	An active low ROM Chip Select signal.
197	**SPKR**	O	This signal is used to drive the speaker. It is a gated output of speaker data and the TMROUT signal from the on-chip 82C206.
188	**PSRSTB***	I	This input pin should be connected to the battery backup circuit. When power is applied to the KS82C388, PSRSTB* initialises the condition of the on-chip 82C206 control registers.
165	**TURBO***	I	Turbo/deturbo input from an external switch.
160	**8042CS***	O	8042 Keyboard Controller chip select.
			CACHE MEMORY INTERFACE (MODE1) \ AT BUS ADDRESS (MODE2) SIGNALS
30	**CRD* \ SA14**	I/O	MODE1 : Cache Read is an active low output signal connected to the SRAM's Output Enable pin. During a read hit cycle, CRD* is enabled to drive the requested data onto the D bus. MODE2 : System Address bus bit 14.
31	**CWE* \ SA13**	I/O	MODE1 : Cache Write Enable is an active low signal to the cache SRAM Write Enable (WE*) pins. It enables the cache to receive data from the CPU data bus (during read miss or write hit cycles). MODE2 : System Address bus bit 13.
32,33	**CBS[1:0]* \ SA[12:11]**	I/O	MODE1 : Cache Byte Select outputs are active low signals connected to the SRAM's Chip Select pins. These output pins control bytes during cache write hit updates. CBS0* controls the least significant byte and CBS1* controls the most significant byte. MODE2 : System Address bus bits 12 and 11.
34	**SRAMA1 \ SA10**	I/O	MODE1 : Cache SRAM A1 Address is an output signal to the SRAM array. It is used to control A1 inversion in data cache access. During a read miss, SRAMA1 drives inverted A1 in the first half of the cycle and will switch to non-inverted A1 for the second half of the cycle. MODE2 : System Address bus bit 10.
35	**TAGWE* \ SA9**	I/O	MODE1 : Tag RAM Write Enable is active during a read miss cache cycle and enables the Tag RAMs to receive Tag address data. MODE2 : System Address bus bit 9.
36-43	**TAGA[7:0] \ SA[8:1]**	I/O	MODE1 : Tag Address data lines. MODE2 : System Address bus bit 8 ~ 1.

Pin No.	NAME	TYPE	DESCRIPTION
			MAIN MEMORY (DRAM) INTERFACE SIGNALS
118-115 114-111	**CASH[3:0]*** **CASL[3:0]***	O O	Column Address Strobe signals for High and Low byte of DRAM banks.
155	**DWE***	O	DRAM Write Enable is an active low output signal to the DRAM array. This signal is buffered before connected to the WE* inputs of DRAMs.
154-144	**MA[10:0]**	O	The DRAM memory address lines.
142-135 131-124	**MD[15:8]** **MD[7:0]**	I/O I/O	MODE1 : Memory Data bits 0 through 15 from DRAMs. MODE2 : These pins can be directly connected to the AT bus (SD).
143,133	**MP1, MP0**	I/O	Memory Parity bit for high and low bytes, respectively.
123-120	**RAS[3:0]***	O	Row address Strobe signals are active low output to the DRAM banks. There is one RAS* signal for each bank of local DRAM.
			PC/AT BUS INTERFACE SIGNALS
175	**AEN**	O	Address Enable is an active high output. It is driven high during DMA cycle. AEN is inactive during CPU/Master cycles.
177	**BALE**	O	Bus Address Latch Enable is an active high output used to validate addresses on the I/O channel. BALE is driven high during DMA or Master cycles.
12,10,8, 183,187, 185,6	**DACK[7:5]** **DACK[3:0]**	I/O O	DMA Acknowledge signals. DACK informs the peirpheral that a DMA request has been granted. The active polarity is programmable. When reset, they are initialised to active low. DACK[7:5] become inputs during system reset and used by the KS82C388 for mode setting. DACK[7:5] require 4.7K ohm pulldown/pullup resistor for proper mode setting during system reset. DACK7 selects between 8bit ROM (pulldown) and 16bit ROM (pullup). DACK6 selects between MODE1 (pulldown) and MODE2 (pullup). DACK5 selects between normal mode (pulldown) and reserved mode for the KS82C388 (pullup). DACK5 should always be pulled down.
13,11,9, 184,182, 186,7	**DREQ[7:5]** **DREQ[3:0]**	I	DMA Request signals are asynchronous inputs and the active polarity is programmable. When reset, they are initialised to active high. They are prioritised, with DREQ0 having the highest priority and DREQ7 the lowest. A DREQ line should remain active until the corresponding DACK becomes active. DREQ[3:0] support 8-bit transfers, DREQ[7:5] support 16 bit transfers.
4,5, 3,2, 207,199, 200-204, 158	**IRQ[15:14]** **IRQ[12:9]** **IRQ[7:3]** **IRQ1**	I	Asynchronous Interrupt Request signals.

Pin No.	NAME	TYPE	DESCRIPTION
176	**IOCHCK***	I	I/O Channel Check is an active low input signal from the AT I/O channel, indicating an error condition. When the NMI feature is enabled and the ENIOCHK (Enable I/O Channel Check) bit in port B is set, KS82C388 generates an NMI if IOCHCK* is active.
181	**IOCHRDY**	I/O	I/O Channel Ready is an active high input signal from AT I/O channel. A slow I/O device on the AT bus drives it low during an AT cycle, and the KS82C388 will insert extra wait states in AT I/O or Memory accesses. When high, the KS82C388 will terminate current AT cycles according to programmed wait states. It becomes output during I/O access cycles to the internal 82C206.
194	**IOCS16***	I	I/O 16 bit Chip Select is an active low input signal from the I/O channel. When active, it indicates that the current I/O cycle is a 16-bit access.
171	**IOR***	I/O	I/O Read Command is an active low signal used by the I/O channel. It is an output during CPU/DMA cycle and an input during Master cycles.
170	**IOW***	I/O	I/O Write Command is an active low signal used by the I/O channel. It is an output during CPU/DMA cycle and an input during Master cycles.
17-23	**LA[23:17]**	I/O	These address lines provide the additional address lines required for the 16MB I/O channel memory address space. Input during Master cycle; Output during CPU cycle; Floated during Refresh cycle.
206	**MASTER***	I	Master is an active low input signal from the I/O channel. When active, it indicates that another CPU or a DMA controller is residing on the I/O channel to control the system bus.
193	**MCS16***	I	Memory 16 bit Chip Select is an active low input signal from the I/O channel. When active, it indicates that the current memory cycle is a 16-bit access.
195	**MEMR***	I/O	Memory Read Command is an active low bidirectional signal used by I/O channel memory. When active, valid data will be driven onto the SD bus. It is an output during CPU/DMA/Refresh cycles. It is an input during Master cycles (except Master Refresh).
196	**MEMW***	I/O	Memory Write Command is an active low bidirectional signal used by I/O channel memory. When active, it directs peripherals to accept data from the XD or SD bus. It is an output during CPU/DMA cycles. It is an input during Master cycles.
178	**REF***	I/O	Refresh is an active low bidirectional signal. During the Master refresh cycle, the I/O channel master drives this signal low. During a normal AT refresh cycle, REF* is an output to the I/O channel.
24-26 27	**SA[19:17]** **SA16**	O I/O	System Address bus bits. During Master cycle, SA16 becomes an input.

Pin No.	NAME	TYPE	DESCRIPTION
16 198	**SA0** **SBHE***	I/O	These signals are outputs to the SA-bus during CPU access. During DMA/Master cycle, SBHE* is driven low for 16 bit and is inverted SA0 for 8 bit operations respectively. SA0 is an output and stays low for 16 bit DMA cycle.
29	**SADIR ** **SA15**	O	MODE1 : SA Bus Direction Control. When high SADIR drives the SA bus towards the I/O channel address bus. MODE2 : System Address bus bit 15.
173,172	**SDIR[1:0]**	O	SD Bus Direction Control. These two signals are used to control the data bus direction between I/O channel data bus (SD) and local bus (MD). When high, SDIR[1:0] drive the MD bus towards the I/O Channel bus. When low, SDIR[1:0] drive the I/O Channel bus towards the MD bus.
169	**SMEMR***	O	System Memory Read Command is an active low output used by I/O channel memory. It is active when the MEMR* signal line is active and the LA[23:20] signal line indicate the first 1 megabyte of address space.
168	**SMEMW***	O	System Memory Write Command is an active low output used by I/O channel memory. It is active when the MEMW* signal line is active and the LA[23:20] signal line indicate the first 1 megabyte of address space.
179	**0WS***	I	Zero Wait State is an active low input signal from AT I/O channel. When active, the KS82C388 will terminate current AT cycle without additional wait state.
192	**TC**	O	Terminal Count indicates that the DMA channel terminal count has been reached.
		POWER & GROUND	
15, 52, 67, 92, 105, 132, 157, 208	**VDD**	I	Supply Voltage at nominal 5.0 Vdc.
189	**BAT_VDD**	I	Internal 82C206 battery backup power.
1,28,44, 53,90, 104,119, 134,156, 174,191	**VSS**	I	Ground.

4. ELECTRICAL CHARACTERISTICS

4.1 Absolute Maximum Ratings

Table 4-1. Absolute Maximum Ratings

PARAMETER	SYMBOL	VALUE		UNIT
		MIN	MAX	
Supply Voltage	Vdd	-0.3	7.0	V
Input Voltage	Vi	-0.3	Vdd + 0.3	V
Storage Temperature	Tstg	-40	125	°C

Stresses above the Absolute Maximum Ratings may cause permanent damage to the device.

4.2 Recommended Operating Conditions

Table 4-2. Recommended Operating Conditions

PARAMETER	SYMBOL	VALUE		UNIT
		MIN	MAX	
Supply Voltage	Vdd	4.75	5.25	V
Input Voltage	Vi	-0.3	Vdd	V
Ambient Temperature	Ta	0	70	°C

4.3 DC Characteristics

(Vdd = 5V ± 5%, Vss = 0V, Ta = 0 to 70°C)

Table 4-3. DC Charateristics

PARAMETER	SYMBOL	CONDITION	VALUE		UNIT
			MIN	MAX	
Input Low Voltage	Vil	TTL level CMOS level Schmitt Trigger level	- - -	0.8 1.5 1.0	V V V
Input High Voltage	Vih	TTL level CMOS level Schmitt Trigger level	2.0 3.5 4.0	- - -	V V V
Input Low Current	Iil	Vin = Vss	-10	10	µA
Input High Current	Iih	Vin = Vdd	-10	10	µA
Output Low Voltage	Vol	4mA buffer, IOL = 4mA 12mA buffer, IOL = 12mA 18mA buffer, IOL = 18mA	- - -	0.4V 0.4V 0.4V	V V V
Output High Voltage	Voh	4mA buffer, IOH = -4mA 12mA buffer, IOH = -12mA 18mA buffer, IOH = -18mA	2.4 2.4 2.4	- - -	V V V
High Impedance Leakage Current	Ioz	Vout = Vss or Vdd	-10	10	µA
Battery Supply Current	Ibat	PWGOOD = 0V BAT_VDD = 3.6V	-	10	µA

Note 1) CMOS input : OSCI

Note 2) Schmitt Trigger inputs : PWGOOD, TURBO*

Note 3) 12mA buffers : ATSCLK, CPUCLK, RSTCPU, READY*, CRD*, CWE*, CBS[1:0]*, SRAMA1, TAGWE*, TAGA[7:0], DWE*, MA[10:0], MD[15:0], MP1, MP0, RAS[3:0]*, AEN, BALE, IOCHRDY, IOR*, IOW*, LA[23:17], MEMR*, MEMW*, REF*, SA[19:16], SA0, SBHE*, SMEMR*, SMEMW*, TC

Note 4) 18mA buffers : CASH[3:0]*, CASL[3:0]*

4.4 AC Characteristics

(Vdd = 5V ± 5%, Vss = 0V, Ta = 0 to 70°C)

PARAMETER	SYMBOL	MIN	MAX	UNIT
CLOCK TIMING				
CLK2IN period	T101	12.5	-	ns
CLK2IN high width	T102	5	-	ns
CLK2IN low width	T103	5	-	ns
CPUCLK delay from CLK2IN rising edge	T104	-	13	ns
CPUCLK delay from CLK2IN falling edge	T105	-	14	ns
RESET TIMING				
RSTCPU inactive from CPUCLK rising edge	T201	-	10	ns
SYSRESET* inactive from CPUCLK rising edge	T202	-	18	ns
AT BUS CYCLE TIMING				
BALE active from ATSCLK falling edge	T301	-	15	ns
BALE inactive from ATSCLK rising edge	T302	-	15	ns
COMMAND active from ATSCLK rising edge	T303	-	14	ns
COMMAND inactive from ATSCLK rising edge	T304	-	14	ns
SDIR<1:0> valid from CPUCLK rising edge	T305	-	24	ns
SA<19:0>, SBHE* valid from ATSCLK falling edge	T306	-	24	ns
LA<23:17> valid from ATSCLK rising edge	T307	-	15	ns
LA<23:17>, SA<19:0> hold from COMMAND inactive	T308	60	-	ns
ROMCS* active from CPUCLK rising edge	T309	-	24	ns
ROMCS* inactive from CPUCLK rising edge	T310	-	24	ns
MD read data setup to COMMAND inactive	T311	30	-	ns
MD read data hold from COMMAND inactive	T312	0	-	ns
MD write data setup to COMMAND active	T313	30	-	ns
MD write data hold from COMMAND inactive	T314	60	-	ns
DMA CYCLE TIMING				
HOLD valid from CPUCLK rising edge	T401	-	19	ns
HOLD invalid from CPUCLK rising edge	T402	-	19	ns
AEN valid from HLDA valid	T403	-	20	ns
RASn* active from CPUCLK rising edge	T404	-	20	ns
RASn* inactive from COMMAND inactive	T405	-	22	ns

PARAMETER	SYMBOL	MIN	MAX	UNIT
CASHn*, CASLn* active from CPUCLK rising edge	T406	-	20	ns
CASHn*, CASLn* inactive from COMMAND inactive	T407	-	20	ns
MA<10:0> valid from CPUCLK rising edge	T408	-	20	ns
MA<10:0> invalid from CPUCLK rising edge	T409	-	20	ns
COMMAND active from ATSCLK rising edge	T410	-	120	ns
DACKn delay from ATSCLK rising edge	T411	-	105	ns
TC delay from ATSCLK rising edge	T412	-	60	ns
MODE1 CACHE CYCLE TIMING				
TAGA<7:0> setup to CPUCLK rising edge	T501	9	-	ns
TAGA<7:0> hold from CPUCLK rising edge	T502	9	-	ns
SRAMA1 valid from A1 valid	T503	-	13	ns
SRAMA1 valid from CPUCLK rising edge	T504	-	20	ns
CRD* active from CPUCLK rising edge	T505	-	18	ns
CRD* inactive from CPUCLK rising edge	T506	-	18	ns
TAGWE* active from CPUCLK rising edge	T507	-	15	ns
TAGWE* inactive from CPUCLK rising edge	T508	-	15	ns
CWE* active from CPUCLK rising edge	T509	-	18	ns
CWE* inactive from CPUCLK rising edge	T510	-	18	ns
CBS<1:0>* valid from BLE*, BHE* valid	T511	-	15	ns
MODE1 DRAM CYCLE TIMING				
DWE* active from CPUCLK rising edge	T601	-	20	ns
DWE* inactive from CPUCLK rising edge	T602	-	22	ns
RASn* inactive from CPUCLK rising edge	T603	-	20	ns
RASn* active from CPUCLK rising edge	T604	-	20	ns
CASHn*, CASLn* active from CPUCLK rising edge	T605	-	15	ns
CASHn*, CASLn* inactive from CPUCLK rising edge	T606	-	16	ns
MA<10:0> invalid from CPUCLK rising edge	T607	-	22	ns
MA<10:0> valid from CPU address valid	T608	-	20	ns
MD to D delay	T609	-	13	ns

PARAMETER	SYMBOL	MIN	MAX	UNIT
REFRESH CYCLE TIMING				
REF* active from HLDA valid	T701	-	22	ns
REF* inactive from CPUCLK falling edge	T702	-	22	ns
MEMR* active from ATSCLK rising edge	T703	-	22	ns
MEMR* inactive from ATSCLK rising edge	T704	-	22	ns
RAS0*, RAS1* active from CPUCLK rising edge	T705	-	20	ns
RAS0*, RAS1* inactive from CPUCLK rising edge	T706	-	20	ns
RAS2*, RAS3* active from CPUCLK rising edge	T707	-	20	ns
RAS2*, RAS3* inactive from CPUCLK rising edge	T708	-	20	ns
A<16:1> valid from ATSCLK rising edge	T709	-	22	ns
A<16:1> invalid from ATSCLK rising edge	T710	-	22	ns
MODE2 DRAM CYCLE TIMING				
RASn* active from CPUCLK rising edge	T801	-	16	ns
RASn* inactive from CPUCLK rising edge	T802	-	16	ns
CASHn*, CASLn* active from CPUCLK rising edge	T803	-	13(5)[5)]	ns
CASHn*, CASLn* inactive from CPUCLK rising edge	T804	-	13	ns
DWE* active from CPUCLK rising edge	T805	-	18	ns
DWE* inactive from CPUCLK rising edge	T806	-	19	ns
MA<10:0>(Column address) valid from A<23:0> valid	T807	-	13	ns
LOCAL BUS CYCLE TIMING				
LOCAL* setup to CPUCLK rising edge	T901	10	-	ns
LOCAL* hold from CPUCLK rising edge	T902	5	-	ns

Note 1) C_L = 75pF.
Note 2) All outputs are measured at 0.5 * VDD
Note 3) Not all parameters are tested.
Note 4) COMMAND refers to the signals MEMR*, MEMW*, IOR*, IOW*
Note 5) The value inside the parentheses is valid only in 0 WS read cyce with the register 4BH bit 0 set.

4.5 Timing Diagrams

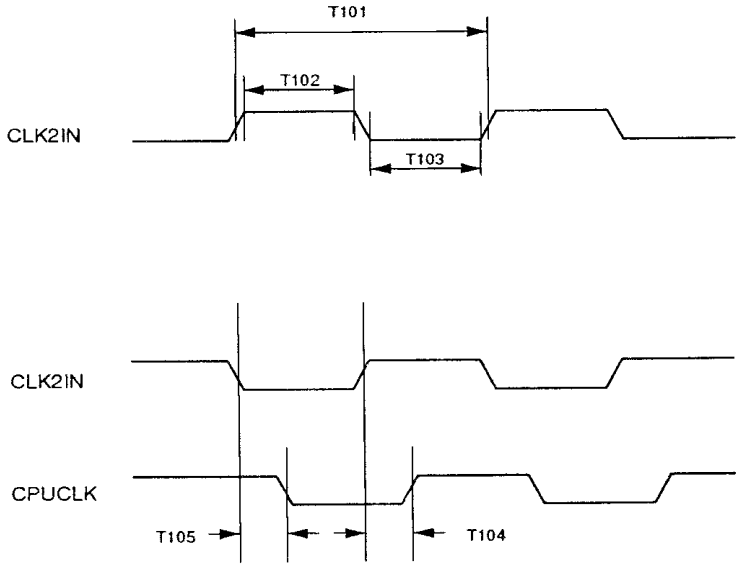


Figure 4-1. Clock Timing

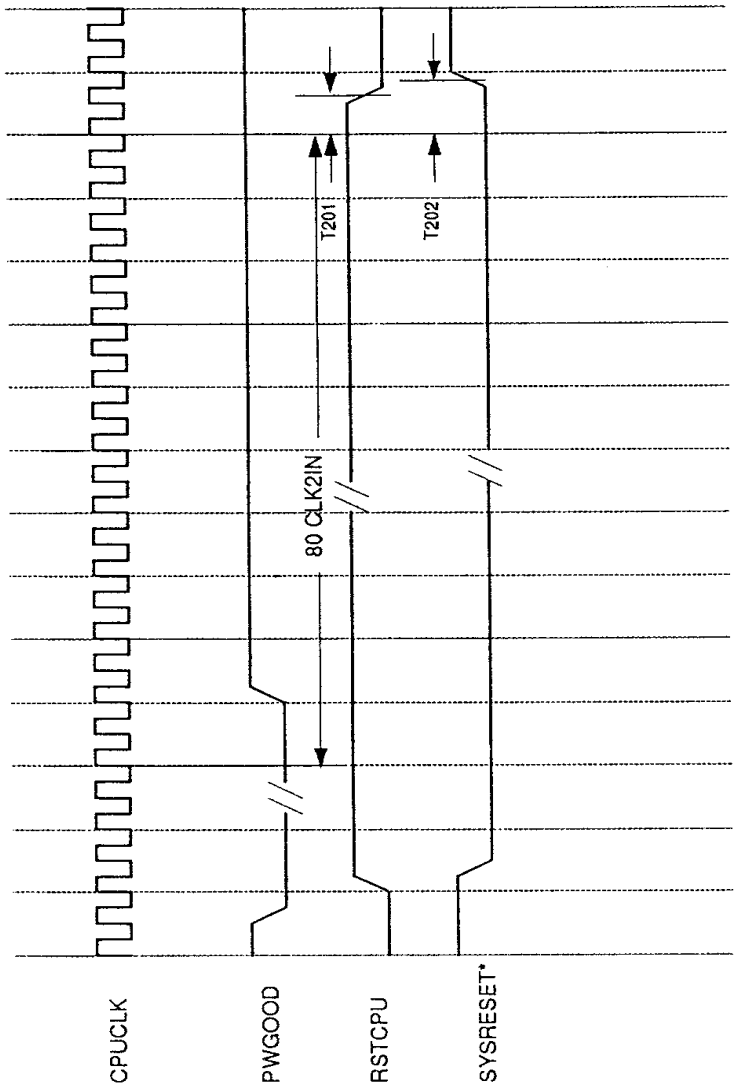


Figure 4-2. Reset Timing

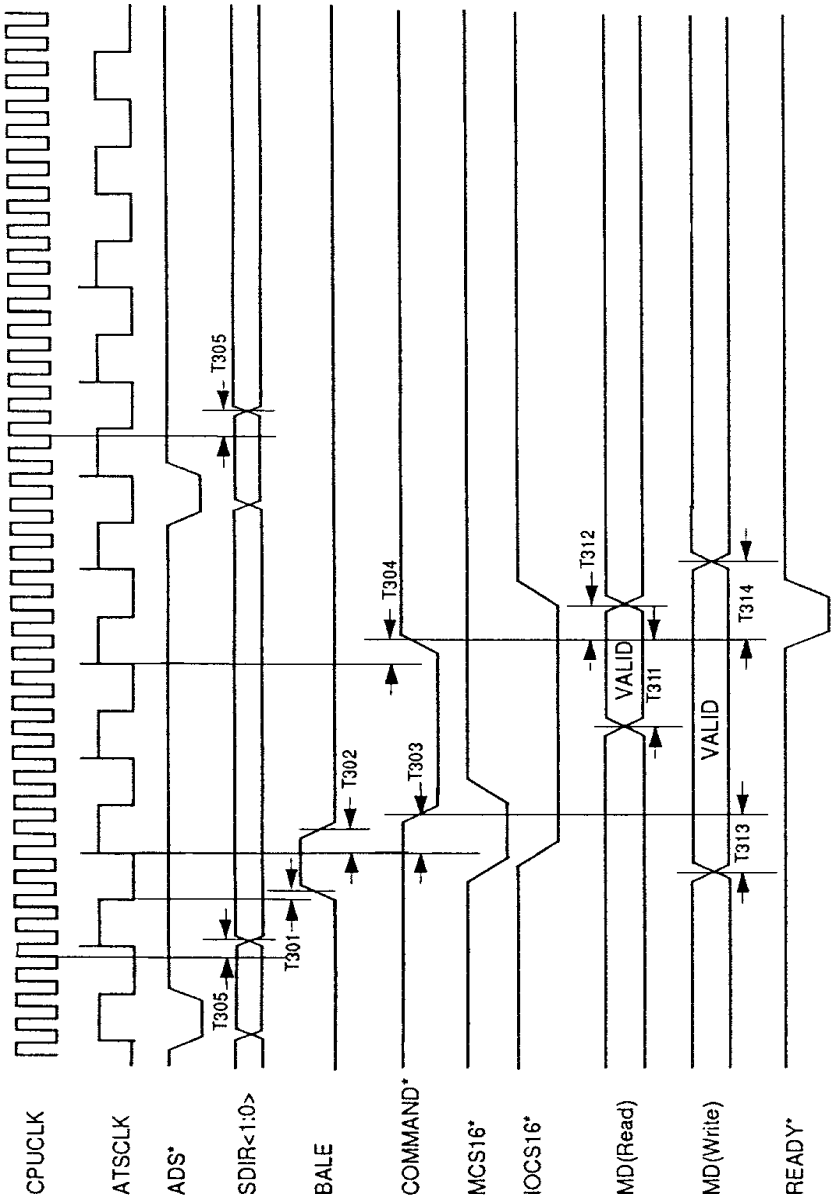


Figure 4-3. 16 Bit AT Bus Cycle (Default)

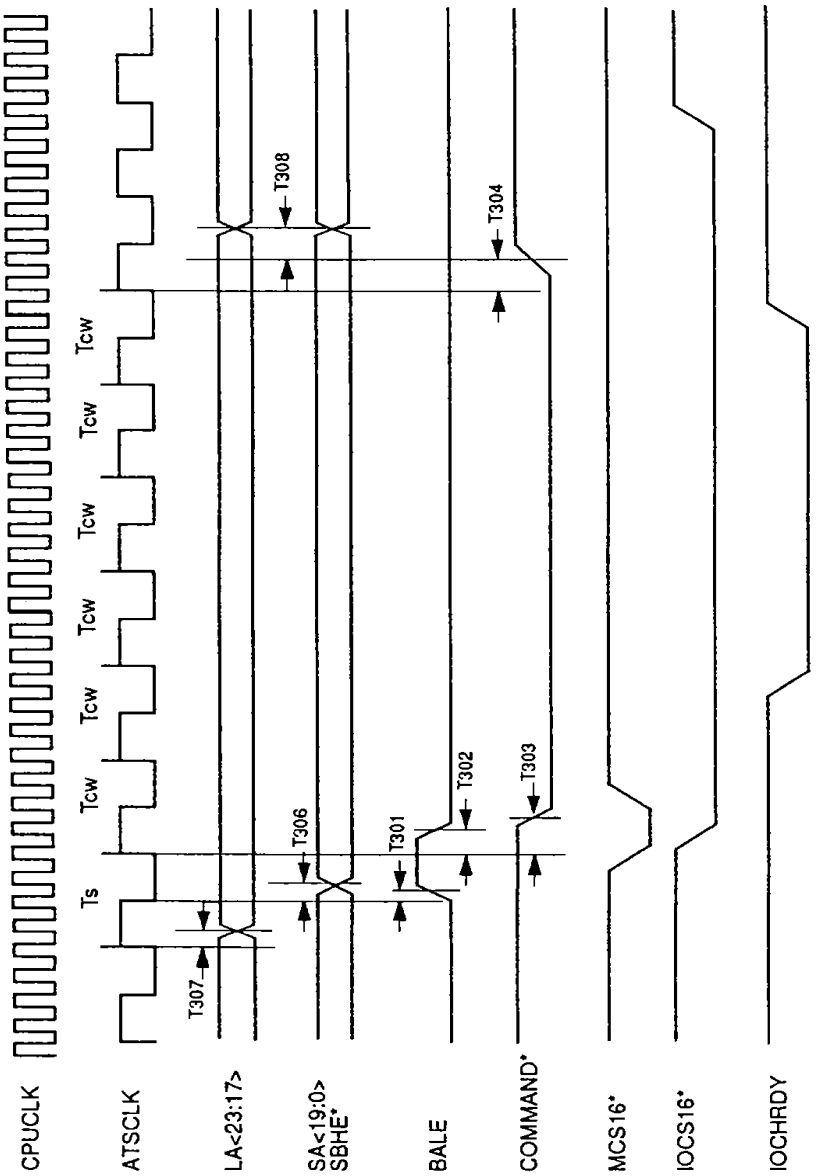


Figure 4-4. 16 Bit AT Bus Cycle (IOCHRDY)

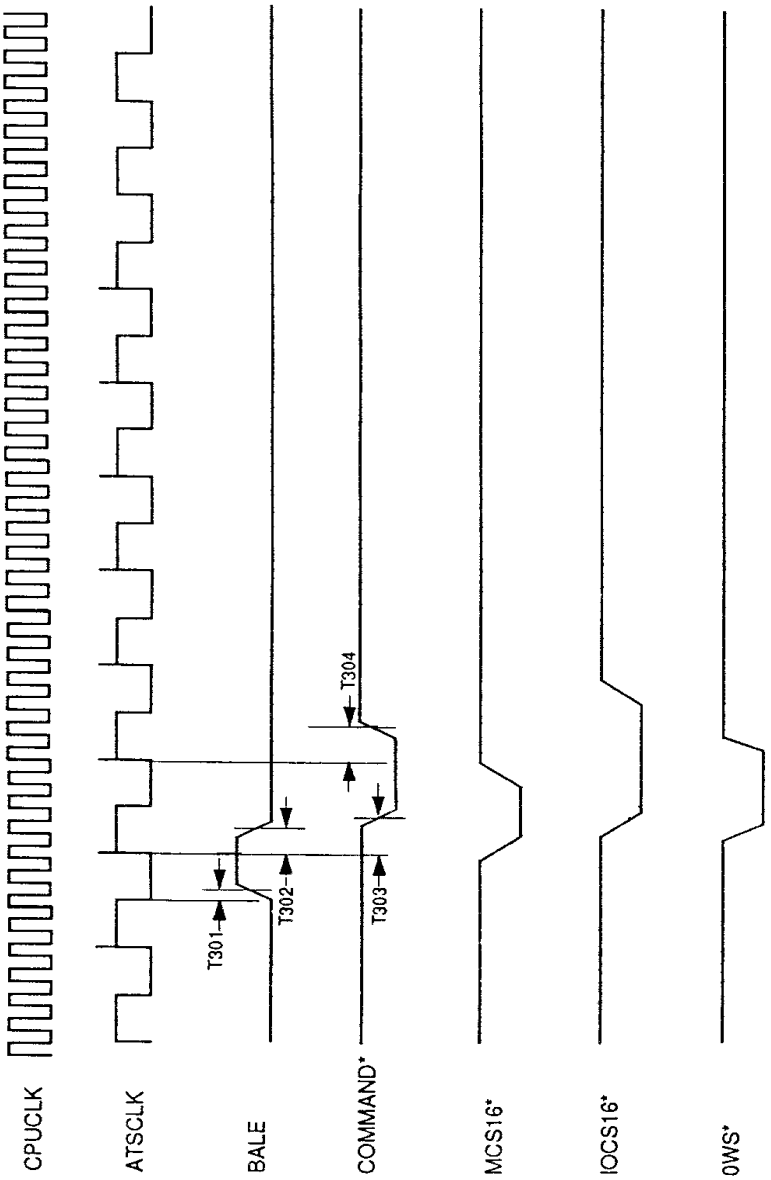


Figure 4-5. 16 Bit AT Bus Cycle (0 Wait)

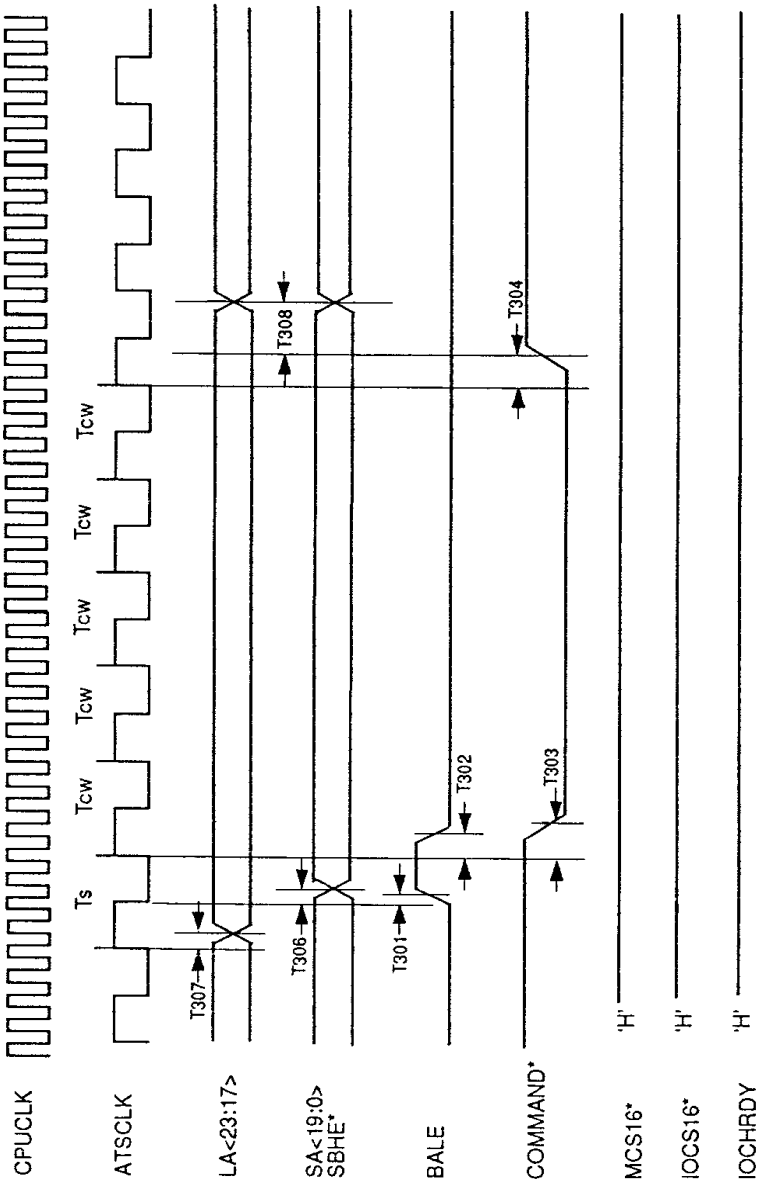


Figure 4-6. 8 Bit AT Bus Cycle

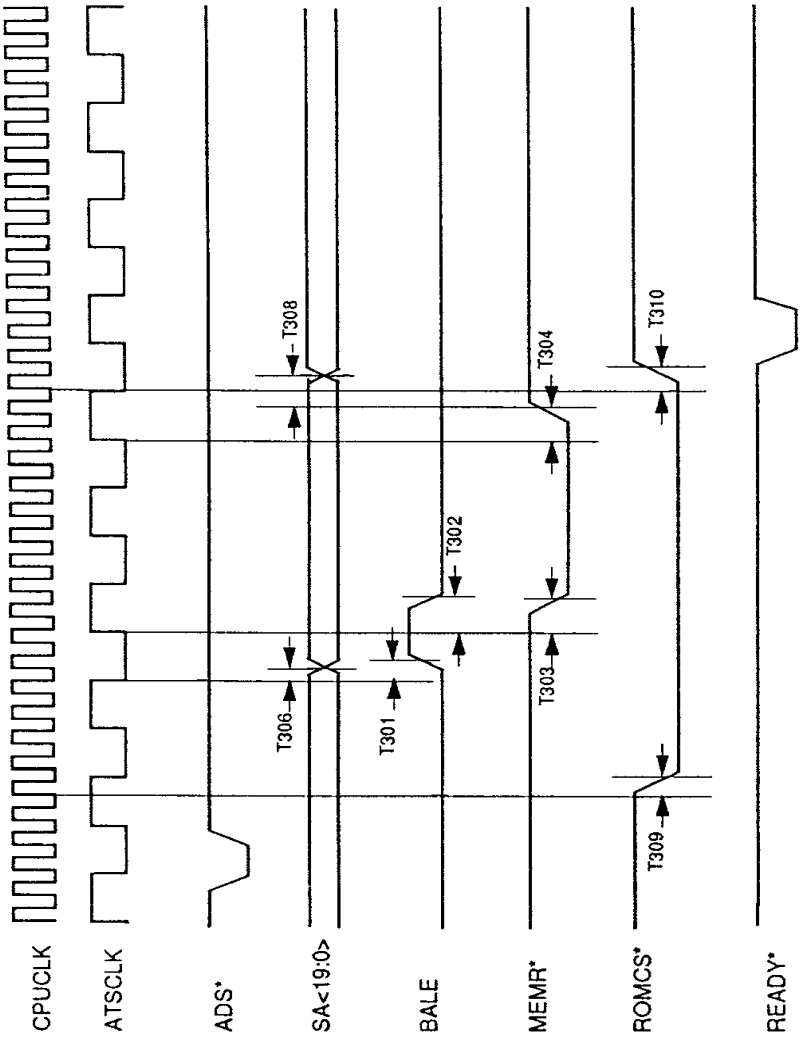


Figure 4-7. 16 Bit ROM BIOS Read Cycle

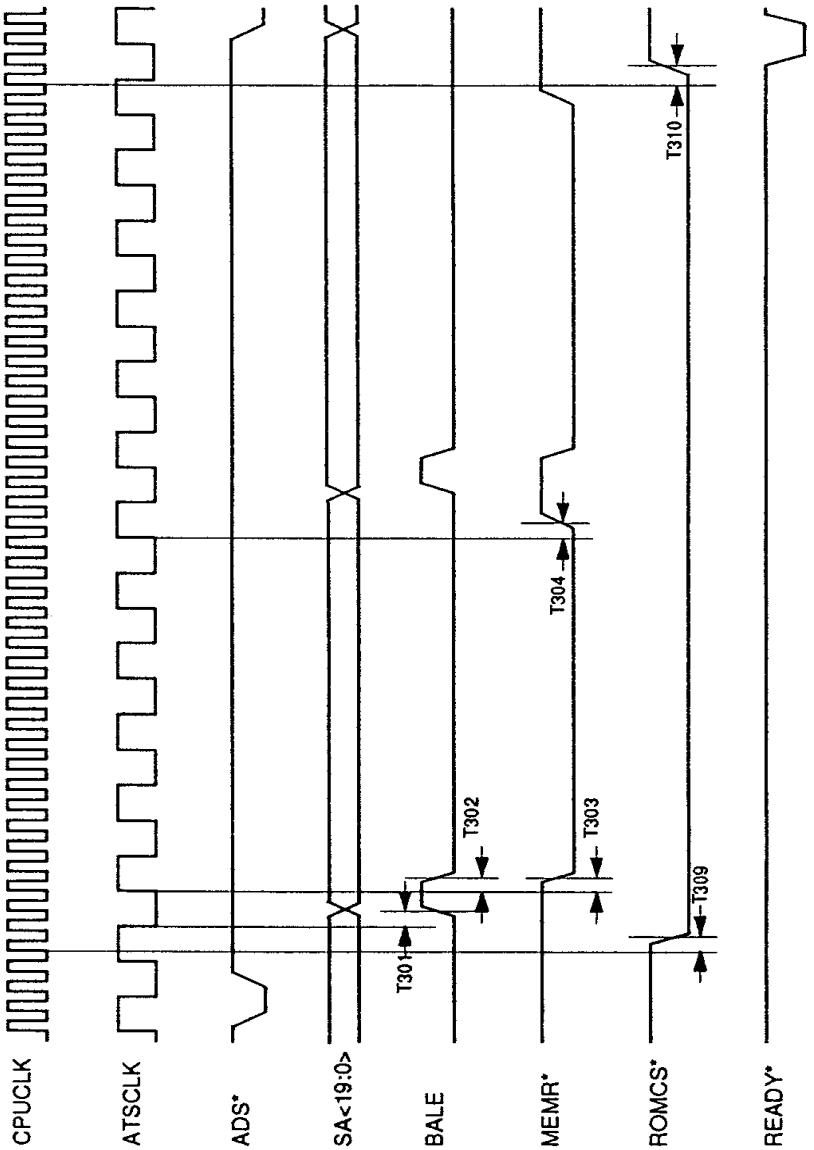
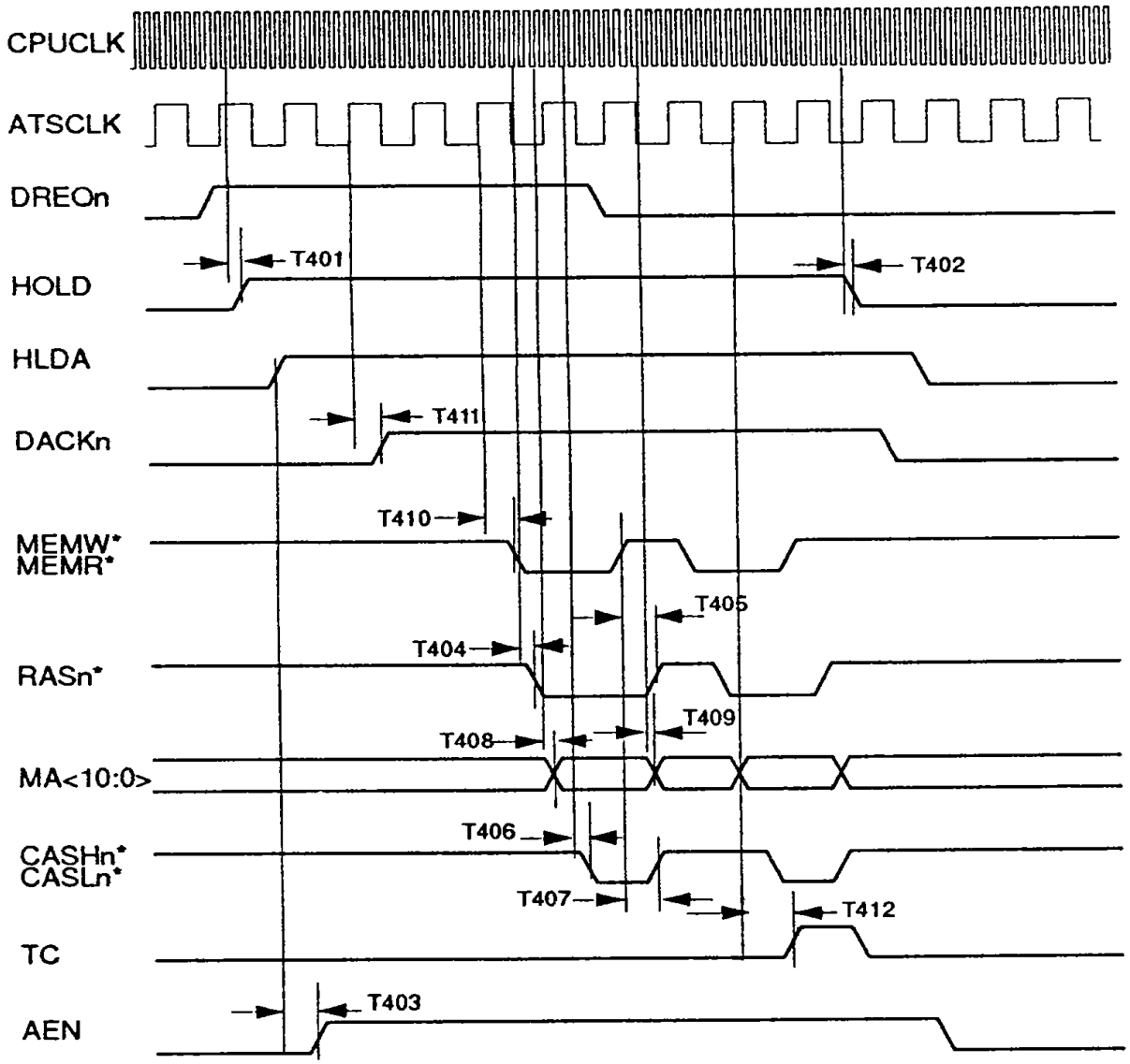


Figure 4-8. 8 Bit ROM BIOS Read Cycle



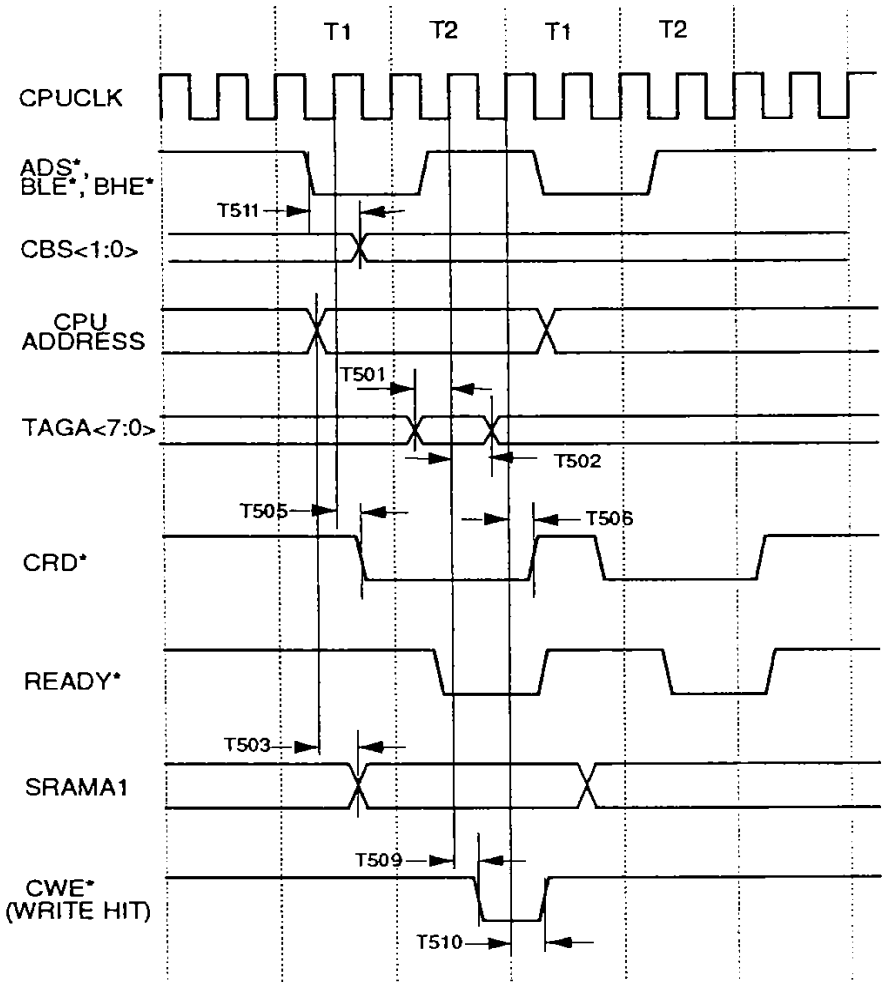


Figure 4-10. Cache Hit, 0 WS SRAM

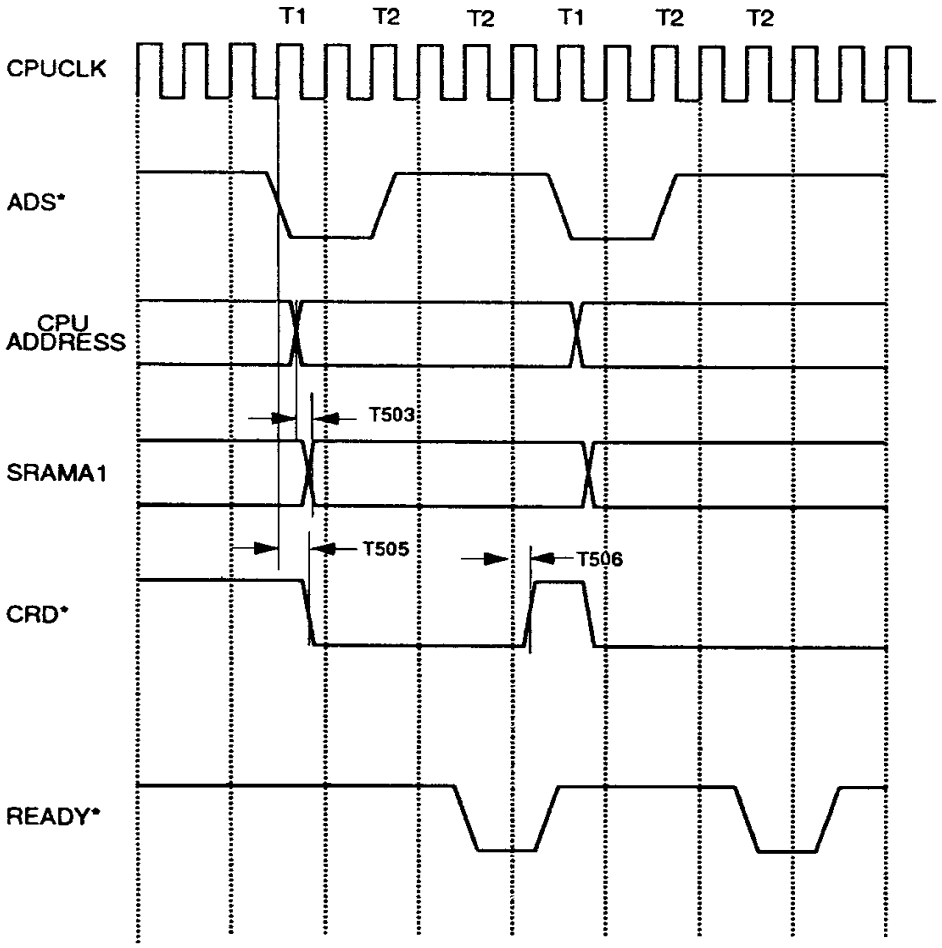


Figure 4-11. Cache HIT, 1 WS SRAM

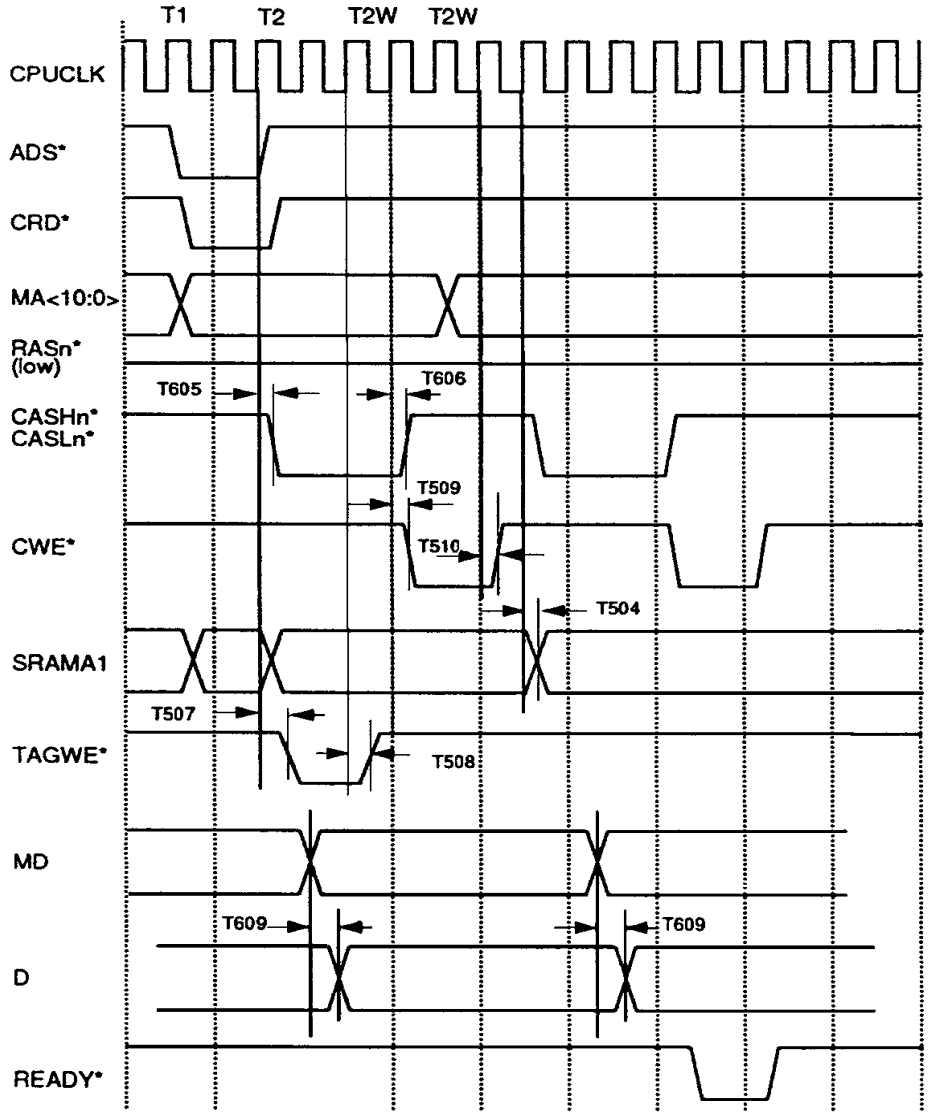


Figure 4-12. Cache Read Miss, Page Hit, 0/1 WS SRAM, 1 WS DRAM

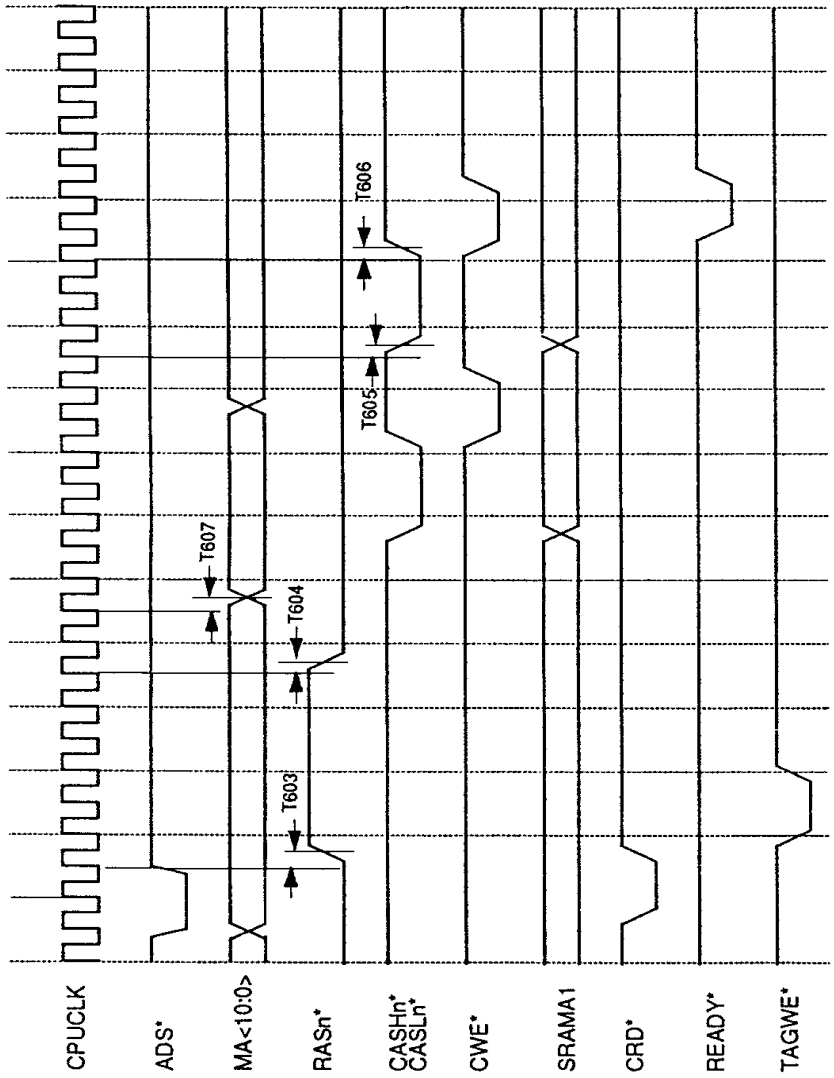


Figure 4-13. Cache Read Miss, Page Miss, 0 WS SRAM, 1 WS DRAM

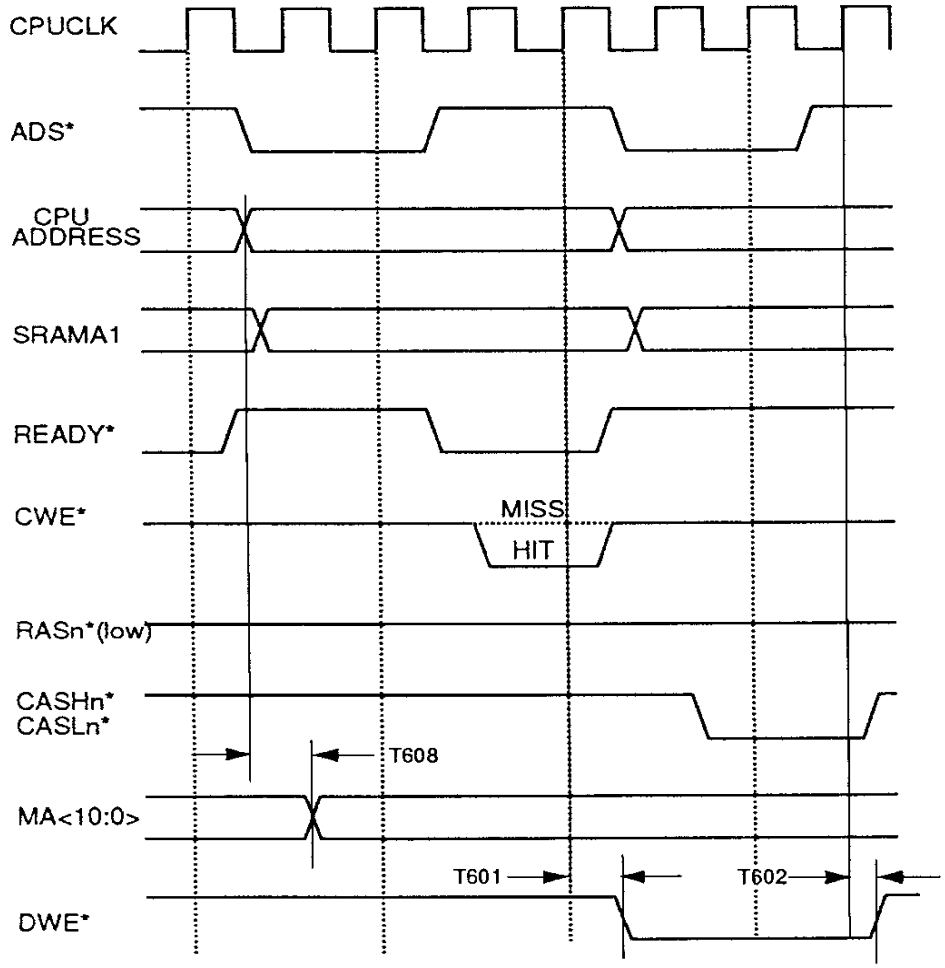


Figure 4-14. CPU Write, Page Hit, 0 WS SRAM, 0 WS DRAM

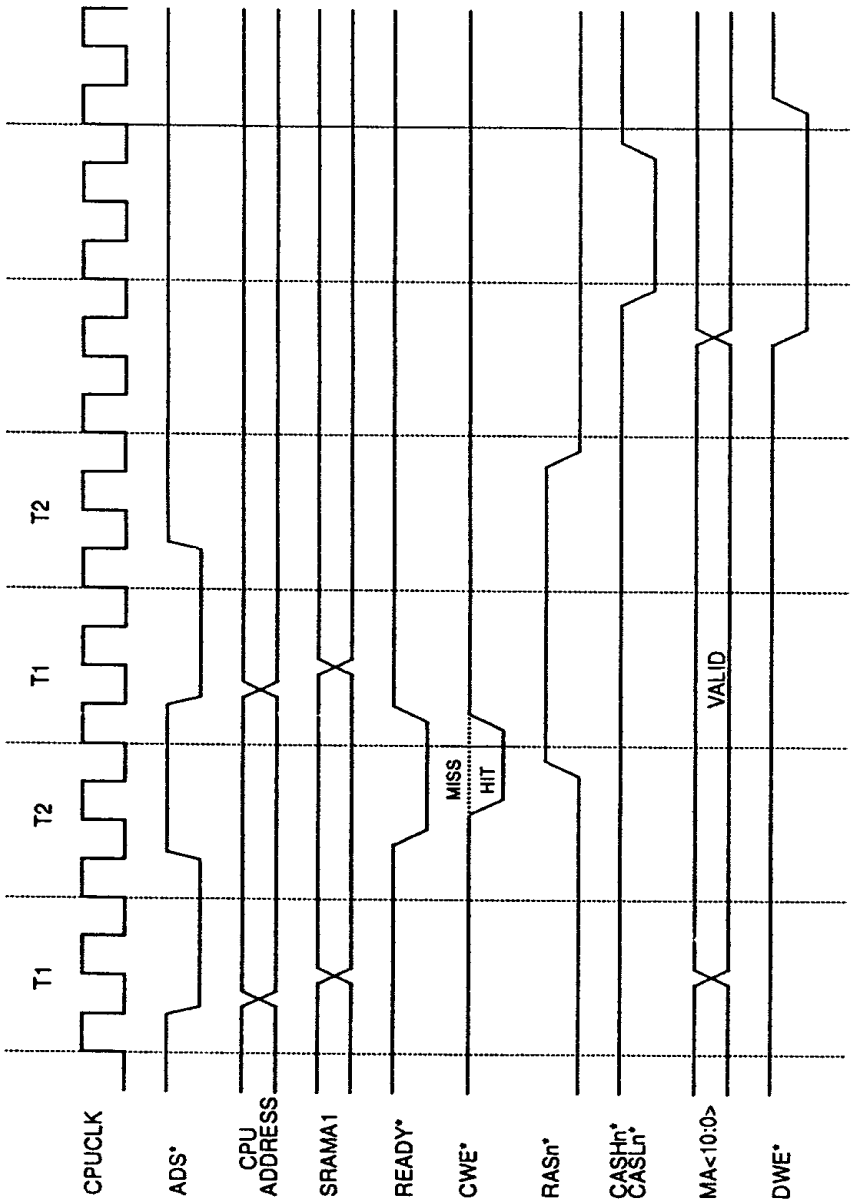


Figure 4-15. CPU Write, Page Miss, 0 WS SRAM, 0 WS DRAM

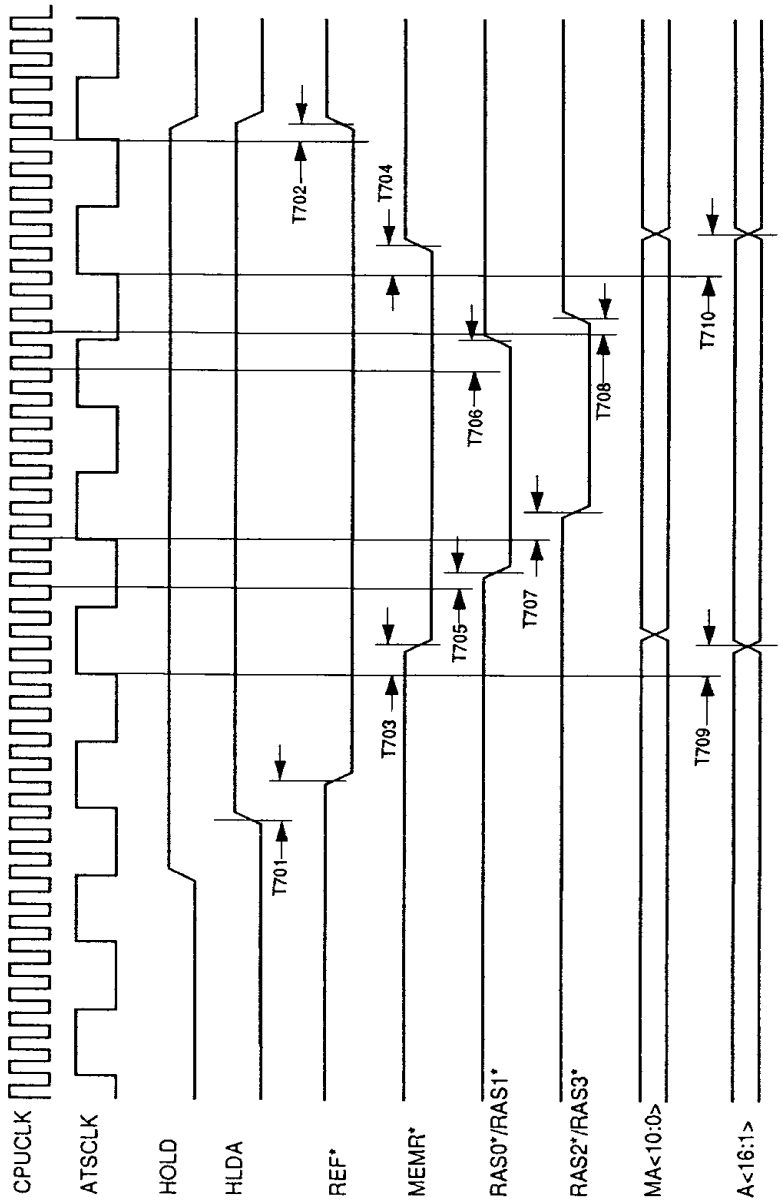


Figure 4-16. Refresh Timing

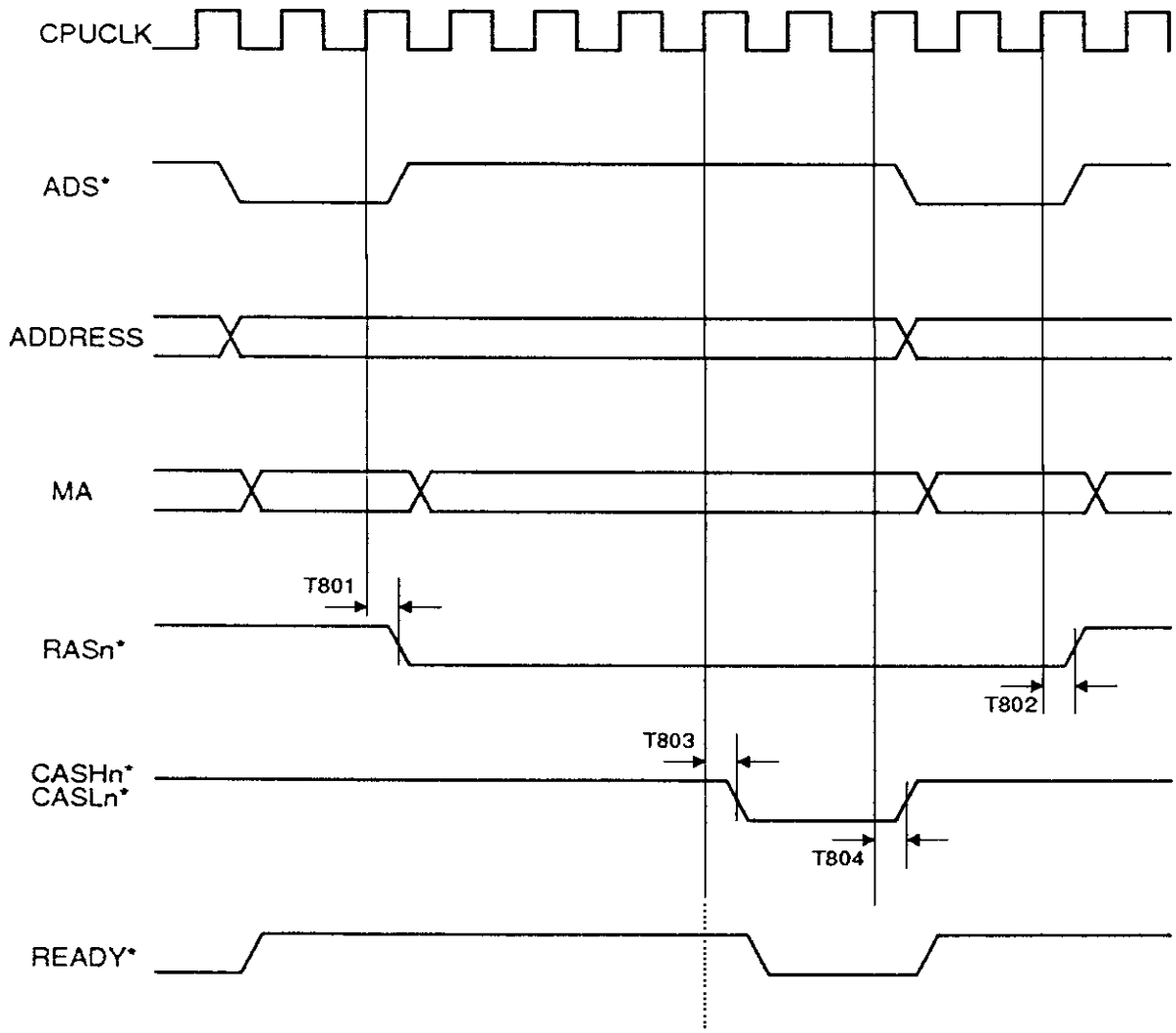


Figure 4-17. 0WS DRAM Read (MODE2)

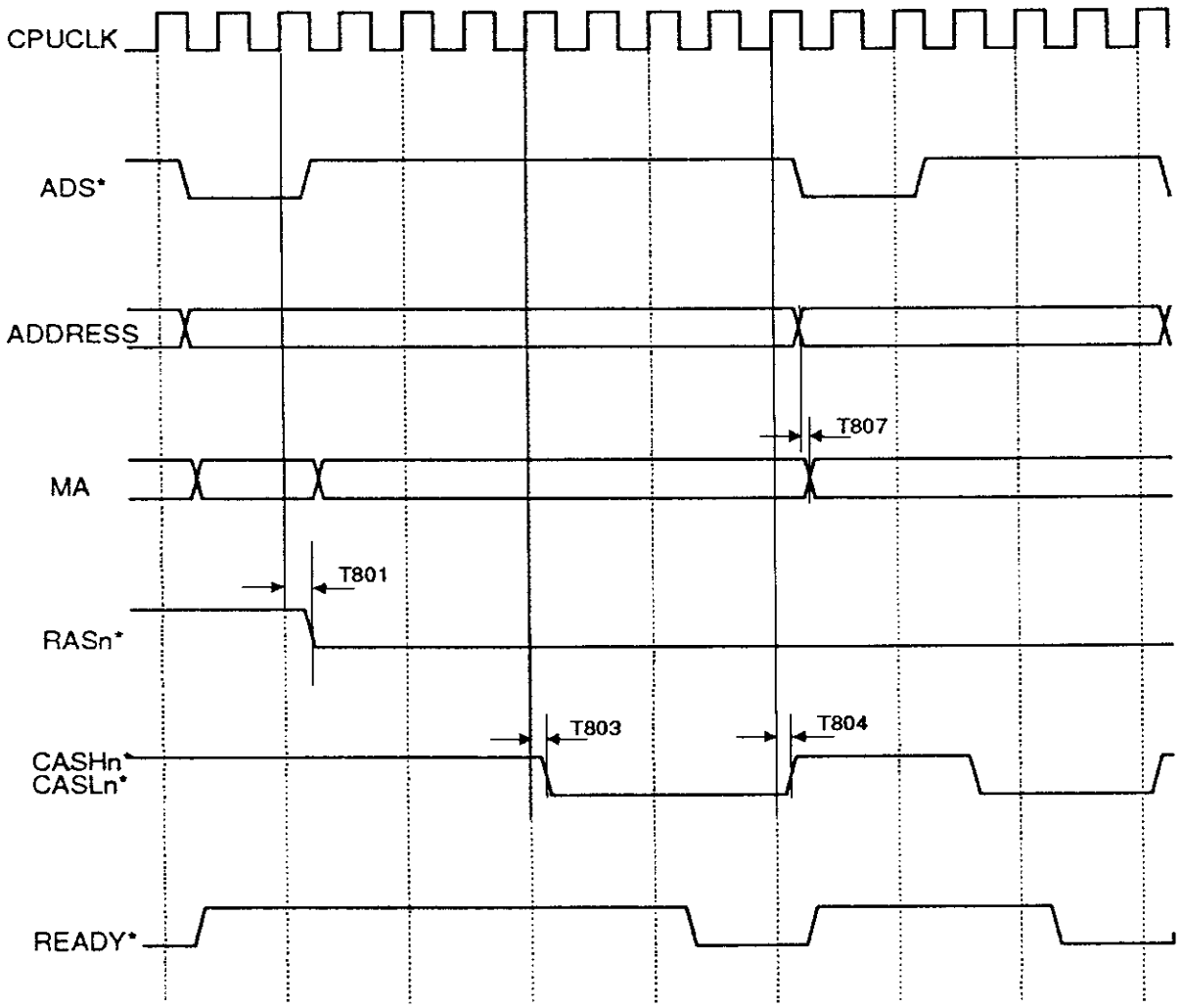


Figure 4-18. 1WS DRAM Read (MODE2)

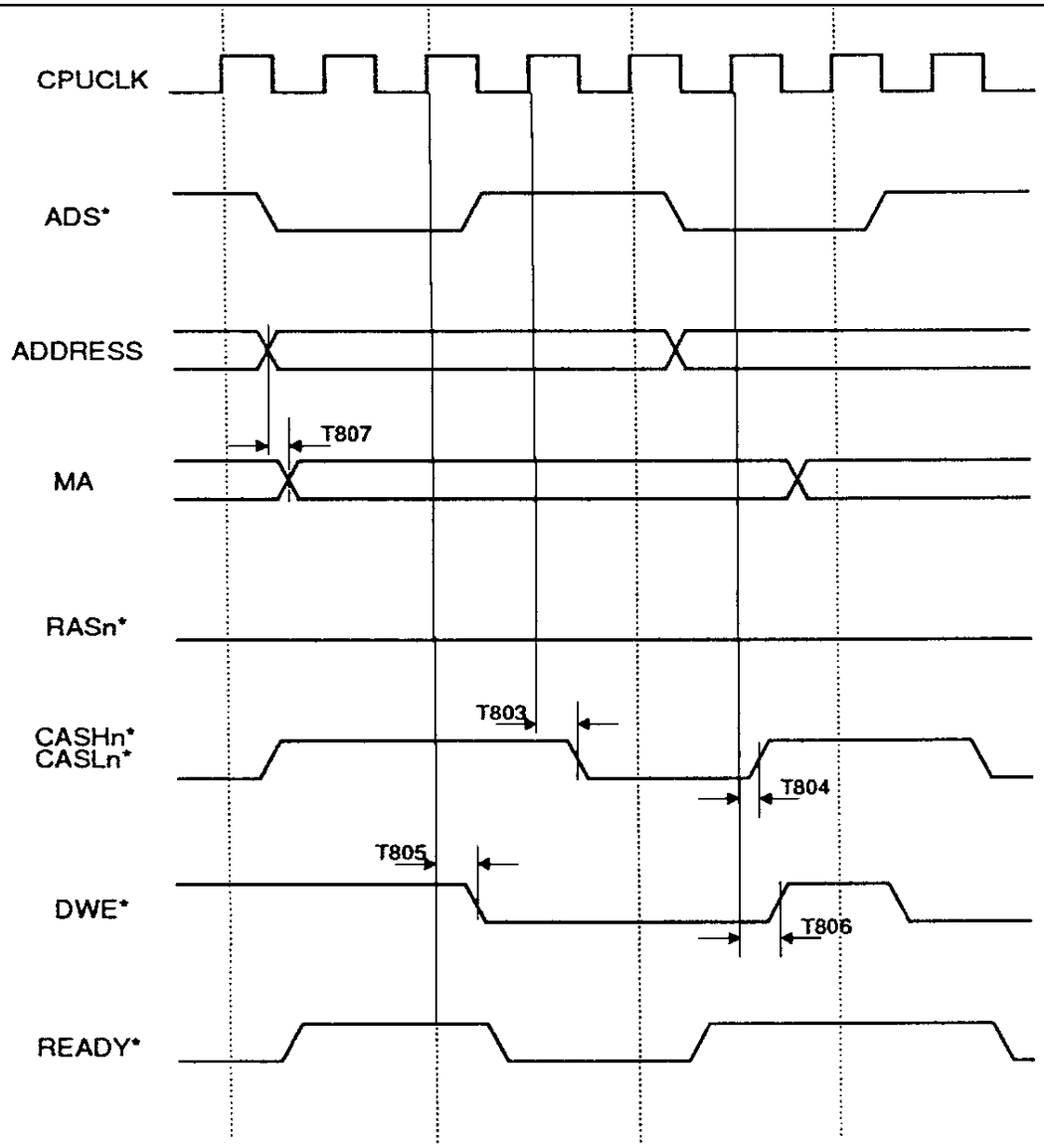


Figure 4-19. 0WS DRAM Write (MODE2)

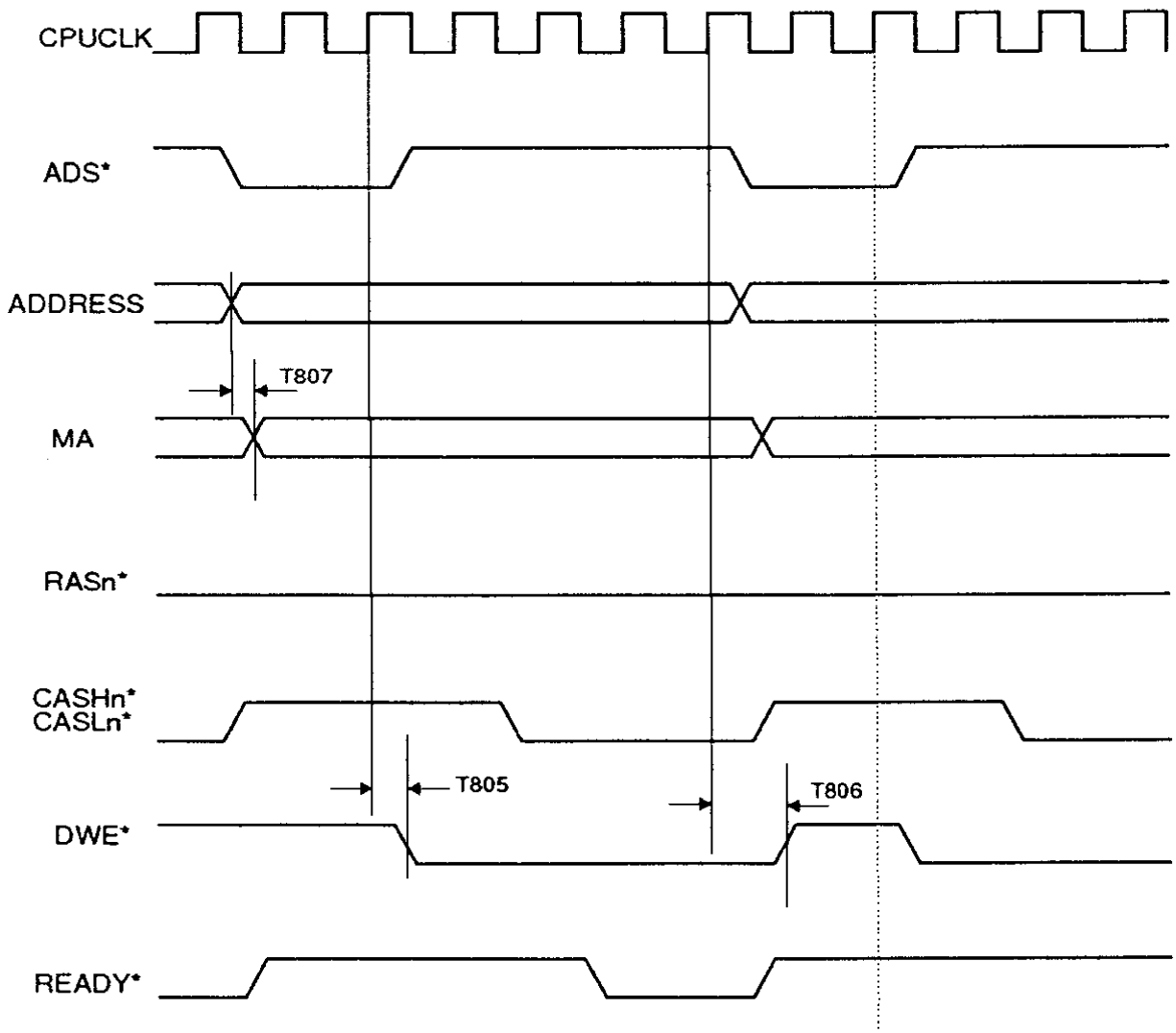


Figure 4-20. 1WS DRAM Write (MODE2)

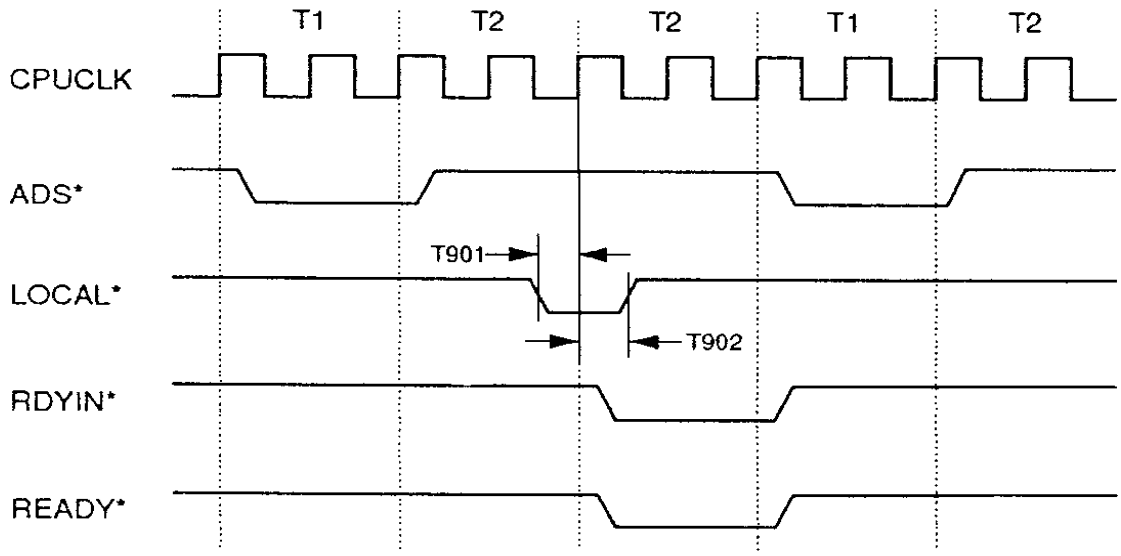
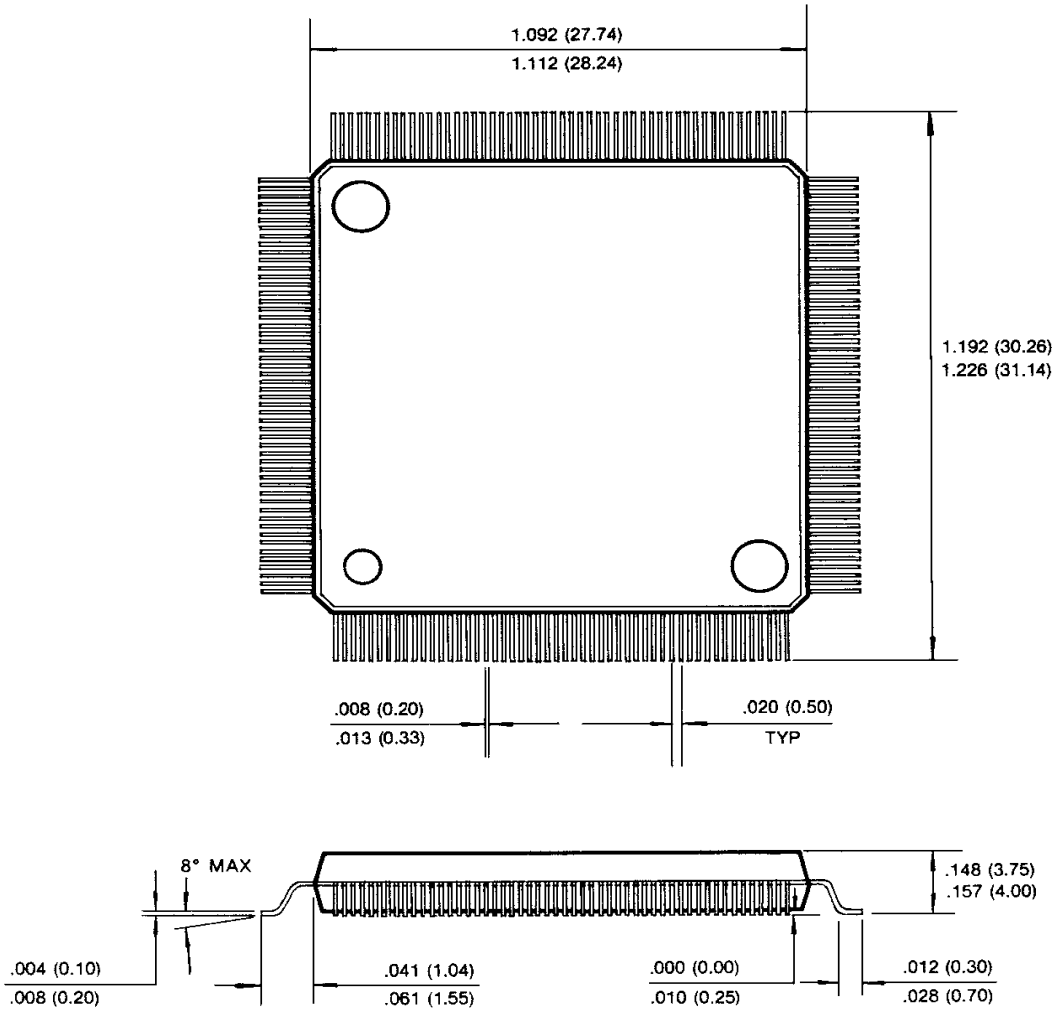


Figure 4-21. Local Cycle

5. KS82C388 PACKAGE



Dimensions in inches
and (Millimeters)