FEATURES

- Up to 16-digit LCD direct drive
- 8-bit × 4-channel A/D converter
- PLL frequency synthesizer
- 8-bit × 6-channel PWM outputs
- 16,384 × 8-bit ROM and 1,024 × 4-bit RAM
- 55 I/O pins
- 8-bit basic timer and timer/counter
- 16-bit IF counter
- Multi-function watch timer
- 8-bit serial I/O interface
- 4 external, 4 internal vectored interrupts
- 4 frequency outputs for buzzer
- On-chip crystal, ceramic, or RC oscillator
- 4 power-down modes
- Operating voltage range: 2.7 V to 6.0 V
- Operating temperature: – 40 °C to + 85 °C
- 100-pin QFP package

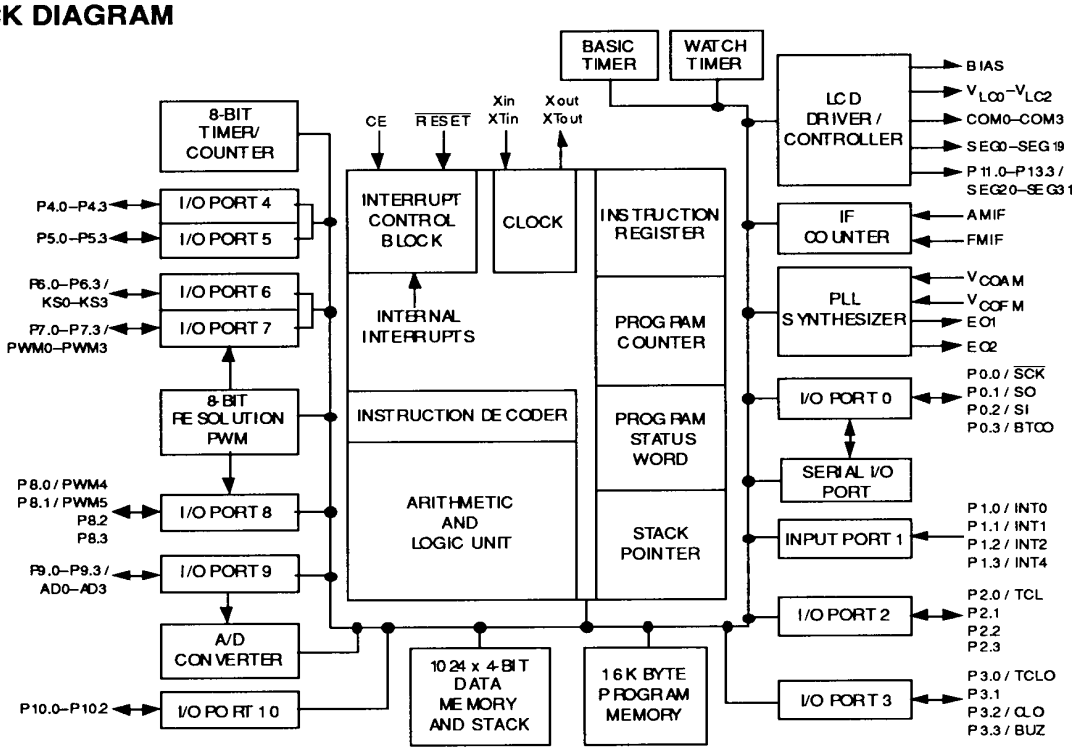
GENERAL DESCRIPTION

The KS57C3016 single-chip CMOS microcontroller has been designed for very high performance using Samsung's newest 4-bit CPU core, SAM4 (Samsung Arrangeable Microcontrollers).

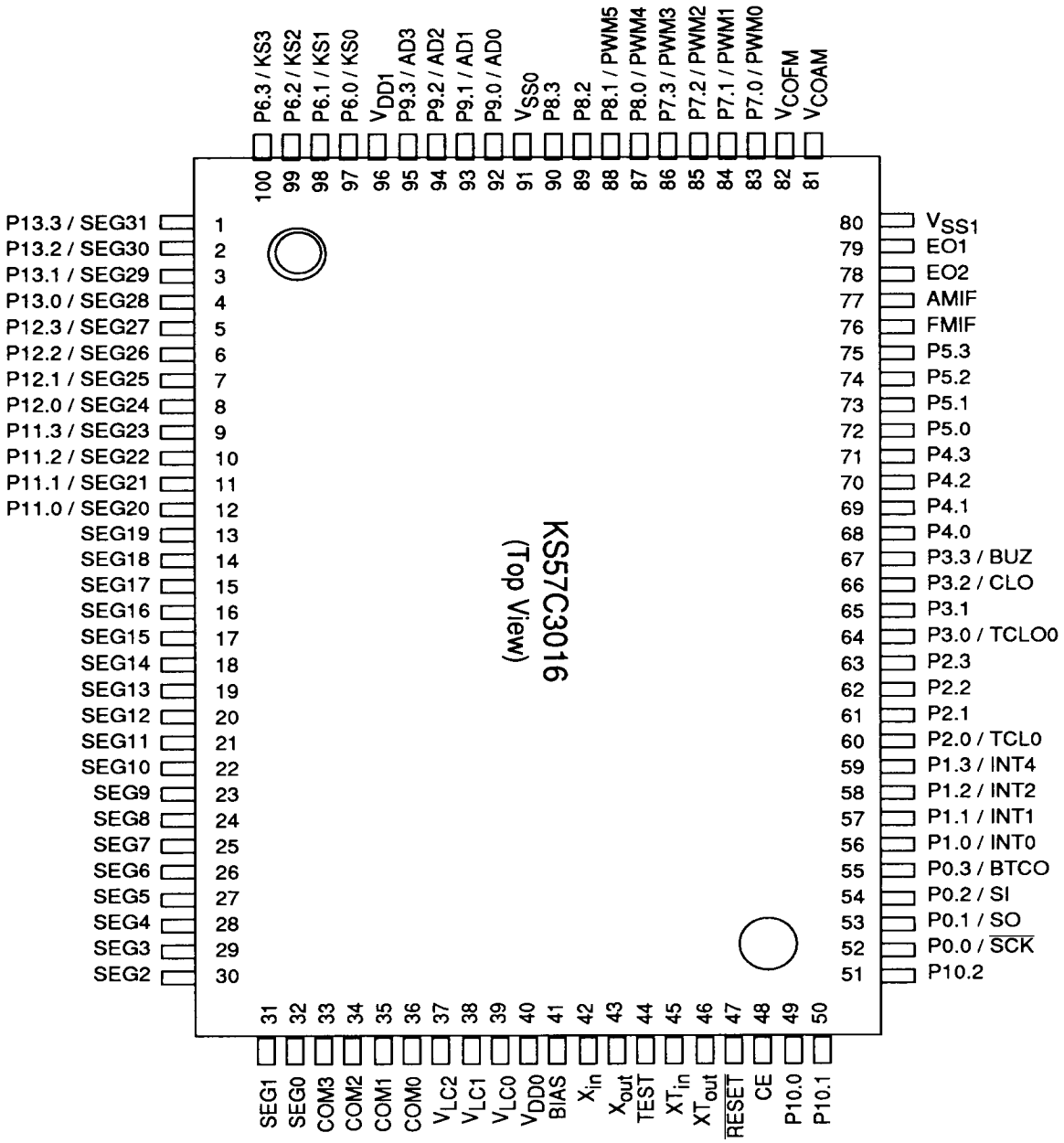
With an up-to-16-digit LCD direct drive capability, a 4-channel A/D converter, 8-bit timer/counter, PLL frequency synthesizer, and 6-channel PWM outputs, the KS57C3016 offers you an excellent design solution for a wide variety of DTS applications.

Up to 55 pins of the 100-pin QFP package can be dedicated to I/O. Eight vectored interrupts provide fast response to internal and external events. In addition, the KS57C3016's advanced CMOS technology provides for low power consumption and a wide operating voltage range.

BLOCK DIAGRAM



PIN ASSIGNMENTS



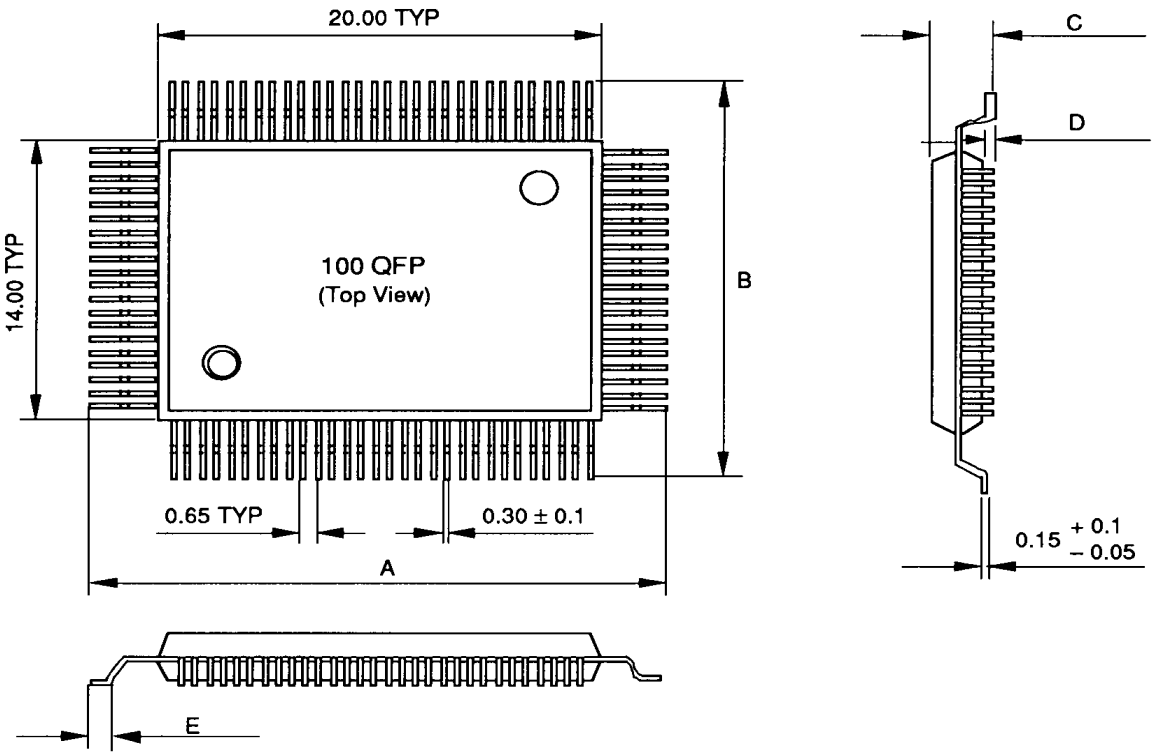
PIN DESCRIPTIONS

Pin Name	Pin Type	Description	Number	Share Pin
P0.0 P0.1 P0.2 P0.3	I/O	4-bit I/O port. 1-bit and 4-bit read/write and test is possible. Individual pins are software configurable as input or output. 4-bit pull-up resistors are software assignable to input pins; pull-up resistors are automatically disabled for output pins.	52 53 54 55	$\overline{SCK}$ SO SI BTCO
P1.0 P1.1 P1.2 P1.3	I	4-bit input port. 1-bit and 4-bit read and test is possible. 3-bit pull-up resistors are assignable by software to pins P1.0, P1.1, and P1.2.	56 57 58 59	INT0 INT1 INT2 INT4
P2.0 P2.1 P2.2 P2.3	I/O	Same as port 0	60 61 62 63	TCL0
P3.0 P3.1 P3.2 P3.3	I/O	Same as port 0	64 65 66 67	TCLO0 — CLO BUZ
P4.0–P4.3 P5.0–P5.3	I/O	4-bit I/O ports. N-channel open-drain output up to 9 volts. 1- and 4-bit read/write and test is possible. Ports 4 and 5 can be paired to support 8-bit data transfer. Pull-up resistors are assignable to individual pins by mask option.	68–71 72–75	—
P6.0–P6.3	I/O	Same as port 0. Ports 6 and 7 can be paired to enable 8-bit data transfer.	97–100	KS0–KS3
P7.0–P7.3 P8.0–P8.3	I/O	N-channel open-drain 4-bit I/O ports up to 9 volts. 1-bit and 4-bit read/write and test is possible. Pins are individually software configurable as input or output. Pull-up resistors are assignable to individual pins by mask option.	83–86 87–90	PWM0–PWM3 PWM4–PWM5
P9.0–P9.3	I/O	Same as port 0	92–95	AD0–AD3
P10.0–P10.2	I/O	Same as port 0 except that port 10 is 3-bit I/O port.	49–51	—
P11.0–11.3 P12.0–12.3 P13.0–13.3	O	Output ports for 1-bit data	12–9 8–5 4–1	SEG20–SEG31
$\overline{SCK}$	I/O	Serial I/O interface clock signal	52	P0.0
SO	I/O	Serial data output	53	P0.1
SI	I/O	Serial data input	54	P0.2

PIN DESCRIPTIONS (Continued)

Pin Name	Pin Type	Description	Number	Share Pin
BTCO	I/O	Basic timer clock output	55	P0.3
INT0, INT1	I	External interrupts. The triggering edge for INT0 and INT1 is selectable.	56–57	P1.0, P1.1
INT2	I	Quasi-interrupt with detection of rising edges	58	P1.2
INT4	I	External interrupt with detection of rising and falling edges	59	P1.3
TCL0	I/O	External clock input for timer/counter 0	60	P2.0
TCLO0	I/O	Timer/counter 0 clock output	64	P3.0
CLO	I/O	Clock output	66	P3.2
BUZ	I/O	2.2 kHz, 4.4 kHz, 8.8 kHz, or 17.6 kHz frequency output at 4.5 MHz for buzzer sound	67	P3.3
KS0–KS3	I/O	Quasi-interrupt inputs with falling edge detection	97–100	P6.0–P6.3
PWM0–PWM5	I/O	PWM outputs	83–88	P7.0–P8.1
AD0–AD3	I/O	A/D converter analog inputs	92–95	P9.0–P9.3
SEG0–SEG19	O	LCD segment data outputs	32–13	—
SEG20–SEG31	O	LCD segment data outputs	12–1	P11.0–P13.3
COM0–COM3	O	LCD common signal outputs	36–34	—
CE	I	Input pin for checking device power. High level during normal operation; low level when PLL operation stops.	48	—
EO1–EO2	O	Output for PLL error data	78–79	—
V_{COAM}, V_{COFM}	I	External V_{COAM} and V_{COFM} inputs	81–82	—
AMIF, FMIF	I	Intermediate AM/FM frequency input	77–76	—
TEST	I	Test signal input (must be connected to V_{SS})	44	—
V_{DD0}	—	Main power supply	40	—
V_{SS0}	—	Main ground	91	—
V_{DD1}	—	Power supply for PLL prescaler	96	—
V_{SS1}	—	PLL prescaler ground	80	—
$\overline{RESET}$	I	Reset signal	47	—
BIAS	—	LCD power control	41	—
V_{LC0}–V_{LC2}	—	LCD power supply. Voltage dividing resistors are assignable by mask option.	39–37	—
X_{in}, X_{out}	—	Crystal, ceramic, or RC oscillator signal for main system clock.	42, 43	—
XT_{in}, XT_{out}	—	Crystal oscillator signal for subsystem clock.	45, 46	—

PACKAGE DIMENSIONS



Item / Package	A	B	C	D	E
100-QFP-1420A	25.00 ± 0.3	19.00 ± 0.3	2.45 MAX	0.15 + 0.1 − 0.05	1.20 ± 0.2
100-QFP-1420B	23.90 ± 0.3	17.90 ± 0.3	2.45 MAX	0.15 + 0.1 − 0.05	0.80 ± 0.2
100-QFP-1420C	23.20 ± 0.3	17.20 ± 0.3	3.00 MAX	0.15 ± 0.1	0.80 ± 0.2

NOTE: Typical dimensions are in millimeters.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

(T_A = 25 °C)

Parameter	Symbol	Conditions	Rating	Units
Supply Voltage	V_{DD}	—	− 0.3 to + 7.0	V
Input Voltage	V_{I1}	Applies to I/O ports 4, 5, 7, and 8. (Pull-up resistors are individually assignable to pins at ports 4, 5, 7 and 8, or they can remain open-drain)	− 0.3 to V_{DD} + 0.3 (With pull-up resistor) − 0.3 to + 9.0 (Open-drain)	V
	V_{I2}	All I/O ports except 4, 5, 7, and 8	− 0.3 to V_{DD} + 0.3	
Output Voltage	V_O	—	− 0.3 to V_{DD} + 0.3	V
Output Current High	I_{OH}	One I/O port active	− 15	mA
		All I/O ports active	− 30	
Output Current Low	I_{OL}	One I/O port active	+ 30 (Peak value)	mA
			+ 15 *	
		Total for ports 0, 2–10 total	+ 100 (Peak value)	
			+ 60 *	
Operating Temperature	T_A	—	− 40 to + 85	°C
Storage Temperature	T_{stg}	—	− 65 to + 150	°C

* The values for Output Current Low (I_{OL}) are calculated as Peak Value × $\sqrt{\text{Duty}}$.

DATA RETENTION IN STOP MODE

(T_A = − 40 °C to + 85 °C)

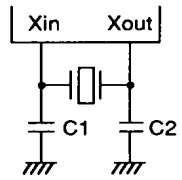
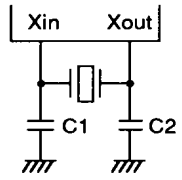
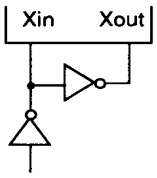
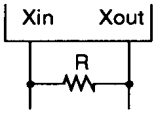
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V_{DDDR}	—	2.0	—	6.0	V
Data retention supply current	I_{DDDR}	V_{DDDR} = 2.0 V	—	0.1	10	µA
Release signal set time	t_{SREL}	—	0	—	—	µs
Oscillator stabilization wait time (1)	t_{WAIT}	Released by $\overline{\text{RESET}}$	—	2^{17} / fx	—	ms
		Released by interrupt	—	(2)	—	

NOTES:
1. During oscillator stabilization wait time, all CPU operations must be stopped to avoid instability during oscillator start-up.
2. Use the basic timer mode register (BMOD) interval timer to delay execution of CPU instructions during the wait time.

ELECTRICAL CHARACTERISTICS

MAIN SYSTEM CLOCK OSCILLATORS

(T_A = − 40 °C + 85 °C, V_{DD} = 2.7 V to 6.0 V)

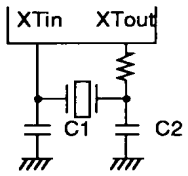
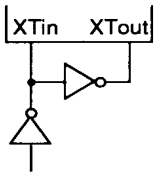
Oscillator	Clock Configuration	Parameter	Test Condition	Min	Typ	Max	Units
Ceramic Oscillator		Oscillation frequency (1)	—	0.4	—	5.0	MHz
		Stabilization time (2)	Stabilization occurs when V_{DD} is equal to the minimum oscillator voltage range.	—	—	4	ms
Crystal Oscillator		Oscillation frequency (1)	—	0.4	4.5	5.0	MHz
		Stabilization time (2)	V_{DD} = 4.5 V to 6.0 V	—	—	10	ms
			V_{DD} = 2.7 V to 4.5 V	—	—	30	
External Clock		X_{in} input frequency (1)	—	0.4	—	4.5	MHz
		X_{in} input high and low level width (t_{XH}, t_{XL})	—	111	—	1250	ns
RC Oscillator		Frequency	R = 40 kΩ, V_{DD} = 5 V	—	2	—	MHz
			R = 65 kΩ, V_{DD} = 3 V	—	1	—	

NOTES:
1. Oscillation frequency and X_{in} input frequency data are for oscillator characteristics only.
2. Stabilization time is the interval required for oscillating stabilization after a power-on occurs, or when stop mode is terminated.

ELECTRICAL CHARACTERISTICS

SYBSYSTEM CLOCK OSCILLATORS

(T_A = − 40 ℃ + 85 ℃, V_{DD} = 2.7 V to 6.0 V)

Oscillator	Clock Configuration	Parameter	Test Condition	Min	Typ	Max	Units
Crystal Oscillator		Oscillation frequency (1)	—	32	32.768	35	kHz
		Stabilization time (2)	V_{DD} = 4.5 V to 6.0 V	—	1.0	2	s
			V_{DD} = 2.7 V to 4.5 V	—	—	10	
External Clock		XT_{in} input frequency (1)	—	32	—	100	kHz
		XT_{in} input high and low level width (t_{XH}, t_{XL})	—	5	—	15	μs

NOTES:
1. Oscillation frequency and XT_{in} input frequency data are for oscillator characteristics only.
2. Stabilization time is the interval required for oscillating stabilization after a power-on occurs.

ELECTRICAL CHARACTERISTICS

D.C.

(T_A = −40 °C to +85 °C, V_{DD} = 2.7 V to 6.0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input High Voltage	V_{IH1}	All input pins except those specified below for V_{IH2}–V_{IH4}	0.7V_{DD}	—	V_{DD}	V
	V_{IH2}	Ports 0, 1, 6, 7, and $\overline{RESET}$	0.8V_{DD}		V_{DD}	
	V_{IH3}	Ports 4, 5, 7, and 8 with pull-up resistors assigned	0.7V_{DD}		V_{DD}	
		Ports 4, 5, 7, and 8 are open-drain	0.7V_{DD}		9	
	V_{IH4}	X_{in}, X_{out}, and XT_{in}	V_{DD} – 0.5		V_{DD}	
Input Low Voltage	V_{IL1}	All input pins except those specified below for V_{IL2}–V_{IL3}	—	—	0.3V_{DD}	V
	V_{IL2}	Ports 0, 1, 6, 7, 9, 10, and $\overline{RESET}$			0.2V_{DD}	
	V_{IL3}	X_{in}, X_{out}, and XT_{in}			0.4	
Output High Voltage	V_{OH1}	V_{DD} = 4.5 V to 6.0 V I_{OH} = − 1 mA Ports 0, 2–10, and BIAS	V_{DD} – 1.0	—	—	V
		I_{OH} = − 100 μA	V_{DD} – 0.5			
	V_{OH2}	V_{DD} = 4.5 V to 6.0 V I_{OH} = − 100 μA Ports 11–13 only	V_{DD} – 2.0			
		I_{OH} = − 30 μA	V_{DD} – 1.0			
Output Low Voltage	V_{OL1}	V_{DD} = 4.5 V to 6.0 V I_{OL} = 1.6 mA Ports 4, 5, 7, and 8 only	—	0.4	2	V
		I_{OL} = 1.6 mA Ports 0, 2, 3, 6, 9, 10, EO1, and EO2 only		—	0.4	
		I_{OL} = 400 μA Ports 0, 2, 3, 6, 9, 10, EO1, and EO2 only			0.2	
	V_{OL2}	V_{DD} = 4.5 V to 6.0 V I_{OL} = 100 μA Port 11, 12, and 13 only			1	
		I_{OL} = 50 μA			1	
Input High Leakage Current	I_{LIH1}	V_I = V_{DD} All input pins except those specified below for I_{LIH2}–I_{LIH3}	—	—	3	μA
	I_{LIH2}	V_I = V_{DD} X_{in}, X_{out}, XT_{in}, and $\overline{RESET}$ only			20	
	I_{LIH3}	V_I = 9 V Ports 4, 5, 7, and 8 are open-drain			20	

ELECTRICAL CHARACTERISTICS

D.C. (Continued)

(T_A = −40 °C to +85 °C, V_{DD} = 2.7 V to 6.0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Low Leakage Current	I_{LIL1}	V_I = 0 V All input pins except X_{in}, X_{out}, and XT_{in}	—	—	−3	μA
	I_{LIL2}	V_I = 0 V X_{in}, X_{out}, XT_{in}, and $\overline{RESET}$ only			−20	
Output High Leakage Current	I_{LOH1}	$V_O = V_{DD}$ All output pins except for ports 4, 5, 7, and 8	—	—	3	μA
	I_{LOH2}	Ports 4, 5, 7 and 8 are open-drain V_O = 9 V			20	
Output Low Leakage Current	I_{LOL}	V_O = 0 V	—	—	−3	μA
Pull-Up Resistor	R_{L1}	V_I = 0 V; V_{DD} = 5 V ± 10% Port 0–3, 6, 9, and 10 (except P1.3)	15	40	80	kΩ
		V_{DD} = 3 V ± 10%	30	—	200	
	R_{L2}	$V_O = V_{DD}$ − 2 V V_{DD} = 5 V ± 10% Ports 4, 5, 7, and 8 only	15	40	70	
		V_{DD} = 3 V ± 10%	10	—	60	
LCD Drive Voltage	V_{LCD}	—	2.5	—	V_{DD}	V
LCD Voltage Dividing Resistor	R_{LCD}	—	50	100	140	kΩ
COM Output Impedance	R_{COM}	V_{DD} = 5 V ± 10%	—	3	6	kΩ
		V_{DD} = 3 V ± 10%		10	15	
SEG Output Impedance	R_{SEG}	V_{DD} = 5 V ± 10%	—	3	20	kΩ
		V_{DD} = 3 V ± 10%		10	60	

ELECTRICAL CHARACTERISTICS

D.C. (Concluded)

(T_A = −40 °C to +85 °C, V_{DD} = 2.7 V to 6.0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Current (1)	I_{DD1} (2)	V_{DD} = 5 V ± 10% (3) 4.5 MHz crystal oscillator C1 = C2 = 22 pF CE high; PLL operates	—	12	20	mA
	I_{DD2} (2)	Idle mode; V_{DD} = 5 V ± 10% 4.5 MHz crystal oscillator C1 = C2 = 22 pF CPU clock = fxx/4 CE low; PLL stops		1.4	1.8	
		V_{DD} = 3 V ± 10% CPU clock = fxx/64		0.23	1.0	
	I_{DD3} (5)	V_{DD} = 3 V ± 10% 32 kHz crystal oscillator CE low; PLL stops	—	25	120	μA
	I_{DD4} (5)	Idle mode; V_{DD} = 3 V ± 10% 32 kHz crystal oscillator		20	30	
	I_{DD5}	Stop 1 mode; XT_{in} = 0 V V_{DD} = 5 V ± 10% CPU clock = fxx/4 CE low; PLL stops		0.6	5	
		V_{DD} = 3 V ± 10% CPU clock = fxx/64		0.2	3	
	I_{DD6}	V_{DD} = 5 V ± 10 % 4.5 MHz crystal oscillator CPU clock = fxx/4 CE low; PLL stops	—	4.2	8	mA
		V_{DD} = 3 V ± 10 % CPU clock = fxx/64		0.7	1.2	
	I_{DD7}	Stop 2 mode; XT_{in} = 0 V V_{DD} = 5 V ± 10% CPU clock = fxx/4 CE low; PLL stops		0.12	2.0	μA
		V_{DD} = 3 V ± 10% CPU clock = fxx/64		0.05	1.0	

NOTES:
1. D.C. electrical values for Supply Current (I_{DD1} to I_{DD5}) do not include current drawn through internal pull-up resistors or through LCD voltage dividing resistors.
2. Data includes power consumption for subsystem clock oscillation.
3. For high-speed controller operation, the power control register (PCON) must be set to 0011B.
4. For low-speed controller operation, the power control register (PCON) must be set to 0000B.
5. When the system clock control register, SCMOD, is set to 1001B, main system clock oscillation stops and the subsystem clock is used.

ELECTRICAL CHARACTERISTICS

A.C.

(T_A = − 40 °C to + 85 °C, V_{DD} = 2.7 V to 6.0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Instruction Cycle Time (NOTE)	t_{CY}	V_{DD} = 4.5 V to 6.0 V	0.89	—	64	µs
		V_{DD} = 2.7 V to 4.5 V	3.8		64	
		With subsystem clock (fxt)	114	122	125	
TCL0, TCL1 Input Frequency	f_{TI0}, f_{TI1}	V_{DD} = 4.5 V to 6.0 V	0	—	1	MHz
		V_{DD} = 2.7 V to 4.5V			275	kHz
TCL0, TCL1 Input High, Low Width	t_{TIH0}, t_{TIL0} t_{TIH1}, t_{TIL1}	V_{DD} = 4.5 V to 6.0 V	0.48	—	—	µs
		V_{DD} = 2.7 V to 4.5 V	1.8			
$\overline{SCK}$ Cycle Time	t_{KCY}	V_{DD} = 4.5 V to 6.0 V External $\overline{SCK}$ source	800	—	—	ns
		Internal $\overline{SCK}$ source	950			
		V_{DD} = 2.7 V to 4.5 V External $\overline{SCK}$ source	3200			
		Internal $\overline{SCK}$ source	3800			
$\overline{SCK}$ High, Low Width	t_{KH}, t_{KL}	V_{DD} = 4.5 V to 6.0 V External $\overline{SCK}$ source	400	—	—	ns
		Internal $\overline{SCK}$ source	$t_{KCY}/2$ – 50			
		V_{DD} = 2.7 V to 4.5 V External $\overline{SCK}$ source	1600			
		Internal $\overline{SCK}$ source	$t_{KCY}/2$ – 150			
SI Setup Time to $\overline{SCK}$ High	t_{SIK}	External $\overline{SCK}$ source	100	—	—	ns
		Internal $\overline{SCK}$ source	150			
SI Hold Time to $\overline{SCK}$ High	t_{KSI}	External $\overline{SCK}$ source	400	—	—	ns
		Internal $\overline{SCK}$ source	400			

NOTE: Unless otherwise specified, Instruction Cycle Time condition values assume a main system clock (fx) source.

ELECTRICAL CHARACTERISTICS

A.C. (Concluded)

(T_A = − 40 °C to + 85 °C, V_{DD} = 2.7 V to 6.0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output Delay for $\overline{SCK}$ to SO	t_{KSO}	V_{DD} = 4.5 V to 6.0 V External $\overline{SCK}$ source	—	—	300	ns
		Internal $\overline{SCK}$ source			250	
		V_{DD} = 2.7 V to 4.5 V External $\overline{SCK}$ source			1000	
		Internal $\overline{SCK}$ source			1000	
Interrupt Input High, Low Width	t_{INTH}, t_{INTL}	INT0	(See Note)	—	—	µs
		INT1, INT2, INT4, KS0–KS3	10			
$\overline{RESET}$ Input Low Width	t_{RSL}	Input	10	—	—	µs

NOTE: Minimum value for INT0 is based on a clock of $2t_{CY}$ or 128 / fx as assigned by the IMOD0 register setting.

CAPACITANCE

(T_A = 25 °C, V_{DD} = 0 V)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Capacitance	C_{IN}	f = 1 MHz; Unmeasured pins are returned to V_{SS}	—	—	15	pF
Output Capacitance	C_{OUT}		—	—	15	pF
I/O Capacitance	C_{IO}		—	—	15	pF

FUNCTIONAL DESCRIPTION

ARITHMETIC AND LOGIC UNIT

All KS57-series microcontrollers have the advanced SAM4 CPU core. The SAM4 CPU can directly address up to 32 K bytes of program memory. The arithmetic logic unit (ALU) performs 4-bit addition, subtraction, logical, and shift-and-rotate operations in one instruction cycle and most 8-bit arithmetic and logical operations in two cycles.

CPU REGISTERS

Program Counter

A 14-bit program counter (PC) stores addresses for instruction fetches during program execution. Usually, the PC is incremented by the number of bytes of the fetched instruction. The one instruction fetch that does not increment the PC is the 1-byte REF instruction which references instructions stored in a look-up table in the ROM. Whenever a reset operation or an interrupt occurs, bits PC13 through PC0 are set to the vector address.

Stack Pointer

An 8-bit stack pointer (SP) stores addresses for stack operations. The stack area is located in general-purpose data memory bank 0. The SP is 8-bit read/writeable and SP bit 0 must always be logical zero.

During an interrupt or a subroutine call, the PC value and the PSW are written to the stack area. When the service routine has completed, the values referenced by the stack pointer are restored. Then, the next instruction is executed.

The stack pointer can access the stack despite data memory access enable flag status. Since the reset value of the stack pointer is not defined in firmware, you use program code to initialize the stack pointer to 00H. This sets the first register of the stack area to data memory location 0FFH.

PROGRAM MEMORY

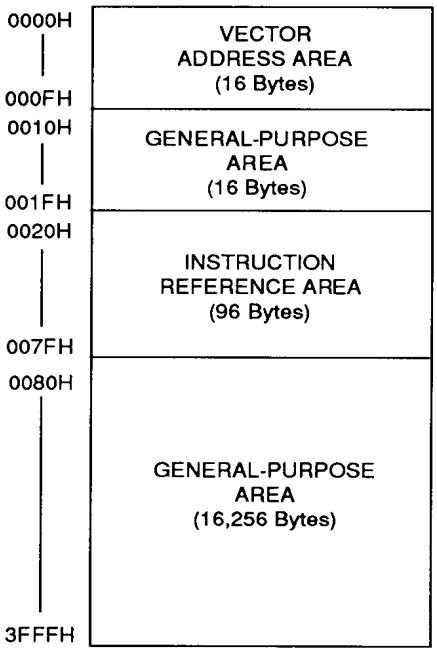
In its standard configuration, the 16,384 × 8-bit ROM is divided into four areas:

— 16-byte area for vector addresses

— 96-byte instruction reference area

— 16-byte general-purpose area (0010–001FH)

— 16,256-byte area for general-purpose program memory



Program Memory Map

The vector address area is used mostly during reset operations and interrupts. These 16 bytes can alternately be used as general-purpose ROM.

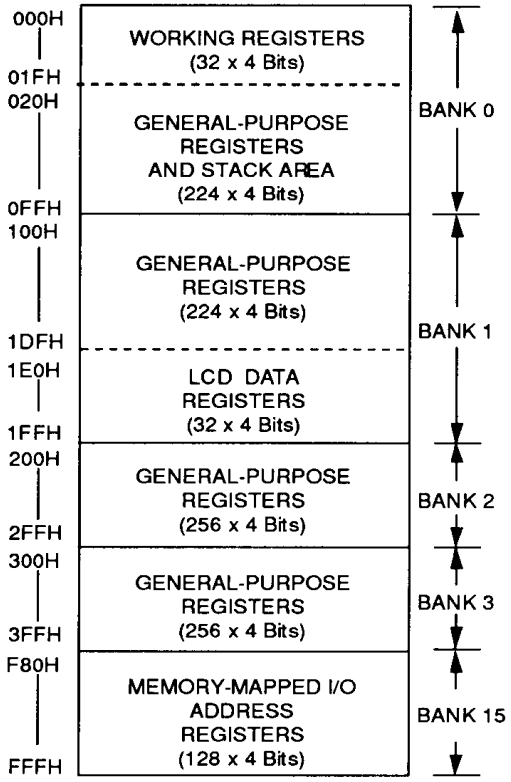
The REF instruction references 2 x 1-byte or 2-byte instructions stored in reference area locations 0020H–007FH. REF can also reference three-byte instructions such as JP or CALL. So that a REF instruction can reference these instructions, however, the JP or CALL must be shortened to a 2-byte format. To do this, JP or CALL is written to the reference area with the format TJP or TCALL instead of the normal instruction name. Unused locations in the REF instruction look-up area can be allocated to general-purpose use.

FUNCTIONAL DESCRIPTION

DATA MEMORY

The 1024 × 4 bit data memory has seven areas:

— 32 × 4-bit working register area
— 224 × 4-bit general-purpose area in bank 0 which is also used as the stack area
— 224 × 4-bit general-purpose area in bank 1
— 32 × 4-bit area for LCD data in bank 1
— 256 × 4-bit general-purpose area in bank 2
— 256 × 4-bit general-purpose area in bank 3
— 128 × 4-bit area in bank 15 for memory-mapped I/O addresses



Data Memory Map

The data memory area is also organized as five memory banks — bank 0, bank 1, bank 2, bank 3 and bank 15.

You use the select memory bank instruction (SMB) to select one of the banks as working data memory.

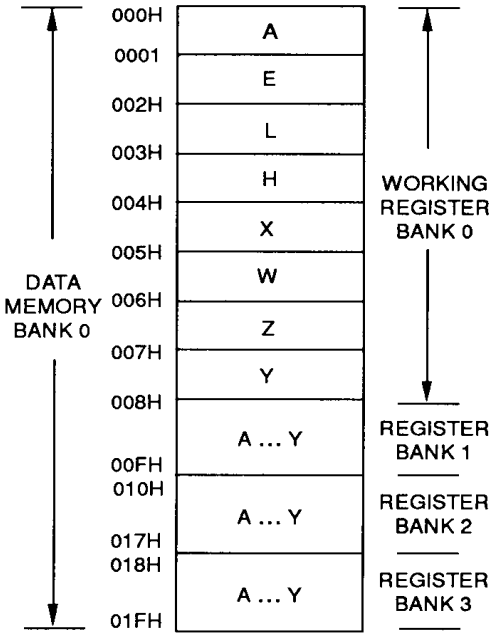
Data stored in RAM locations are 1-, 4-, and 8-bit addressable. An exception is the LCD data register area, which is 1-bit and 4-bit addressable only. After a hardware reset, data memory initialization values must be defined by program code.

Data Memory Addressing Modes

The enable memory bank (EMB) flag controls the addressing mode for data memory banks 0, 1, 2, 3 or 15. When the EMB flag is logical zero, only locations 00H–7FH of bank 0 and bank 15 can be accessed. When the EMB flag is set to logical one, all five data memory banks can be accessed based on the current SMB value.

Working Registers

The RAM's working register area in data memory bank 0 is also divided into four *register* banks. Each register bank has eight 4-bit registers. Paired 4-bit registers are 8-bit addressable.



Working Register Map

FUNCTIONAL DESCRIPTION

Register A can be used as a 4-bit accumulator and double register EA as an 8-bit extended accumulator; double registers WX, WL, and HL are used as address pointers for indirect addressing.

To limit the possibility of data corruption due to incorrect register addressing, it is advisable to use bank 0 for main programs and banks 1, 2, and 3 for interrupt service routines.

LCD Data Register Area

Bit values for LCD segment data are stored in data memory bank 1. Register locations that are not used to store LCD data can be assigned to general-purpose use.

Bit Sequential Carrier

The bit sequential carrier (BSC) is a 16-bit general register that you can manipulate using 1-, 4-, and 8-bit RAM control instructions. The BSC register is mapped to RAM addresses FC0H–FC3H.

Using the BSC register, addresses and bit locations can be specified sequentially using 1-bit indirect addressing instructions. In this way, a program can generate 16-bit data output by moving the bit location sequentially, incrementing or decrementing the value of the L register. You can also use direct addressing to manipulate data in the BSC.

CONTROL REGISTERS

Program Status Word

The 8-bit program status word (PSW) controls ALU operations and instruction execution sequencing. It is also used to restore a program's execution environment when an interrupt has been serviced. Program instructions can always address the PSW regardless of the current value of data memory access enable flags.

Before an interrupt is processed, the PSW is pushed onto the stack in data memory bank 0. When the routine is completed, PSW values are restored.

IS1	IS0	EMB	ERB
C	SC2	SC1	SC0

Interrupt status flags (IS1, IS0), the enable memory bank and enable register bank flags (EMB, ERB), and the carry flag (C) are 1- and 4-bit read/write or 8-bit read-only addressable. Skip condition flags (SC0–SC2) can be addressed using 8-bit read instructions only.

Select Bank (SB) Register

Two 4-bit locations called the SB register store address values used to access specific memory and register banks: the select memory bank register, SMB, and the select register bank register, SRB.

'SMB n' instructions select a data memory bank (0, 1, 2, 3 or 15) and store the upper four bits of the 12-bit data memory address in the SMB register. The 'SRB n' instruction is used to select register bank 0, 1, 2, or 3, and to store the address data in the SRB.

The instructions 'PUSH SB' and 'POP SB' move SMB and SRB values to and from the stack for interrupts and subroutines.

CLOCK CIRCUITS

Main system and subsystem oscillation circuits generate the internal clock signals for the CPU and peripheral hardware. The main system clock can use a crystal, ceramic, or RC oscillation source, or an externally-generated clock signal. The subsystem clock requires either a crystal oscillator or an external clock source.

Bit settings in the 4-bit power control and system clock mode registers select the oscillation source, the CPU clock, and the clock used during power-down mode. The internal system clock signal (fxx) can be divided internally to produce three CPU clock frequencies — fxx/4, fxx/8, or fxx/64.

The watch timer, buzzer frequency output, and LCD display operate when either the main system or subsystem clock is used. However, the basic timer, timer/ counters, and serial I/O interface must always be driven by the main system clock, since they require higher operating speeds.

INTERRUPTS

Interrupt requests may be generated internally by on-chip processes (INTB, INTT0, INTIF and INTS) or externally by peripheral devices (INT0, INT1, INTCE and INT4). There are two quasi-interrupts: INT2 and INTW.

INT2/KS0–KS3 detects rising/falling edges of incoming signals and INTW detects time intervals of 0.5 seconds or 3.91 milliseconds. The following components support interrupt processing:

- Interrupt enable flags
- Interrupt request flags
- Interrupt priority registers
- Power-down termination circuit

FUNCTIONAL DESCRIPTION

POWER-DOWN

To reduce power consumption, there are four power-down modes: idle, stop1, stop2 and CE low. Idle mode is initiated by the idle instruction, stop1 mode by the stop instruction, stop2 mode by setting SUBSTP register, and CE low mode by forcing CE pin to low state.

A power-down affects the main and the sub system clock: In idle mode, only the CPU clock stops while peripherals and the oscillation source continue to operate normally. Only the main system clock stops in stop1 mode, but the main and the sub system clock stop in stop2 mode. In addition, the PLL block is disabled in CE low mode. Idle or stop1 mode is terminated either by external $\overline{\text{RESET}}$ or by vectored interrupts. Stop2 mode, however, terminated by external $\overline{\text{RESET}}$ only.

$\overline{\text{RESET}}$

When a $\overline{\text{RESET}}$ signal occurs during normal operation or during power-down mode, the CPU enters idle mode when the reset operation is initiated. When the standard oscillation stabilization interval (29.1 ms at 4.5 MHz) has elapsed, normal CPU operation resumes.

I/O PORTS

The KS57C3016 has 14 ports. Pin addresses for all ports except ports 11–13 are mapped to bank 15 of the RAM. Ports 11–13 pin addresses are bank 1 of the RAM.

There are 4 input pins, 12 output pins, 23 configurable I/O pins, and 16 n-channel open-drain I/O pins, for a total of 55 pins. The contents of I/O port pin latches can be read, written, or tested at the corresponding address using bit manipulation instructions.

TIMERS and TIMER/COUNTER

The timer function has four main components: an 8-bit basic interval timer, an 8-bit timer/counter and a watch timer. The 8-bit basic timer generates interrupt requests at precise intervals, based on the selected CPU clock frequency.

The programmable 8-bit timer/counter is used for external event counting, generation of arbitrary clock frequencies for output, and dividing external clock signals. The 8-bit timer/counter is the source of the clock signal that is required to drive the serial I/O interface.

The watch timer has an 8-bit watch timer mode register, a clock selector, and a frequency divider circuit. Its functions include real-time and watch-time measurement, clock generation for the LCD controller, and frequency outputs for buzzer sound.

A/D CONVERTER

The KS57C3016's 8-bit resolution analog-to-digital converter is based successive approximation logic and has the following functional components:

- Digital-to-analog converter
- Comparator
- Analog data register
- A/D mode register
- Analog flag register

One of the four analog input channels (AD0–AD3) is selected by setting bits in the ADC mode register. The data conversion speed is controlled by the CPU clock frequency selection.

When a data conversion operation ends, an internal check is made to verify that the conversion was successful. Then, a flag is cleared automatically to logical zero.

The converted digital data stored in the ADC data register can be read at any time after performing a program check of the ADC flag status.

PLL FREQUENCY SYNTHESIZER

The PLL (Phase-Locked Loop) frequency synthesizer uses a phase difference comparison method to lock medium frequency, high frequency, and very high frequency signals to a fixed frequency. The PLL frequency synthesizer consists of an input selection circuit, programmable divider, phase detector, reference frequency generator, and a charge pump.

The PLL frequency synthesizer divides the frequency of a signal from the V_{COAM} or V_{COFM} pin using the programmable divider, and outputs the phase difference between the divided frequency and reference frequency through the charge pump at the EO1 and EO2 pins. Depending on the phase difference, EO1 and EO2 pin levels go high, low, or float.

The reference frequency generator produces the reference frequency that is compared with the divided frequency using a phase comparator. The PLMOD control register lets you enable or disable the PLL module, select reference frequencies, and select the V_{COAM} or V_{COFM} pin as for PLL input.

FUNCTIONAL DESCRIPTION

INTERMEDIATE FREQUENCY (IF) COUNTER

The intermediate frequency (IF) counter measures AM and FM intermediate frequency signals from an external IF control device. It consists of 16-bit binary counter, 1/2 divider for FMIF signals, and a gate control circuit. The input frequency at the FMIF or AMIF pin is measured by counting the number of signal pulses during the gate time. (There are four selectable gate times.) The gate signals are not synchronized with the internal system clock.

The FMIF signal is sent to the 16-bit IF counter through the 1/2 divider; the AMIF signal is sent directly to the IF counter with no division. The IFMOD control register selects an FMIF or AMIF signal source, and controls IF counter operation.

The counter starts when the IFMOD register is written, and continues counting until the gate closes. An interrupt is generated when the IF counter overflows. The IF counter gate flag can be checked by software to determine when a count operation has completed.

PULSE WIDTH MODULATION (PWM) OUTPUTS

Six PWM output channels with 8-bit resolution are used to output pulses of programmable length. The PWM module consists of six data registers, an 8-bit counter, six comparators, and two delay circuits. The value of the 8-bit counter is compared to the contents of the reference register, PWMREF. When the count value matches that of the PWM reference register, the PWM output goes low. When the counter overflows, the PWM output is forced high.

The pulse width ratio (duty cycle) is defined by the reference register value and is programmed in increments of 1/256. The PWM output can be held continuously low by loading the reference register with 00H and continuously high (except for the 255th clock pulse) by loading the reference register with FFH. The PWM mode register PWMOD contains the PWM module's enable bit.

N-channel, open-drain I/O ports 7 and 8 are alternately used as PWM output pins. Pull-up resistors can be configured by mask option. The PWM module includes output delay logic for noise reduction. The system clock (fx) divided by two is used as the counter input clock. A reset disables the PWM module.

LCD DRIVER/CONTROLLER

The KS57C3016 can directly drive an up-to-16-digit LCD panel. The LCD function block has the following components:

- RAM area for storing display data
- 32 segment output pins (SEG0–SEG31)
- 4 common output pins (COM0–COM3)
- 3 operating power supply pins (V_{LC0}–V_{LC2})
- BIAS pin for the driver and bias voltage

Frame frequency, LCD clock, duty and bias, and segment pins used for display output are controlled by bit settings in the 8-bit mode register, LMOD. You use the 4-bit LCD control register, LCON, to turn the LCD display on and off, and to control current supplied to the dividing resistors. Segment data are output using a direct memory access method synchronized with the LCD frame frequency (f_{LCD}).

Using the main system clock, the LCD panel operates in idle mode; during stop mode, it is turned off. If a subsystem clock is used as a clock source, the LCD panel will continue to operate during stop and idle modes.

SERIAL I/O INTERFACE

The serial I/O interface supports the transmission or reception of 8-bit serial data with an external device. The serial interface has the following functional components:

- 8-bit mode register
- Clock selector circuit
- 8-bit buffer register
- 3-bit serial clock counter

The serial I/O circuit can be set either to transmit-and-receive or to receive-only mode. MSB-first or LSB-first transmission is also selectable. The serial interface operates with an internal or an external clock source, or using the clock signal generated by the 8-bit timer/counter. To modify transmission frequency, the appropriate bits in the serial I/O mode register (SMOD) must be manipulated.

INSTRUCTION SET

ADDRESSING MODES

Direct Addressing

Data memory locations can be addressed directly by 1-bit and 4-bit instructions using a specific register or bit address as the instruction's operand.

Double registers are directly addressable by 8-bit instructions.

Indirect Addressing

Indirect addressing specifies a memory location that contains the required direct address.

The SAM4 instruction set supports both 4-bit and 8-bit indirect addressing.

For 8-bit indirect addressing, an even-numbered RAM address must always be used as the instruction operand.

Bit Manipulation

To facilitate program control of I/O, bit manipulation instructions can be used to flexibly address specific bit locations in data memory independently of the enable memory bank (EMB) and select memory bank (SMB) values.

REGISTER ADDRESSING

Registers	
4-bit accumulator	A
4-bit working registers	E, L, H, X, W, Z, Y
8-bit extended accumulator	EA
8-bit memory pointer	HL
8-bit working registers	WX, YZ, WL
Select register bank 'n'	SRB n
Select memory bank 'n'	SMB n
Carry flag	C
Program status word	PSW
Port 'n'	P n
'm'-th bit of port 'n'	P n.m
Interrupt priority register	IPR
Enable memory bank flag	EMB
Enable register bank flag	ERB

INSTRUCTION SUMMARY

Data Transfer Instructions

Name	Operation
XCH	Exchange A and data memory contents Exchange A and register (Ra) contents Exchange A and indirect data memory Exchange EA and direct data memory contents Exchange EA and register pair (RRb) contents Exchange EA and indirect data memory contents
XCHI	Exchange A and data memory contents; increment contents of register L and skip on carry
XCHD	Exchange A and data memory contents; decrement contents of register L and skip on carry
LD	Load 4-bit immediate data to A Load indirect data memory contents to A Load direct data memory contents to A Load register contents to A Load 4-bit immediate data to register Load 8-bit immediate data to register Load contents of A to direct data memory Load contents of A to register Load indirect data memory contents to EA Load direct data memory contents to EA Load register contents to EA Load contents of A to indirect data memory Load contents of EA to data memory Load contents of EA to register Load contents of EA to indirect data memory
LDI	Load indirect data memory to A; increment register L contents and skip on carry
LDD	Load indirect data memory contents to A; decrement register L contents and skip on carry

INSTRUCTION SET

Data Transfer Instructions (Continued)

Name	Operation
LDC	Load code byte from WX to EA Load code byte from EA to EA
RRC	Rotate right through carry bit
PUSH	Push register pair onto stack Push SMB and SRB values onto stack
POP	Pop to register pair from stack Pop SMB and SRB values from stack

Input/Output Instructions

Name	Operation
LD	Input I/O port n value to A Input I/O port n value to EA Output A to I/O port n Output EA to I/O port n

Program Control Instructions

Name	Operation
CPSE	Compare and skip if register equals #im Compare and skip if indirect data memory equals #im Compare and skip if A equals R Compare and skip if A equals indirect data memory Compare and skip if EA equals indirect data memory Compare and skip if EA equals RR
JP	Jump to direct address (14 bits)
JPS	Jump direct in page (12 bits)
JR	Jump to immediate address Branch relative to WX register Branch relative to contents of EA
CALL	Call direct in page (14 bits)
CALLS	Call direct in page (11 bits)
RET	Return from subroutine
IRET	Return from interrupt
SRET	Return from subroutine and skip

Logic Instructions

Name	Operation
AND	Logical-AND A immediate data to A Logical-AND A indirect data memory to A Logical-AND register pair (RR) to EA Logical-AND EA to register pair (RRb)
OR	Logical-OR immediate data to A Logical-OR indirect data memory contents to A Logical-OR double register to EA Logical-OR EA to double register
XOR	Exclusive-OR immediate data to A Exclusive-OR indirect data memory to A Exclusive-OR register pair (RR) to EA Exclusive-OR register pair (RRb) to EA
COM	Complement accumulator (A)

Arithmetic Instructions

Name	Operation
ADC	Add indirect data memory to A with carry Add register pair (RR) to EA with carry Add EA to register pair (RRb) with carry
ADS	Add 4-bit immediate data to A and skip on carry Add 8-bit immediate data to EA and skip on carry Add indirect data memory to A and skip on carry Add register pair (RR) contents to EA and skip on carry Add EA to register pair (RRb) and skip on carry
SBC	Subtract indirect data memory from A with carry Subtract register pair (RR) from EA with carry Subtract EA from register pair (RRb) with carry
SBS	Subtract indirect data memory from A; skip on borrow Subtract register pair (RR) from EA; skip on borrow

INSTRUCTION SET

Arithmetic Instructions

Name	Operation
SBS	Subtract EA from register pair (RRb); skip on borrow
DECS	Decrement register (R); skip on borrow Decrement register pair (RR); skip on borrow
INCS	Increment register (R); skip on carry Increment direct data memory; skip on carry Increment indirect data memory; skip on carry Increment register pair (RRb); skip on carry

CPU Control Instructions

Name	Operation
SCF	Set carry flag
RCF	Reset carry flag
CCF	Complement carry flag
EI	Enable all interrupts
DI	Disable all interrupts
IDLE	Engage CPU idle mode
STOP	Engage CPU stop mode
NOP	No operation
SMB	Select memory bank
SRB	Select register bank
REF	Reference code
VENTn	Load enable memory bank flag (EMB), enable register bank flag (ERB), and program counter to vector address and branch to the corresponding location

Bit Manipulation Instructions

Name	Operation
BTST	Test specified bit and skip if carry flag is set Test specified bit and skip if memory bit is set
BTSF	Test specified memory bit and skip if bit equals "0"
BTSTZ	Test specified bit; skip and clear if memory bit is set

Bit Manipulation Instructions (Continued)

Name	Operation
BITS	Set specified memory bit
BITR	Clear specified memory bit to logic zero
BAND	Logical-AND carry flag with memory bit
BOR	Logical-OR carry with specified memory bit
BXOR	Exclusive-OR carry with memory bit
LDB	Load carry bit to a specified memory bit Load carry bit to a specified indirect memory bit Load a specified memory bit to carry bit Load a specified indirect memory bit to carry bit

DEVELOPMENT SUPPORT

The Samsung Microcontroller Development System provides you with a complete PC-based development environment for the KS57C3016 microcontroller that is powerful, reliable, and portable.

In addition to its window-based program development structure, the SMDS toolset includes versatile debugging, trace, instruction timing, and performance measurement applications.

The Samsung Generalized Assembler (SAMA) has been designed specifically for the SMDS environment and accepts assembly language sources in a variety of microprocessor formats.

SAMA generates industry-standard hex files that also contain program control data for SMDS compatibility.

ORDERING INFORMATION

Answers to technical questions about this device can be obtained directly by calling a member of the MICOM Application Development Team at Ki-Heung, Korea: (02): 760-7970~77, or by faxing your inquiries to us at (02) 236-1454.

If you have questions about documentation for this product, you can contact the MICOM Documentation Team at Ki-Heung, Korea by calling (02) 760-7982, or by fax at (02) 236-1454.

To order additional copies of this document, or to ask about other available documentation, please call the MICOM Sales Team in Seoul. The telephone numbers are (02) 727-7593~8.