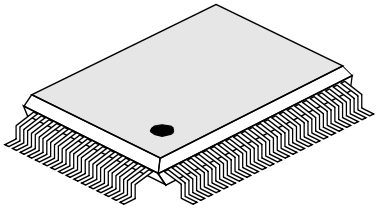
KS0127 Data Sheet

MULTISTANDARD VIDEO DECODER/SCALER

The KS0127 converts analog NTSC, PAL or SECAM video in composite, S-video, or component format to digitized component video. Output data can be selected for CCIR 601 or square pixel sample rates in either YCbCr or RGB formats. The digital video can be scaled down in both the horizontal and vertical directions. The KS0127 also decodes Intercast, Teletext, Closed Caption, and SMPTE data with a built-in bit data slicer. Digitized CVBS data can be output directly during VBI for external processing.

100 PQFP



FEATURES

- **Accepts NTSC-M/N/4.43, PAL-M/N/B/G/H/I/D/K/L and SECAM formats with auto detection**
- **6 analog inputs: 3 S-video, 6 composite, or 1 3-wire YCbCr component video**
- **2-line luma and chroma comb filters including adaptive luma comb for NTSC**
- **Programmable luma bandwidth, contrast, brightness, and edge enhancement**
- **Programmable chroma bandwidth, hue, and saturation**
- **High quality horizontal and vertical down scaler**
- **Intercast, Teletext and Closed Caption decoding with built-in bit slicer**
- **Direct output of digitized CVBS during VBI for Intercast application**
- **Analog square pixel or CCIR 601 sample rates**
- **Output in 4:4:4, 4:2:2, or 4:1:1 YCbCr component, or 24-bit or 16-bit RGB formats with dithering**
- **YCbCr 4:2:2 output can be 8 or 16 bits wide with embedded timing reference code support for 8-bit mode**
- **Simultaneous scaled and non scaled digital output ports outputs for 8-bit mode.**
- **Direct access to scaler via bi-directional digital port.**
- **Programmable Gamma correction table**
- **Programmable timing signals**
- **Industry standard 2 wire serial interface**

ORDERING INFORMATION

Device	Package	Temperature Range
KS0127	100 PQFP	0°~+70°C

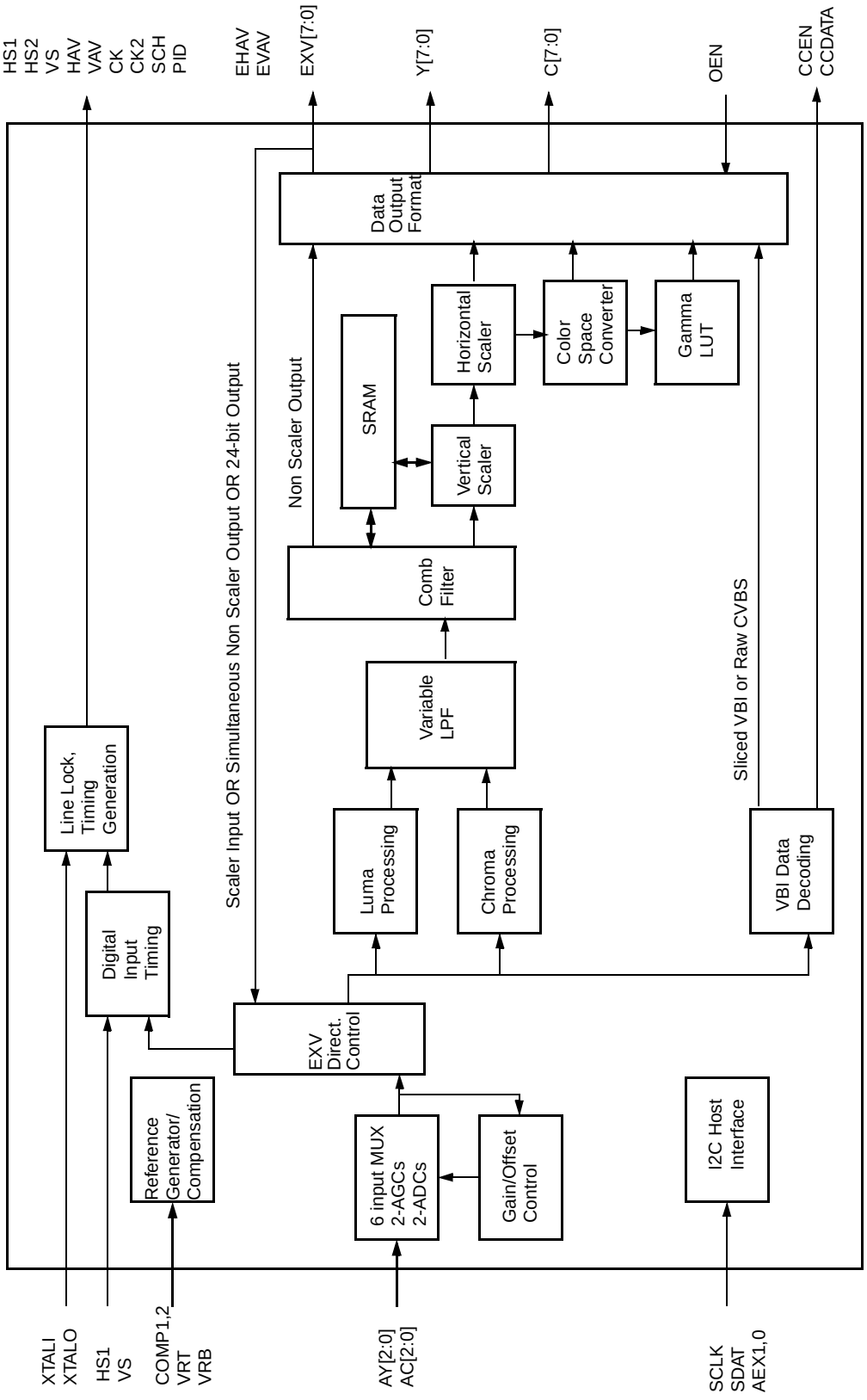
APPLICATIONS

- **Multimedia**
- **Digital Video**
- **Video Capture/Editing**

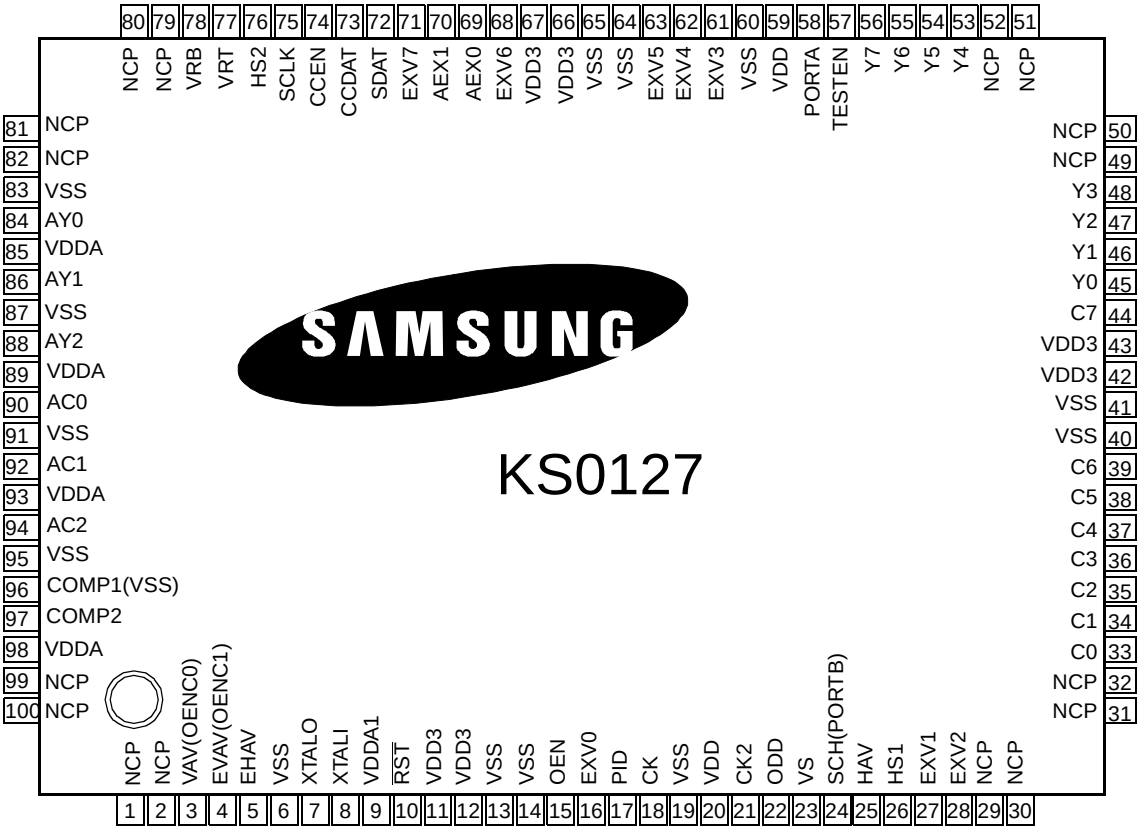
RELATED PRODUCTS

- **KS0119 NTSC VIDEO ENCODER**
- **KS0123 MULTISTANDARD VIDEO ENCODER**
- **KS0125 MULTISTANDARD VIDEO ENCODER**
- **KS0122 MULTISTANDARD VIDEO DECODER**

BLOCK DIAGRAM



PIN ASSIGNMENT - 100 PQFP



PIN DESCRIPTION

Pin Name	Pin #	Type	Description
INPUT			
AY0	84	I	1 of 6 analog CVBS or 1of 3 S-video Y inputs.
AY1	86	I	1 of 6 analog CVBS or 1of 3 S-video Y inputs.
AY2	88	I	1 of 6 analog CVBS input or 1 of 3 S-video Y inputs or Y input for 3 wire component input
AC0	90	I	1 of 6 analog CVBS or 1 of 3 S-video C inputs.
AC1	92	I	1 of 6 analog CVBS or 1 of 3 S-video C inputs or Cb input for 3 wire component input
AC2	94	I	1 of 6 analog CVBS or 1 of 3 S-video C inputs or Cr input for 3 wire component input
XTALI	8	I	Pin 1 for external crystal or TTL clock input.
XTALO	7	O	Pin 2 for external crystal.
$\overline{\text{RST}}$	10	I	Chip reset. Active low signal.
OUTPUT (All output pins can be selectively three-stated)			
C0 - C7, Y0 - Y7	45-48,53-56,33-39,44	O	Digital video outputs.
EXV0 - EXV7	16,27,28,61-63, 68,71	I/O	Expanded digital video I/O port. Can be configured as an additional 8-bit output port (no scaling), or additional outputs of the main digital output stream for 24 bit output modes, or as a 8-bit input for direct digital access of the down scaler
HS1	26	I/O	Programmable horizontal timing signal. One pulse every video line. When the EXV port is configured as an input, this pin can be programmed as an input.
HS2	76	O	Programmable horizontal timing signal. One pulse every video line.
VS	23	I/O	Programmable vertical timing signal. When the EXV port is configured as an input, this pin can be programmed as an input.
HAV	25	O	Programmable horizontal active video flag.
VAV(OENC0)	3	I/O	Programmable vertical active video flag. During reset, the pin is an input and the logic state of this pin is latched into the **OENC**[0] register bit. Use a 10 kΩ resistor for pull-up or pull-down.
EHAV	5	O	Valid pixel data flag. Polarity is programmable. Active when output video data is valid.

PIN DESCRIPTION (Continued)

Pin Name	Pin #	Type	Description
EVAV(OENC1)	4	I/O	Valid line flag. Polarity is programmable. Active when output video line is valid. During reset, the pin is an input and the logic state of this pin is latched into the **OENC**[1]register bit. Use a 10 kΩ resistor for pull-up or pull-down.
ODD	22	O	Odd field flag. Polarity is programmable. Active for fields 1 and 3.
PID	17	O	PAL ID flag. High for phase alternating line.
OEN	15	I	Digital video data, timing and clock output 3-state control.
CK	18	I/O	Pixel clock. In normal decoding mode, this is an output. When the EXV port is used as an input, this can be programmed as an input. pixel clock.
CK2	21	O	Pixel output clock (rate is one half of CK) aligned to HAV signal.
CCDAT	73	O	Sliced VBI data output. Data can be from Closed Caption, Teletext, Intercast, or SMPT type encoded data.
CCEN	74	O	When high, this pin indicates that valid VBI data is being clocked out at the CCDAT pin or at the digital video output.
MULTI-PURPOSE I/O PORTS AND TEST ENABLE			
PORTA	58	I/O	Multi-purpose I/O port.
SCH(PORTB)	24	I/O	Multi-purpose I/O port.
TESTEN	57	I	When tied to VDD, the chip is put into the test mode. For normal use, this pin should be connected to VSS.
REFERENCE AND COMPENSATION			
VRT	77	I/O	ADC VRT compensation (requires an external 0.1 µF capacitor connected to VSS).
VRB	78	I/O	ADC VRB compensation (requires an external 0.1 µF capacitor connected to VSS).
COMP2	97	I/O	Internal 1.3 V reference (requires an external 0.1 µF capacitor connected to VSS).
COMP1(VSS)	96	I/O	A connection to this pin is not required. Internally this pin is connected to VSS.
HOST INTERFACE			
SCLK	75	I	Serial clock for I2C host interface.
SDAT	72	I/O	Serial data for I2C host interface.
AEX0 - AEX1	69 - 70	I	Device ID selection for for I2C host interface.

PIN DESCRIPTION (Continued)

Pin Name	Pin #	Type	Description
POWER AND GROUND			
VDD	20,59	+5V	Digital power supply for output buffers.
VDD3	11,12,42,43,66, 67	+3.3V	Digital power supply for internal logic.
VDDA	85,89,93,98	+5V	Analog power supply for ADC, AGC and reference circuits.
VDDA1	9	+5V	Analog power supply for clock generation circuitry.
VSS	6,13,14,19,40, 41,60,64,65,83, 87,91,95	GND	Common ground.
NC			
NCP	1,2,29-32,49-52, 79-82,99,100	-	These pins are directly connected to the die substrate. If electrical connect is desired (not required) only connection to VSS is allowed.

PIN CROSS REFERENCE: NUMERICAL ORDER BY PIN NUMBER

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
1	NCP	26	HS1	51	NCP	76	HS2
2	NCP	27	EXV1	52	NCP	77	VRT
3	VAV(OENC0)	28	EXV2	53	Y4	78	VRB
4	EVAV(OENC1)	29	NCP	54	Y5	79	NCP
5	EHAV	30	NCP	55	Y6	80	NCP
6	VSS	31	NCP	56	Y7	81	NCP
7	XTALO	32	NCP	57	TESTEN	82	NCP
8	XTALI	33	C0	58	PORTA	83	VSS
9	VDDA1	34	C1	59	VDD	84	AY0
10	$\overline{\text{RST}}$	35	C2	60	VSS	85	VDDA
11	VDD3	36	C3	61	EXV3	86	AY1
12	VDD3	37	C4	62	EXV4	87	VSS
13	VSS	38	C5	63	EXV5	88	AY2
14	VSS	39	C6	64	VSS	89	VDDA
15	OEN	40	VSS	65	VSS	90	AC0
16	EXV0	41	VSS	66	VDD3	91	VSS
17	PID	42	VDD3	67	VDD3	92	AC1
18	CK	43	VDD3	68	EXV6	93	VDDA
19	VSS	44	C7	69	AEX0	94	AC2
20	VDD	45	Y0	70	AEX1	95	VSS
21	CK2	46	Y1	71	EXV7	96	COMP1(VSS)
22	ODD	47	Y2	72	SDAT	97	COMP2
23	VS	48	Y3	73	CCDAT	98	VDDA
24	SCH(PORTB)	49	NCP	74	CCEN	99	NCP
25	HAV	50	NCP	75	SCLK	100	NCP

1. FUNCTIONAL DESCRIPTION

1.1. VIDEO INPUT

The KS0127 supports complete video decoding of many analog video standards. In addition, the chip can support direct 8-bit YCbCr input for high quality video scaling and other processing.

1.1.1. Analog Video Input

Figure 1 shows the detailed block diagram of the analog front end. Up to six composite video sources, three S-video sources, one 3-wire YCbCr component video source, or any combination can be selected. The allowed inputs are selected using the **INSEL[3:0]** bits in the **CMDB** register. Table 1 lists all possible input selections. The front end has two paths each containing an analog gain control, a clamping control, and an 8-bit ADC. Composite video input uses only the luma path. S-video and analog component YCbCr inputs utilize both the luma and chroma paths. The ADC digital data is used to calculate the correct gain and clamp values. The data is fed back to the analog clamping and gain control. This architecture eliminates any offset and gain mismatch in the analog front end.

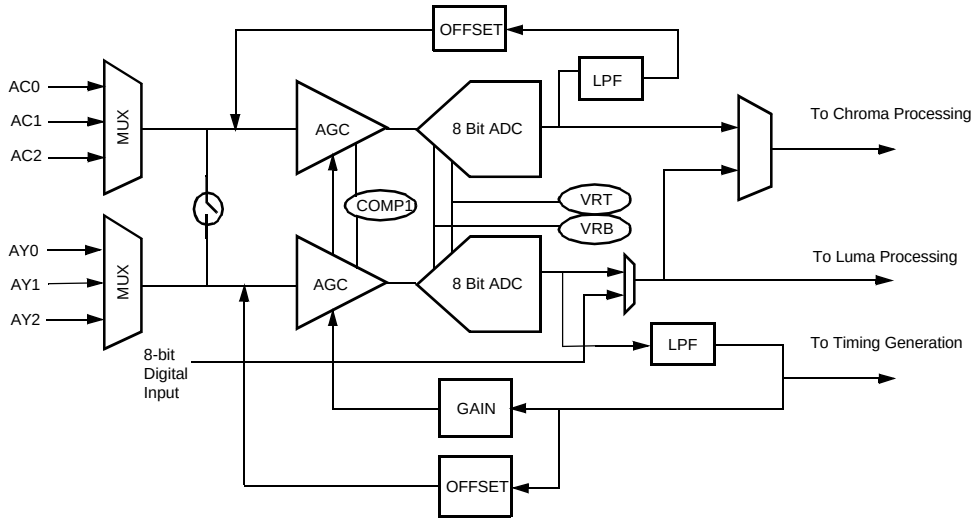


Figure 1. Analog Front End

The analog inputs must be AC coupled through an external 0.1 µF capacitor. Due to the high sampling rate of the ADC′s inside the KS0127, most video sources will not require a low-pass filter for alias reduction. For those video sources with harmonics above 13 MHz, a simple single order pole at 6 MHz will provide sufficient high frequency signal reduction. This can be implemented with a 400 pf capacitor in parallel with the 75 Ω load.

Figure 2. Typical Analog Video Input

Table 1: Analog Video Input selections

INSEL[3:0](hex)	Selected Input(s)	Video Type
0	AY0	Composite
1	AY1	Composite
2	AY2	Composite
4	AC0	Composite
5	AC1	Composite
6	AC2	Composite
8	AY0, AC0	S-Video
9	AY1, AC1	S-Video
A	AY2, AC2	S-Video
F	AY2(Y), AC1(Cb), AC2(Cr)	YCbCr component video

1.1.2. Digital AGC Control

The AGC normally references to the ADC code difference between sync tip and back porch. Two sets of sync tip-back porch ADC values are available for different AGC gain requirements: if **AGCGN** = 0, the sync tip locks to code 2, and the back porch locks to code 70; when **AGCGN** = 1, the sync tip locks to 16, and the back porch locks to code 70. Video signal with abnormal sync tip or very bright saturated colors may cause the ADC to limit the maximum value. This situation can be corrected by enabling the **AGCOVF** bit in the **CMDB** register to force the gain tracking loop to reduce AGC when maximum limiting conditions occur. The AGC may also be programmed to freeze the AGC at the current value by setting the **AGCFRZ** bit in the **CMDB** register. Once the AGC is frozen, the gain can be manually adjusted with the **AGC** register.

1.1.3. Digital Video Input

The high quality digital video down scaler in the KS0127 can be directly accessed via the EXV bi-directional port. The KS0127 accepts CCIR 656 compliant 8-bit YCbCr digital video input with embedded or external timing. Video timing may also be generated by the KS0127. Data path for 8-bit YCbCr input is shown in Figure 3. Selection of analog video input or digital CCIR 656 data is with the **INPSL[1:0]** register bits. The KS0127 can operate in master or slave timing mode when the chip is programmed for digital video input.

1.1.4. Pixel Clock and Timing Mode Selection for Digital Video Input

Pixel clock and synchronization timing can be individually selected to either come from an external generator or be generated internally. In addition, if synchronization is provided by an external source, the KS0127 supports embedded syncs as defined in CCIR 656, or TTL HS and VS inputs. Selection of pixel clock is via **CKDIR** bit in **CMDD** register. Timing selection is through either **SYNDIR** or **EAV** bit.

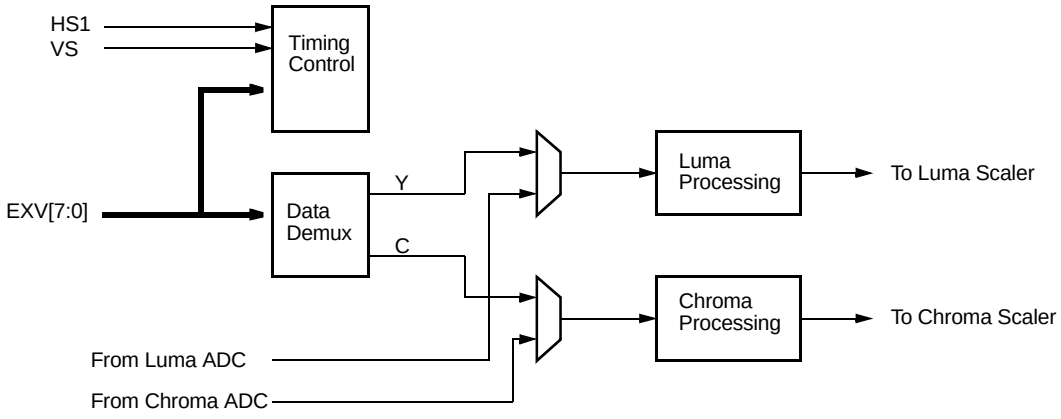


Figure 3. 8-bit YCbCr Input Data Path

By using an external pixel clock, the reference clock input at XTALI is no longer required. Additional register bits have to be programmed for different selections of pixel clock and timing, which are detailed in Table 2. The following register/bit-settings are required for digital video input:
INSEL[3:0] = 8, 9, A, or F.
TSTCGN = 1.
DMCTL[1:0] = 2 or 3.
UGAIN = 238.
BRT = 34.
SAT = 229.
RGB = **UNIT** = **PED** = 1.

Table 2: Digital Video Input Pixel Clock and Timing Selection

Pixel Clock	TTL Timing	Embedded Timing	Additional Register Programming						
CKDIR[*1]	**SYNDIR**[*2]	**EAV**[*3]	**VMEN**	**TSTPH**	**TSTGEN**	**TSTGFR**	**PIXSEL**	**MNFMT**	**IFMT**
0	0	0	1	0	1	3	0 if input data is at square pixel rate. 1 if input is at CCIR 601 rate.	1	0 if input is 50 Hz video. 1 if input is 60 Hz video.
0	0	1	0	1	1	3		1	
0	1	0	0	1	1	1		1	
1	0	0	1	0	1	3		1	
1	0	1	0	1	1	1		1	
1	1	0	0	1	1	1		1	

[*1]: **CKDIR** = 0 - CK is output and is internally generated. **CKDIR** = 1 - CK is input from an external source.
[*2]: **SYNDIR** = 0 - HS1 and VS are output. **SYNDIR** = 1 - HS1 and VS are inputs from external sources.
[*3]: **EAV** = 0 - chip will not sync to embedded timing. **EAV** = 1 - chip will sync to embedded timing.
Note: the combination X11 for **CKDIR**, **SYNDIR**, **EAV** is not valid.

When in digital input mode, all programmable timing registers are still functional except for HS1 and VS when they are inputs. An example of horizontal timing for digital input is shown in Figure 4.

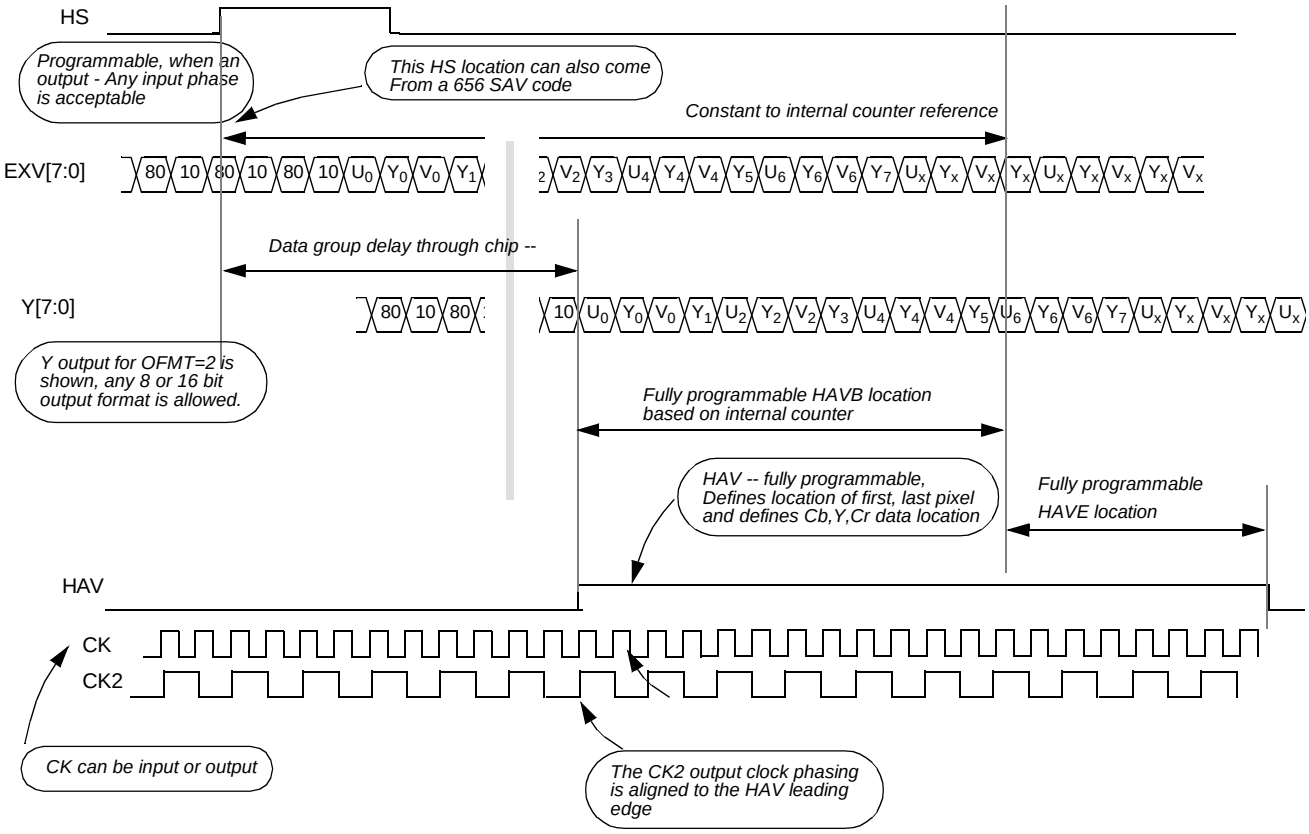


Figure 4. Horizontal Timing for EXV Port as Digital Input

1.2. VIDEO TRACKING AND TIMING GENERATION

When the KS0127 is configured for analog video input, the chip tracks the video input and generates a sampling clock that is line locked to the input video. The KS0127 requires an external reference clock for video tracking. This reference can be supplied via a crystal using the on chip crystal interface or any TTL compatible source. These configurations are shown in Figure 5

1.2.1. Clock Input Timing Reference

The KS0127 can use either a 24.576 MHz or a 26.8 MHz reference. However, it is recommended that the 24.576 MHz reference be used for CCIR 601 operation, and the 26.8 MHz reference be used for square pixel or dual mode operation. Other specifications for the crystal are:

- Fundamental or third overtone
- Load capacitance of ~20 pF
- Series resonance resistance of 40 Ω or less
- Frequency deviation of 50 ppm or less

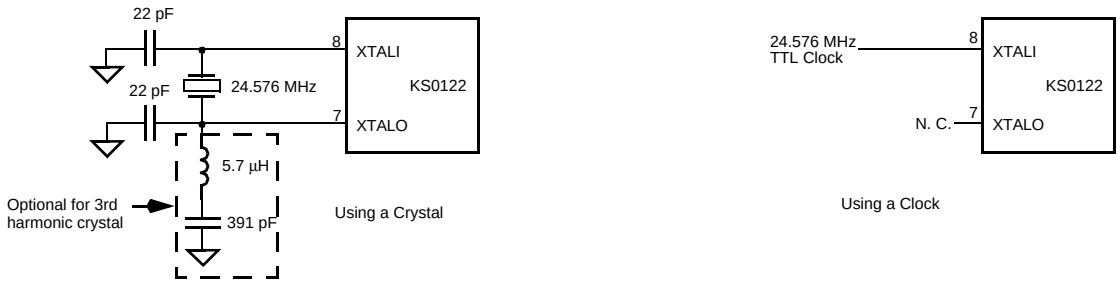


Figure 5. Standard Clock Configurations

1.2.2. THe Sampling Clock

The sampling clock is generated by multiplying the line rate by N. This ensures that samples are aligned horizontally, vertically and in time. The required N factor for the KS0127 is based upon the field rate (60 Hz or 50 Hz) and the desired sampling rates (CCIR 601 or square pixel). Field rate can be automatically detected and can be monitored with the **FFRDET** bit in the **STAT** register. Manual control of the field rate can be controlled with the **MNFMT** and **IFMT** bits. The **PIXSEL** bit in register **CMDD** selects CCIR 601 or square pixel. Table 3 shows the constants for the various combinations of input formats and output pixel rates.

Table 3: Timing for Different Pixel Rates

	CCIR 601 Data Rates		Square Pixel Data Rates		Units
	M	N,B,G,H,I,D,K,K1,L	M	N,B,G,H,I,D,K,K1,L	
Field Rate	60	50	60	50	Hz
Pixels/Line (N)	858	864	780	944	Pixels
Active Pixels/Line	720	720	640	768	Pixels
Active Lines/Frame	480	580	480	580	Lines
Pixel Rate	13.5	13.5	12.27	14.75	MHz
ADC Sampling Rate	27	27	24.54	29.5	MHz

The time constants for the pixel clock tracking loop can be adjusted with the **HFSEL**[1:0] bits.

In addition to providing the pixel clock, the KS0127 also outputs various timing signals to indicate the beginning of a line, a field, and for field and frame identification. All the timing and clock pins may be optionally put into high impedance state. Three-state of these pins are software controlled and initial state of these pins at power up is controlled via two configuration pins (3 and 4).

The KS0127 can generate all the video timing without video input. This enables the KS0127 to be used as a video timing generator for a system that contains both the KS0127 for live video input and a MPEG decoder which requires a video timing generator.

1.2.3. Horizontal Timing

The KS0127 creates many internal timing signals aligned to the horizontal sync tip (mid-way of the falling edge of horizontal sync, typically ADC code 36). These include locations of color burst (CBG, CBGW) used in chrominance

processing, back porch (BPG), and sync tip timing signals (SLICE, FS_PULSE) used for AGC and clamp functions. SLICE is high whenever the input is below half way level of horizontal sync (typically ADC code 36). FS_PULSE is a single clock pulse coincide with the start of SLICE. One of these internal signals can be made available at the PORTA or PORTB pin at any time.

The chip outputs two horizontal synchronization signals: HS1 and HS2**.** The start and stop locations for these signals are fully programmable. Offset programmed to HSXB, HSXE, and HSXBE0 are added to the default edge locations as shown in Table 4. Note that there are different modulo numbers for different input video standards and output pixel rates.

An additional signal, HAV, is provided for horizontal video cropping. This signal has programmable polarity, start and stop locations. Two 11-bit registers, **HAVB** and **HAVE**, are used to define the first and last pixel locations of the horizontal portion of the cropped video. Numbers programmed into these registers are used as offset to the default locations as shown in Table 4.

Table 4 shows the default edge locations relative to the midway of the falling edge of the analog horizontal sync. Note the numbers shown are in multiple of CK clocks. Figure 6 shows the approximate locations for the horizontal timing signals.

Table 4: Horizontal Timing Signal Edge Locations (in # of CK)

Description	Signal	60 Hz		50 Hz	
		CCIR 601 (modulo 1716)	Square Pixel (modulo 1560)	CCIR 601 (modulo 1728)	Square Pixel (modulo 1888)
Chip delay		120	120	120	120
Sync gate (1-CK pulse)	SYG	72	72	72	72
Back porch gate	BPG	[147 222]	[129 204]	[154 234]	[168 254]
Color burst gate (1-CK pulse)	CBG	222	204	234	254
Wide color burst gate	CBGW	[159 254]	[147 233]	[173 254]	[186 277]
Two pulses per line (1-CK each pulse)	FH2	42, 900	42, 822	42, 906	42, 986
Default one pulse per line	HS1	[65 238]	[45 220]	[69 250]	[65 270]
Default one pulse per line	HS2	[65 238]	[45 220]	[69 250]	[65 270]
Default horizontal cropping	HAV	[351 75]	[334 58]	[379 91]	[415 59]

Horizontal timing signal used for scaling will be discribed in Section 1.6.1.

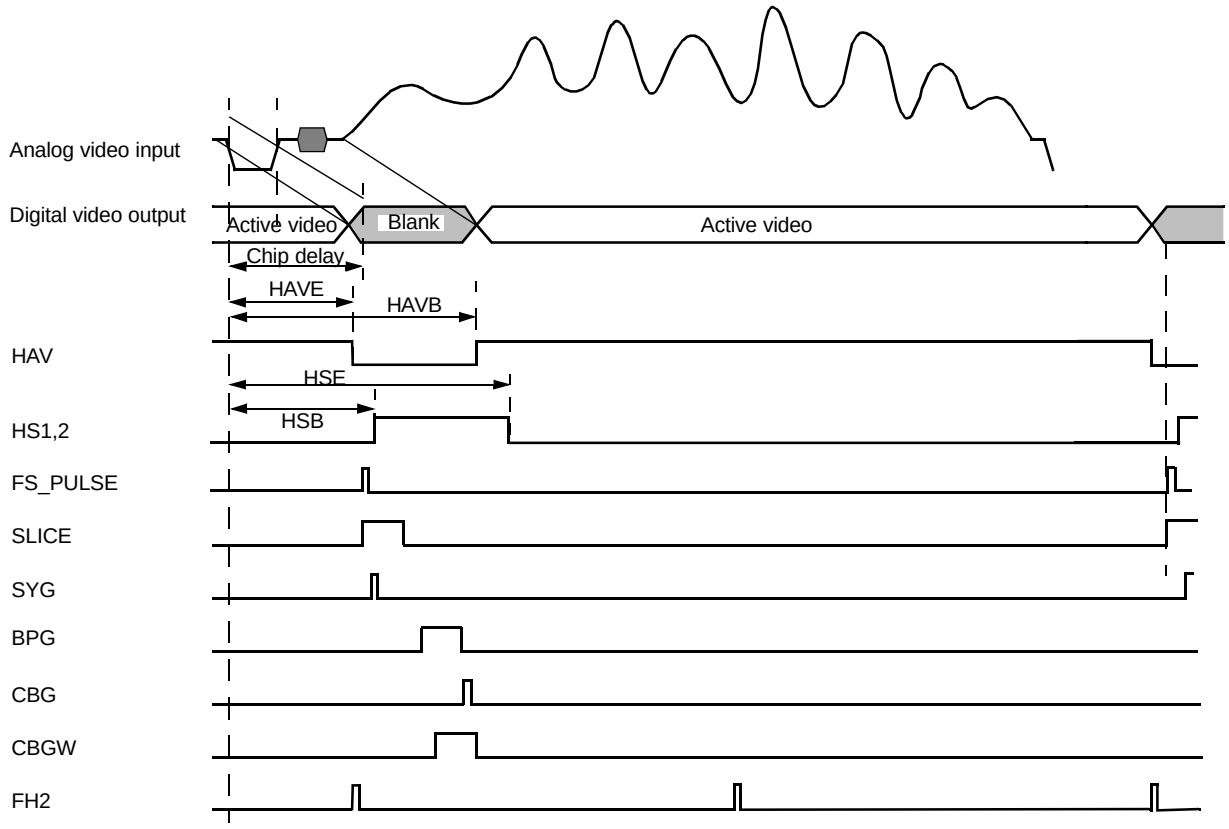


Figure 6. Approximate Locations for the Horizontal Timing Signals

1.2.4. Vertical Timing

The vertical timing signals include VS, VAV, ODD, SCH, and PID.

The VS is used for identifying the first line of video in the vertical position. The VS leading edge can be programmed to either track the incoming video's serration pulses or to be aligned to the beginning of the video line or half way, as shown in Figure 7 and Figure 8. If **VALIGN** = 0, the VS leading edge is based on an internal low pass filter, and its location is dependent on the noise conditions of the video input. The trailing edge of VS is locked to either the beginning of the video line or half way. The half way location relative to the beginning of the video line changes depending on current input standard and output format. If **VALIGN** = 1, the leading edge of the VS is aligned to the beginning of the video line or half way. The trailing edge is always aligned to the beginning of the video line. The **VSE** bit in the **CMDA** register can be programmed to shorten the VS falling edge by one horizontal line.

The VAV signal is used for vertical cropping. The start and stop lines for VAV are programmable through the **VAVB** and **VAVE** registers.

The ODD signal signifies the current field number. When ODD is active, the current field is 1 or 3 (or 5 or 7 if in PAL mode). The leading and trailing edges of ODD can be aligned to either the leading edge of VS (**VALIGN** = 1) or the trailing edge of VS (**VALIGN** = 0). The signal may be used in conjunction with SCH and PID to exactly identify the current field. To distinguish between fields 1, 2 verse fields 3, 4 (or fields 1, 2, 3, 4 verse fields 5, 6, 7, 8 for PAL) the phase of the color burst relative to the sync tip must be measured. That information is provided by the SCH pin.

The KS0127 provides the output of a comparator that measures whether the current color burst phase relative to the falling edge of the sync is greater or less than a predetermined constant. This constant is controlled with **SCHCMP[3:0]**. The polarity of the SCH output pin depends on the current **SCHCMP[3:0]** value. The SCH signal changes every video line. The SCH for line 260 is held for the entire vertical blanking period. By using the SCH signal for the same line from each field, proper field identification can be determined. Figure 10 shows field identification values for **SCHCMP[3:0]**=0. It is important to note that the SCH value is only valid for video signals that have a constant sync tip to color burst relationship. This is not the case with consumer VCRs.

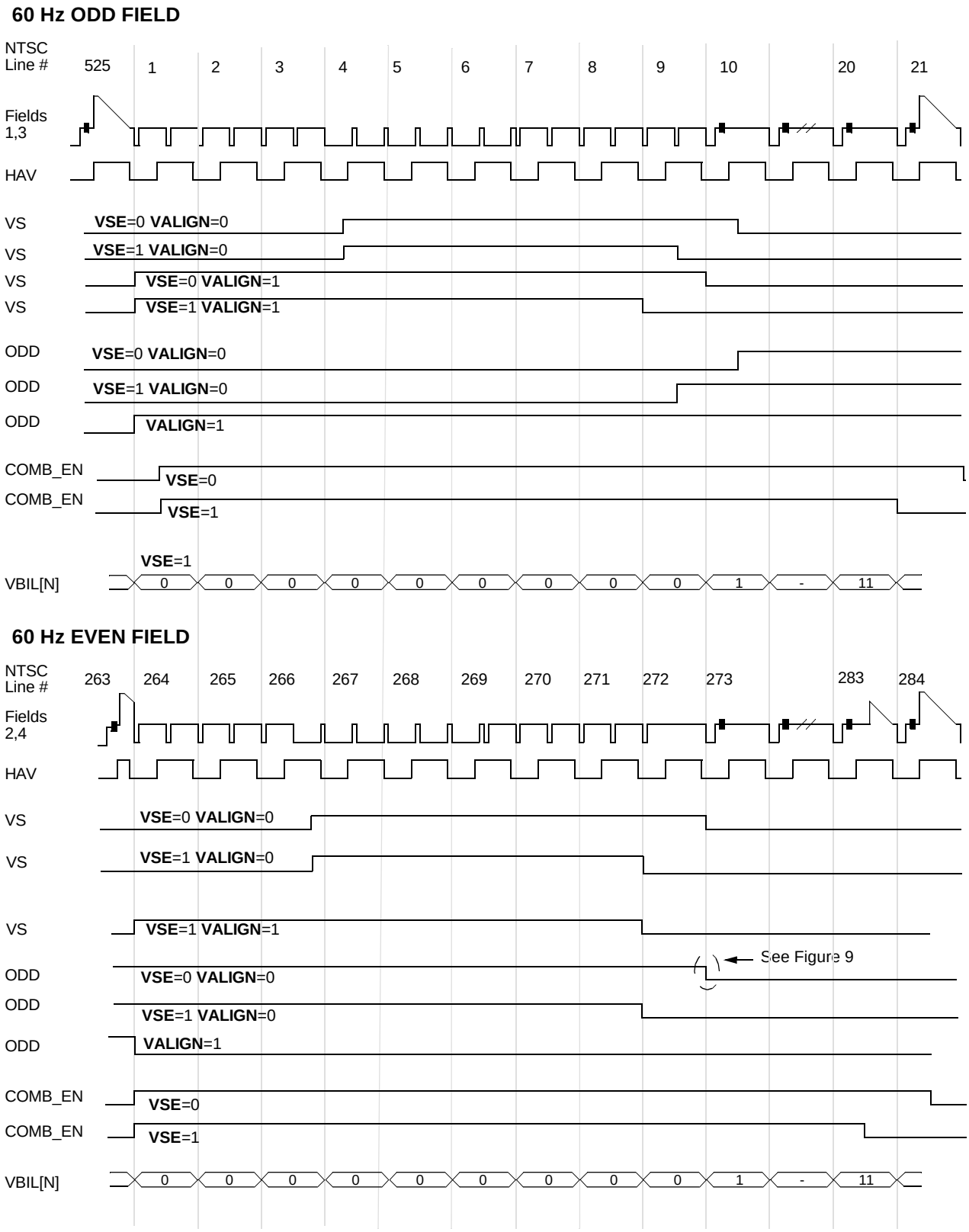


Figure 7. Vertical Timing for 60 Hz Video

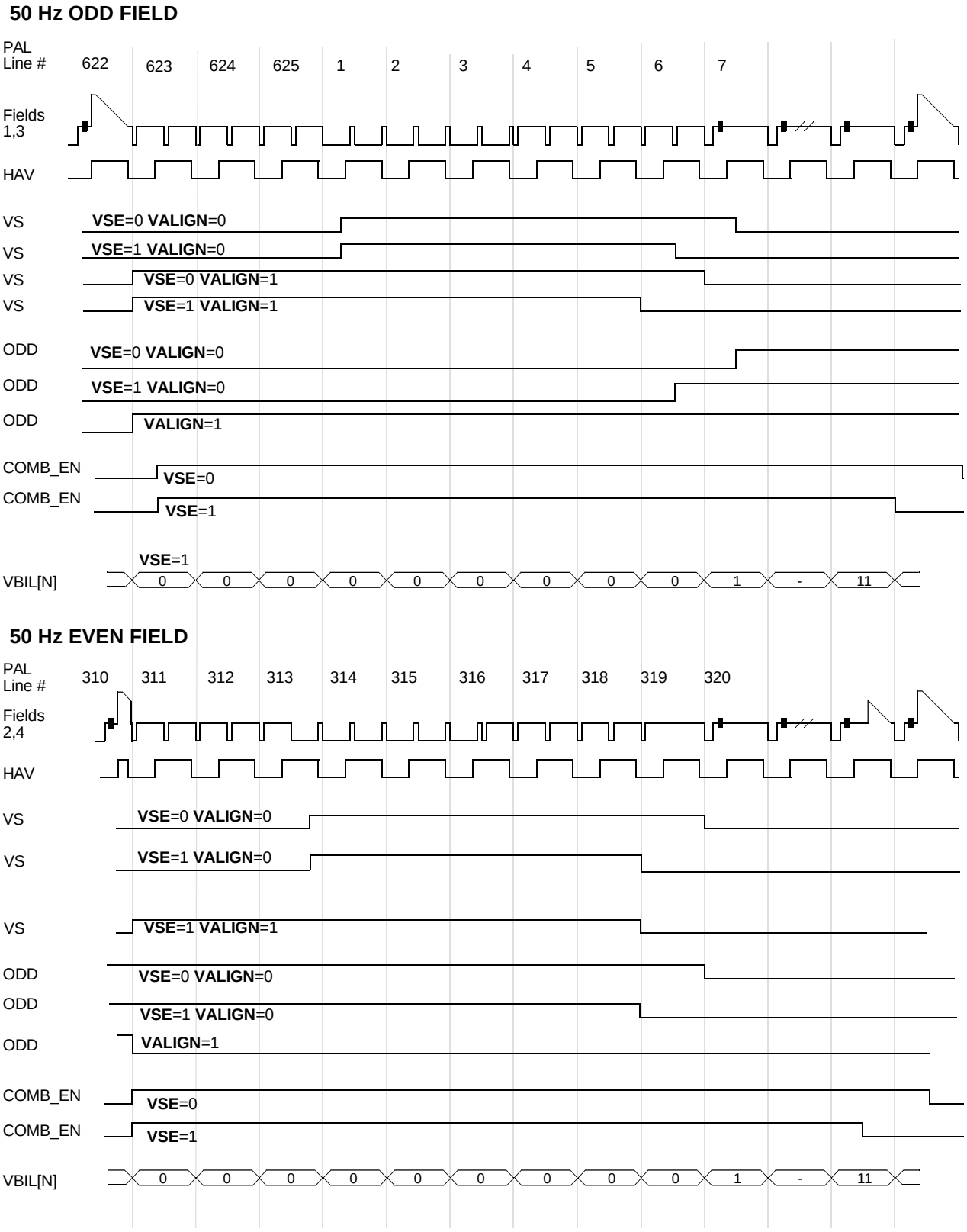
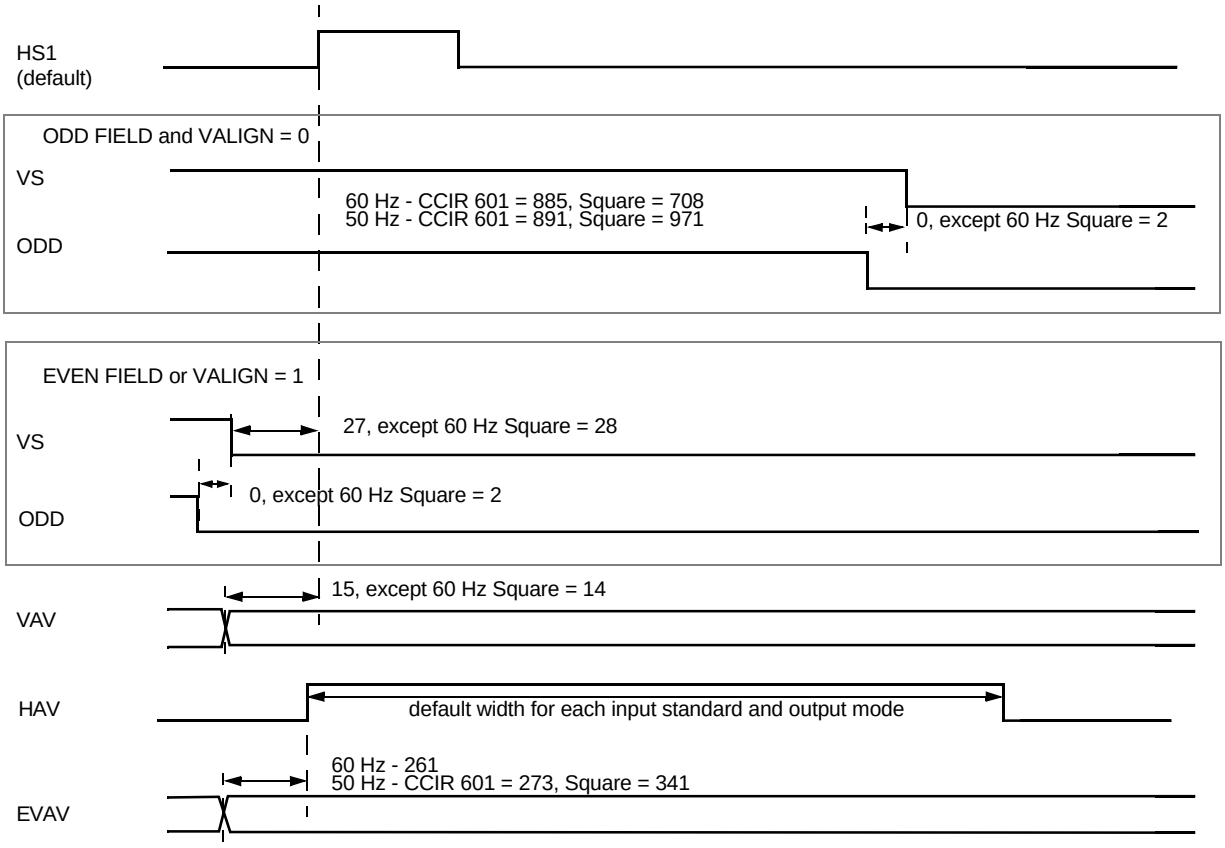


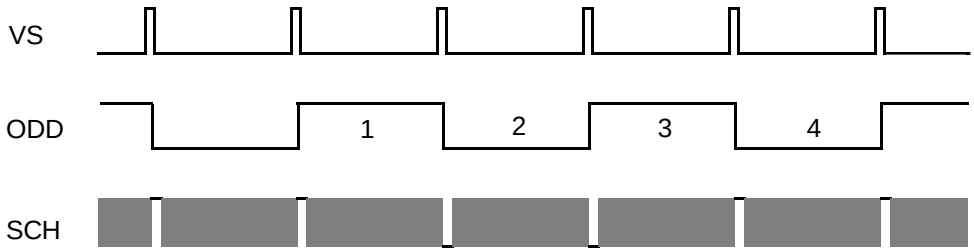
Figure 8. Vertical Timing for 50 Hz Video

.



Note: Numbers shown are in CK. Active high polarities are used. Timing shown for VAV and EVAV are with qualifier off.

Figure 9. Short Term Vertical Timing



Truth Table

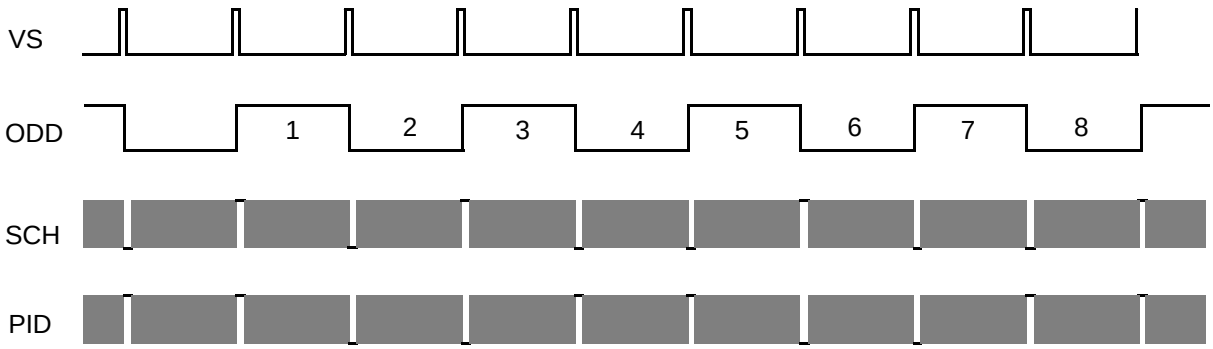
FIELD	1	2	3	4
ODD	H	L	H	L
SCH	H	L	L	H

Note:
ODD and SCH are measured at the trailing edge of VS.

Figure 10. NTSC Vertical Timing Signals

The PID pin is used to identify whether the current V-axis is inverted in PAL mode. This signal changes at the color burst. By noting this value at the same line of each field, a determination of whether a field is from {1-4} or {5-8} can be made. As with the SCH pin, the KS0127 is designed to hold the line 260 PID measurement for the entire vertical blank period. This allows easy sampling of the PID or current field identification.

The ODD, SCH and PID signals change at different times and more than once within the video fields. Proper data for field identification is determined by latching all three signals at the trailing edge of VS. Figure 11 shows the VS, ODD, SCH, and PID signals and their latched values for each of the 8 possible fields. Figure 12 is the line to line timing diagram for these signals in PAL mode.



Truth Table

FIELD	1	2	3	4	5	6	7	8
ODD	H	L	H	L	H	L	H	L
SCH	H	L	H	L	L	H	L	L
PID	H	L	L	H	H	L	L	H

Note:
ODD, SCH and PID are measured at the trailing edge of VS (**VALIGN** = 0).

Figure 11. PAL Vertical Timing Signals

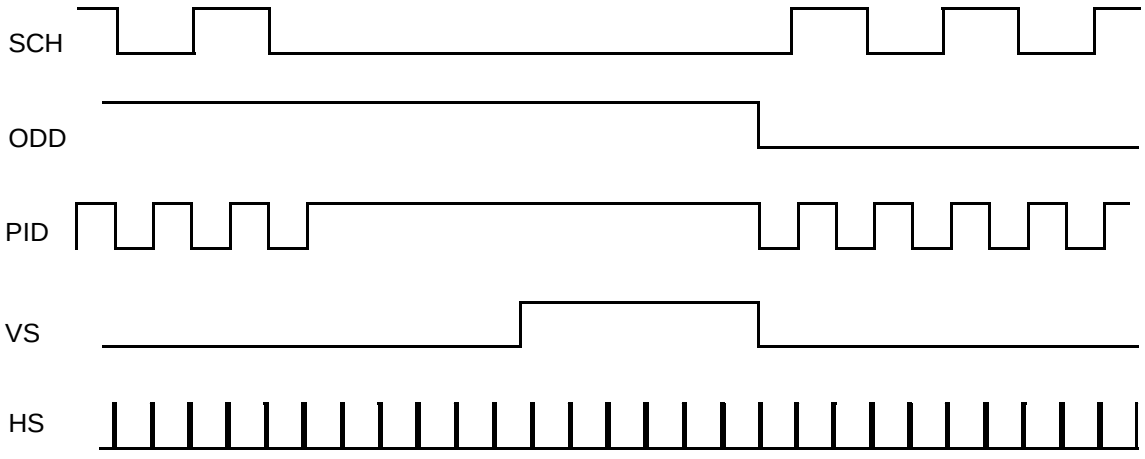


Figure 12. Line to Line VS, SCH and PID Timing (PAL input)

1.3. HORIZONTAL LUMA PROCESSING

A simplified block diagram for the luma path is shown in Figure 13.

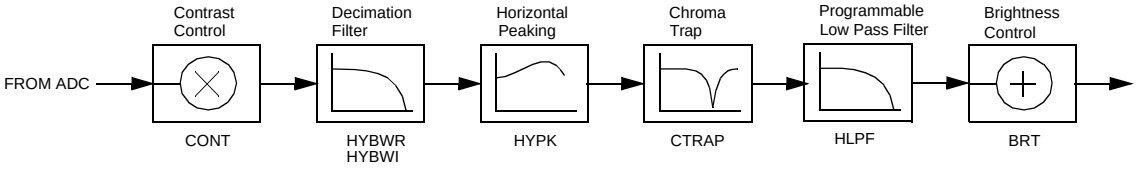


Figure 13. Horizontal Luma Processing Unit

1.3.1. Luminance DC Gain

The KS0127 can accommodate CCIR 624 M/N/H/G standards, which fall into categories of -40 or -43 sync tip and inclusion or exclusion of 7.5 setup. The KS0127 can produce correct CCIR 601 luminance output levels by controlling the gain and offset in the luminance path via **PED**. This register should be set for the appropriate input standard. The programmable **CONT** and **BRT** registers provide the user with additional flexibility to create non-standard luminance gain and offset values.

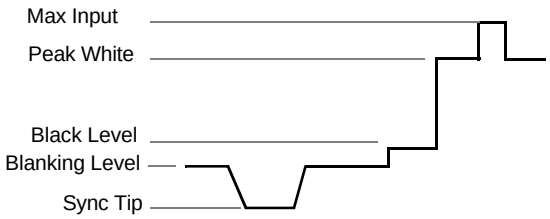


Figure 14. Luminance Signal

Luminance levels produced by the KS0127 for different broadcast standards (assuming **AGCGN**=0, **CONT**=0 and **BRT**=0) are summarized in Table 5.

Table 5: Luminance Digital Level Code

Signal	M/N PED=1			M/N PED=0			B/G/H PED=1		
	Level (IRE)	ADC (CVBS)	Y[7:0]	Level (IRE)	ADC (CVBS)	Y[7:0]	Level (IRE)	ADC (CVBS)	Y[7:0]
Max Input	109	255	255	109	255	255	117	255	255
Peak White	100	240	235	100	240	235	100	229	235
Black	7.5	83	16	0	70	16	0	70	16
Blank	0	70	1	0	70	16	0	70	
Sync	-40	2	1	-40	2	1	-43	2	
KS0127 Data Path Equation	$C_Y = 1.37CVBS - 100$			$C_Y = 1.288CVBS - 74$			$C_Y = 1.37CVBS - 80$		

When digital component output is desired in RGB mode, the **RGBH** register can be programmed to increase the 0-100% values from standard CCIR 601 levels to full range levels.The gain variations are shown in Table 6.

Table 6: RGB Output Range

	RGB normal gain (RGBH=0)		RGB high gain (RGBH=1)	
Signal	Cy	RGB (U,V=0)	Cy	RGB (U,V=0)
Peak White	235	235	255	255
Black	16	16	0	0

For CCIR 601 digital video input (**INPSL[1:0]** = 1), register **UNIT** must be set to 1 to produce unit gain.

1.3.2. Horizontal Luma Frequency Shaping

The luma path contains many programmable filters for different purposes. The combination of these filters will give different frequency characteristics.

The over sampled video data from the ADC pass through a decimation filter. The decimation filter has user programmable bandwidth. Three registers are used to control the decimation filter characteristics and each is designed for certain purposes. The **HYBWI**, when set to "1", provides extra bandwidth for very high quality video source. The **HYBWR**, when set to "1", reduces the bandwidth so high frequency noise can be eliminated. The 3-bit register **HYLPF[2:0]** provides the necessary bandwidth reduction for horizontal scaling. When all three registers are programmed to "0", the decimation filter has the bandwidth of the normal video. The KS0127 provides the option of bypassing the decimation filter. This option should be used only when the input video is band limited and with low high frequency noise.

For composite video input, the notch filter can be enabled (**CTRAP** set to "1") to extract the luminance. The notch filter has different center frequencies for different input video format. User selectable peaking function is included for edge enhancement. The notch filter should be bypassed for S-video and component video input, or if luma comb filter is enabled.

The luminance filter characteristics have been designed to be very similar for all combinations of 60/50 Hz video and CCIR 601/square pixel sampling rates. Figure 15 and Figure 16 show the output characteristics of the luminance path with different filter combinations for the supported input standards and output pixel rates.

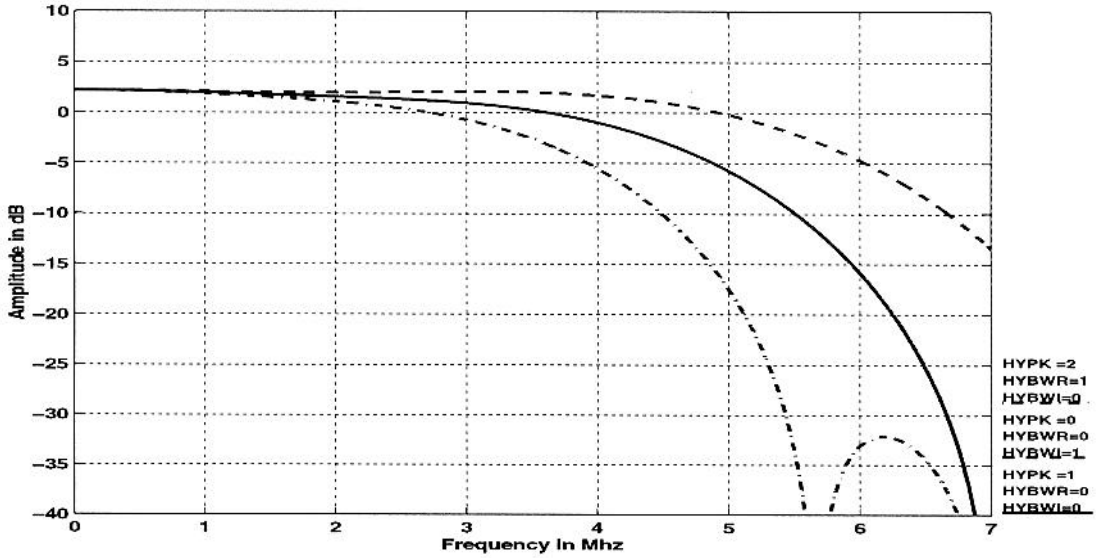


Figure 15. Medium to High Frequency Luma Filter Characteristics (CTRAP=0)

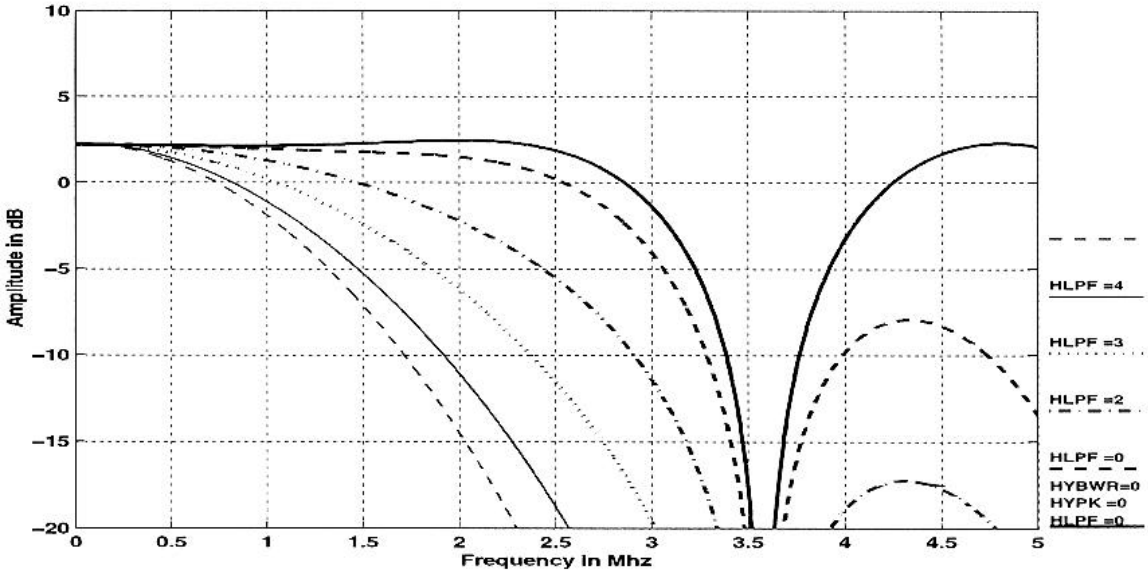


Figure 16. Medium to Low Frequency Luma Filter Characteristics (NTSC, CTRAP=1)

Figure 17. Medium to Low Frequency Luma Filter Characteristic (PAL, CTRAP=1)

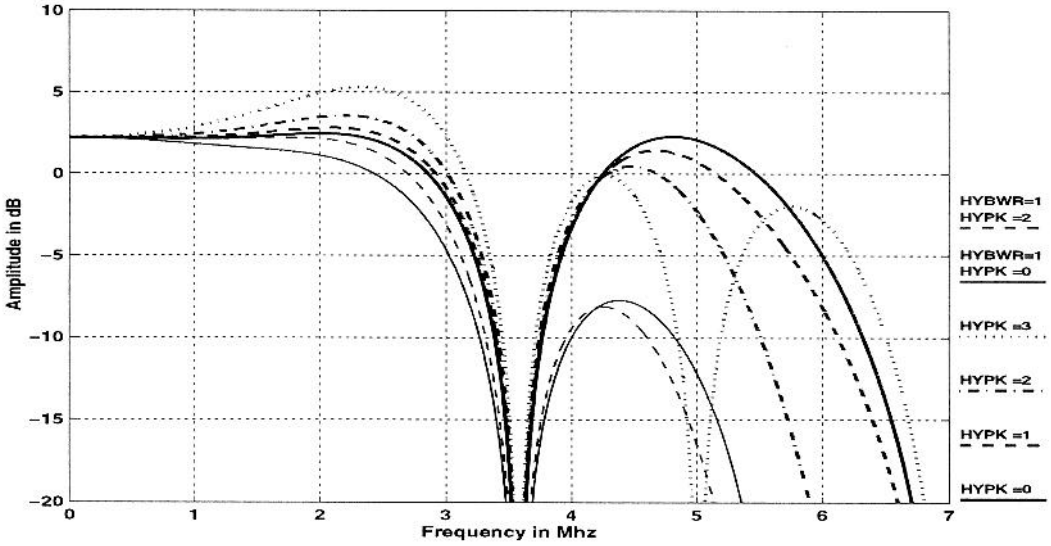


Figure 18. Luma Filter Characteristic with Peaking On (NTSC, CTRAP=1)

1.4. Horizontal Chroma Processing

A simplified block diagram for the horizontal chroma processing unit is shown in Figure 19.

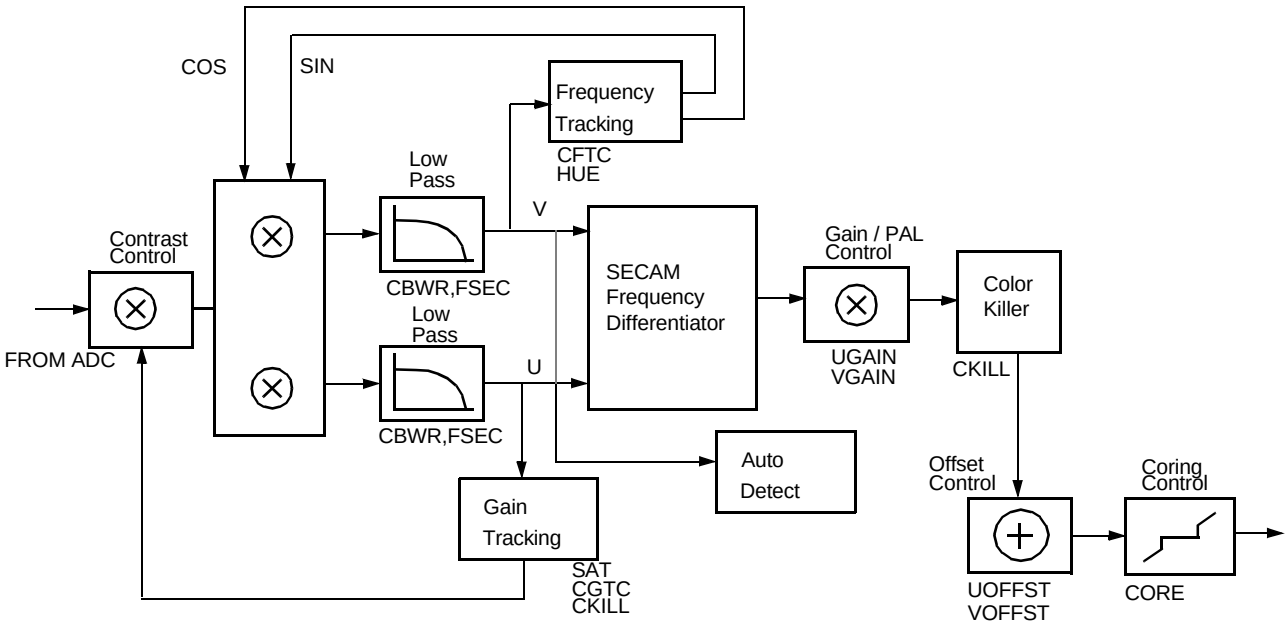


Figure 19. Horizontal Chroma Processing Unit

The KS0127 supports chroma input in NTSC, PAL, SECAM and component formats. The color standard is automatically detected and the various chroma processing blocks are enabled as required for the given chroma standard. Details of the various chroma processing blocks follow.

1.4.1. IF Compensation

For improved chroma demodulation when the input video is from a mis-tuned IF source, an IF compensation filter is included that has variable gain for the upper chroma side band. This is controlled by the **CIFCMP**[1:0] bits at location **CHROMA**. The frequency response is shown in Figure 20. For convenience, all plots are normalized to the NTSC modulation frequency.

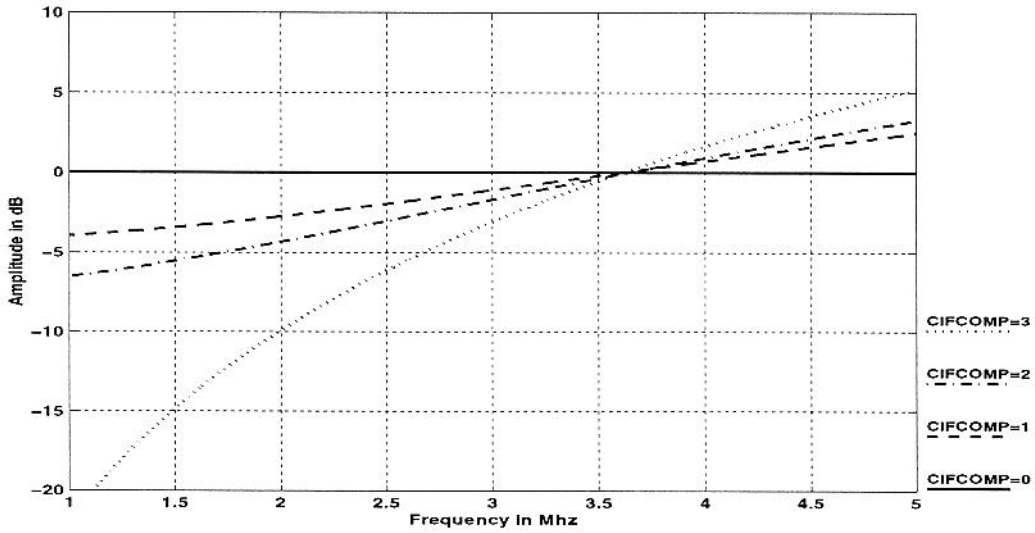


Figure 20. Chroma IF Compensation Frequency Response

1.4.2. Demodulation Gain

The demodulation gain block is controlled by feedback from the gain tracking block. For NTSC and PAL type inputs, the gain constant is derived from a programmable reference compared against the U component of the input video. This reference is controlled by the **SAT** register. The default value "0" is the correct gain (saturation for nominal output). For SECAM type input, the feedback is calculated such that proper frequency demodulation is obtained. When external calibration is desired, the gain feed back loop can be "opened" be setting **TSTCGN**=1. The **SAT** then controls bits 8 through 1 of a 10 bit multiplier.

For standard auto tracking applications, it is recommended that the **SAT** register be used as an end customer saturation control. This register is 2's compliment

1.4.3. Demodulation Low Pass Filter

The demodulation circuit also contains a programmable low pass filter and a coring function for noise reduction. The chroma low pass filter frequency response for the demodulation circuit for the various video standards are shown in Figure 21

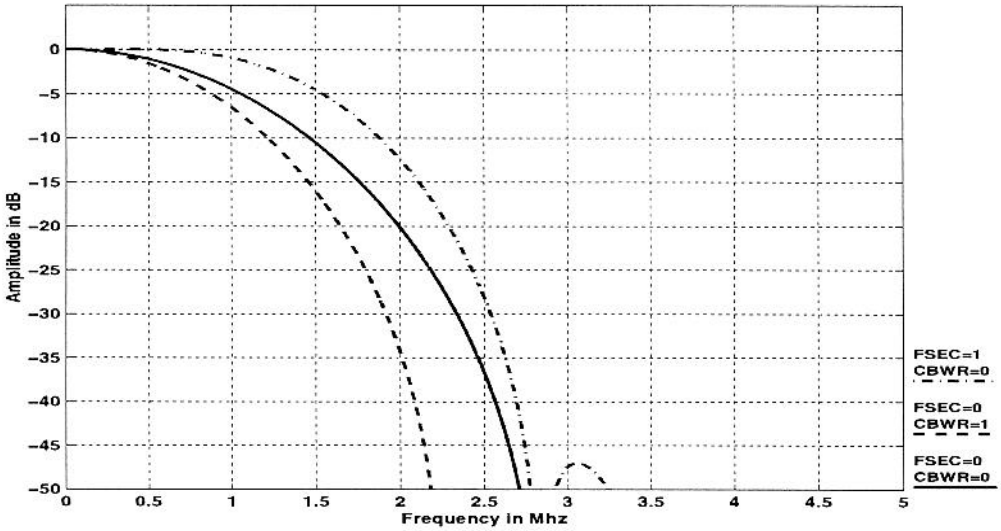


Figure 21. Chroma Low Pass Filter Frequency Response

1.4.4. SECAM Demodulation

SECAM processing includes a frequency differentiator, a Cloche and a de-emphasis filter. Frequency response for the filters are shown in Figure 22 and Figure 23.

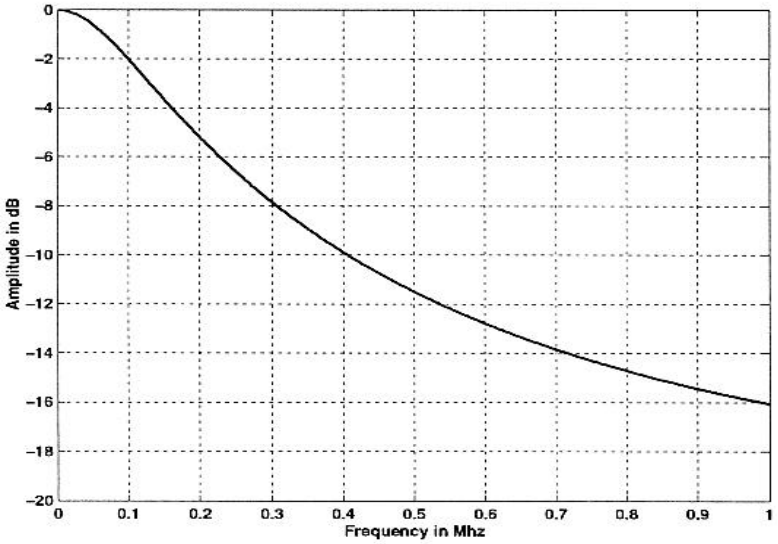


Figure 22. Cloche Filter Frequency Characteristic

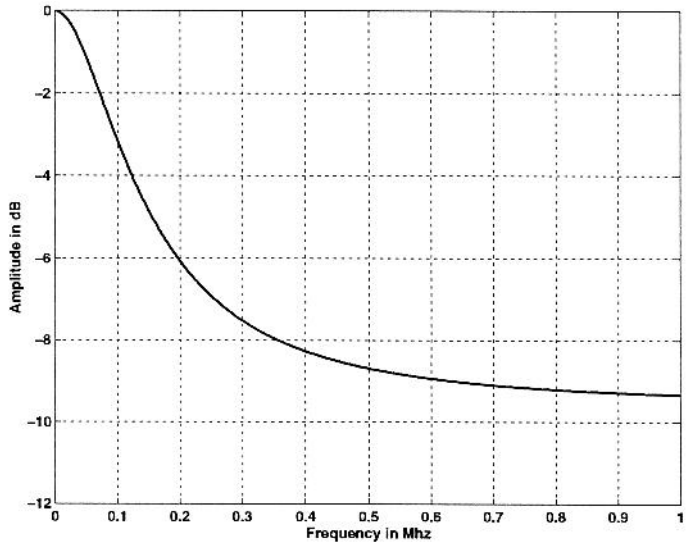


Figure 23. De-emphasis Filter Frequency Response

1.4.5. Additional Chroma Functions

KS0127 has many built in auto detection circuits. These allow KS0127 to track any type of video standard input automatically.

For analog component video input, the demodulation function is not enabled. The low pass filter provides a group delay for Cb and Cr alignment. This enables the two components to be sampled by one ADC.

1.5. COMB FILTER

Comb filters provide superior Y/C separation for composite NTSC and PAL than simple chroma trap filter. The KS0127 contains on-chip separate 2-line stored luma and chroma comb filters. An internal signal $\overline{\text{COMB}}$ controls for what lines the comb function is enabled. This signal is available through the PORTB pin. The timing for $\overline{\text{COMB}}$ is shown in Figure 7 and Figure 8. Combing is part of the vertical processing which also includes vertical scaling, which is discussed in Section 1.6. A block diagram for the vertical processing section is shown in Figure 24.

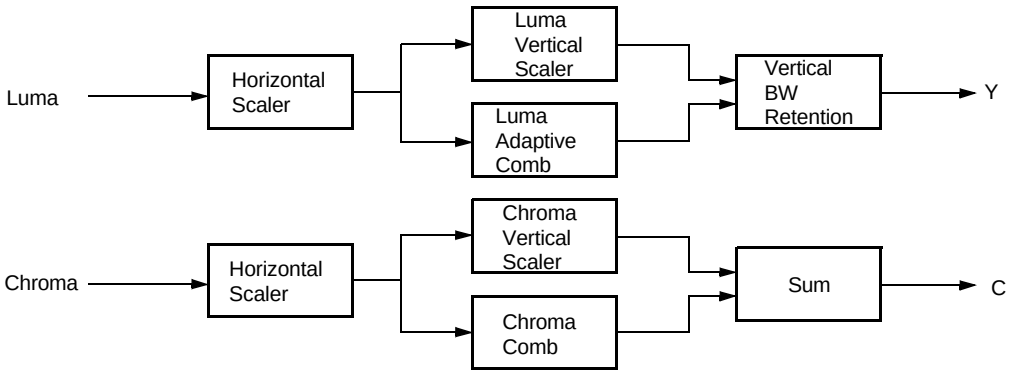


Figure 24. Vertical Processing

1.5.1. Luma Comb Filter

The luma comb filter reduces high frequency chroma leakage into the luminance path. The KS0127 uses 2-line stored luma data for combing. Filter coefficients for different video input standards are provided and can be selected automatically based on the video input. Filter coefficients may also be set manually.

An optional active comb is employed for NTSC video. Selection of luma comb coefficients is based on line-to-line chroma correlation.

Provision is made to disable luma comb for S-video, component, or digital video input. This is achieved by programming the luma comb control register **MNYCMB** to "1", and by choosing the value 3 or 4 for **YCMBCO[2:0]**. This will result either a 1-line or 2-line luma delay. Care must be exercised when disabling the luma comb so that luma line delay matches the chroma path line delay.

Special filtering is applied to ensure that high vertical bandwidth is retained for the luma path.

1.5.2. Chroma Comb Filter

The chroma comb filter provides further color separation from the composite video. Filter coefficients can be automatically selected based on the input video standard or manually set using **NMCCMB** and **CCMBCO[2:1]**.

1.6. SCALING

The KS0127 includes a high quality down scaler. The video images can be down scaled in both horizontal and vertical direction to an arbitrary size.

1.6.1. Horizontal Scaler

The horizontal scaler uses a 5-tap 32-phase interpolation filter for luma, and a 3-tap 8-phase interpolation filter for chroma. Scaled pixel data are stored in an on-chip FIFO so they can be sent out in a continuous stream.

Horizontal scaling ratio is programmed via the 15-bit register **HSCL**. The timing signal EHAV is used to indicate when scaled pixel data is available at the video output port. EHAV can be programmed so that it is active for every line regardless of vertical cropping and scaling. It can also be programmed to be active only for valid video lines. For example, Figure 25 shows the timing for CIF output assuming HAV is programmed to be active for 720 pixels. The **HSCL** register is programmed with the value 4000 (hex). The trailing edge of EHAV is either aligned with the trailing edge of HAV if the total number of scaled pixels is even, or is one pixel clock earlier if the number is odd.

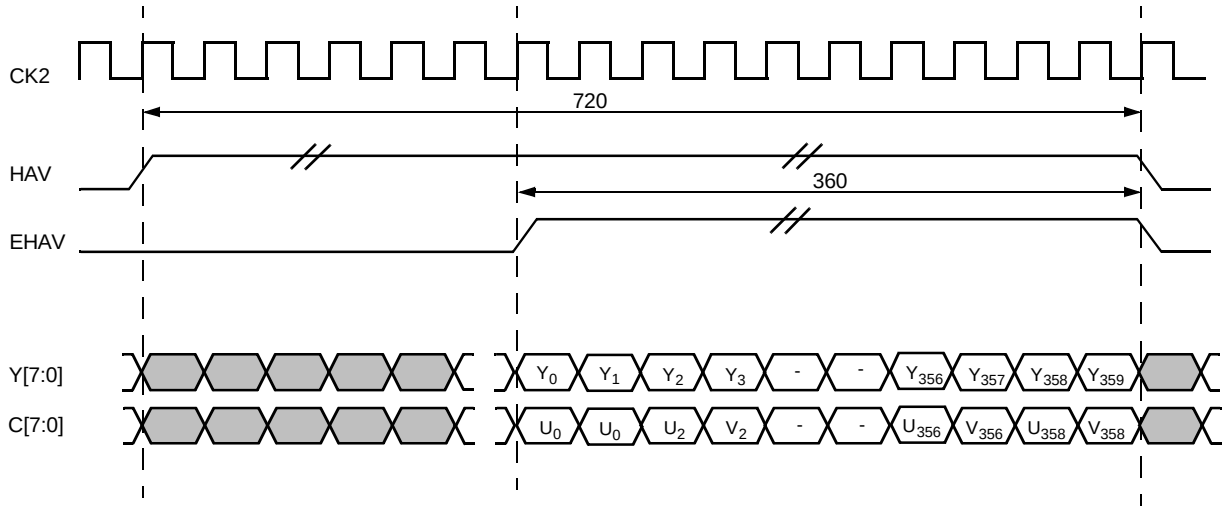


Figure 25. Horizontal Scaler Timing for CIF Output (CCIR 601 Pixel Rate)

Frequency response and group delay for the luma scaler are shown in Figure 26 and Figure 27, respectively. The luma interpolation filter is designed to achieve relatively flat frequency response and minimal group delay up to the normal video bandwidth. A flat full data path frequency response may be obtained with the help of the luma peaking control register **HYPK[1:0]**. The high quality filter ensures minimal artifacts for any scaling ratio.

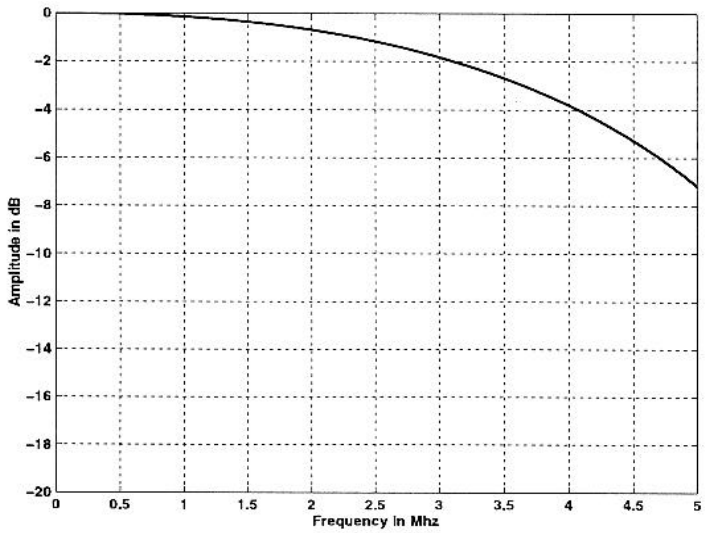


Figure 26. Horizontal Luma Scaler Interpolation Filter Frequency Response

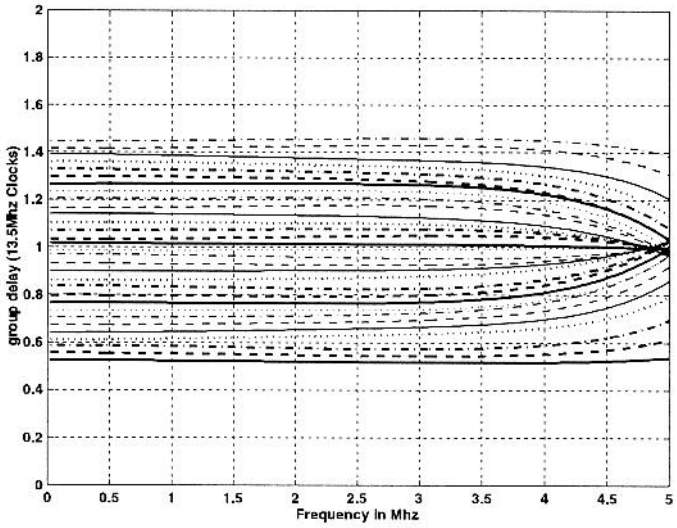


Figure 27. Horizontal Luma Scaler Interpolation Filter Group Delay

Because of the limited bandwidth of the chroma data, a simpler interpolation filter is used for the horizontal chroma scaler. The frequency response and group delay for this filter are shown in Figure 28 and Figure 29, respectively.

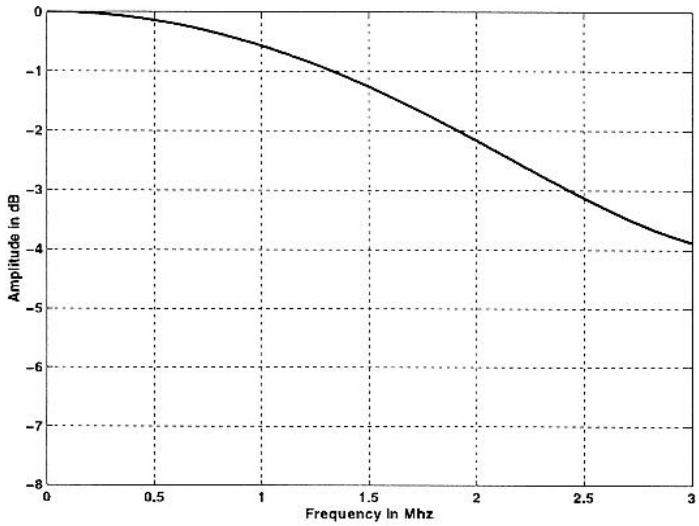


Figure 28. Horizontal Chroma Scaler Interpolation Filter Frequency Response

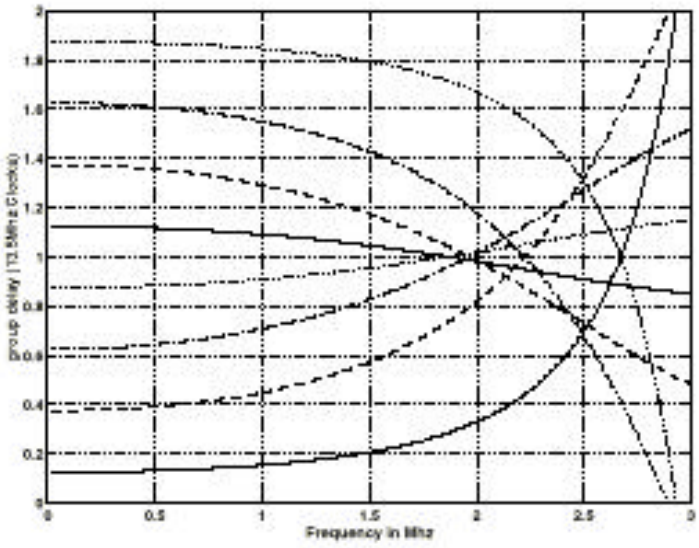


Figure 29. Horizontal Chroma Scaler Interpolation Filter Group Delay

1.6.2. Luma Vertical Scaler

Vertical luma scaling uses either a 3-tap or 5-tap 8-phase interpolation filter depending on the horizontal scaling ratio.

Vertical scaling ratio is programmed via the 14-bit register **VSCL**. A valid scaled line is indicated by the timing signal EVAV being active. The EVAV can be programmed to be internally gated by the VAV signal so it can only be valid within the vertically cropped region.

Luma horizontal scaling can use either a 3-tap or a 5-tap interpolation filter depending on the horizontal scaling ration. If the scaled horizontal line has less than or equal to 384 pixels, the 5-tap luma interpolation filter can be turned on by programming the **VRT2X** bit to a "1". Otherwise, the **VRT2X** bit should be set to "0" and the 3-tap filter be used.

The **VYBWR** bit provides additional vertical bandwidth control for vertical scaling. Typically, when the vertical scaling ratio is less than 1/2, this bit should be set to "1" to eliminate any aliasing effect.

Luma vertical scaler interpolation filter frequency response is shown in Figure 30.

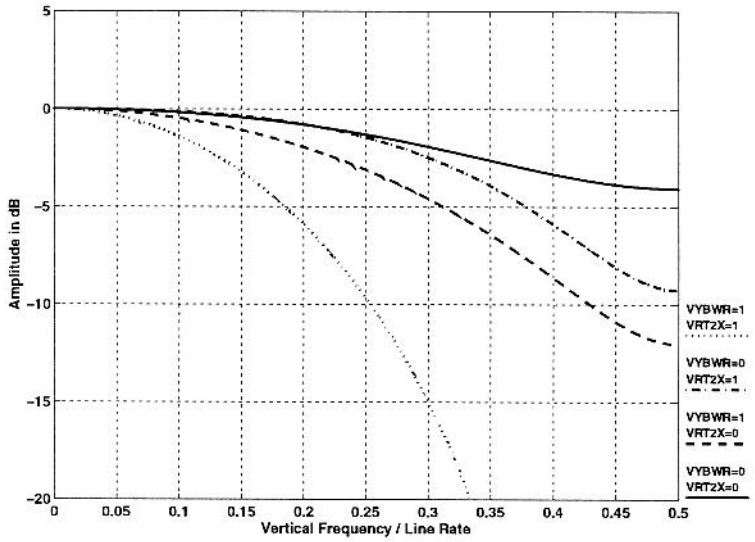


Figure 30. Luma Vertical Scaler Interpolation Filter Frequency Response

In vertical scaling, the start of signal VAV controls the phase of the vertical scaler interpolation filter. If **VAVB**, **VAVE**, **VAVOD0**, **VAVEV0**, and **VSCL** are programmed such that the vertical interpolation filter has the same phase and scaling ratio as that of a memory controller (most memory controller has simple line dropping vertical scaling), it is possible to interface the KS0127 to the memory controller without using EVAV.

1.6.3. Chroma Vertical Scaling

Chroma vertical scaling uses different algorithms depending on video input standard and horizontal scaling ratio. If horizontal scaling results in line with less than or equal to 384 pixels, and the **VRT2X** is set to a "1", a 5-tap interpolation filter will be used for all video inputs. Otherwise, for NTSC, a 3-tap interpolation filter will be used for NTSC input, and decimation (line dropping without filtering) will be used for PAL and SECAM. Filter characteristics for the 3-tap and 5-tap filters are shown in Figure 31.

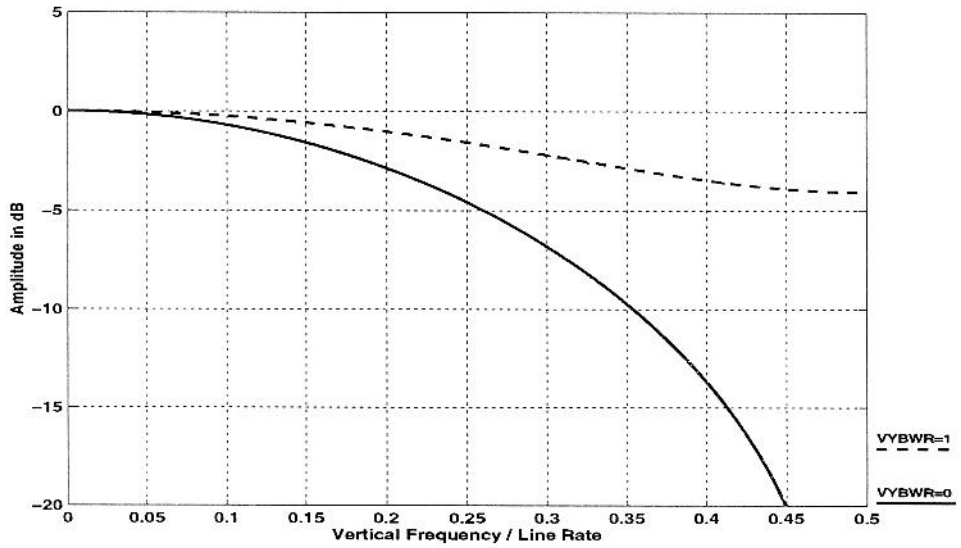


Figure 31. Chroma Vertical Scaler Interpolation Filter Frequency Response

1.7. VBI DATA PROCESSING

The KS0127 VBI data processing is very flexible in that it supports VBI data formats of:

- Closed Caption
- Teletext NTSC standards (Intercast)
- Teletext European standard
- SMPTE time code.

This data can be accessed from the part via 4 different methods:

- Enabling the ADC samples to be output for the appropriate lines
- Slicing the data (creating a clock and comparing the data to a threshold at the clock) and bursting this data out on Y output.
- Reading the data from the I2C bus.
- Via 2 external pins that output the sliced VBI data and the time at which the slice is valid.

In the interests of simplicity and standards compatibility, the KS0127 has been designed to always output VBI data during the active video period, that is, when the output timing signal HAV is active. Output of VBI data starts at the leading edge of HAV. If the KS0127 is programmed to CCIR 656 mode with SAV and EAV codes (**OFMT**=3), the EAV and SAV code will remain for the VBI processing lines. A simplified block diagram for the VBI section is shown in Figure 32.

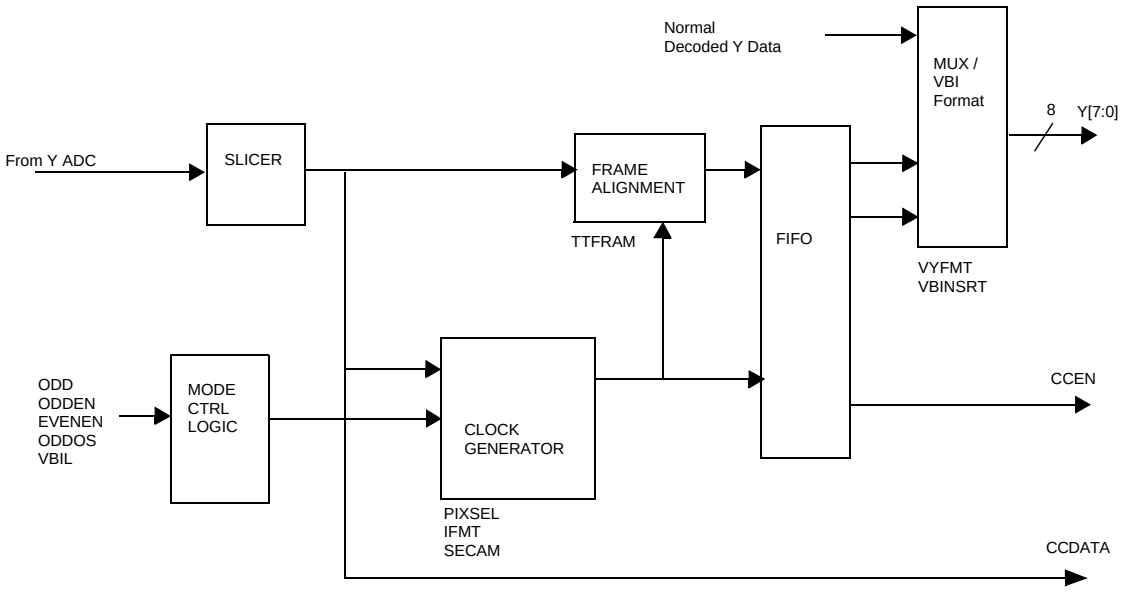


Figure 32. VBI Decoder Block Diagram

Table 7 lists all the video standards that the VBI decoder supports.

Table 7: Video Standards Supported by VBI Decoder

Mode	Sample Clock Freq	Format	Pixel	SECAM	Generated Freq MHz
Intercast / Teletext NTSC 601	27	1	1	0	5.7272
Intercast /Teletext NTSC Square Pixel	24.54	1	0	0	5.7272
Teletext PAL 601	27	0	1	0	6.9375
Teletext PAL Square Pixel	29.5	0	0	0	6.9375
Teletext SECAM 601	27	0	1	1	6.2031
Teletext SECAM Square Pixel	29.5	0	0	1	6.2031
Closed Caption NTSC 601	27	1	1	0	0.503
Close Capt. NTSC Square Pixel	24.54	1	0	0	0.503
SMPTE Time Code NTSC 601	27	1	1	0	3.579545
SMPTE Time Code NTSC Square Pixel	24.54	1	0	0	3.579545

Configuring the VBI processing consists of many different steps which are individually explained below.

1.7.1. Enabling the VBI Processor

The VBI processor can be enabled independently for the ODD or EVEN fields with the **ODDEN** and **EVEN** bits. Some VBI data lines are only present on 1 of the 2 fields, These independent field enables allow control of the total VBI data output from the chip.

1.7.2. Selecting the Type of Output Data

As previously mentioned, there are 4 different ways the VBI data can be extracted. Three of these are selected as shown in the table, the fourth method (CCEN and CCDAT pins) is always available if VBI processing is enabled.

Table 8: VBI Data Output Mode

VBCVBS	VBINSRT	Output Mode
0	0	The VBI data is available via the I2C registers CCDAT1 and CCDAT2. Only the Last 2 extracted bytes are stored in these registers. Thus, this mode is only useful for extraction of Closed Caption data.
0	1	This mode enables output of the sliced VBI data.
1	0	Not a valid mode.
1	1	This mode enables output of direct data from the ADC.

1.7.3. Select Individual Lines enabled for VBI processing

KS0127 allows programmable selection of processing for the various video lines. For example Teletext/Intercast data can be sliced for lines 14 - 17, and closed caption for line 21.

The VBIL0 through VBIL15 define 2 bit register locations that enable specific VBI processing for a video line. As can be seen in Figure 7 for 60Hz and Figure 8 for 50Hz video The following alignments exist:

Table 9: VBI Line(s) Selection

VBIL number	Line Number That the VBIL Processing command applies to (Assuming ODDOS=1)			
	Odd Field 60 Hz	Even Field 60 Hz	Odd Field 50 Hz	Even Field 50Hz
VBIL0	All Lines Except 10-24	All Lines Except 273-287	All lines Except 7-21	All lines Except 320 - 334
VBIL1	10	273	7	320
VBIL2	11	274	8	321
VBIL3	12	275	9	322
VBIL4	13	276	10	323
VBIL5	14	277	11	324
VBIL6	15	278	12	325
VBIL7	16	279	13	326
VBIL8	17	280	14	327
VBIL9	18	281	15	328
VBIL10	19	282	16	329
VBIL11	20	283	17	330
VBIL12	21	284	18	331
VBIL13	22	285	19	332
VBIL14	23	286	20	333
VBIL15	24	287	21	334

The **ODDOS[1:0**] bits allow offset between the odd and even fields. Thus VBIL9 can be lines 17,18 or 19 for ODD fields while VBIL9 is still line 281 for EVEN fields. This extra controls account for variations of VBI data locations from ODD and EVEN fields.

When Intercast or Teletext data is selected, an 8-bit user programmable register (**TTFRAM**) is provided for the framing byte. The frame alignment processor uses this information to properly locate the first data bit on each line.

Table 10: VBI Data Insertion On Y Output

VYFMT[1:0]	Bit Alignment	Header	Number of Output Bytes				
			Teletext			Closed Caption	SMPTE
			NTSC	PAL	SECAM		
0	1 bit on Y7	None	264	352	232	16	88
1	1 bit on Y7	1 bit on Y3	264	352	232	16	88
2	4 bits on Y7...Y4	1 bit on Y3	66	88	58	4	22
3	8 bits on Y7...Y0	None	33	44	29	2	11

Figure 33 shows the timing diagram for **VYFMT[1:0]**=3.

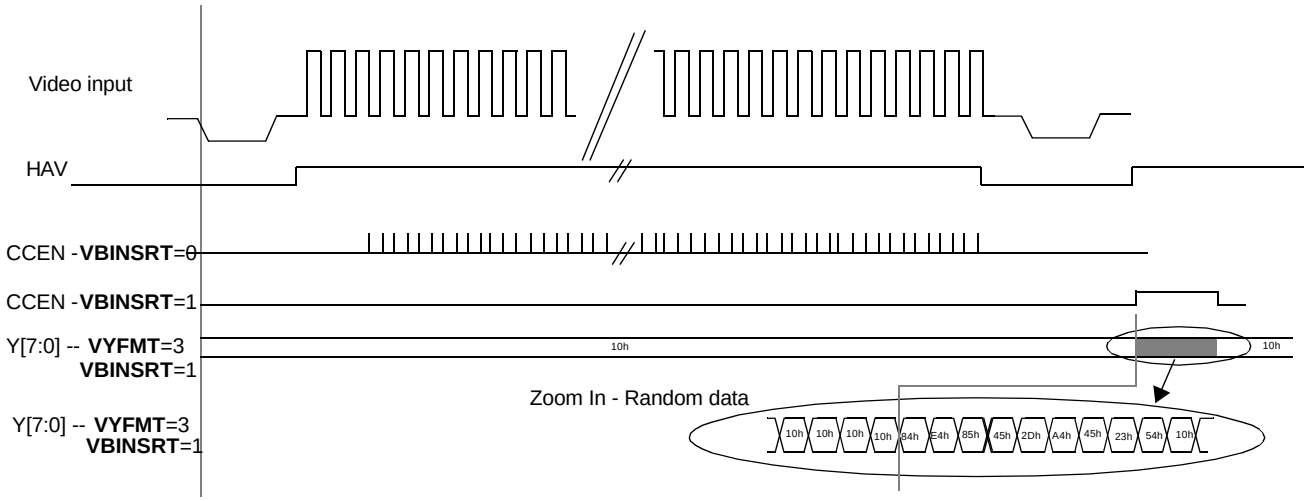


Figure 33. VBI Insertion Timing for VYFMT[1:0]=3

Digitized CVBS data can also be output on the video output port using output format (**OFMT[**3:0]) 8 or 9. CVBS is always digitized at the CK clock rate. CVBS data is available when HAV is active. For byte alignment and output sequence, refer to Table 11. More detail is shown in the Digital Output Section.

For Closed Caption data, two read-only registers, **CCDAT1** and **CCDAT2**, are provided so the Closed Caption data can be read via the host interface. The **VBIFLG** bit can be polled to see if data captured in the two registers can be safely read.

1.8. COLOR SPACE CONVERTER AND GAMMA CORRECTION

The color space converter processes the video data as YCbCr 4:4:4 when converting to RGB. A programmable limiter **(YCRANG)** can be imposed on the Y/C data to limit the ranges. One can choose to limit the Y/C to 1 - 254, or Y to 16 - 235 and C to 16 - 240.

When selected, YCbCr 4:4:4 is converted to 24 bit RGB according to the following equations:

$$R = C_Y + 1.375C_R$$
$$G = C_Y - 0.703C_R - 0.328C_B$$
$$B = C_Y + 1.734C_B$$

For 16-bit RGB output, truncation with dithering is used to convert the data from 24 bit to 16 bit.

The KS0127 provides programmable ga,,a correction. For details on how to utilize this feature, please contact the Application Department.

1.9. DIGITAL VIDEO OUTPUT

The KS0127 can output digital video data in various formats, which are tabulated in Table 11. All 8-bit output

Table 11: Digital Video Output Format

Clock	CK2										CK			
OFMT	0		1				4	5	6	7	2, 3, 8[*1], 9[*2]			
Type	YCbCr 4:2:2		YCbCr 4:1:1				YCbCr 4:4:4	RGB 565	RGB 888	RGB 888	YCbCr 4:2:2			
Pin	2N	+1	4N	+1	+2	+3	N	N	N	N	4N	+1	+2	+3
C0	Cb0	Cr0					Cb0	B0	B0	B3				
C1	Cb1	Cr1					Cb1	B1	B1	B4				
C2	Cb2	Cr2					Cb2	B2	B2	B5				
C3	Cb3	Cr3					Cb3	B3	B3	B6				
C4	Cb4	Cr4	Cr6	Cr4	Cr2	Cr0	Cb4	B4	B4	B7				
C5	Cb5	Cr5	Cr7	Cr5	Cr3	Cr1	Cb5	G0	B5	G2				
C6	Cb6	Cr6	Cb6	Cb4	Cb2	Cb0	Cb6	G1	B6	G3				
C7	Cb7	Cr7	Cb7	Cb5	Cb3	Cb1	Cb7	G2	B7	G4				
Y0	Y0	Y0	Y0	Y0	Y0	Y0	Cr0	G3	G0	G5	Cb0	Y0	Cr0	Y0
Y1	Y1	Y1	Y1	Y1	Y1	Y1	Cr1	G4	G1	G6	Cb1	Y1	Cr1	Y1
Y2	Y2	Y2	Y2	Y2	Y2	Y2	Cr2	G5	G2	G7	Cb2	Y2	Cr2	Y2
Y3	Y3	Y3	Y3	Y3	Y3	Y3	Cr3	R0	G3	R3	Cb3	Y3	Cr3	Y3
Y4	Y4	Y4	Y4	Y4	Y4	Y4	Cr4	R1	G4	R4	Cb4	Y4	Cr4	Y4
Y5	Y5	Y5	Y5	Y5	Y5	Y5	Cr5	R2	G5	R5	Cb5	Y5	Cr5	Y5
Y6	Y6	Y6	Y6	Y6	Y6	Y6	Cr6	R3	G6	R6	Cb6	Y6	Cr6	Y6
Y7	Y7	Y7	Y7	Y7	Y7	Y7	Cr7	R4	G7	R7	Cb7	Y7	Cr7	Y7
EXV0							Y0		R0	B0				
EXV1							Y1		R1	B1				
EXV2							Y2		R2	B2				
EXV3							Y3		R3	G0				
EXV4							Y4		R4	G1				
EXV5							Y5		R5	R0				
EXV6							Y6		R6	R1				
EXV7							Y7		R7	R2				

[*1] This mode is the same as mode 2 plus non-scaled video also available at EVX0..7.

[*2] This mode is the same as mode 3 plus non-scaled video also available at EVX0..7.

formats use CK as pixel clock; the other formats use CK2 as pixel clock. The first pixel is always aligned to the leading edge of the HAV signal.

1.9.1. Validation Code Insertion

KS0127 inserts Validation codes during inactive video (HAV is inactive), and invalid video (HAV is active but EHAV is inactive) to assist in recognition of scaled data and VBI data. Table 12 lists the available codes, when they are inserted, and related programming registers.

Table 12: Invalid and Unused Code Insertion

Code	Description
INVALY	This user programmed code is inserted in the Y or G output stream in scaling operation when HAV is active while EHAV is inactive. Insertion of this code is independent of the output format. Related register is **INVALY**.
INVALU	This user programmed code is inserted in the U or B output stream in scaling operation when HAV is active while EHAV is inactive. Insertion of this code is independent of the output format. Related register is **INVALU**.
INVALV	This user programmed code is inserted in the V or R output stream in scaling operation when HAV is active while EHAV is inactive. Insertion of this code is independent of the output format. Related register is **INVALV**.
UNUSEY	This user programmed code is inserted in the Y or G output stream when HAV is inactive and no other reference code is inserted. Insertion of this code is independent of the output format. Related register is **UNUSEY**.
UNUSEU	This user programmed code is inserted in the U or B output stream when HAV is inactive and no other reference code is inserted. Insertion of this code is independent of the output format. Related register is **UNUSEU**.
UNUSEV	This user programmed code is inserted in the V or R output stream when HAV is inactive and no other reference code is inserted. Insertion of this code is independent of the output format. Related register is **UNUSEV**.

An example timing diagram for some of the programmable modes is shown in Figure 34. In this diagram, The field rate is 60 Hz, A CCIR 601 sampling rate has been selected thus giving 720 active pixels. The horizontal scaling ratio has been selected for an output of 718 out of 720 pixels.

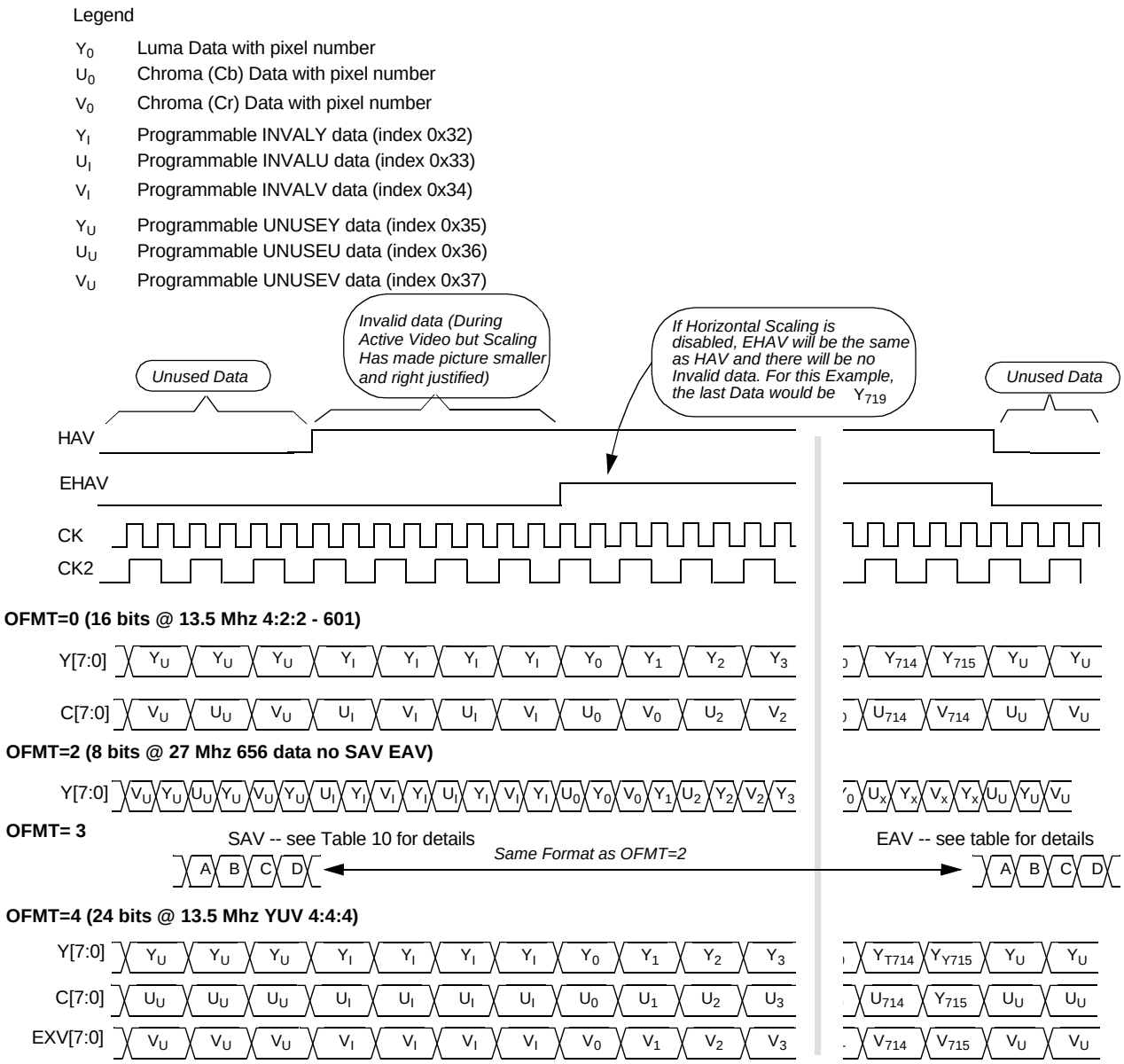


Figure 34. Horizontal Data Timing for Various Output Modes

1.9.2. 656 Op Codes

The KS0127 supports timing synchronization through embedded (656) timing reference codes in the output video data stream. This mode is available for output format 3 (**OFMT**[3:0] = 3). The 656 Op Codes follow the CCIR 656 standard. An optional set of 656 Op Codes can be enabled to identify VBI data using the **TASKB** bit.

The (A,B,C,D) inserted codes for 656 output modes are explained below. Locations in the data stream are shown in Figure 34. The D′ data is substituted for the standard codes shown in column D if **TASKB** bit is set and the current line is processing VBI data (sliced or raw ADC data format).

:

Table 13: 656 and TASKB 656 Op Codes

Condition			SAV / EAV Output Sequence -- Reference Output timing pictures					656 FVH values		
Field	**Vertical**	**Horizontal**	**A**	**B**	**C**	**D**	**D'**	**F**	**V**	**H**
Field 2	Vertical Blank	End Active Video	FFh	00h	00h	F1h	7Fh	1	1	1
Field 2	Vertical Blank	Start Active Video	FFh	00h	00h	ECh	62h	1	1	0
Field 2	Vertical Active	End Active Video	FFh	00h	00h	DAh	54h	1	0	1
Field 2	Vertical Active	Start Active Video	FFh	00h	00h	C7h	49h	1	0	0
Field 1	Vertical Blank	End Active Video	FFh	00h	00h	B6h	38h	0	1	1
Field 1	Vertical Blank	Start Active Video	FFh	00h	00h	ABh	24h	0	1	0
Field 1	Vertical Active	End Active Video	FFh	00h	00h	9Dh	13h	0	0	1
Field 1	Vertical Active	Start Active Video	FFh	00h	00h	80h	0Eh	0	0	0

1.9.3. 656 Op Code Vertical Transitions

The vertical transition locations of the various 656 Op Codes are shown in the following figures. Note that for proper transition locations of the SAV and EAV Op Codes **VSE**=0 and **VALIGN**=1.

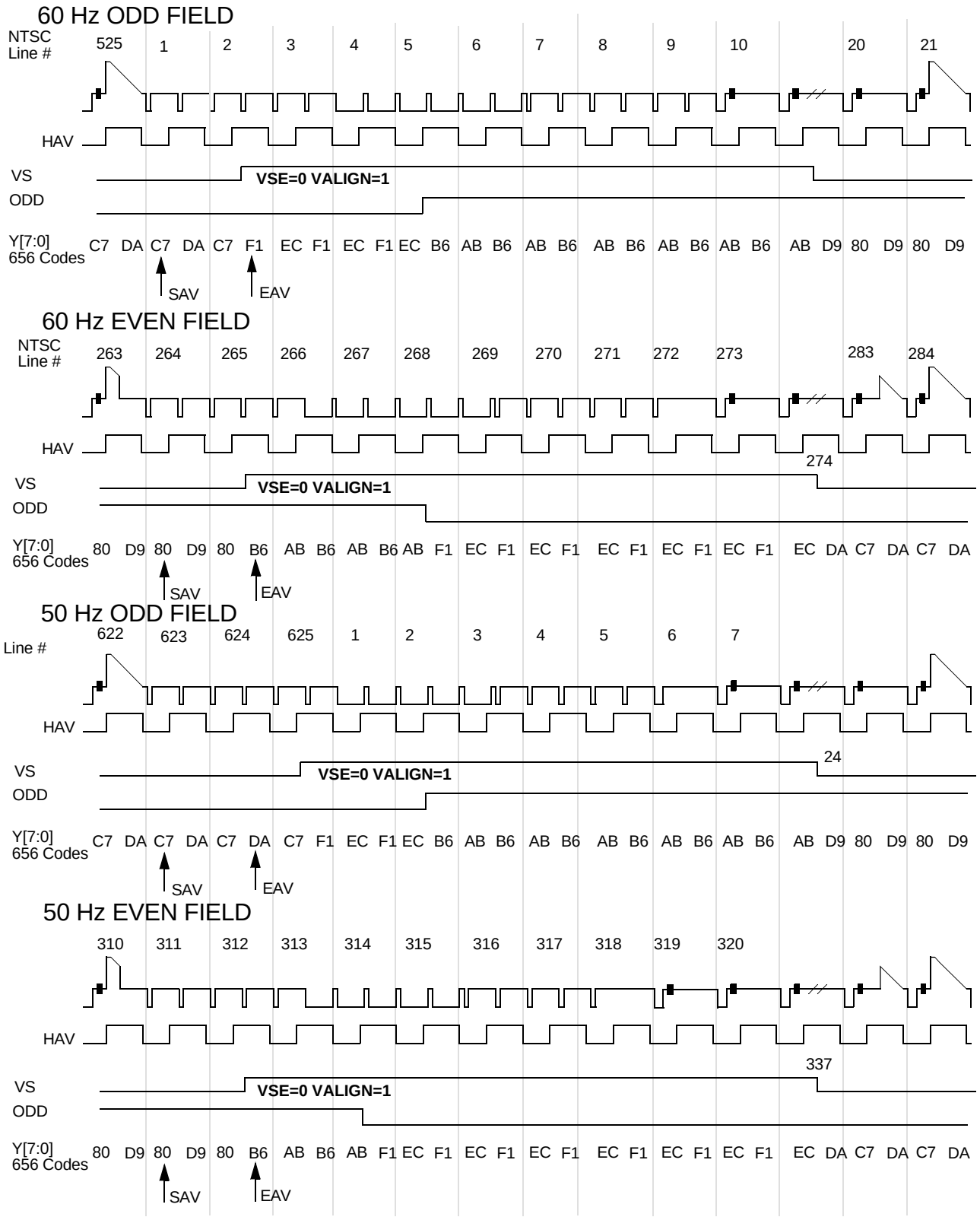


Figure 35. 656 Op Code Vertical Transition Points

1.10. HOST INTERFACE

The KS0127 supports the IIC serial interface for programming the chip registers.

1.10.1. IIC Interface

The two wire interface consists of the SCLK and SDAT signals. Data can be written to or read from the KS0127. For both read and write, each byte is transferred MSB first, and the data bit is valid when the SCLK is high.

To write to the slave device, the host initiates a transfer cycle with a START signal. The START signal is HIGH to LOW transition on the SDAT while the SCLK is high. The host then sends a byte consisting of the 7-bit slave device ID and a 0 in the R/$\overline{W}$ bit. The arrangement for the slave device ID and the R/W bit is depicted in Figure 36. AEX1 and AEX0 are configuration pins used to configure the KS0127 to use one of the four addresses. Up to four KS0127's can be used in one system each with a unique address.

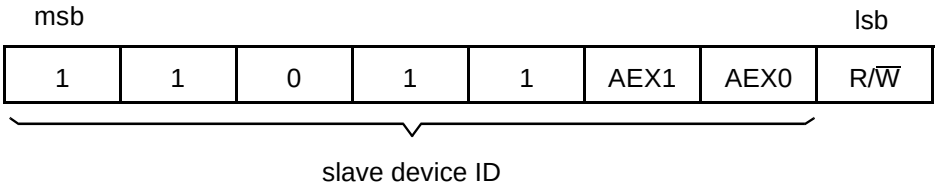


Figure 36. IIC Slave Device ID and R/$\overline{W}$ Byte

The second byte the host sends is the base register index. The host then sends the data. The KS0127 increments the index automatically after each byte of data is sent. Therefore, the host can write multiple bytes to the slave if they are in sequential order. The host completes the transfer cycle with a STOP signal which is a LOW to HIGH transition when the SCLK is high.

Each byte transfer consists of 9 clocks. When writing to the KS0127, an acknowledge signal is asserted by the salve device during the 9th clock.

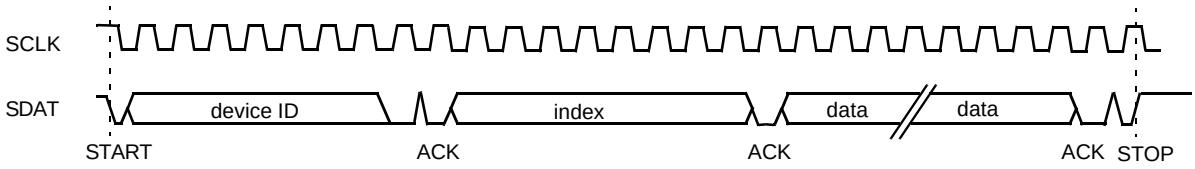


Figure 37. IIC Data Write

A read cycle takes two START-STOP phases. The first phase is a write to the index register. The second phase is the read from the data register.

The host initiates the first phase by sending the START signal. It then sends the slave device ID along with a 0 in the R/$\overline{W}$ position. The index is then sent followed by the STOP signal.

The second phase also starts with the START signal. It then sends the slave device ID but with a 1 in the R/$\overline{W}$ position to indicate data is to be read from the slave device. The host uses the SCLK to shift data out from the

KS0127. A typical second phase in a read transaction is depicted in Figure 38.

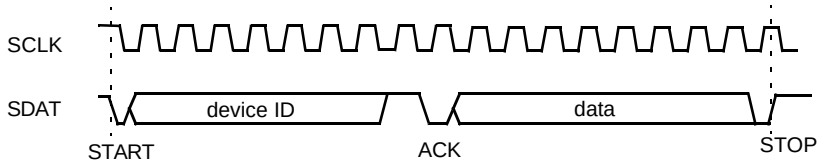


Figure 38. Second Phase of a Read Cycle

2. CONTROL REGISTER DESCRIPTION

This section contains information concerning the programmable control registers. Table 14 provides the default power up values for each index, and a bit map for each register. The following pages describe each register in detail and the possible programing values (an * indicates the power-on default).

Table 14: Register Summary

Index	Mnemonic	Default	Bit Map							
			7	6	5	4	3	2	1	0
0x00	STAT	-	CHIPID	VBIFLG	NOVID	FFRDET	PALDET	CDET	HLOCK	CLOCK
0x01	CMDA		POWDN	VSE	HFSEL[1:0]		XT24	PIXSEL	MNFMT	IFMT
0x02	CMDB		AGCGN	VALIGN	AGCOVF	AGCFRZ	INSEL[3:0]			
0x03	CMDC		VMEN	TSTGE1	0	TSTGPK	TSTGPH	TSTGFR[1:0]		TSTGEN
0x04	CMDD		EAV	0	CKDIR	INPSL[1:0]		SYNDIR	Y1MHZ	GPPORT
0x05	HAVB		HAVB[7:0]							
0x06	HAVE		HAVE[7:0]							
0x07	HS1B		HS1B[8:1]							
0x08	HS1E		HS1E[8:1]							
0x09	HS2B		HS2B[8:1]							
0x0A	HS2E		HS2E[8:1]							
0x0B	AGC		AGC[7:0]							
0x0C	HXTRA		HAVB[10:8]			HAVE[10:8]			HS1BE0	HS2BE0
0x0D	CDEM		OUTHIZ	FSEC	-	CIFCMP[1:0]		0	0	0
0x0E	PORTAB		DIRB	DATAB[2:0]			DIRA	DATAA[2:0]		
0x0F	LUMA		-	UNIT	RGBH	PED	HYBWR	CTRAP	HYPK[1:0]	
0x10	CON		CONT[7:0]							
0x11	BRT		BRT[7:0]							
0x12	CHROMA		ACCFRZ	PALM	PALN	CBW	CORE[1:0]		CKILL[1:0]	
0x13	CHROMB		CDLY[3:0]				SCHCMP[3:0]			
0x14	DEMOD		FSCDET	SECDET	CDMLPF	CTRACK	MNFSC[1:0]		MNSECAM[1:0]	
0x15	SAT		SAT[7:0]							
0x16	HUE		HUE[7:0]							
0x17	VERTIA		MNYCMB	YCMBCO[2:0]			VRT2X	VCTRL[2:0]		
0x18	VERTIB		HYLPF[2:0]			HYBWI	HYDEC	VSCLEN[1:0]		0
0x19	VERTIC		MNCCMB	CCMBCO[2:0]			ACMBEN	VYBW	EVAVEV	EVAVOD
0x1A	HSCLL		HSCL[6:0]							CMBMOD
0x1B	HSCLH		HSCL[14:7]							
0x1C	VSCLL		VSCL[5:0]						ACMBCO	ACMBRE
0x1D	VSCLH		VSCL[13:6]							

Table 14: Register Summary

Index	Mnemonic	Default	Bit Map							
			7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x1E	OFMTA		0	0	OENC[1:0]		OFMT[3:0]			
0x1F	OFMTB		VSVAV	EVAND[1:0]		EVHS1	EVHAV	EVEHAV	EVAVG	-
0x20	VBICTL		VBCVBS	VYFMT[1:0]		VBINSRT	ODDEN	EVENEN	ODDOS[1:0]	
0x21	CCDAT2		b0	b1	b2	b3	b4	b5	b6	P2
0x22	CCDAT1		b0	b1	b2	b3	b4	b5	b6	P1
0x23	VBIL30		VBIL3		VBIL2		VBIL1		VBIL0	
0x24	VBIL74		VBIL7		VBIL6		VBIL5		VBIL4	
0x25	VBIL118		VBIL11		VBIL10		VBIL9		VBIL8	
0x26	VBIL1512		VBIL15		VBIL14		VBIL13		VBIL12	
0x27	TTFRAM		TTFRAM[7:0]							
0x28	TESTA		-	-	0	0	-	-	-	-
0x29	UVOFFH		TSTCLC	TSTCGN	0	TSTCFR	UOFFST[5:4]		VOFFST[5:4]	
0x2A	UVOFFL		UOFFST[3:0]				VOFFST[3:0]			
0x2B	UGAIN		UGAIN[7:0]							
0x2C	VGAIN		VGAIN[7:0]							
0x2D	VAVB		VAVB[6:1]						VAVOD0	VAVEV0
0x2E	VAVE		VAVE[8:1]							
0x2F	CTRACK		0	0	DMCTL[1:0]		CGTC[1:0]		CFTC[1:0]	
0x30	POLCTL		EVAVPL	VSPL	ODDPL	HAVPL	EHAVPL	HS2PL	VAVPL	HS1PL
0x31	REFCOD		YCRANG	VSINST	1	HSINST[1:0]		1	0	0
0x32	INVALY		INVALY[7:0]							
0x33	INVALU		INVALU[7:0]							
0x34	INVALV		INVALV[7:0]							
0x35	UNUSEY		UNUSEY[7:0]							
0x36	UNUSEU		UNUSEU[7:0]							
0x37	UNUSEV		UNUSEV[7:0]							
0x38			Reserved							
0x39			Reserved							
0x3A	SHS1A		SHS1A[7:0]							
0x3B	SHS1B		SHS1B[7:0]							
0x3C	SHS1C		SHS1C[7:0]							
0x3D	CMDE		ODFST	VSALG	-	-	-	-	-	-
0x3E	VSDEL		-	-	VSDEL[5:0]					
0x3F	CMDF		-	-	EVAVY	UVDLEN	UVDLSL	REGUD	TASKB	CBWI

Read Only Status Bits									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
00h	**STAT**	CHIPID	VBIFLG	NOVID	FFRDET	PALDET	CDET	HLOCK	CLOCK

CLOCK Status for color lock.
- 0 Not locked.
- 1 Color lock achieved.

HLOCK Status for current line tracking mode.
- 0 Chip is in initial tracking mode.
- 1 Chip is in steady state tracking mode.

CDET Status for detection of color.
- 0 No color signal is detected.
- 1 Color signal is detected.

PALDET Status for current detected color format. Information contained in this bit is valid only if **CLOCK** is 1.
- 0 NTSC color format.
- 1 PAL color format.

FFRDET Status for current detected field frequency.
- 0 50 Hz field frequency, i.e. N,B,G,H,I,D,K,K1,L system.
- 1 60 Hz field frequency, i.e. M system.

NOVID Video detect flag.
- 0 Sync has been detected for the last 32 lines.
- 1 No sync has been detected.

VBIFLG Vertical blanking interval flag.
- 0 Video is in active region.
- 1 Video is in vertical blanking region.

CHIPID Chip version ID.
- 0 KS0122.
- 1 KS0127.

Control Register A									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
01h	**CMDA**	POWDN	VSE	HFSEL[1:0]		XT24	PIXSEL	MNFMT	IFMT

IFMT — Manual video input standard select. Standard selection can be controlled automatically if **MNFMT**=0.

- 0 — Chip is forced to assume input is 50 Hz.*
- 1 — Chip is forced to assume input is 60 Hz.

MNFMT — Manual input format control override. When this bit is 1 the **IFMT** bit is enabled.

- 0 — The chip determines the input video standard based on the detected field rate:* NTSC if 60 Hz. PAL/SECAM if 50 Hz.
- 1 — Input video standard is selected with the **IFMT** bit.

PIXSEL — Select pixel sampling rate.

- 0 — Output data is at square pixel rate.
- 1 — Output data is at CCIR 601 rate.*

XT24 — Select the external clock reference frequency.

- 0 — External clock is 26.8 MHz.
- 1 — External clock is 24.576 MHz.*

HFSEL[1:0] — Horizontal tracking loop frequency select.

- 0 — Force loop to very fast.
- 1 — Force loop to fast.
- 2 — Force loop to normal time constant. Use for signal with small frequency variation.*
- 3 — Force loop to slow time constant. Use for very good signal such as that from a signal generator, as tracking range is limited.

VSE — Change the vertical end location of the VS.

- 0 — Line 10/10.5.*
- 1 — Line 9/9.5.

POWDN — Power down mode.

- 0 — Normal operation.*
- 1 — All chip functions except microprocessor interface and CK/CK2 generation are disabled. The output of the CK/CK2 pins retains the most recent frequency when the power done mode is enabled.

Control Register B									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
02h	**CMDB**	AGCGN	VALIGN	AGCOVF	AGCFRZ	INSEL[3:0]			

INSEL[3:0] Analog input channel select.

0	AY0 is composite input.*
1	AY1 is composite input.
2	AY2 is composite input.
4	AC0 is composite input.
5	AC1 is composite input.
6	AC2 is composite input.
8	AY0 is luminance input, AC0 is chrominance input.
9	AY1 is luminance input, AC1 is chrominance input.
A	AY2 is luminance input, AC2 is chrominance input.
F	AY2 is luminance input, AC1 is Cb input, AC2 is Cr input.

AGCFRZ Freeze the analog AGC for the Y and C paths at their current values. When set to "1", the current gain value for the Y and C AGCs can be read or set using the AGC register.

0	AGC is running. Reading AGC register returns register setting, not the current AGC gain.*
1	AGC is frozen. Gain can be changed or read with AGC register.

AGCOVF AGC gain control mode.

0	AGC gain tracks to sync tip and back porch delta.
1	If ADC overflows, AGC gain will be reduced (this has higher priority over normal sync tip - back porch tracking).*

VALIGN VS edge alignment control.

0	VS leading edge occurs during serration pulses (typically within the first serration pulse). VS trailing edge is aligned to half line or beginning of the line depending on the field.*
1	VS leading edge is aligned to half line or beginning of the line depending on the field. VS trailing edge is always aligned to beginning of the line.

AGCGN AGC gain calculation.

0	Normal mode. AGC gain calculation is based on sync tip to back porch difference equal to 68 ADC code.*
1	AGC gain calculation is base on sync tip to back porch difference equal to 54 ADC code. This will reduce the AGC gain by a factor of 1/1.25 compare to normal mode. When used in conjunction with **PED** and **RGBH**, this effectively increases the input dynamic range.

Control register C									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
03h	**CMDC**	VMEN	TSTGE1	0	TSTGPK	TSTGPH	TSTGFR[1:0]		TSTGEN

TSTGEN — Enable manual control of horizontal phase and frequency tracking.

- 0 — Auto phase and frequency tracking.*
- 1 — Enable manual control of horizontal phase and frequency with **TSTGFR[1:0]** and **TSTGPH**.

TSTGFR[1:0] — When **TSTGEN** == 1, these two bits control the horizontal frequency tracking.*

- 00 — Stop frequency tracking and freeze the frequency at the current value.
- 01 — Horizontal frequency tracks the input.
- 1X — Horizontal frequency tracking ignores video input and runs at nominal value based on the field rate and output pixel rate selected by **IFMT** and **PIXEL** bits.

TSTGPH — When **TSTGEN** == 1, this bit controls the horizontal phase tracking.

- 0 — No phase tracking.*
- 1 — Horizontal phase tracks the input video or HS1 input if in slave mode.

TSTGPK — If **TSTGE1** == 1, this bit controls AGC.

- 0 — AGC clamps to back porch and gain is set based on sync tip-back porch difference.*
- 1 — AGC clamps to sync tip and gain is set based on peak-valley difference.

TSTGE1 — Enables the function of **TSTGPK**.

- 0 — Disables **TSTGPK**.*
- 1 — Enables **TSTGPK**.

VMEN — Vertical master mode.

- 0 — Normal vertical sync operation.*
- 1 — Vertical sync ignores input and free runs at 50 Hz or 60 Hz. This mode can be used to generate video timing for a slave device.

Note: Indice 03h and 04h should always be written as a pair in that order. NEVER WRITE TO INDEX 03h WITHOUT FOLLOWING BY WRITING TO INDEX 04h.

Control Register D									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
04h	**CMDD**	EAV	0	CKDIR	INPSL[1:0]		SYNDIR	Y1MHZ	GPPORT

GPPORT — General purpose port. This register is useful only if **DATAA[2:0]** == 7. If **DIRA** == 0, this bit is read only and reflects the logic state at PORTA pin. If **DIRA** == 1, any value written to this bit will appear at PORTA pin.

Y1MHZ — Luma bandwidth control.

- 0 Luma bandwidth is controlled by other luma filters in the luma path.*
- 1 Luma data is low pass filtered to 1MHz bandwidth.

SYNDIR — HS1 and VS pin direction control.

- 0 HS1 and VS are output.*
- 1 HS1 and VS are input.

INPSL[1:0] — Video input and clock source select.

- 0 Video source is analog and connected to the chip's analog input. Clock is internally generated.*
- 1 Video source is 8-bit digital CbYCr and connected to EXV0 through EXV7 pins.
- 3 Video source is 8-bit digitized CVBS and connected to EXV0 through EXV7 pins.

CKDIR — Clock select.

- 0 Clock is from internal clock generator. A reference clock at XTALI pin is required.*
- 1 Clock is from CK pin. When this is selected, the CK pin automatically becomes an input.

EAV — In 8-bit digital CbYCr input mode, this bit selects the sync source.

- 0 Horizontal and vertical syncs are from HS1 and VS pins, respectively.*
- 1 Syncs are embedded in the 8-bit digital data stream (CCIR 656 compatible).

HAV Start Control									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
05h	**HAVB**	HAVB[7:0]							
0Ch	**HXTRA**	HAVB[10:8]			HAVE[10:8]			HS1BE0	HS2BE0

HAVB[10:0] This 11-bit register is used to define the start location of the HAV signal relative to the sync tip (for CVBS input, this is the composite video sync tip. For 8-bit CbYCr input, this is the leading edge of the HS1 or EAV). The content of this register is a 2′complement number which is used as an offset to the default HAVB location as defined in Table 4. The resolution for this register is 1 CK clock.

HAV End Control									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
06h	**HAVE**	HAVE[7:0]							
0Ch	**HXTRA**	HAVB[10:8]			HAVE[10:8]			HS1BE0	HS2BE0

HAVE[10:0] This 11-bit register is used to define the end location of the HAV signal relative to the sync tip. The content of this register is a 2′complement number which is used as an offset to the default HAVE location as defined in Table 4. The resolution for this register is 1 CK clock.

HS1 Start Control									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
07h	**HS1B**	HS1B[8:1]							
0Ch	**HXTRA**	HAVB[10:8]			HAVE[10:8]			HS1BE0	HS2BE0

HS1B[8:1] - HS1BE0 If HS1 is programmed as an output, this 9-bit register defines the start location of the HS1 signal. The content of this register is a 2′s complement number which is used as an offset to the default HS1B location as defined in Table 4. The resolution for this register is 1 CK clock.

HS1 End Control									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
08h	**HS1E**	HS1E[8:1]							
0Ch	**HXTRA**	HAVB[10:8]			HAVE[10:8]			HS1BE0	HS2BE0

HS1E[8:1] - HS1BE0 — If HS1 is programmed as an output, this 9-bit register defines the end location of the HS1 signal. The content of this register is a 2′s complement number which is used as an offset to the default HS1E location as defined in Table 4. The resolution for this register is 1 CK clock.

HS2 Start Control									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
09h	**HS2B**	HS2B[8:1]							
0Ch	**HXTRA**	HAVB[10:8]			HAVE[10:8]			HS1BE0	HS2BE0

HS2B[8:1] - HS2BE0 — This 9-bit register defines the start location of the HS2 signal. The content of this register is a 2′s complement number which is used as an offset to the default HS2B location as defined in Table 4. The resolution for this register is 1 CK clock.

HS2 End Control									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
0Ah	**HS2E**	HS2E[8:1]							
0Ch	**HXTRA**	HAVB[10:8]			HAVE[10:8]			HS1BE0	HS2BE0

HS2E[8:1] - HS2BE0 — This 9-bit register defines the end location of the HS2 signal. The content of this register is a 2′s complement number which is used as an offset to the default HS2E location as defined in Table 4. The resolution for this register is 1 CK clock.

AGC Control									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
0x0B	**AGC**	AGC[7:0]							

AGC[7:0] This register is used to manually set AGC when **AGCFRZ** is set to "1". The content in the register is unsigned.

Chroma Demodulation Control									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
0Dh	**CDEM**	OUTHIZ	FSEC	-	CIFCMP[1:0]		0	0	0

CIFCMP[1:0] IF compensation for the chroma path.

0 No compensation.*

1 Upper chroma side band is 1 dB higher than lower side band.

2 Upper chroma side band is 3 dB higher than lower side band.

3 Upper chroma side band is 6 dB higher than lower side band.

FSEC Chroma frequency demodulation filter select for SECAM video.

0 Select SECAM chroma frequency demodulation filter if SECAM video is detected.*

1 Always use SECAM chroma frequency demodulation filter.

OUTHIZ This is the software output three-state control bit. If this bit is set to a "1", or the OEN pin is at a logic LOW level, output pins can be selectively put in the high impedance state using the additional software control bits **OENC[1:0]**.

0 This is default setting.*

1 This will enable the output pins to be three-stated regardless the state of the OEN pin.

Port A and B Control									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
0Eh	**PORTAB**	DIRB	DATAB[2:0]			DIRA	DATAA[2:0]		

DATAA[2:0] Port A data select. For internal gate signal locations, refer to Table 4.

- 0 Port A is disconnected from the internal signal path.*
- 1 Port A is connected to the BPG (back porch gate) signal.
- 2 Port A is connected to the SYG (sync tip gate) signal.
- 3 Port A is connected to the CBG (color burst gate) signal.
- 4 Port A is connected to the CBGW (color burst gate wide) signal. The CBGW is high for the entire color burst period.
- 5 Port A is connected to the SLICE (mid way of the sync tip) signal.
- 6 Port A is connected to the VBI (vertical blanking interval) signal.
- 7 Port A is connected to the **GPPORT** bit.

DIRA Port A direction control.

- 0 Port A is configured as input. The input is connected directly to the signal path selected by **DATAA[2:0]**. The internally generated gate signal is disconnected from the signal path.*
- 1 Port A is an output and is driven by the internally generated signal as selected by **DATAA[2:0]**.

DATAB[2:0] Port B data select. For internal gate signal locations, refer to Table 4.

- 0 Port B is disconnected from the internal signal path.*
- 1 Port B is connected to the SCH (sync tip to color burst phase) signal.
- 2 Port B is connected to the FH2 (twice per line pulses) signal.
- 3 Port B is connected to the FS_PULSE (falling edge of the sync tip) signal.
- 4 Port B is connected to the VBI_CVBS (VBI raw ADC) signal.
- 5 Port B is connected to the VBI_PROC (VBI sliced) signal.
- 6 Do not use.
- 7 Port A is connected to the $\overline{\text{COMB}}$ (comb enable) signal.

DIRB Port B direction control.

- 0 Port B is configured as input. The input is connected directly to the signal path selected by **DATAB[2:0]**. The internally generated gate signal is disconnected from the signal path.*
- 1 Port B is an output and is driven by the internally generated signal as selected by **DATAB[2:0]**.

Luma Control Register									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
0x0F	**LUMA**	-	UNIT	RGBH	PED	HYBWR	CTRAP	HYPK[1:0]	

HYPK[1:0] Luminance horizontal peaking control around 3 MHz.

0 Less than nominal peaking.*

1 Nominal peaking.

2 Increased peaking.

3 Maximum peaking.

CTRAP Chroma trap (notch filter) in the luma path.

0 No chroma trap. This mode is recommended for S-video or component video input.

1 Chroma trap is enabled*

HYBWR Luminance horizontal bandwidth reduction control.

0 Full bandwidth.*

1 Reduced bandwidth.

PED Enable gain correction for 7.5 blank-to-black setup (pedestal).

0 No pedestal. 0% = Y code 16. 100% = Y code 235.*

1 Gain adjusted for 7.5% blank-to-black setup (pedestal). 7.5% = Y code 16. 7.5% - 100% input produce Y code 16 - 235.

RGBH High gain to produce full range Y for 0% (or 7.5% if **PED** = 1) to 100% input.

0 Black (0% or 7.5%) to peak white(100%) input produce Y code 16 to 235.*.

1 Black (0% or 7.5%) to peak white(100%) input produce Y code 0 to 255.

UNIT When **PED** and **RGBH** are both set to a "1", setting this bit to a "1" produces a unit gain for CCIR 601 digital input (**INPSL[1:0]** = 1).

0 Luma DC gain is controlled by **PED** and **RGBH** as described for each bit.*

1 Luma DC gain is unity for CCIR 601 digital input.

Contrast Control									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
0x10	**CON**	CON[7:0]							

CON[7:0] This 8-bit register contains a 2's compliment number for contrast control.

Brightness Control									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
0x11	**BRT**	BRT[7:0]							

BRT[7:0] Brightness control register. The number contained in the register is 2's compliment.

Chroma Control Register A									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
0x12	**CHROMA**	ACCFRZ	PALM	PALN	CBW	CORE[1:0]		CKILL[1:0]	

CKILL[1:0] Color kill.

- 0 Auto detect mode. If color burst is too low or no color burst, chroma data is forced to code 128.*
- 2 Chroma is always ON.
- 3 Chroma data is always forced to code 128.

CORE[1:0] Chroma data coring.

- 0 No coring.
- 1 Chroma data within the range 128±1, inclusive, will be forced to 128.
- 2 Chroma data within the range 128±3, inclusive, will be forced to 128.*
- 3 Chroma data within the range 128±7, inclusive, will be forced to 128.

CBW Chroma bandwidth control.

- 0 Chroma 3 dB bandwidth is 850 kHz.*
- 1 Chroma 3 dB bandwidth is 550 kHz.

PALN Select color tracking for PAL-N, or NTSC-N when input field rate is 50 Hz and Fsc is 3.58 MHz.

- 0 Select NTSC-N.*
- 1 Select PAL-N.

PALM Select color tracking for PAL-M or NTSC-M when input field rate is 60 Hz.

- 0 Select color tracking for NTSC-M.*
- 1 Select color tracking for PAL-M.

ACCFRZ Chroma gain tracking freeze control.

- 0 Chroma gain tracks the input. Color saturation can be adjusted with **SAT**.*
- 1 Chroma gain freezes at the current saturation level.

Chroma Control Register B									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
0x13	**CHROMB**	CDLY[3:0]				SCHCMP[3:0]			

SCHCMP[3:0] Phase constant compare value for color burst phase relative to sync tip. Each step is 22.5 degrees with the value of 0 equal to 0 degree.

CDLY[3:0] Chroma path group delay relative to the luma path (in unit of CK):

0	No delay.*
1	-0.5
2	1
3	0.5
4	2
5	1.5
6	3
7	2.5
8	-4
9	-4.5
A	-3
B	-3.5
C	-2
D	-2.5
E	-1
F	-1.5

Chroma Demodulation Control and Status									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
0x14	**DEMOD**	FSCDET	SECDET	CDMLPF	CTRACK	MNFSC[1:0]		MNSECAM[1:0]	

MNSECAM[1:0] Enable manual SECAM input detection.

0 Detection of SECAM input is automatic.*

2 Force the chip to assume input is not SECAM.

3 Force the chip to assume input is SECAM.

MNFSC[1:0] Enable manual Fsc detection.

0 Detection of Fsc frequency is automatic.*

2 Force chip to assume input Fsc is 4.43 MHz or 4.286 MHz.

3 Force chip to assume input Fsc is 3.58 MHz.

CTRACK Chroma frequency tracking mode.

0 Chroma frequency tracking is based on the field rate and Fsc.*

1 Chroma frequency tracking is based on field rate only.

CDMLPF Bypass the LPF in the chroma demodulator.

0 Chroma data pass through the LPF for color demodulation.*

1 Chroma data bypass the LPF. This setting is used for component video input.

SECDET SECAM detection (read only).

0 Chip did not detect SECAM input.

1 Chip detected SECAM input.

FSCDET Color subcarrier detection (read only).

0 Chip detected 4.43 MHz or 4.286 MHz Fsc.

1 Chip detected 3.58 MHz Fsc.

Color Saturation Control									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
0x15	**SAT**	SAT[7:0]							

SAT[7:0] Color saturation control register. Register content is in 2′s compliment if **TSTCGN**=0. 0 value corresponds to nominal saturation.

Hue Control									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
0x16	**HUE**	HUE[7:0]							

HUE[7:0] Hue control register. The register content is in 2's compliment format. It covers the range from -180° to +178.59°. The resolution is 1.41°/LSB.

Vertical Processing Control A									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
0x17	**VERTIA**	MNYCMB	YCMBCO[2:0]			VRT2X	VCTRL[2:0]		

VCTRL[2:0] Luminance vertical filter control.

- 0 Scaler uses LPF path, comb uses HPF.*
- 1 Scaler uses full bandwidth, comb is disabled.
- 2 Scaler is disabled, comb uses full bandwidth.
- 3 Scaler uses LPF, comb is disabled.
- 4 Scaler is disabled, comb uses HPF.

VRT2X 3/5-tap vertical scaler filter select.

- 0 Select 3-tap vertical scaler filter.*
- 1 Select 5-tap vertical scaler filter. This option can be used only if horizontally cropped line is less than or equal to 384 pixels.

YCMBCO[2:0] Luma comb filter coefficients selection when the **MNYCMB** is set to "1".

- 0 [1/4 1/2 1/4].*
- 1 [3/8 1/2 1/8].
- 2 [1/2 1/2 0].
- 3 [1 0 0].
- 4 [0 1 0].
- 5 [1/2 0 1/2].
- 6 [0 1/2 1/2].
- 7 [1/8 1/2 3/8].

MNYCMB Select between auto and manual luma comb filter coefficients.

- 0 Luma comb filter coefficients are automatically selected based on input video standard.*
- 1 Luma comb filter coefficients are selected with **YCMBCO[2:0]**.

Vertical Processing Control B									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
0x18	**VERTIB**	HYLPF[2:0]			HYBWI	HYDEC	VSCLEN[1:0]		0

VSCLEN[1:0] Vertical scaling enable.

0 Vertical scaling is enabled.*

1 Vertical scaling is disabled.

2 Vertical scaling is disabled. Video is 1-line delayed.

3 Vertical scaling is disabled. Video is 2-line delayed.

HYDEC Luma path decimation filter enable.

0 Luma path decimation is enabled.*

1 Luma path decimation is disabled.

HYBWI Luma path decimation filter bandwidth select.

0 Normal bandwidth.*

1 Bandwidth is 1 MHz higher.

HYLPF[2:0] Horizontal luma LPF bandwidth control.

0 Full bandwidth.*

1 4.5 MHz bandwidth.

2 3.5 MHz bandwidth.

3 2.5 MHz bandwidth.

4 1.5 MHz bandwidth.

Vertical Processing Control C									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
0x19	**VERTIC**	MNCCMB	CCMBCO[2:0]			ACMBEN	VYBW	EVAVEV	EVAVOD

EVAVOD Enable VAV signal output during ODD field.

0 VAV signal is disabled (always inactive) during ODD field.

1 VAV signal is enabled during ODD field.*

EVAVEV Enable VAV signal output during EVEN field.

0 VAV signal is disabled (always inactive) during EVEN field.

1 VAV signal is enabled during EVEN field.*

VYBW Luma vertical bandwidth control.

0 Full bandwidth.*

1 Reduced bandwidth.

ACMBEN Enable luma active comb for NTSC.

0 Active comb is disabled.*

1 Active comb is enabled.

CCMBCO[2:0] Manual chorma comb filter coefficients select.

0 Select the coefficient set [1/2 1/2 0] (if **VRT2X** = 0).*

1 Select the coefficient set [1/4 1/2 1/4] (if **VRT2X** = 0).

2 Select the coefficient set [0 1/2 1/2 0 0] (if **VRT2X** = 1).

3 Select the coefficient set [0 1/4 1/2 1/4 0] (if **VRT2X** = 1).

4 Select the coefficient set [1 0 0].

5 Select the coefficient set [0 1 0].

6 Select the coefficient set [0 0 1].

7 No output (disabled).

MNCCMB Chroma comb filter coefficients are selected automatically or manually.

0 Filter coefficients are automatically selected based on the selected video input standard.*

1 Filter coefficients are selected manually with **CCMBCO[2:0]**.

Horizontal Scaling Ratio									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
0x1A	**HSCLL**	HSCL[6:0]							CMBMOD
0x1B	**HSCLH**	HSCL[14:7]							

CMBMOD This bit controls when comb is enabled internally.

0 Comb is enabled by the internal signal COMB_EN.*

1 Comb is enabled when VAV is active.

HSCL[14:0] The 15-bit register defines a horizontal scaling ratio of HSCL[14:0]/2^{15}. Any change to this value will become effective during the next vertical sync.

Vertical Scaling Ratio									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
0x1C	**VSCLL**	VSCL[5:0]						ACMBCO	ACMBRE
0x1D	**VSCLH**	VSCL[13:6]							

ACMBRE Active comb filter threshold select.

0 High threshold.*

1 Low threshold.

ACMBCO Active comb filter coefficient set select.

0 Use the set of coefficients for 100% comb.*

1 Use the set of coefficients for 75% comb.

VSCL[13:0] The 14-bit register defines a vertical scaling ratio of VSCL[13:0]/2^{14}. Any change to this value will become effective during the next vertical sync.

Output Control A									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
0x1E	**OFMTA**	0	0	OENC[1:0]		OFMT[3:0]			

OFMT[3:0] Digital video output format select. 16 and 24 bit data are output at CK2 clock rate. 8 bit data are output at CK clock rate.

0 16-bit YCbCr 4:2:2.*

1 12-bit YCbCr 4:1:1.

2 8-bit YCbCr 4:2:2 without embedded timing reference codes.

3 8-bit YCbCr 4:2:2 with embedded timing reference codes.

4 24-bit YCbCr 4:4:4.

5 16-bit RGB 565

6 24-bit RGB 888 with linear bit ordering.

7 24-bit RGB 888, bit ordering is an extension of the 16-bit RGB 565 format.

OENC[1:0] When either the OEN pin is low or the **OUTHIZ** is a "1", these two bits will determine which output pins are three-stated.

0 All video pins are three-stated.

1 All video pins, plus HAV, VAV, EVAV, EHAV, PID, ODD, HS1, HS2, VS, and SCH are three-stated.

2 All pins listed above, plus CK and CK2 are three-stated.

3 Reserved.

Output Control B									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
0x1F	**OFMTB**	VSVAV	EVAND[1:0]		EVHS1	EVHAV	EVEHAV	EVAVG	-

EVAVG Gate EVAV with VAV before sending to output.
- 0 EVAV is not gated with VAV. EVAV may be active outside of active VAV region.*
- 1 EVAV is gated with VAV. EVAV can be active only when VAV is active.

EVEHAV Additional qualifier for EHAV.
- 0 No additional qualifier.*
- 1 EHAV uses qualifier from **EVAND[1:0**].

EVHAV Additional qualifier for HAV.
- 0 No additional qualifier.*
- 1 HAV uses qualifier from **EVAND[1:0]**.

EVHS1 Additional qualifier for HS1.
- 0 No additional qualifier.*
- 1 HS1 uses qualifier from **EVAND[1:0]**.

EVAND[1:0] Qualifier based on EVAV and VAV (these are the internal active high signals).
- 0 Qualifier is logic "0".*
- 1 Qualifier is EVAV.
- 2 Reserved.
- 3 Qualifier is VAV

VSVAV Enable VAV to be output to VS.
- 0 Output normal VS.*
- 1 VS has the same output as VAV.

VBI Decoder Control									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
0x20	**VBICTL**	VBCVBS	VYFMT[1:0]		VBINSRT	ODDEN	EVENEN	ODDOS[1:0]	

ODDOS[1:0] Line offset for ODD field. See also **VBIL**[15:0].

0 ODD field line offset is -1 compared to EVEN field.*

1 No offset.

2 ODD field line offset is 1 compared to EVEN field.

3 ODD field line offset is 2 compared to EVEN field.

EVENEN VBI data processing for EVEN field.

0 No processing.*

1 VBI processing is enabled for EVEN field.

ODDEN VBI data processing for ODD field.

0 No processing.*

1 VBI processing is enabled for ODD field.

VBINSRT Enable VBI data to be output on the Y bus.

0 VBI data is not output on the Y bus.*

1 VBI data is output on the Y bus.

VYFMT[1:0] When **VBINSRT** = 1, these bits control how VBI data are output on the Y bus.

0 1 bit on Y7 per CK2 clock.*

1 1 bit on Y7 plus a "1" on Y3 per CK2 clock.

2 4 bits on Y7..Y4, with first bit on Y7, last bit on Y4, plus a "1" on Y3 per CK2 clock.

3 8 bits on Y7..Y0, with first bit on Y7, last bit on Y0, per CK2 clock.

VBCVBS Enable digitized CVBS data from ADC to be output for the selected VBI line instead of sliced VBI data.

0 Output sliced VBI data.*

1 Output digitized CVBS data.

First Decoded Close-Caption Data Byte (Read Only)									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
0x21	**CCDAT2**	b0	b1	b2	b3	b4	b5	b6	P2

CCDAT2 This byte contains the second byte of the decoded close-caption data as defined in EIA-608. In order for this register to receive the CC data, **VBINSRT** must be programmed to a "1", and **VYFMT[1:0]** must be programmed with the value 3. The same applies to **CCDAT1**. For normal NTSC Closed Caption decoding, **ODDEN** should be set to a "1"; **VBIL12** should be programmed with the value 1.

Second Decoded Close-Caption Data Byte (Read Only)									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
0x22	**CCDAT1**	b0	b1	b2	b3	b4	b5	b6	P1

CCDAT1 This byte contains the first byte of the decoded close-caption data as defined in EIA-608.

VBI Data Decoding									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
0x23	**VBIL30**	VBIL3		VBIL2		VBIL1		VBIL0	
0x24	**VBIL74**	VBIL7		VBIL6		VBIL5		VBIL4	
0x25	**VBIL118**	VBIL11		VBIL10		VBIL9		VBIL8	
0x26	**VBIL1512**	VBIL15		VBIL14		VBIL13		VBIL12	

VBIL0..VBLI15 These 16 2-bit numbers select how the chip should decode the VBI data for each VBI line. For 60 Hz video, **VBIL1** through **VBIL15** correspond to lines 10 through 24 in the ODD field, and lines 273 through 286 in the EVEN filed for NTSC (refer to Figure 10 for NTSC line numbering convention). For 50 Hz video, **VBIL1** corresponds to line 7 in the ODD field, and line 320 in the EVEN field. **VBIL0** is used for all other lines not covered by **VBIL1** through **VBIL15**.

0 Decode normal video.*

1 Decode Closed Caption data.

2 Decode Teletext data.

3 Decode SMPTE data.

Teletext Frame Alignment Pattern									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
0x27	**TTFRAM**	TTFRAM[7:0]							

TTFRAM[7:0] User programmable Teletext frame alignment pattern.

UV Offset Adjustment									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
0x29	**UVOFFH**	TSTCLC	TSTCGN	0	TSTCFR	UOFFST[5:4]		VOFFST[5:4]	
0x2A	**UVOFFL**	UOFFST[3:0]				VOFFST[3:0]			

VOFFST[5:0], UOFFST[5:0] These two 6-bit 2's compliment values are for offset adjustment to the U and V components of the chroma data. The resolution is 1/4 LSB of the 8-bit U and V.

TSTCFR Chroma frequency tracking control.

0 Chroma frequency tracking is enabled.*

1 Chroma frequency tracking is open loop.

TSTCGN Chroma gain control.

0 Chroma gain tracks input.*

1 Chroma gain is controlled by SAT only.

TSTCLC Cloche filter bypass.

0 Cloche filter is enabled for SECAM input.*

1 DC bypass of the cloche filter.

U Component Gain Adjustment									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
0x2B	**UGAIN**	UGAIN[7:0]							

UGAIN[7:0] U component gain adjustment. The nominal value is 0.

V Component Gain Adjustment									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
0x2C	**VGAIN**	VGAIN[7:0]							

VGAIN[7:0] V component gain adjustment. The nominal value is 0.

VAV Begin									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
0x2D	**VAVB**	VAVB[6:1]						VAVOD0	VAVEV0

VAVEV0 The LSB for VAVB and VAVE for the even field.

VAVOD0 The LSB for VAVB and VAVE for the odd field.

VAVB[6:1] The 6 MSB's of a 7-bit unsigned number which defines the start of VAV. The value "0" corresponds to line 4.

VAV End									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
0x2E	**VAVE**	VAVE[8:1]							

VAVE[8:1] The 8 MSB's of a 9-bit unsigned number which defines the end of VAV. The value "0" corresponds to line 4.

Chroma Tracking Control Register									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
0x2F	**CTRACK**	0	0	DMCTL[1:0]		CGTC[1:0]		CFTC[1:0]	

CFTC[1:0] Chroma frequency tracking time constant.

0 Slower.*

1 Slow.

2 Fast.

3 Faster.

CGTC[1:0] Chroma gain tracking time constant.

0 Slower.*

1 Slow.

2 Fast.

3 Faster.

DMCTL[1:0] Chroma demodulation bypass mode.

0 Chroma demodulation is enabled.*

1 Chroma demodulation is bypassed for digital YCbCr input.

2 Chroma demodulation is bypassed for analog YCbCr input. Cb path is phase delayed by one half of CK2 clock period.

3 Chroma demodulation is bypassed for analog YCbCr input. Cr path is phase delayed by one half of CK2 clock period.

Timing Signal Polarity Control									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
0x30	**POLCTL**	EVAVPL	VSPL	ODDPL	HAVPL	EHAVPL	HS2PL	VAVPL	HS1PL

HS1PL HS1 polarity.
0 Active high.*
1 Active low.

VAVPL VAV polarity.
0 Active high.*
1 Active low.

HS2PL HS2 polarity.
0 Active high.*
1 Active low.*

EHAVPL EHAV polarity.
0 Active high.*
1 Active low.

HAVPL HAV polarity.
0 Active high.*
1 Active low.

ODDPL ODD polarity.
0 Active high.*
1 Active low.

VSPL VS polarity.
0 Active high.*
1 Active low.

EVAVPL EVAV polarity.
0 Active high.*
1 Active low.

Reference Code Insertion Control									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
0x31	**REFCOD**	YCRANG	VSINST	1	HSINST[1:0]		1	0	0

HSINST[1:0] HS1 leading edge timing reference code insertion.

0 Never insert HS1 leading edge timing code.*

1 Insert HS1 timing code for every line.

2 Insert HS1 timing code only if EVAV is inactive.

VSINST VS leading edge timing reference code insertion.

0 Never insert VS leading edge timing code.*

1 Insert VS leading edge timing code.

YCRANG Digital video output range control.

0 Y and C ranges are limited to 1 - 254; R, G, and B ranges are limited to 1 - 254.*

1 Y range is limited to 16 - 235; C range is limited to 16 - 240; R, G, and B ranges are limited to 16 - 240.

Invalid Y Code									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
0x32	**INVALY**	INVALY[7:0]							

INVALY[7:0] User programmed code to be output for Y data when HAV is active but EHAV is inactive.

Invalid U Code									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
0x33	**INVALU**	INVALU[7:0]							

INVALU[7:0] User programmed code to be output for U data when HAV is active but EHAV is inactive.

Invalid V Code									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
0x34	**INVALV**	INVALV[7:0]							

INVALV[7:0] User programmed code to be output for V data when HAV is active but EHAV is inactive.

Unused Y Code									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
0x35	**UNUSEY**	UNUSEY[7:0]							

UNUSEY[7:0] User programmed code to be output for Y data when HAV is inactive.

Unused U Code									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
0x36	**UNUSEU**	UNUSEU[7:0]							

UNUSEU[7:0] User programmed code to be output for U data when HAV is inactive.

Unused V Code									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
0x37	**UNUSEV**	UNUSEV[7:0]							

UNUSEV[7:0] User programmed code to be output for V data when HAV is inactive.

User Defined SHS1 A									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
0x3A	**SHS1A**	SHS1A[7:0]							

SHS1A[7:0] Programmable HS1 leading edge timing reference code inserted when VAV and EVAV are both inactive.

User Defined SHS1 B									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
0x3B	**SHS1B**	SHS1B[7:0]							

SHS1B[7:0] Programmable HS1 leading edge timing reference code inserted when VAV is inactive and EVAV is active.

User Defined SHS1 C									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
0x3C	**SHS1C**	SHS1C[7:0]							

SHS1C[7:0] Programmable HS1 leading edge timing reference code inserted when VAV is active and EVAV is inactive.

Command Register E									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
0x3D	**CMDE**	ODFST	VSALG	-	-	-	-	-	-

VSALG Vertical scaling line dropping algorithm.

0 Vertical scaling drops the same lines in the Odd and Evan fields -- good for fast motion video.*

1 Vertical scaling drops lines based on the final de-interlaced video. This is a better vertical scaling but may be sensitive to fast motion video.

ODFST Alternate the first scaling line between Odd and Even fields.

0 Even field is the first scaled field.*

1 Odd field is the first scaled field.

VS Delay Control									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
0x3E	**VSDEL**	-	-	VSDEL[5:0]					

VSDEL[5:0] When the chip is programmed for digital video input operation, this register provides an offset for the internal line counter to align with input video (VS can be either from the VS pin or from embedded timing code). The register content is unsigned.

Command Register F									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
0x3F	**CMDF**	-	-	EVAVY	UVDLEN	UVDLSL	REGUD	TASKB	CBWI

CBWI — Chroma bandwidth increase.

- 0 — Normal chroma bandwidth.*
- 1 — Increased chroma bandwidth.

TASKB — Select between task A and B as described in "VIP Specification V. 1.0".

- 0 — Select CCIR 656 timing codes (T-bit is always 1).*
- 1 — Select between task A and B when VBI data is output. If active video is output, T-bit is set to 1(task A). If VBI data is output, T-bit is set to 0 (task B).

REGUD — Control register update control.

- 0 — Registers are updated immediately after being written to.*
- 1 — The following registers and register bits are updated only during the start of vertical sync after they are written to:
  Index 0x02, indices 0x17 through 0x1D, bit 0 of index 0x04, bits [2:0] and [6:4] of index 0x0E.

UVDLSL — U or V delay control when **UVDLEN** is set to 1.

- 0 — V is delayed by 1 CK period.*
- 1 — U is delayed by 1 CK period.

UVDLEN — Enable the function of **UVDLSL**.

- 0 — **UVDLSL** is disabled.*
- 1 — **UVDLSL** is enabled.

EVAVY — Control the output of INVALY, INVALU, and INVALV codes when EVAV is inactive.

- 0 — Output of these codes are not affected by EVAV.*
- 1 — These codes are output when EVAV is inactive (line is being dropped by the vertical scaler).

ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Value	Units
5-V supply voltage (measured to VSS)	V_{DD}	-0.5 to + 7.0	V
3.3-V supply voltage (measured to VSS)	V_{DD3}		V
Voltage on any digital pin	V_{PIN}	-0.5 to (V_{DD}+0.5)	V
Ambient operating temperature (case)	T_A	-10 to + 100	°C
Storage temperature	T_S	-65 to + 150	°C
Junction temperature	T_J	150	°C
Vapor phase soldering (1 min.)	Tvsol	220	°C

Notes: 1.Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions.
2.Functional operation under any of these conditions is not implied.
3.Applied voltage must be current limited to a specified range.

OPERATING CONDITIONS

Characteristics	Symbol	Min	Typ	Max	Units
5-V supply voltage (measured to VSS)	V_{DD}	4.75	5.0	5.25	V
3.3-V supply voltage (measured to VSS)			3.3		V
Ambient operating temperature, still air	T_A	0		70	°C

ELECTRICAL CHRACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Units
Supply					
+5V supply current	I_{DD5}	133	142	151	mA
+3.3V supply current	I_{DD3}	124	141	160	mA
Analog Characteristics					
Integral linearity error (AGC/ADC only)	$E_{I\text{-}ADC}$			1.5	lsb
Differential linearity error (AGC/ADC only)	$E_{D\text{-}ADC}$			0.75	lsb
Total harmonic distortion (4 MHz full scale)	THD		42		dB
Signal to noise ratio (4 MHz full scale)	SNR		42		dB
Analog bandwidth (50 IRE to 3 dB point)	BW	4			MHz
Input voltage range (peak-peak) 100 IRE input	$V_{I(PP)}$	0.5		1.5	V_{pp}
Input resistance AY0-AY2,AC0-AC2	R_{IN}	200			kΩ
Input capacitance for analog video inputs	C_{IN}		10		pF
Charge current for offset control	I_{OFF}		±4		μA
Cross talk between analog inputs	α			-50	dB
Video Performance					
Luminance frequency response (maximum variation to 4.2 MHz - multi burst)	F_{LUMA}		2		dB
Differential gain - complete chip (Modulated 40 IRE ramp)	D_G		1.5		%
Differential phase - complete chip (Modulated 40 IRE ramp)	D_P		1.0		degree
Chrominance frequency response (3 dB point) - CBWR=0/1	F_{CHROMA}		800/500		kHz
Chroma nonlinear gain distortion (NTC-7 Combination)	C_{NGD}		1		%
Chroma nonlinear phase distortion (NTC-7 Combination)	C_{NPD}		1.25		degree
Chroma to luma intermodulation (NTC-7 Combination)	C_{LI}		1		IRE
Chroma luma gain equality (NTC-7 Composite)	DEL_{CL}		±20		ns
Chroma luma delay equality (NTC-7 Composite)	AMP_{CL}		98-101		%
Noise level for unified weighting 10 kHz-5 MHz (100 IRE unmodulated ramp)	N_{LUMA}		-58		dB
Chroma AM noise (red field)	N_{CAM}		-60		dB
Chroma PM noise (red field)	N_{CPM}		-54		dB
Digital I/O Characteristics					
Input low voltage	V_{IL}	VSS-0.5		0.8	V
Input high voltage	V_{IH}	2.0		VDD+0.5	V

Characteristics	Symbol	Min	Typ	Max	Units
Input low current (V_{IN} = 0.4 V)	I_{IL}			-1	µA
Input high current(VIN=2.4)	I_{IH}			-1	µA
Digital output low voltage (I_{OL}=3.2mA)	V_{OL}			0.4	V
Digital output high voltage (IOH=400µA)	V_{OH}	2.4			V
Digital three-state current	I_{OZ}			50	µA
Digital output capacitance	C_{OUT}			7	pF
Maximum capacitance load for digital data pins	$C_{L\text{-}DATA}$			30	pF
Maximum capacitance load for CK and CK2 outputs	$C_{L\text{-}CK}$			60	pF
Timing Characteristics - Digital Inputs					
XTALI input pulse width low	t_{pwlX}	15	20		ns
XTALI input pulse width high	t_{pwhX}	15	20		ns
Clock and Data Timing					
Analog video input to digital video output delay	t_{dCHIP}		120		CK
Pulse width high for CK (KS0112 operates at frequencies from 24.5 MHz to 29 MHz)	t_{pwhCK}	15	18.5	22	ns
Pulse width high for CK2	t_{pwhCK2}	30	37	44	ns
Delay from rising edge of CK to CK2	t_{CK2}		1.5		ns
Delay from rising edge CK2 to data change (including pins Y0-Y7, C0-C7, HAV, VAV, EHAV, EVAV, HS1, HS2, VS, ODD, PID, SCH)	t_{dD}		20		ns
Minimum hold time from rising edge of CK2 for data output)	t_{hD}	7			ns
Delay from falling edge of OEN to data bits in 3-state	t_{zD}			30	ns
Delay from rising edge OEN to data bits enabled	t_{enD}			35	ns
Timing Characteristics -I2C Host Interface					
SCLK clock frequency	r_{SCLK}	0		400	kHz
Capacitive load for each bus line	C_b			400	pF
Hold time for START condition	t_{hSTA}	0.6			µs
Setup time for STOP condition	t_{sSTO}	0.6			µs
Rise and fall times for SCLK and SDAT	t_R, t_F	20		300	ns
SCLK minimum pulse width low	$t_{pwlSCLK}$	1.3			µs
SCLK minimum pulse width high	$t_{pwhSCLK}$	0.6			µs
SDAT setup time to rising edge of SCLK	t_{SSDAT}	100			ns
SDAT hold time from rising edge of SCLK	t_{hSDAT}	0			ns

Note: AC/DC characteristics provided are per design specifications.

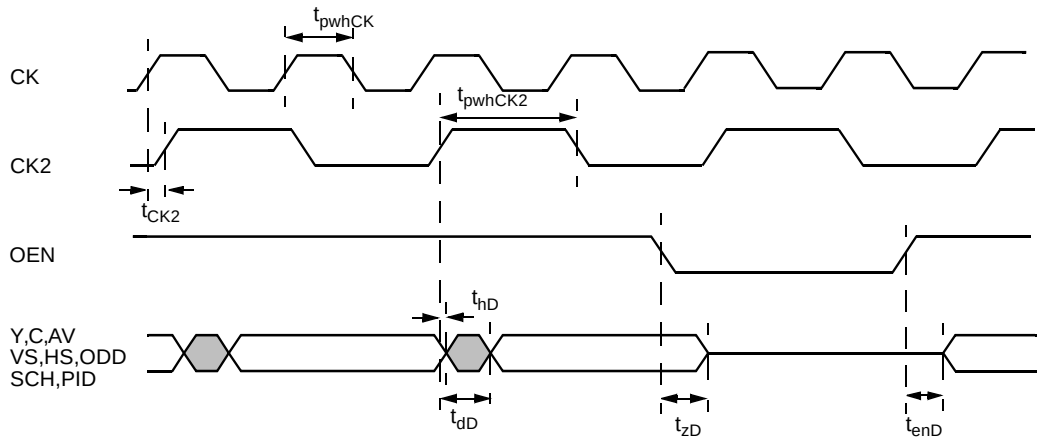


Figure 39. Data Output

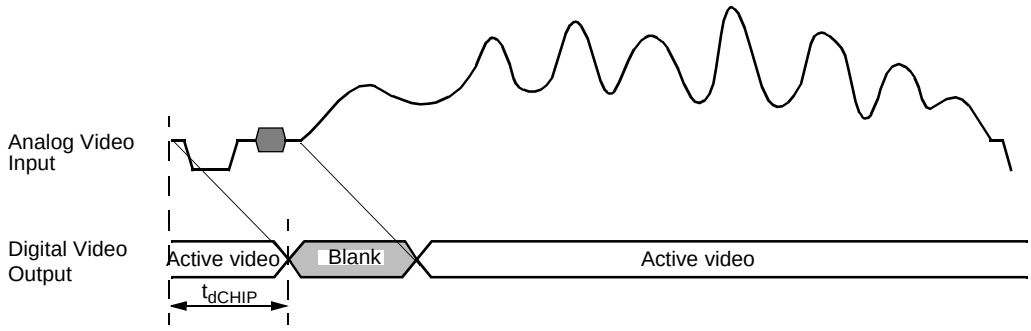


Figure 40. Analog Video Input to Digital Video Output Delay

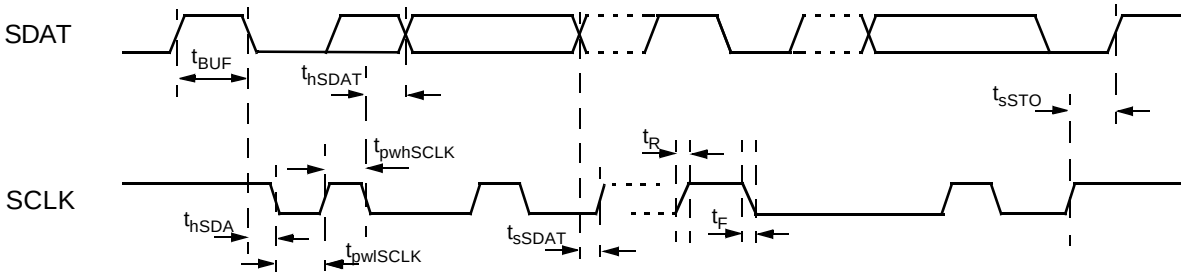


Figure 41. IIC Host Interface Detailed Timing

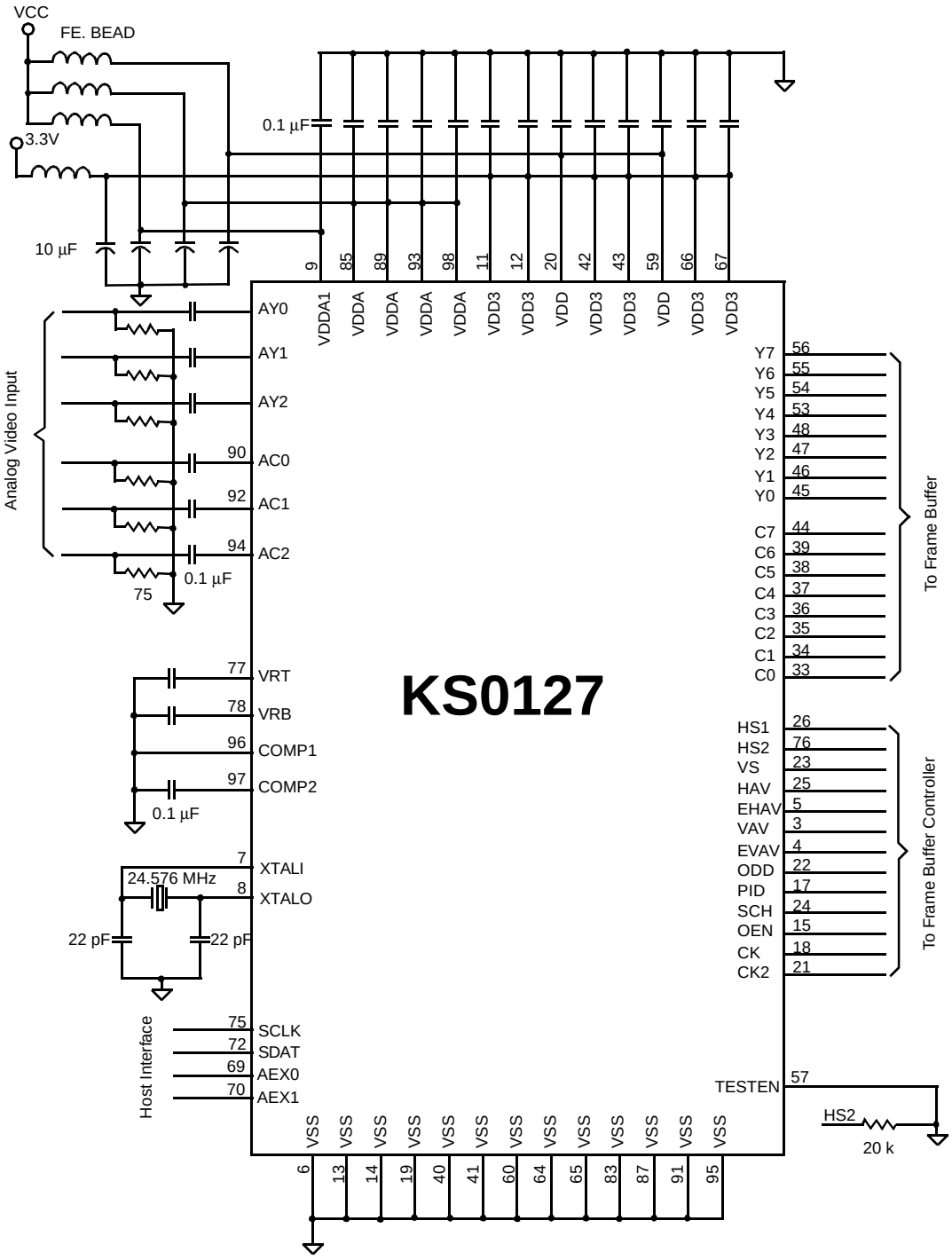
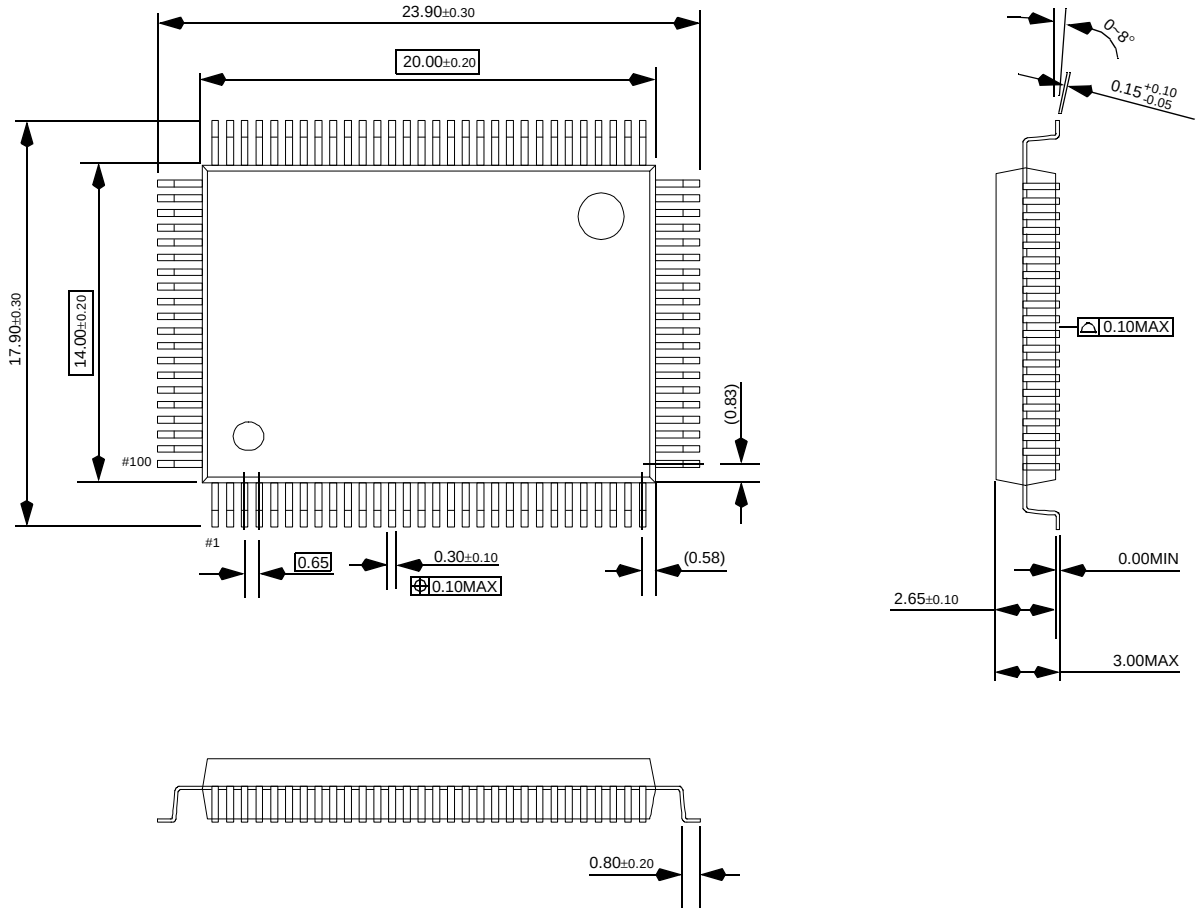


Figure 42. KS0127 Application Circuit Example

Package Dimension

100-QFP-1420C



Dimensions are in Millimeters