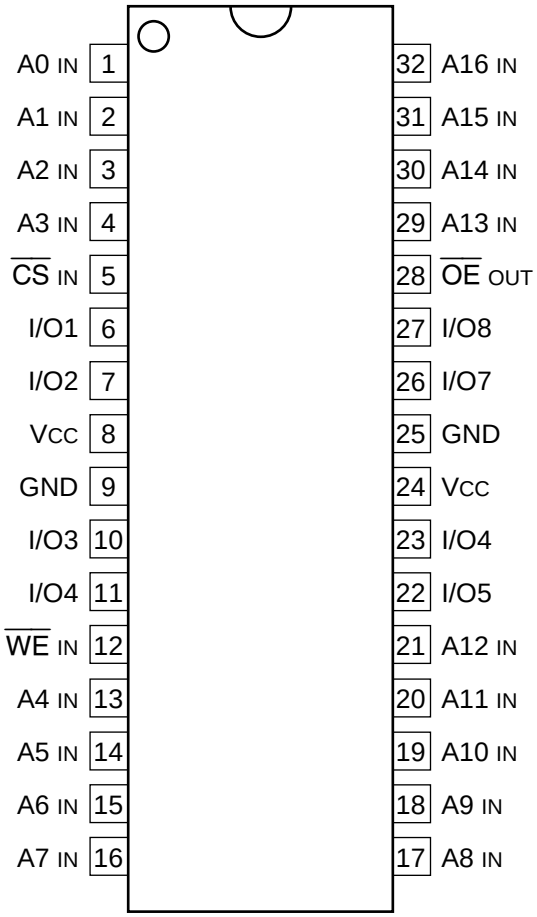
1M (128 K × 8)-BIT SRAM

—TOP VIEW—



INPUTS

A0 - A16 : ADDRESS
CS : CHIP SELECT
WE : WRITE ENABLE

OUTPUT

OE : ENABLE

INPUTS/OUTPUTS

I/O1 - I/O8 : DATA