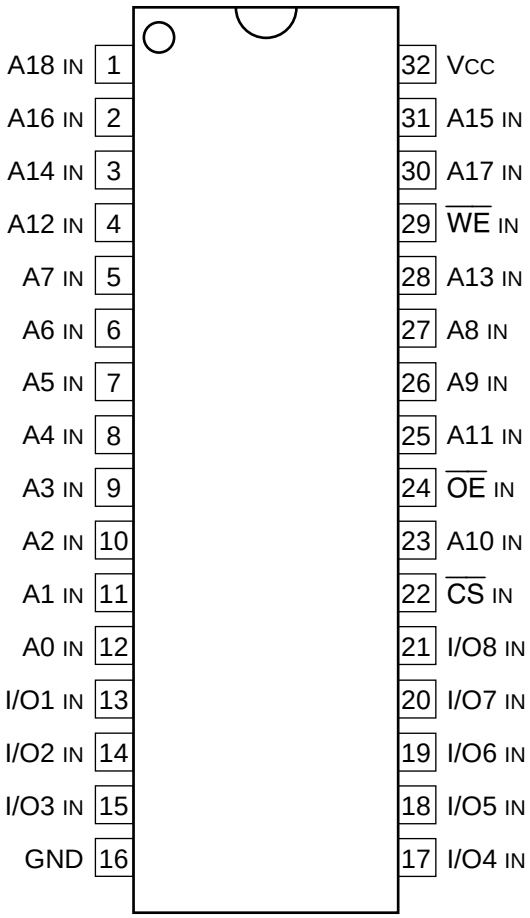
4 M (524,288 × 8)-BIT SRAM

—TOP VIEW—



INPUTS

A0 - A18 : ADDRESS
$\overline{CS}$: CHIP SELECT
$\overline{OE}$: OUTPUT ENABLE
$\overline{WE}$: WRITE ENABLE

INPUTS/OUTPUTS

I/O0 - I/O8 : DATA