16M x 4bit CMOS Dynamic RAM with Fast Page Mode

DESCRIPTION

This is a family of 16,777,216 x 4 bit Fast Page Mode CMOS DRAMs. Fast Page Mode offers high speed random access of memory cells within the same row. Refresh cycle(4K Ref. or 8K Ref.), access time(-5 or -6), package type(SOJ or TSOP-II) are optional features of this family. All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities. This 16Mx4 Fast Page Mode DRAM family is fabricated using Samsung′s advanced CMOS process to realize high band-width, low power consumption and high reliability.

FEATURES

- **Part Identification**

  - KM44C16000B(5.0V, 8K Ref.)
  - KM44C16100B(5.0V, 4K Ref.)

- **Active Power Dissipation**

Unit : mW

Speed	8K	4K
-5	495	660
-6	440	609

- **Refresh Cycles**

Part NO.	Refresh cycle	Refresh time
		Normal
KM44C16000B*	8K	64ms
KM44C16100B	4K	

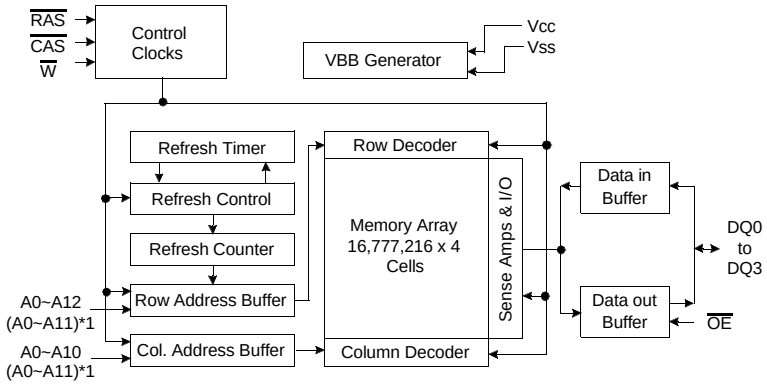
* Access mode & $\overline{RAS}$ only refresh mode
: 8K cycle/64ms
$\overline{CAS}$-before-$\overline{RAS}$ & Hidden refresh mode
: 4K cycle/64ms

- **Performance Range**

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{PC}
-5	50ns	13ns	90ns	35ns
-6	60ns	15ns	110ns	40ns

- Fast Page Mode operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- Fast parallel test mode capability
- TTL(5.0V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC Standard pinout
- Available in Plastic SOJ and TSOP(II) packages
- +5.0V±10% power supply

FUNCTIONAL BLOCK DIAGRAM



Note) *1 : 4K Refresh

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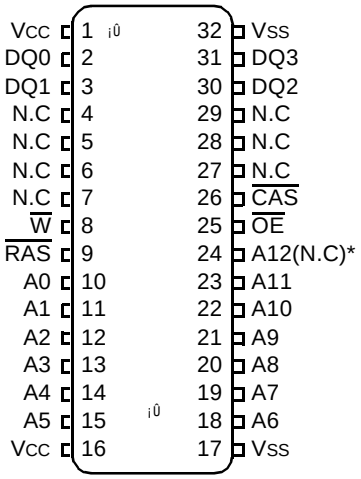
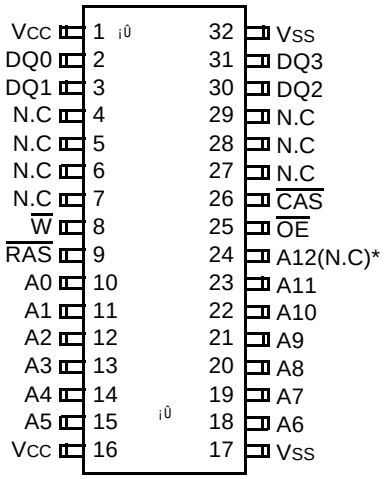
PIN CONFIGURATION (Top Views)

• **KM44C160(1)00BK**



(K : 400mil SOJ)

• **KM44C160(1)00BS**



(S : 400mil TSOP(II))

* (N.C) : N.C for 4K Refresh product

Pin Name	Pin Function
A0 - A12	Address Inputs(8K Product)
A0 - A11	Address Inputs(4K Product)
DQ0 - 3	Data In/Out
VSS	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Outputs Enable
VCC	Power(+5.0V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN},V_{OUT}	-1.0 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-1.0 to +7.0	V
Storage Temperature	Tstg	-55 to +150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A= 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	V_{CC}*1	V
Input Low Voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : V_{CC}+2.0V at pulse width≤20ns which is measured at V_{CC}
*2 : -2.0 at pulse width≤20ns which is measured at V_{SS}

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input 0≤V_{IN}≤V_{CC}+0.5V, all other pins not under test=0 Volt)	$I_{I(L)}$	-5	5	uA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤V_{CC})	$I_{O(L)}$	-5	5	uA
Output High Voltage Level(IOH=-5mA)	V_{OH}	2.4	-	V
Output Low Voltage Level(IOL=4.2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS (Continued)

Symbol	Power	Speed	Max		Units
			KM44C16000B	KM44C16100B	
I_{CC1}	Don't care	-5 -6	90 80	120 110	mA mA
I_{CC2}	Normal	Don't Care	2	2	mA
I_{CC3}	Don't care	-5 -6	90 80	120 110	mA mA
I_{CC4}	Don't care	-5 -6	60 50	70 60	mA mA
I_{CC5}	Normal	Don't Care	1	1	mA
I_{CC6}	Don't care	-5 -6	120 110	120 110	mA mA

I_{CC1}* : Operating Current ($\overline{RAS}$ and $\overline{CAS}$, Address cycling @t_{RC}=min.)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}* : $\overline{RAS}$-only Refresh Current ($\overline{CAS}$=V_{IH}, $\overline{RAS}$, Address cycling @t_{RC}=min.)

I_{CC4}* : Fast Page Mode Current ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address cycling @t_{PC}=min.)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)

I_{CC6}* : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

***Note :** I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1}, I_{CC3} and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one fast page mode cycle time, t_{PC}.

CAPACITANCE (T_A=25°C, V_{CC}=5.0V, f=1MHz)

Parameter	Symbol	Min	Max	Units
Input capacitance [A0 ~ A12]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output capacitance [DQ0 - DQ3]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 2)

Test condition : V_{CC}=5.0V±10%, Vih/Vil=2.4/0.8V, Voh/Vol=2.4/0.4V

Parameter	Symbol	-5		-6		Units	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		ns	
Read-modify-write cycle time	t_{RWC}	133		153		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		13		15	ns	3,4,5
Access time from column address	t_{AA}		25		30	ns	3,10
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	13	0	13	ns	6
Transition time (rise and fall)	t_T	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15		ns	
$\overline{CAS}$ hold time	t_{CSH}	50		60		ns	
$\overline{CAS}$ pulse width	t_{CAS}	13	10K	15	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	37	20	45	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		ns	
Row address set-up time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	10		10		ns	
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	10		10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		ns	
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		ns	8
Write command hold time	t_{WCH}	10		10		ns	
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		15		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	13		15		ns	
Data set-up time	t_{DS}	0		0		ns	9
Data hold time	t_{DH}	10		10		ns	9

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		Units	Note
		Min	Max	Min	Max		
Refresh period (4K, Normal)	t_{REF}		64		64	ms	
Refresh period (8K, Normal)	t_{REF}		64		64	ms	
Write command set-up time	t_{WCS}	0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	36		38		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	73		83		ns	7
Column address to $\overline{W}$ delay time	t_{AWD}	48		53		ns	7
$\overline{CAS}$ precharge $\overline{W}$ delay time	t_{CPWD}	53		60		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$ -before-$\overline{RAS}$ refresh)	t_{CSR}	5		5		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$ -before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		ns	13
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		30		35	ns	3
Fast Page mode cycle time	t_{PC}	35		40		ns	
Fast Page mode read-modify-write cycle time	t_{PRWC}	76		85		ns	
$\overline{CAS}$ precharge time (Fast Page cycle)	t_{CP}	10		10		ns	
$\overline{RAS}$ pulse width (Fast Page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	30		35		ns	
$\overline{OE}$ access time	t_{OEA}		13		15	ns	
$\overline{OE}$ to data delay	t_{OED}	13		13		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	0	13	0	13	ns	6
$\overline{OE}$ command hold time	t_{OEH}	13		15		ns	
Write command set-up time (Test mode in)	t_{WTS}	10		10		ns	11
Write command hold time (Test mode in)	t_{WTH}	15		15		ns	11
$\overline{W}$ to $\overline{RAS}$ precharge time (CBR refresh)	t_{WRP}	10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time (CBR refresh)	t_{WRH}	10		10		ns	

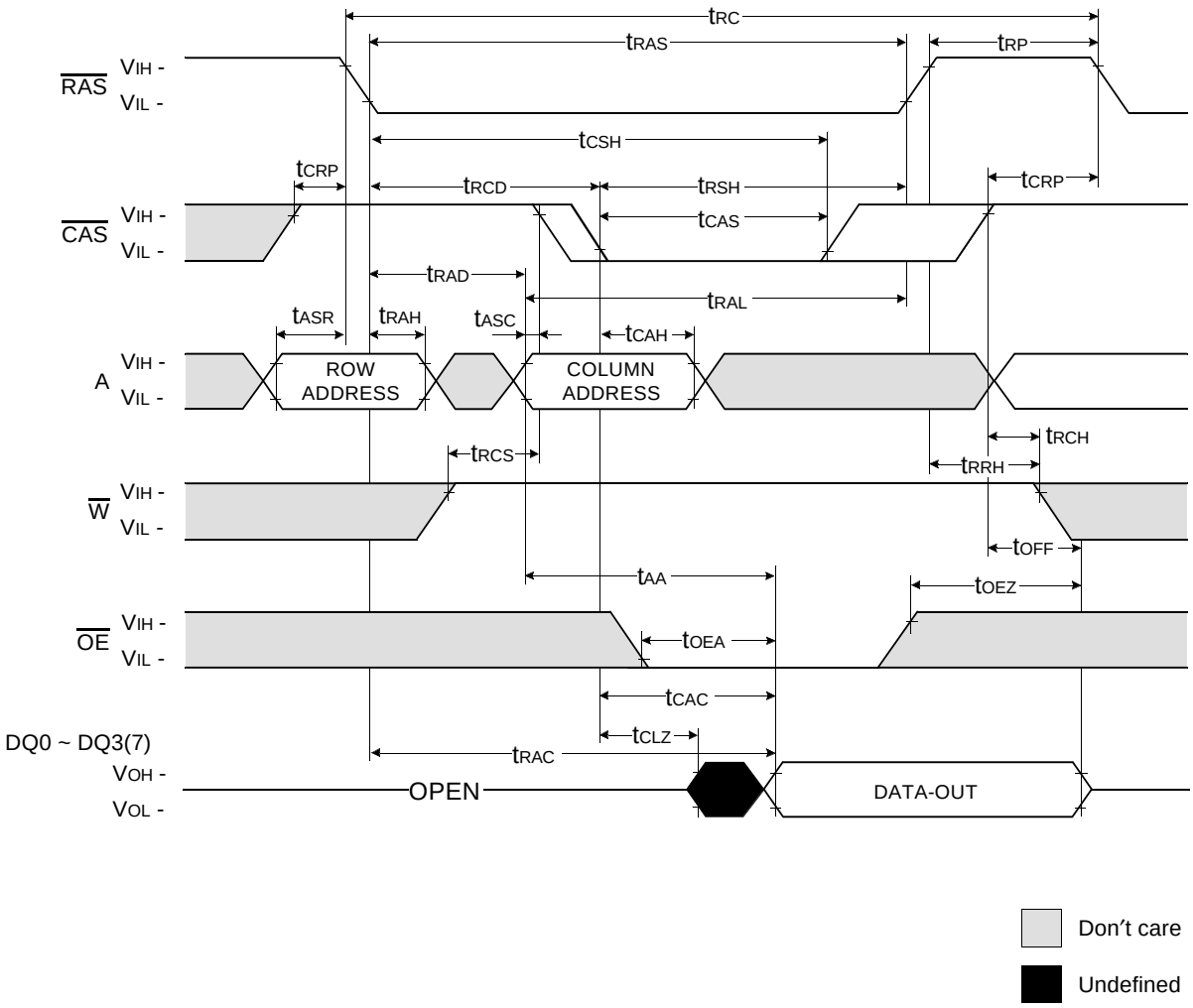
TEST MODE CYCLE

Parameter	Symbol	-5		-6		Units	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	95		115		ns	
Read-modify-write cycle time	t_{RWC}	138		160		ns	
Access time from $\overline{RAS}$	t_{RAC}		55		65	ns	3,4,10,12
Access time from $\overline{CAS}$	t_{CAC}		18		20	ns	3,4,5,12
Access time from column address	t_{AA}		30		35	ns	3,10,12
$\overline{RAS}$ pulse width	t_{RAS}	55	10K	65	10K	ns	
$\overline{CAS}$ pulse width	t_{CAS}	18	10K	20	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	18		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	55		65		ns	
Column Address to $\overline{RAS}$ lead time	t_{RAL}	30		35		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	41		43		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	78		88		ns	7
Column Address to $\overline{W}$ delay time	t_{AWD}	53		58		ns	7
Fast Page mode cycle time	t_{PC}	40		45		ns	
Fast Page mode read-modify-write cycle time	t_{PRWC}	81		90		ns	
$\overline{RAS}$ pulse width (Fast Page cycle)	t_{RASP}	55	200K	65	200K	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40	ns	3
$\overline{OE}$ access time	t_{OEA}		18		20	ns	
$\overline{OE}$ to data delay	t_{OED}	18		18		ns	
$\overline{OE}$ command hold time	t_{OEH}	18		20		ns	

NOTES

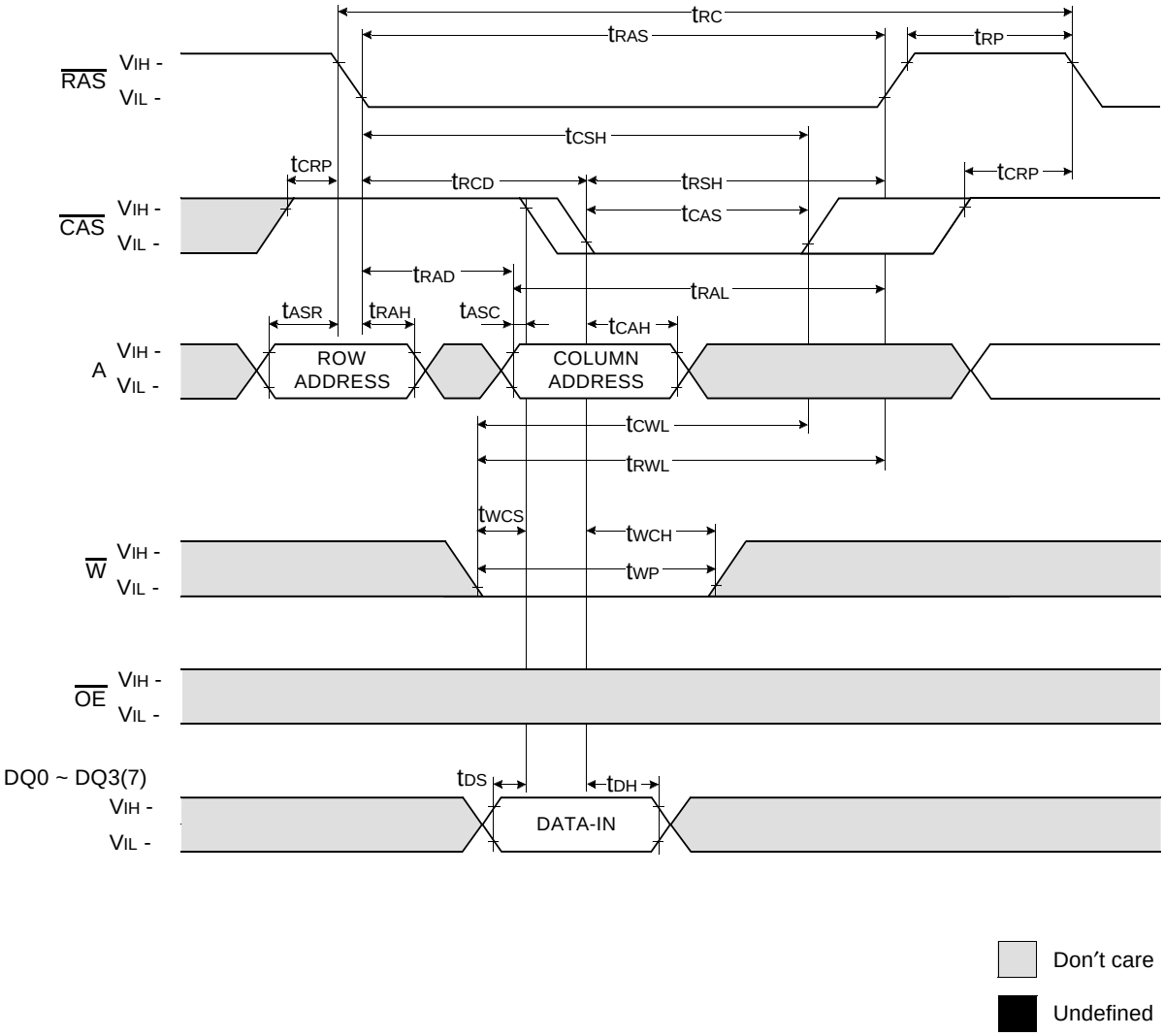
1. An initial pause of 200§Á is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL load and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. t_{OFF}(min)and t_{OEZ}(max) define the time at which the output achieves the open circuit condition and are not referenced V_{oh} or V_{ol}.
7. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}$(min), the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ falling edge in early write cycles and to the $\overline{W}$ falling edge in read-modify-write cycles.
10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
11. These specifications are applied in the test mode.
12. In test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} is delayed by 2ns to 5ns for the specified values. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
13. It can get less $\overline{CAS}$-before-$\overline{RAS}$ current loss if $t_{CHR} \geq t_{RAS}$ or $\overline{CAS} \leq 0.2V$ at $\overline{CAS}$-before $\overline{RAS}$ refresh mode.

READ CYCLE


tRC
tRAS
tRP
RAS
VIH -
VIL -
tCSH
tCRP
tRCD
tRSH
tCRP
CAS
VIH -
VIL -
tCAS
tRAD
tRAL
tASR
tRAH
tASC
tCAH
A
VIH -
VIL -
ROW ADDRESS
COLUMN ADDRESS
tRCH
tRCS
tRRH
W
VIH -
VIL -
tOFF
tAA
tOEZ
OE
VIH -
VIL -
tOEA
tCAC
tCLZ
DQ0 ~ DQ3(7)
tRAC
VOH -
VOL -
OPEN
DATA-OUT
Don't care
Undefined

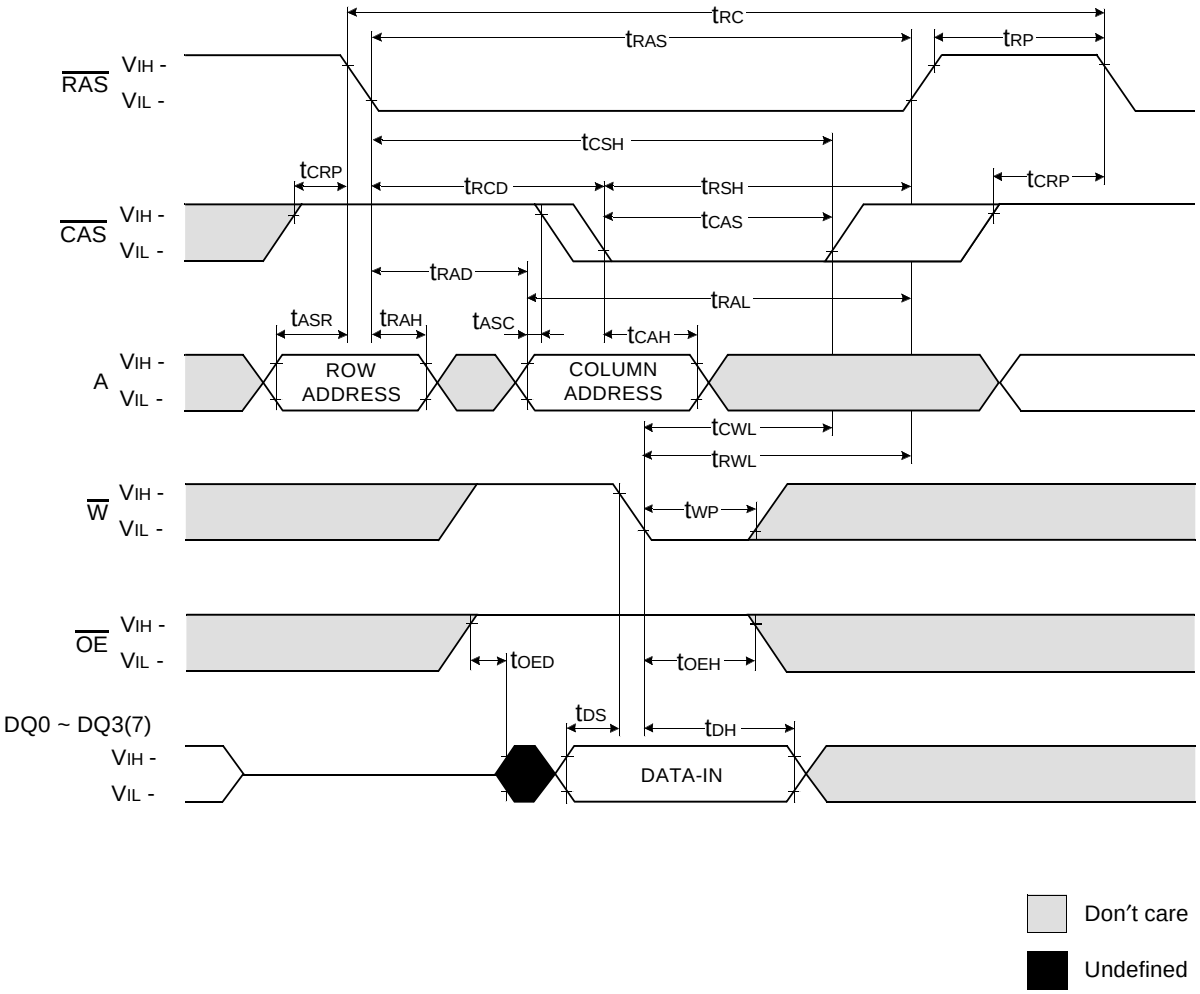
WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN

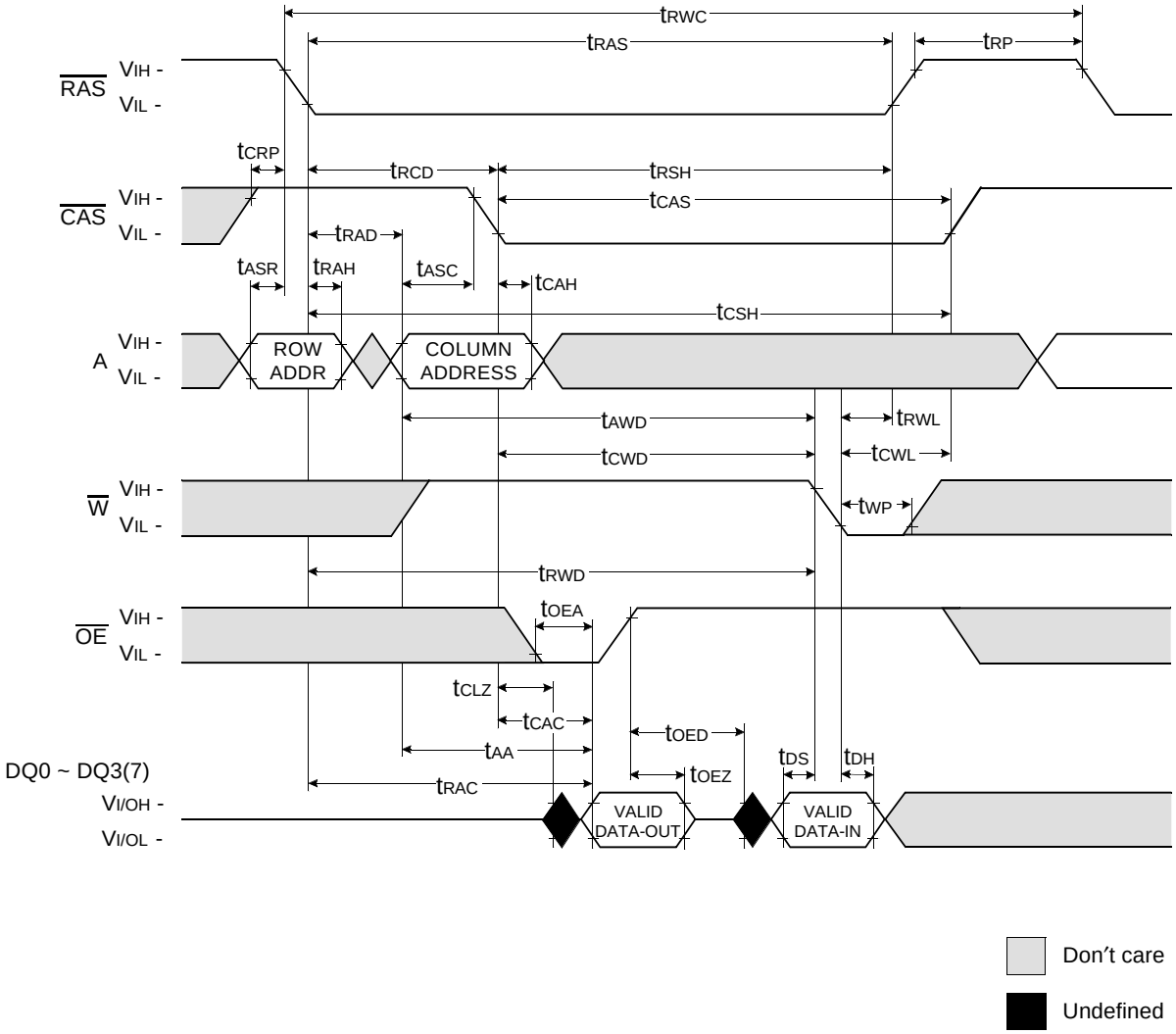


WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

NOTE : DOUT = OPEN

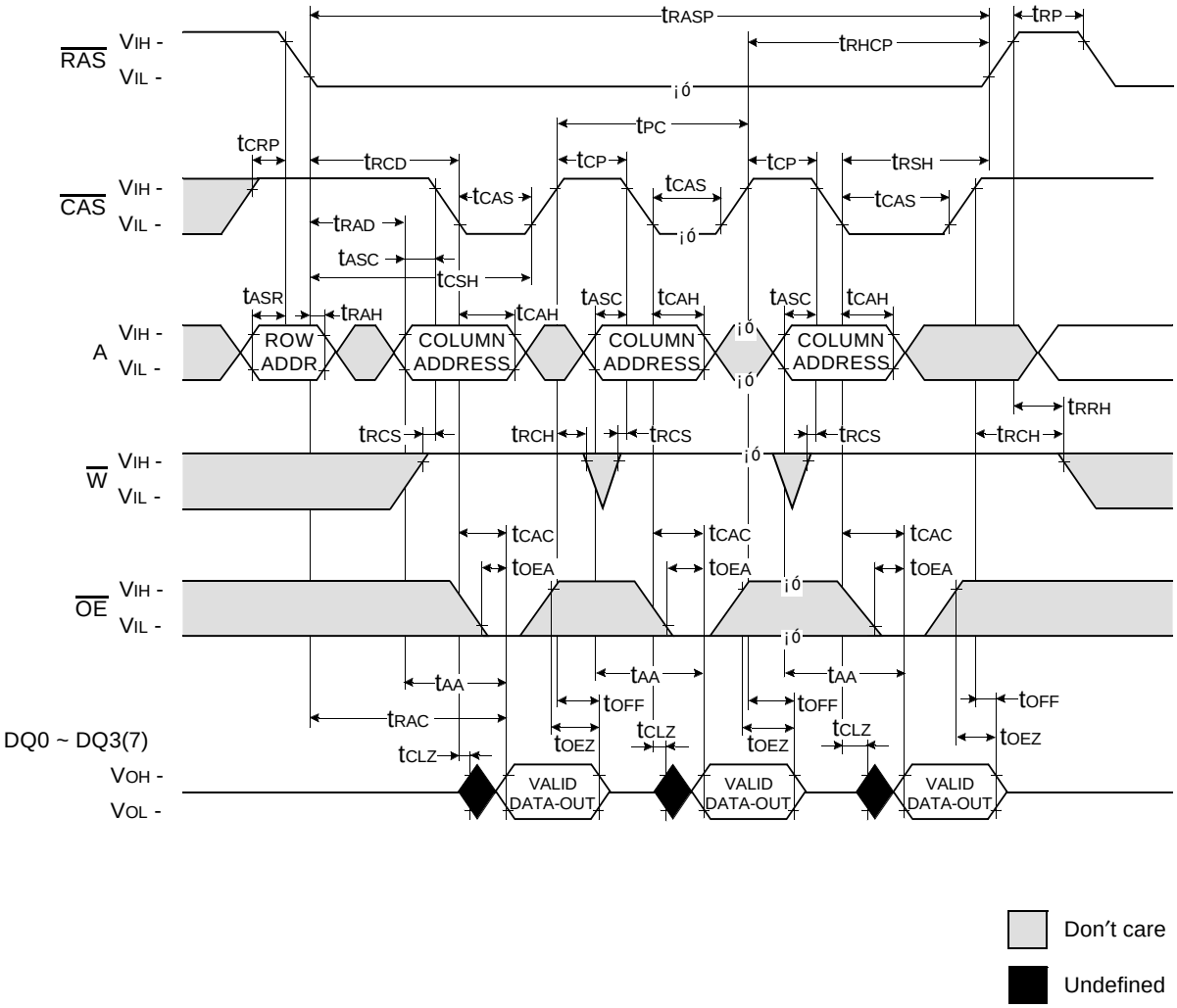


READ - MODIFY - WRTIE CYCLE



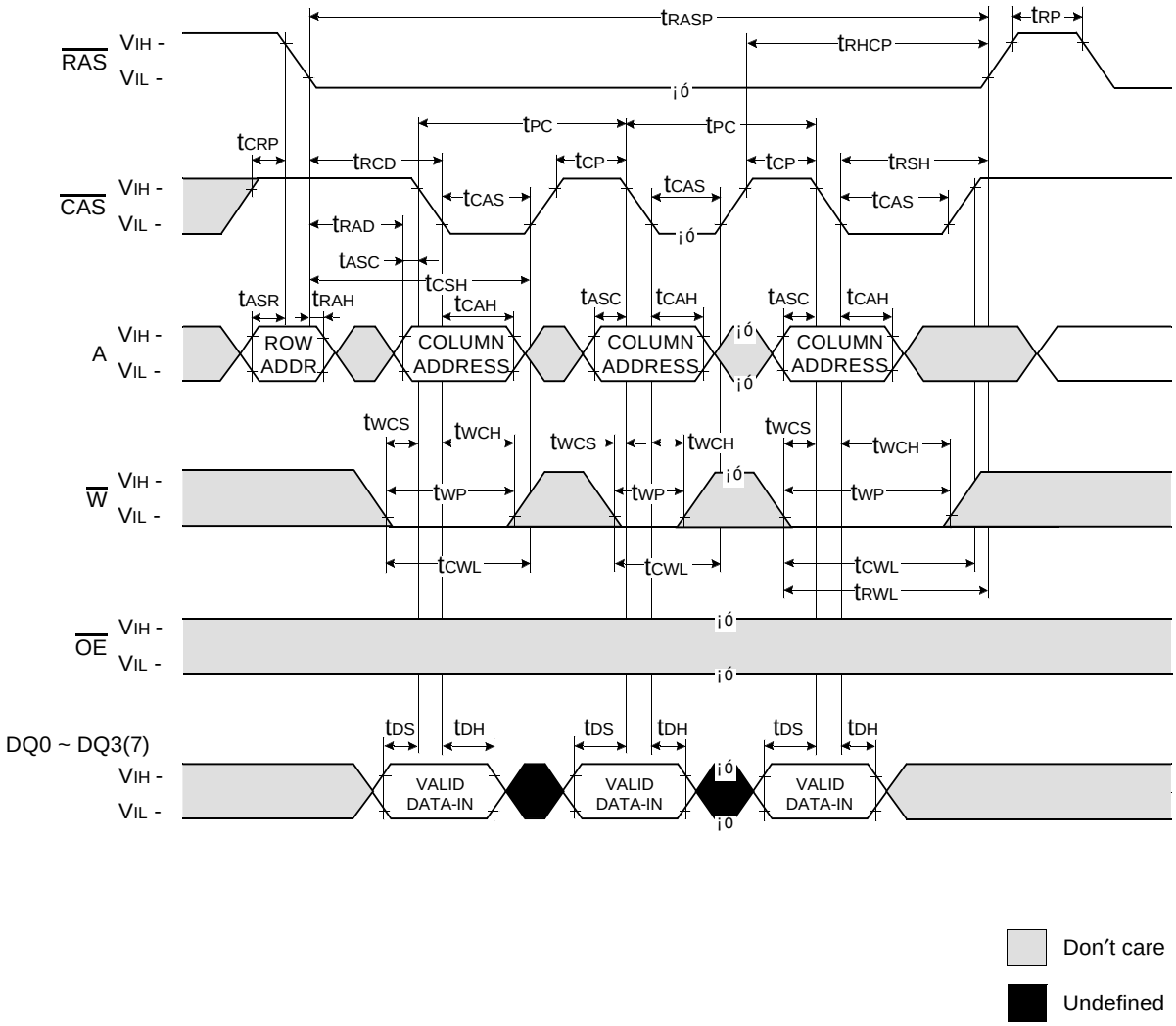
FAST PAGE READ CYCLE

NOTE : DOUT = OPEN

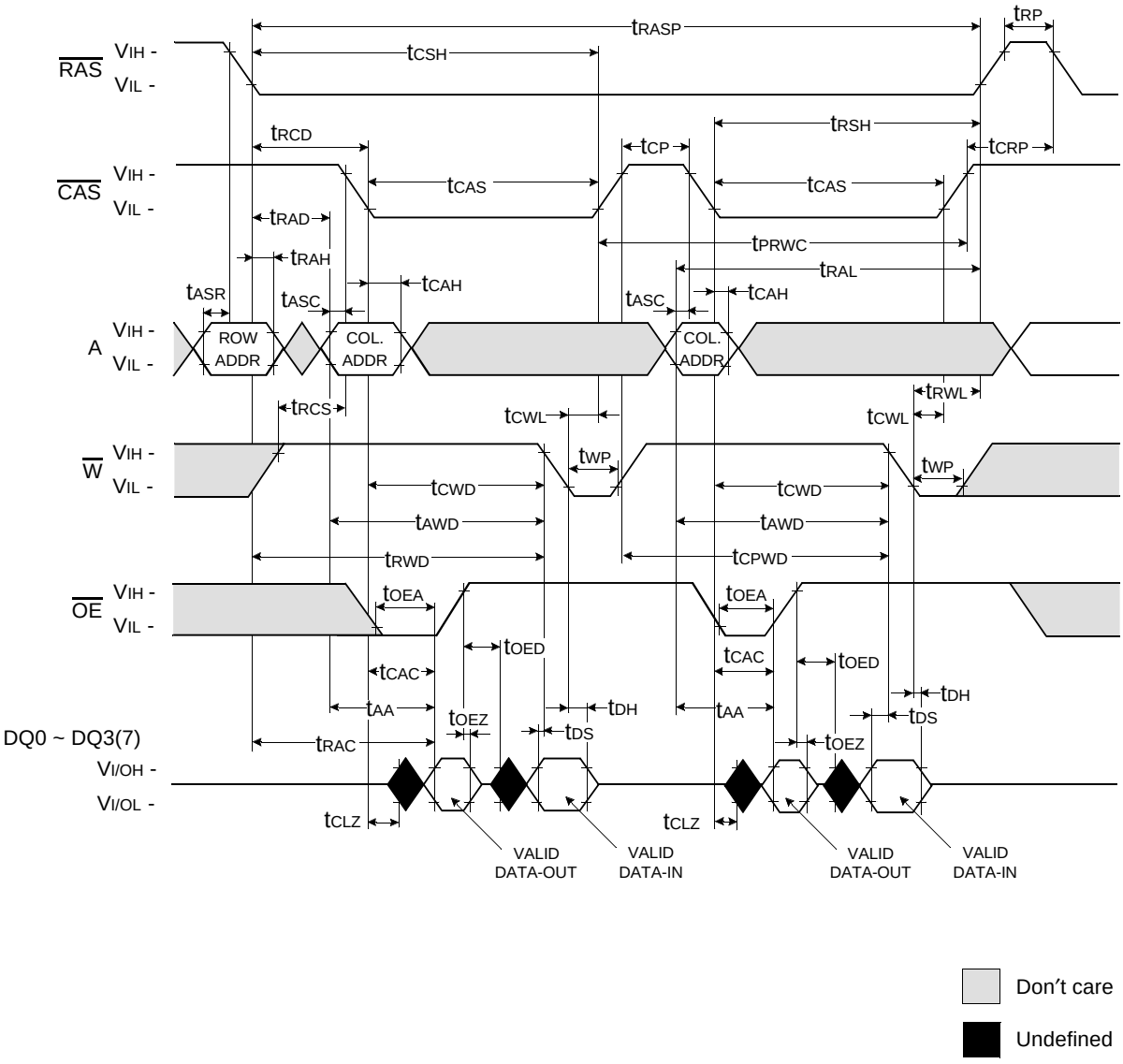


FAST PAGE WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN



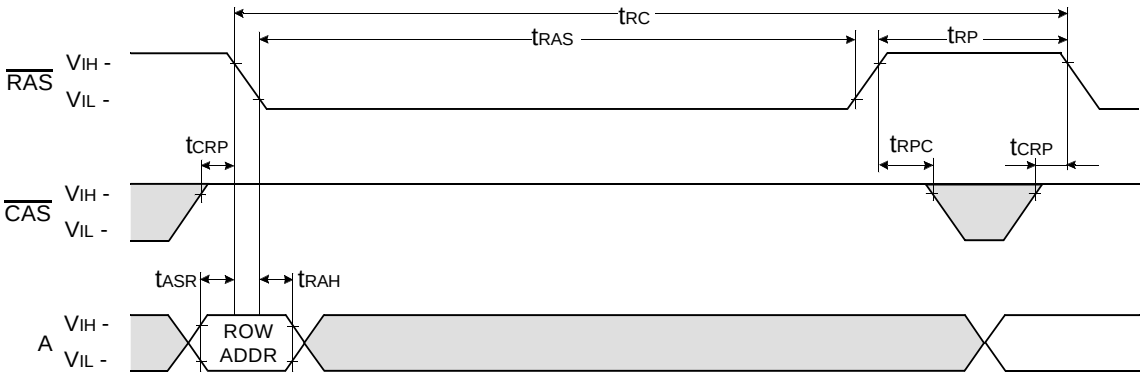
FAST PAGE READ - MODIFY - WRITE CYCLE



$\overline{RAS}$ - ONLY REFRESH CYCLE

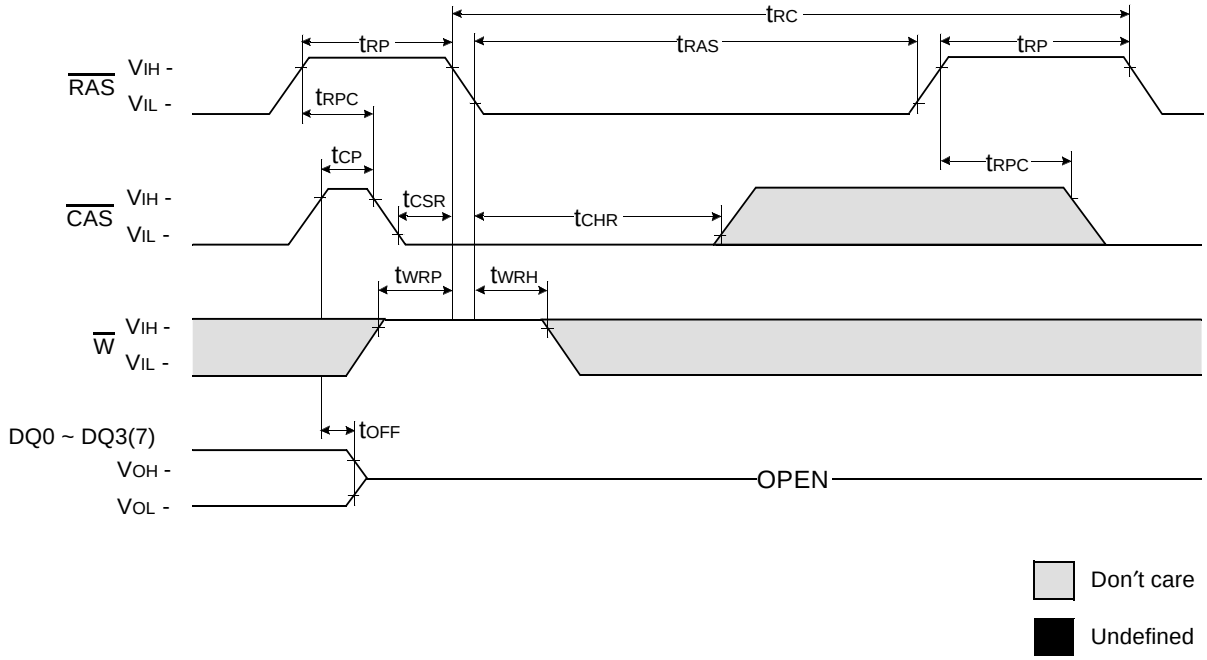
NOTE : $\overline{W}$, $\overline{OE}$, D_{IN} = Don't care

D_{OUT} = OPEN

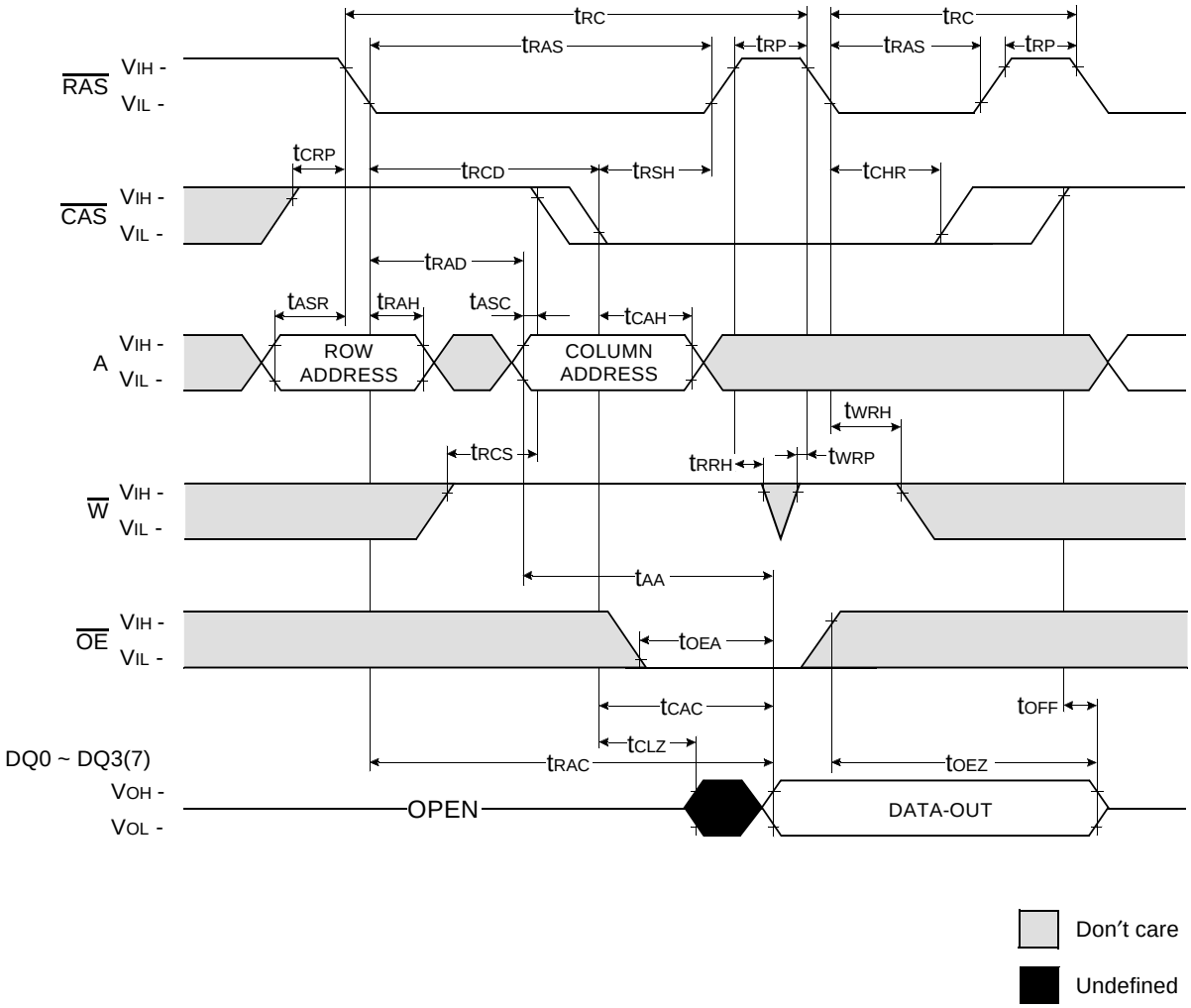


$\overline{CAS}$ - BEFORE - $\overline{RAS}$ REFRESH CYCLE

NOTE : $\overline{OE}$, A = Don't care

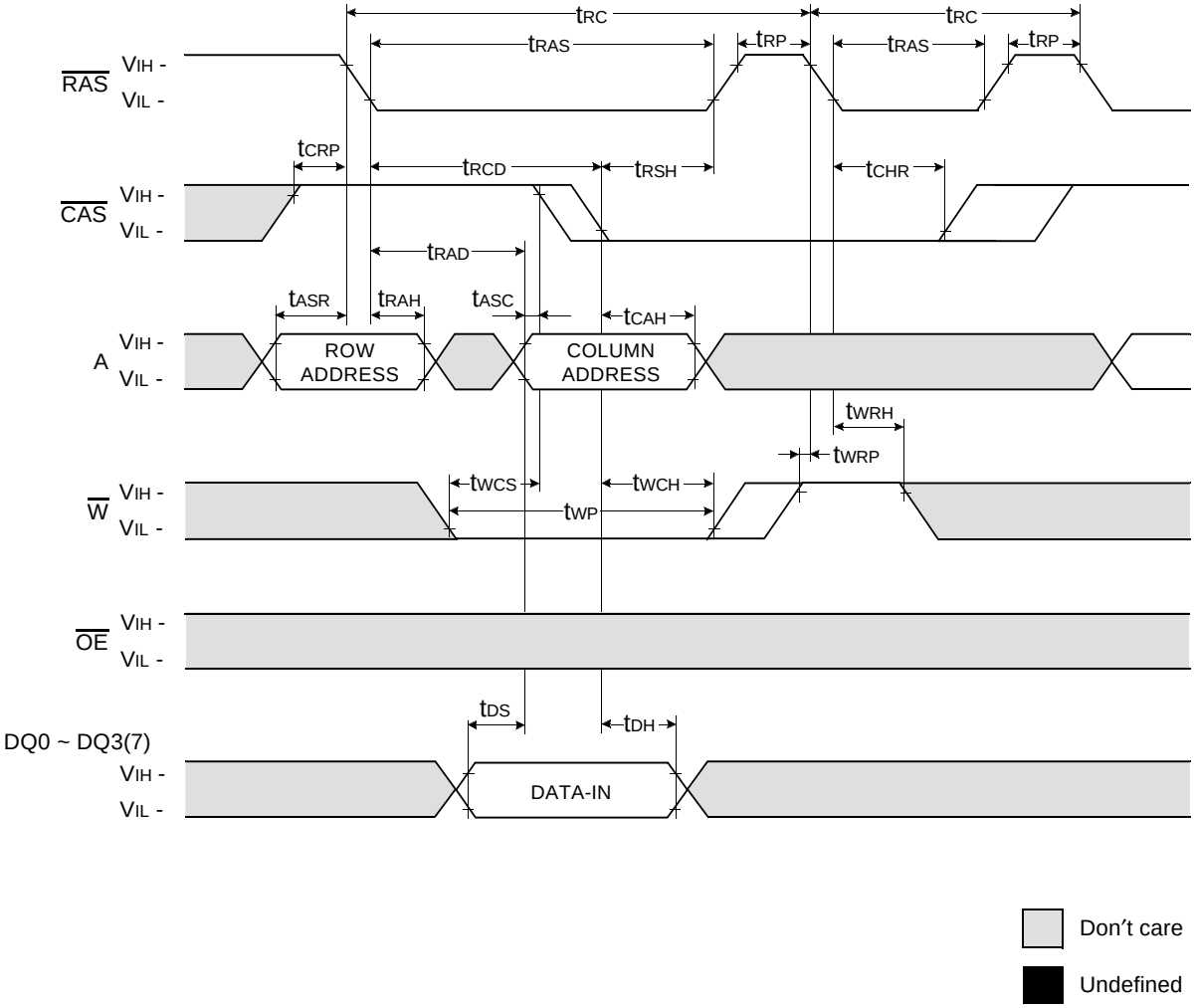


HIDDEN REFRESH CYCLE (READ)

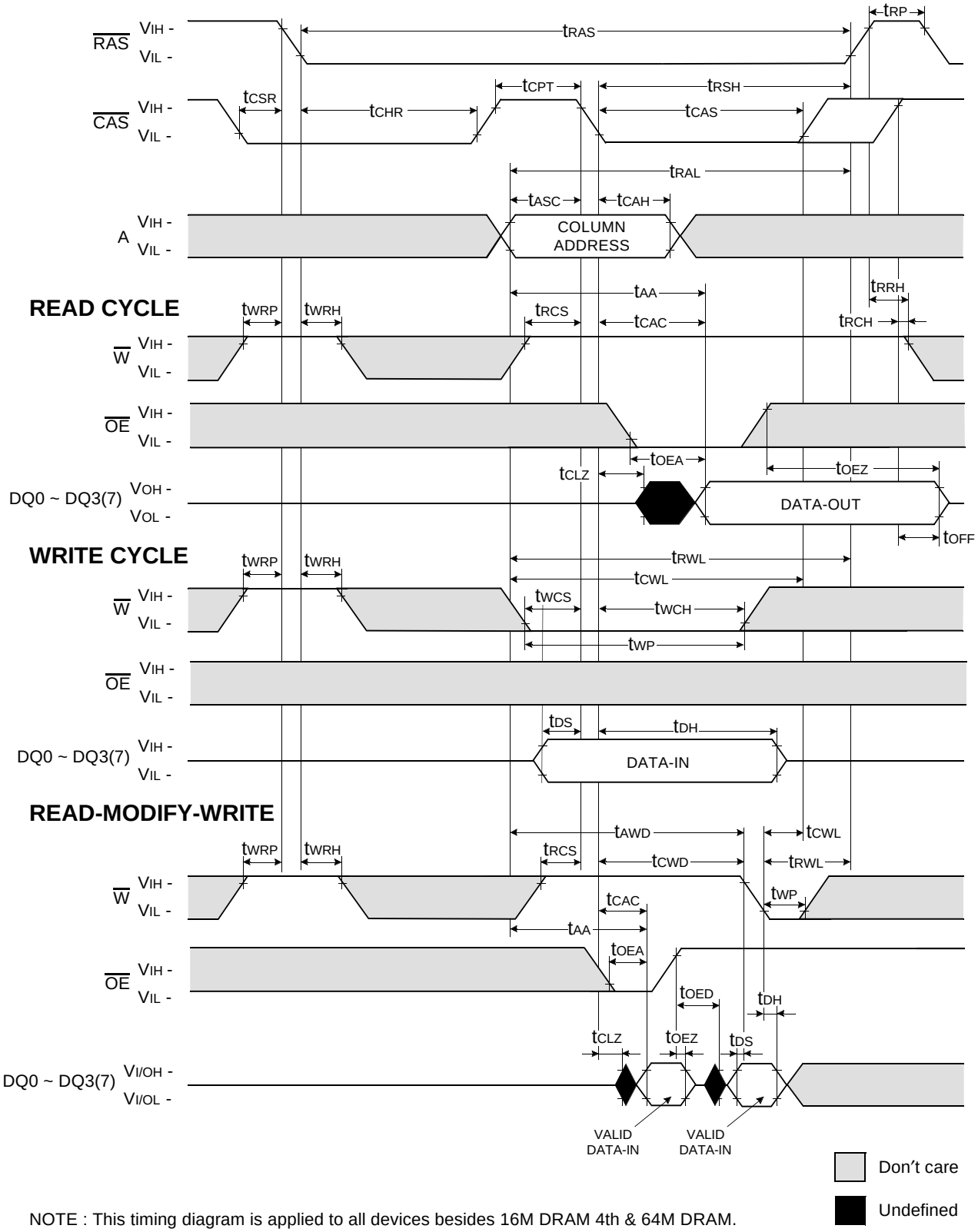


HIDDEN REFRESH CYCLE (WRITE)

NOTE : DOUT = OPEN



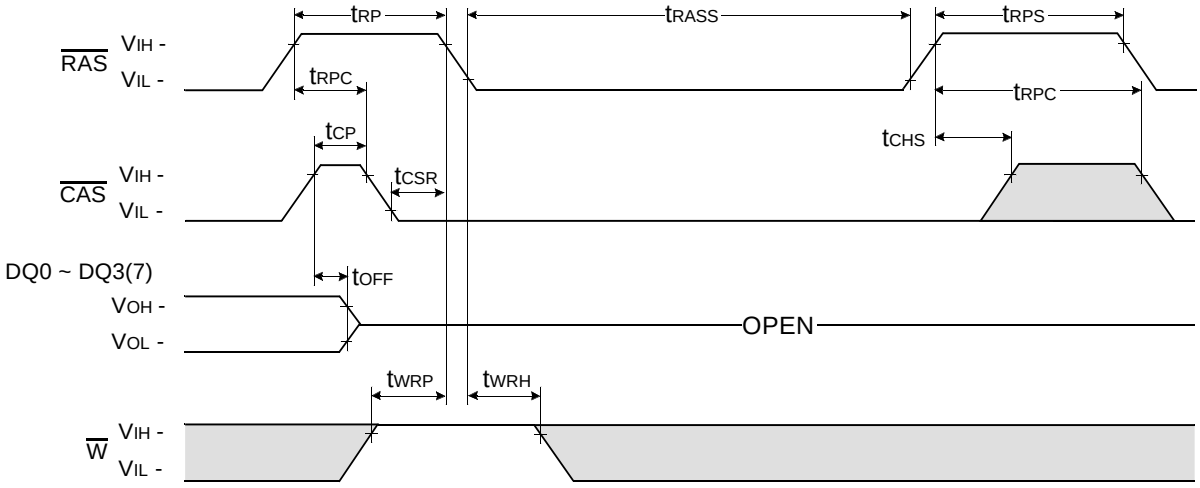
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



NOTE : This timing diagram is applied to all devices besides 16M DRAM 4th & 64M DRAM.

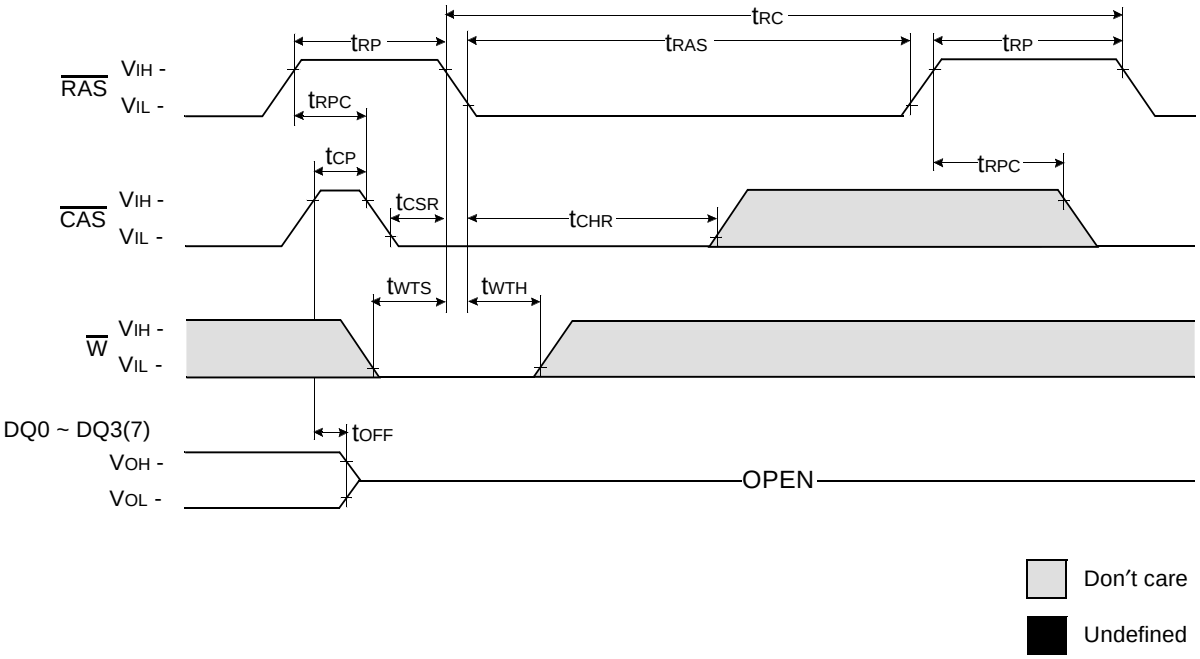
$\overline{CAS}$ - BEFORE - $\overline{RAS}$ SELF REFRESH CYCLE

NOTE : $\overline{OE}$, A = Don't care



TEST MODE IN CYCLE

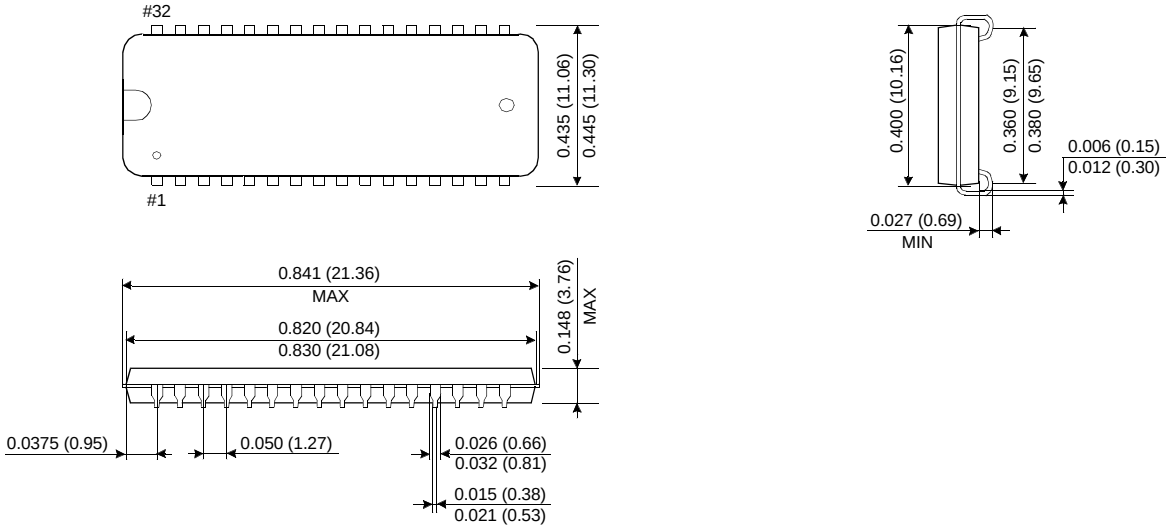
NOTE : $\overline{OE}$, A = Don't care



PACKAGE DIMENSION

32 SOJ 400mil

Units : Inches (millimeters)



32 TSOP(II) 400mil

Units : Inches (millimeters)