8M Bit (1M x8/512K x16) NOR Flash Memory

FEATURES

- Single Voltage, 2.7 to 3.6 V for Read and Write operations
- Organization
  1,048,576 x 8 bit (Byte mode) / 524,288 x 16 bit (Word mode)
- Fast Read Access Time : 90ns
- Byte & Word programming
- Block Architectures :
  19 separately erasable asymmetrical blocks
- Power Consumption
  - Read Current : 7mA (typical)
  - Program/Erase Current : 20mA (typical)
  - Standby Mode/Auto Sleep Mode : 200nA (typical)
- Internal Program/Erase Routines
- Data Polling and Toggle Bit features for detection of program/erase cycle completion
- Erase Suspend/Resume
- Hardware RESET Pin
- Command Register Operation
- Endurance : 100,000 Program/Erase Cycles Minimum
- Data Retention : 10 years
- Package : 48 pin TSOP Type1 : 12 x 20 / 0.5 mm pitch

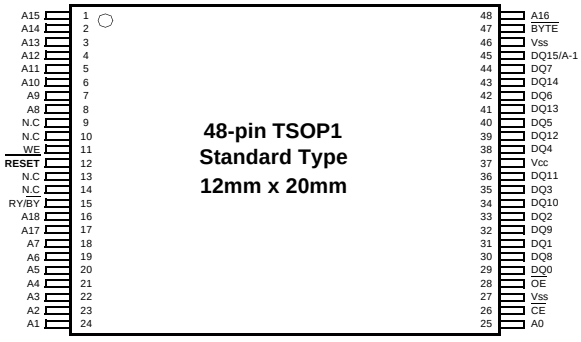
GENERAL DESCRIPTION

The KM28U800 featuring single 3.0 V power supply, is an 8Mbit NOR-type Flash Memory organized as 1M x8 or 512K x16. The memory architecture of the device is designed to divide its memory arrays into 19 blocks with independent hardware protection. This block architecture provides highly flexible erase and program capability.

Access times of 90ns, 100ns, 120ns and 150ns are available for the device. The device's fast access times allow high speed microprocessors to operate without wait states. The device performs a program operation in units of 8bits (Byte) or 16bits (Word) and erases in units of a block. Single or multiple blocks can be erased. The block erase operation is completed within typically 1sec. The device requires 20mA as program/erase current over the standard and industrial temperature ranges and less than 1μA at Stand-by/Autosleep modes.

The KM28U800 NOR Flash Memory is created by using Samsung′s advanced CMOS process technology. This device is available in 48-pin TSOP packages. The device is compatible with EPROM applications requiring high-density and cost-effective nonvolatile read/write storage solutions.

PIN CONFIGURATION



Note :
Please refer to the last page for package dimension.

PIN DESCRIPTION

Pin Name	Pin Function
A0 - A18	Address Inputs
DQ0 - DQ14	Data Inputs / Outputs
DQ15/A-1	DQ15 Data Input / Output A-1 LSB Address
$\overline{BYTE}$	Word / Byte Selection
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{RESET}$	Hardware Reset Pin
RY/$\overline{BY}$	Ready/Busy output
$\overline{WE}$	Write Enable
Vcc	Power Supply
VSS	Ground
N.C	No Connection

ORDERING INFORMATION

K M 2 8 U 8 0 0 I T - T 9

Samsung
NOR Flash Memory

Operating Voltage Range
2.7V to 3.6V

Density / Organization
8Mbit, x8/x16 Selectable

Operating Temperature Range
Blank = Standard Temp. (0 °C to 70 °C)
I = Industrial Temp. (-40 °C to 85 °C)

Access Time
9 = 90 ns
10 = 100 ns
12 = 120 ns
15 = 150 ns

Block Architecture
T = Top Boot Block

Package
T = 48 TSOP1

Figure 1. FUNCTIONAL BLOCK DIAGRAM

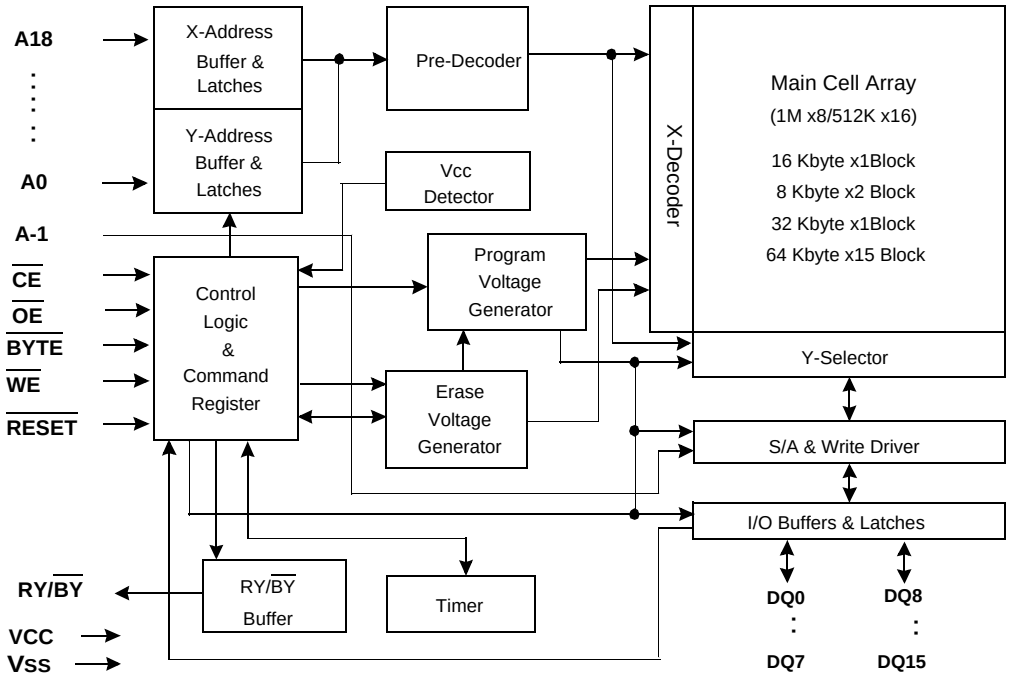


Table 1. Top Boot Block Address (KM28U800-T)

	A18	A17	A16	A15	A14	A13	A12	Block Size (Word/Byte)	Address Range	
									Word Mode	Byte Mode
BA18	1	1	1	1	1	1	X	8K / 16K	7E000H-7FFFFH	FC000H-FFFFFH
BA17	1	1	1	1	1	0	1	4K / 8K	7D000H-7DFFFH	FA000H-FBFFFH
BA16	1	1	1	1	1	0	0	4K / 8K	7C000H-7CFFFH	F8000H-F9FFFH
BA15	1	1	1	1	0	X	X	16K / 32K	78000H-7BFFFH	F0000H-F7FFFH
BA14	1	1	1	0	X	X	X	32K / 64K	70000H-77FFFH	E0000H-EFFFFH
BA13	1	1	0	1	X	X	X	32K / 64K	68000H-6FFFFH	D0000H-DFFFFH
BA12	1	1	0	0	X	X	X	32K / 64K	60000H-67FFFH	C0000H-CFFFFH
BA11	1	0	1	1	X	X	X	32K / 64K	58000H-5FFFFH	B0000H-BFFFFH
BA10	1	0	1	0	X	X	X	32K / 64K	50000H-57FFFH	A0000H-AFFFFH
BA9	1	0	0	1	X	X	X	32K / 64K	48000H-4FFFFH	90000H-9FFFFH
BA8	1	0	0	0	X	X	X	32K / 64K	40000H-47FFFH	80000H-8FFFFH
BA7	0	1	1	1	X	X	X	32K / 64K	38000H-3FFFFH	70000H-7FFFFH
BA6	0	1	1	0	X	X	X	32K / 64K	30000H-37FFFH	60000H-6FFFFH
BA5	0	1	0	1	X	X	X	32K / 64K	28000H-2FFFFH	50000H-5FFFFH
BA4	0	1	0	0	X	X	X	32K / 64K	20000H-27FFFH	40000H-4FFFFH
BA3	0	0	1	1	X	X	X	32K / 64K	18000H-1FFFFH	30000H-3FFFFH
BA2	0	0	1	0	X	X	X	32K / 64K	10000H-17FFFH	20000H-2FFFFH
BA1	0	0	0	1	X	X	X	32K / 64K	08000H-0FFFFH	10000H-1FFFFH
BA0	0	0	0	0	X	X	X	32K / 64K	00000H-07FFFH	00000H-0FFFFH

PRODUCT INTRODUCTION

The KM28U800 is an 8Mbit (8,388,608 bits) NOR-type Flash memory. The device features single voltage power supply operating within the range of 2.7 to 3.6 V. The device is programmed by using the Channel Hot Electron (CHE) injection mechanism which is used to program EPROMs. The device is erased electrically by using Fowler-Nordheim tunneling mechanism. To provide highly flexible erase and program capability, the device adapts a block memory architecture that divides its memory array into 15 symmetric blocks (64-Kbyte per block) and 4 asymmetric blocks (two 8-Kbyte, one 16-Kbyte, and one 32-Kbyte blocks). Programming is done in units of 8bits (Byte) or 16bits (Word). All bits of data in one or multiple blocks can be erased simultaneously when the device executes the erase operation. To prevent the device from accidental erasing or over-writing the programmed data, each of 19 memory blocks can be hardware protected. Byte/Word modes are available for read operation. These modes can be selected via $\overline{BYTE}$ pin. The device provides read access times of 90ns, 100ns, 120ns and 150ns, supporting high speed microprocessors to operate without any wait states.

The KM28U800 is fully command set compatible with standard Flash devices. The device is controlled by separate chip enable ($\overline{CE}$), output enable ($\overline{OE}$) and write enable ($\overline{WE}$) controls. Device operations are executed by selective command codes. The command codes specified by addresses and data sequences are written to the command register using microprocessor write timing. The command codes serve as inputs to an internal state machine which controls the program/erase circuitry. Register contents also internally latch addresses and data necessary to execute the program and erase operations. The KM28U800 is implemented with Internal Program/Erase Algorithms to execute the program/erase operations. The Internal Program/Erase Algorithms are invoked by program/erase command sequences. The Internal Program Algorithm automatically programs and verifies data at specified addresses. The Internal Erase Algorithm automatically pre-programs the memory cell which is not programmed and then executes the erase operation. The KM28U800 has means to indicate the status of completion of program/erase operations. The status can be indicated via the RY/$\overline{BY}$ pin, Data polling of DQ7, or the Toggle bit (DQ6). Once the operations have been completed, the device automatically resets itself to the read mode. The KM28U800 guarantees virtual zero stand-by current (typical 200nA), significantly reducing power consumption. The device requires only 7mA as active read current and 20mA for program/erase operations.

Table 2. Operations Table

Operation		$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BYTE}$	A9	A6	A1	A0	DQ15/ A-1	DQ8/ DQ14	DQ0/ DQ7	$\overline{Reset}$
Read	word	L	L	H	H	A9	A6	A1	A0	DQ15	DOUT	DOUT	H
	byte	L	L	H	L	A9	A6	A1	A0	A-1	High-Z	DOUT	H
Stand-by		H	X	X	X	X	X	X	X	High-Z	High-Z	High-Z	H
Output Disable		L	H	H	X	X	X	X	X	High-Z	High-Z	High-Z	H
Reset		X	X	X	X	X	X	X	X	High-Z	High-Z	High-Z	L
Write	word	L	H	L	H	A9	A6	A1	A0	DQ15	PD(3)	PD(3)	H
	byte	L	H	L	L	A9	A6	A1	A0	A-1	High-Z	PD(3)	H
Enable Block Protect (4)		L	VID	Pulse/H	X	V_{ID}	L	H	L	X	X	X	H
Temporary Block Unprotect		X	X	X	X	X	X	X	X	X	X	X	V_{ID}
Auto Select - Manufacturer ID		L	L	H	X	V_{ID}	L	L	L	High-Z	High-Z	ECH(5)	H
Auto Select - Device Code top boot block	word	L	L	H	H	V_{ID}	L	L	H	DQ15=0	22(5)	DAH(5)	H
	byte	L	L	H	L	V_{ID}	L	L	H	High-Z	High-Z	DAH(5)	H
Auto Select - Device Code bottom boot	word	L	L	H	H	V_{ID}	L	L	H	DQ15=0	22(5)	5BH(5)	H
	byte	L	L	H	L	V_{ID}	L	L	H	High-Z	High-Z	5BH(5)	H
Auto Select - Verify Block Protect		L	L	H	X	V_{ID}	L	H	L	High-Z	High-Z	01H(5)	H

Notes :

1. L = V_{IL} (Low), H = V_{IH} (High), V_{ID}=12.0±0.5 Volts, X=Don't care.
2. Manufacturer and device codes may also be accessed via a command register write sequence.
3. See Table 4 for valid PD (Data to be programmed at location program address) during write operation.
4. Addresses must be composed of the block address (A12 - A18), A1 = 1 and A0 = 0.
5. These are output data. Please refer to Table 5 "Autoselect code".

COMMAND DEFINITIONS

The KM28U800 operates by selecting and executing its operational modes. Each operational mode has its own command set. In order to select a certain mode, a proper command with specific address and data sequences must be written into the command register. Writing incorrect information which include address and data or writing an improper command will reset the device to the read mode. The defined valid register command sequences are stated in Table 4. Note that Erase Suspend (B0H) and Erase Resume (30H) commands are valid only while the Block Erase Operation is in progress.

Table 3. Command Sequences

Command Sequence		Cycle	1st Cycle		2nd Cycle		3rd Cycle		4th Cycle		5th Cycle		6th Cycle	
			Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte
Read	Addr	1	RA											
	Data		RD											
Reset	Addr	1	XXXH											
	Data		F0H											
Autoselect (2, 3) Manufacturer ID	Addr	4	555H	AAAH	2AAH	555H	555H	AAAH	X00H	X00H				
	Data		XXAAH	AAH	XX55H	55H	XX90H	90H	XXECH	ECH				
Autoselect (2, 3) Device Code -Top Block	Addr	4	555H	AAAH	2AAH	555H	555H	AAAH	X01H	X02H				
	Data		XXAAH	AAH	XX55H	55H	XX90H	90H	22DAH	DAH				
Autoselect (2, 3) Device Code -Bottom Block	Addr	4	555H	AAAH	2AAH	555H	555H	AAAH	X01H	X02H				
	Data		XXAAH	AAH	XX55H	55H	XX90H	90H	225BH	5BH				
Autoselect (2, 3) Block Protect Verify	Addr	4	555H	AAAH	2AAH	555H	555H	AAAH	BA / X02H	BA/ X04H				
	Data		XXAAH	AAH	XX55H	55H	XX90H	90H	XX01H	01H				
Program	Addr	4	555H	AAAH	2AAH	555H	555H	AAAH	PA	PA				
	Data		XXAAH	AAH	XX55H	55H	XXA0H	A0H	PD	PD				
Chip Erase	Addr	6	555H	AAAH	2AAH	555H	555H	AAAH	555H	AAAH	2AAH	555H	555H	AAAH
	Data		XXAAH	AAH	XX55H	55H	XX80H	80H	XXAAH	AAH	XX55H	55H	XX10H	10H
Block Erase	Addr	6	555H	AAAH	2AAH	555H	555H	AAAH	555H	AAAH	2AAH	555H	BA	BA
	Data		XXAAH	AAH	XX55H	55H	XX80H	80H	XXAAH	AAH	XX55H	55H	XX30H	30H
Block Erase Suspend (4, 5)	Addr	1	XXXH	XXXH										
	Data		XXB0H	B0H										
Block Erase Resume	Addr	1	XXXH	XXXH										
	Data		XX30H	30H										

Notes : 1. RA : Read Address, PA : Program Address, BA : Block Address (A18 - A12), RD : Read Data, PD : Program Data
2. To terminate the Autoselect Mode, it is necessary to write Read/Reset command to the register.
3. The 4th cycle data of Autoselect Mode are output data. Refer to Table 5 " Autoselect Code "
4. The Read and Program operations at non-erasing blocks are allowed in the Erase Suspend mode.
5. The Erase Suspend command is applicable only to the Block Erase operation.

Table 4. Autoselect/Block Protection Code

Type	Mode	A12~A18	A6	A1	A0	Code (HEX)	DQ8~DQ15	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Manufacturer Code		X	L	L	L	ECH	High-Z	1	1	1	0	1	1	0	0
Top Boot Block	Word	X	L	L	H	22DAH	DQ9=DQ13=1 Others=0	1	1	0	1	1	0	1	0
	Byte	X				DAH	High-Z								
Bottom Boot Block	Word	X	L	L	H	225BH	DQ9=DQ13=1 Others=0	0	1	0	1	1	0	1	1
	Byte	X				5BH	High-Z								
Block Protection Verification		Set Block Addresses	L	H	L	01H	X	0	0	0	0	0	0	0	1

DEVICE OPERATION

Read Mode

The KM28U800 is controlled by separate Chip Enable ($\overline{CE}$), Output Enable ($\overline{OE}$) and Write Enable ($\overline{WE}$) commands. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the specified address location,will be the output of the device. The outputs are in high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high.

Standby Mode

The KM28U800 features Stand-by Mode to reduce power consumption. This mode puts the device on hold when the device is either unselected or deselected by making $\overline{CE}$ high ($\overline{CE} = V_{IH}$). Refer to the DC characteristics for more details on stand-by modes.

Output Disable

The device outputs are disabled when $\overline{OE}$ is High ($\overline{OE} = V_{IH}$). The output pins are in high impedance state.

Automatic Sleep Mode

KM28U800 features Automatic Sleep Mode to minimize the device power consumption. Since the device typically draws 200nA of current in Automatic Sleep Mode, this feature plays an extremely important role in battery-powered applications. When addresses remain steady for 200ns, the device automatically activates the Automatic Sleep Mode. While in the sleep mode, output data is latched and always available to the system. When addresses are changed, the device provides new data without wait time.

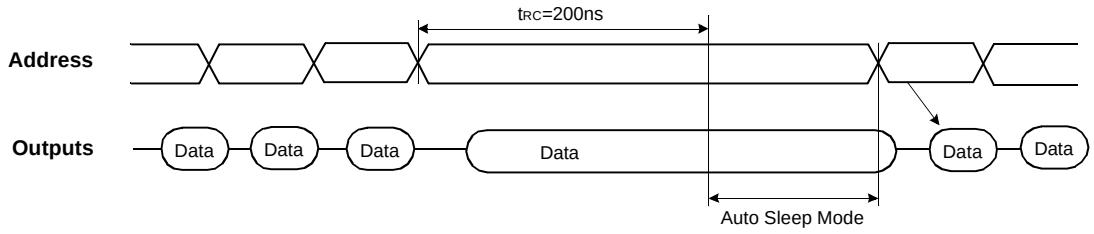


Figure 2. Auto Sleep Mode Operation

Autoselect

The KM28U800 offers the Autoselect Mode to identify manufacturer and device type by reading a binary code. The Autoselect Mode allows programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. In addition, this mode allows the verification of the status of write protected blocks. This mode is activated when the programming equipment externally forces high voltage V_{ID} (11.5 - 12.5 Volts) on address pin A9 followed by sequencing two identifier bytes from the device outputs by toggling address A0 from low to high. The rest of addresses except A0, A1 and A6 are Don't Care. Table 5 shows Autoselect/Block Protection Codes.

The manufacturer and device code may also be read via the command register. The Command Sequence is shown in Table 4. The autoselect operation is initiated by writing the Autoselect Command into the command register. Following the command write, read cycle from addresses stated in Table 5 retrieve the manufacturer code and device code. In addition, block protection status can be detected by scanning the block addresses (A12 - A18) while (A6, A1, A0) = (0,1,0). Once the command is set, it will produce a logical "1" at the device output DQ0 to indicate a write protected block. To terminate the autoselect operation, write Reset command(FOH) into the command register.

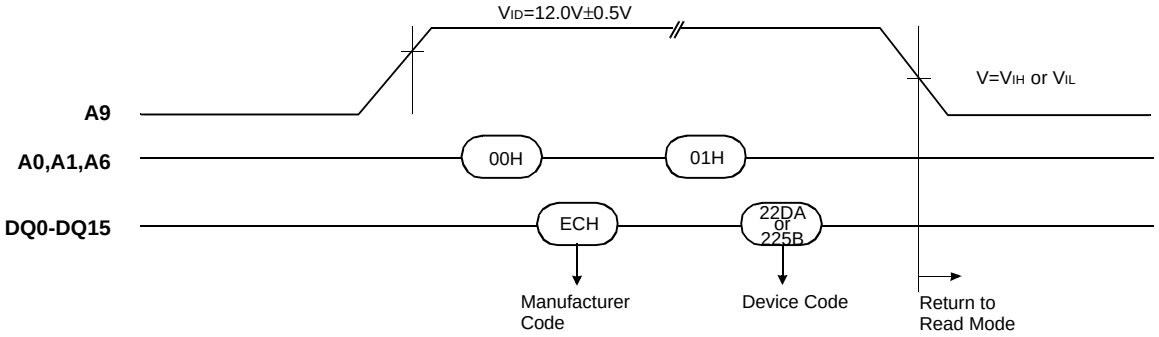


Figure 3. Autoselect Operation (by address pin)

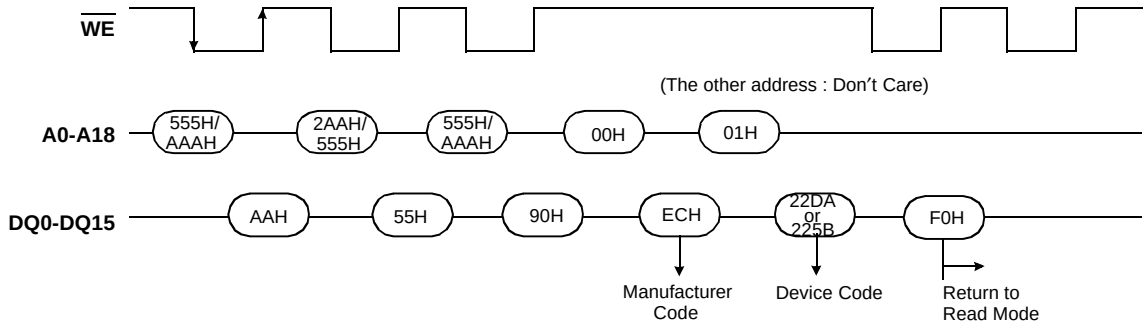


Figure 4. Autoselect Operation (by command sequence)

Write (Program/Erase) Mode

The KM28U800 executes its program/erase operations by writing commands into the command register. In order to write the commands to the register, $\overline{CE}$ and $\overline{WE}$ must be low and $\overline{OE}$ must be high. Addresses and data are latched on the falling edges of $\overline{CE}$ or $\overline{WE}$ (whichever occurs last) and/or on the rising edges of $\overline{CE}$ or $\overline{WE}$ (whichever occurs first). The device uses standard microprocessor write timing.

Program

The KM28U800 can be programmed in units of a word or a byte. Programming is writing 0's into the memory array by executing the Internal Program Routine. In order to perform the Internal Program Routine, a four-cycle command sequence is necessary. The first two cycles are unlock cycles. The third cycle is assigned for the program setup command. In the last cycle, the address of the memory location and the data to be programmed at that location are written. The device automatically generates adequate program pulses and verifies the programmed cell margin by the Internal Program Routine. During the execution of the Routine, the system is not required to provide further controls or timings.
During the Internal Program Routine, commands written to the device will be ignored. Note that a hardware reset during a program operation will cause data corruption at the corresponding location.

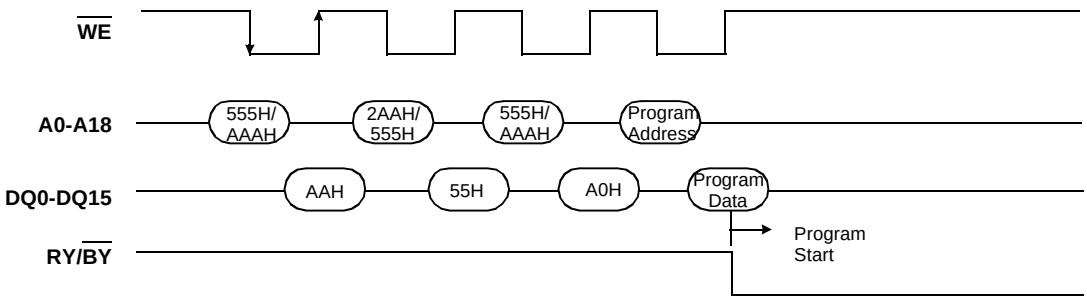


Figure 5. Program Command Sequence

Chip Erase

To erase a chip is to write 1's into the entire memory array by executing the Internal Erase Routine. The Chip Erase requires six bus cycles to write the command sequence. The erase set-up command is written after first two "unlock" cycles. Then, there are two more write cycles prior to writing the chip erase command. The Internal Erase Routine automatically pre-programs and verifies the entire memory for an all zero data pattern prior to erase. The automatic erase begins on the rising edge of the last $\overline{WE}$ pulse in the command sequence and terminates when DQ7 is "1". After that the device returns to read mode.

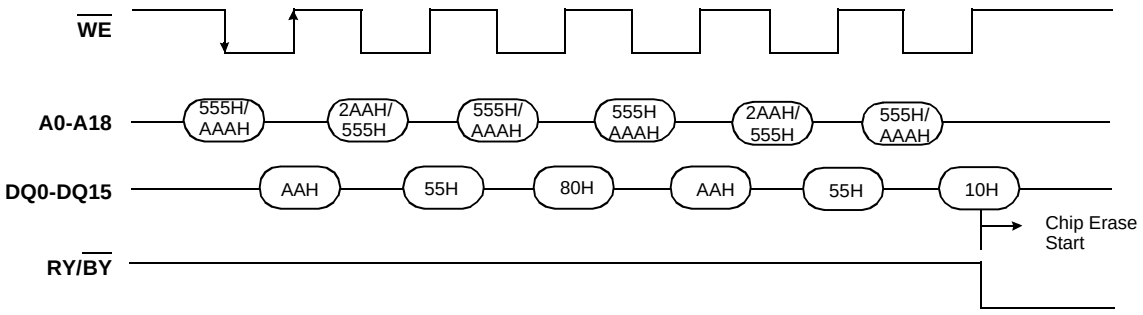


Figure 6. Chip Erase Command Sequence

Block Erase

To erase a block is to write 1′s into the desired memory block by executing the Internal Erase Routine. The Block Erase requires six bus cycles to write the command sequence shown in Table 4. After the first two "unlock" cycles, the erase setup command (80H) is written at the third cycle. Then there are two more "unlock" cycles followed by the Block Erase command. The Internal Erase Routine automatically pre-programs and verifies the entire memory prior to erasing it. The block address is latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, while the Block Erase command is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$.

Multiple blocks can be erased sequentially by writing the six bus-cycle operation in Table 4. Upon completion of the last cycle for the Block Erase, additional block address and the Block Erase command (30H) can be written to perform the Multi-Block Erase. An 80us (typical) "time window" is required between the Block Erase command writes. The Block Erase command must be written within the 80us "time window", otherwise the Block Erase command will be ignored. The 80us "time window" is reset when the falling edge of the $\overline{WE}$ occurs within the 80us of "time window" to latch the Block Erase command. During the 80us of "time window", any command other than the Block Erase or the Erase Suspend command written to the device will reset the device to read mode. After the 80 us of "time window", the Block Erase command will initiate the Internal Erase Routine to erase the selected blocks. No other commands will be recognized except the Erase Suspend command.

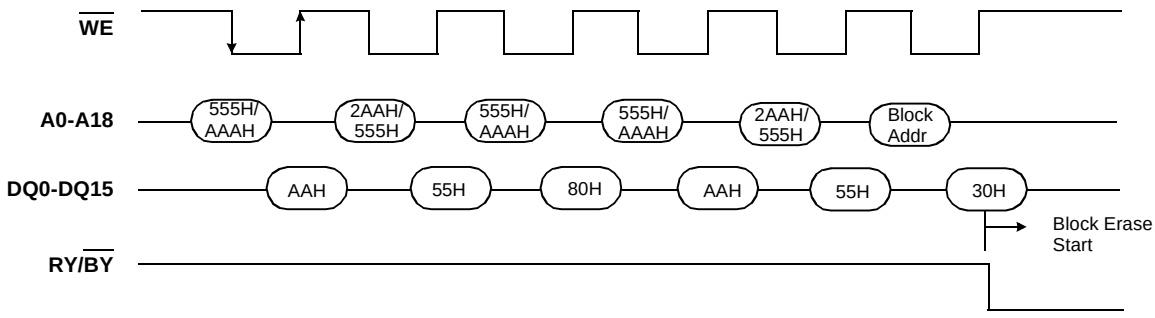


Figure 7. Block Erase Command Sequence

Erase Suspend / Resume

The Erase Suspend command interrupts the Block Erase to read or program data in a block that is not being erased. The Erase Suspend command is only valid during the Block Erase operation. The Erase Suspend command is not valid while the Chip Erase or the Internal Program Routine sequence is running. When the device is in the Erase Suspend mode, any other command will be ignored except for the Erase Resume command. When the Erase Resume command is executed, the Block Erase operation will resume. When the Erase Suspend or Erase Resume command is executed, the addresses are Don't Care.

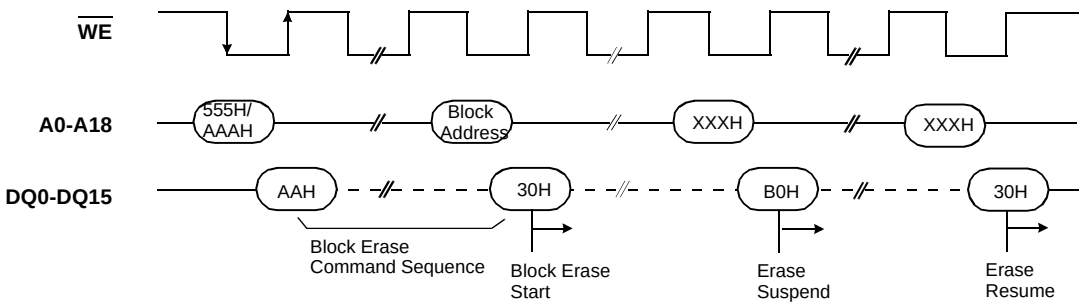


Figure 8. Erase Suspend/Resume Command Sequence

Block Protect

All blocks in the KM28U800 can be hardware protected by using external programming equipment. This will disable the device to erase and program on the protected blocks. Commands to erase or program the protected blocks will be ignored by the device. The protected blocks can only be read. It is possible to determine if a block is protected in the system by writing an Autoselect command. Performing a read operation at the address location XX02H, where the higher order address A_{18} - A_{12} represents the block address, will produce a logical "1" at DQ0 for a protected block. The KM28U800 needs the recovery time (20us) from the rising edge of WE in order to execute its program/erase operations.

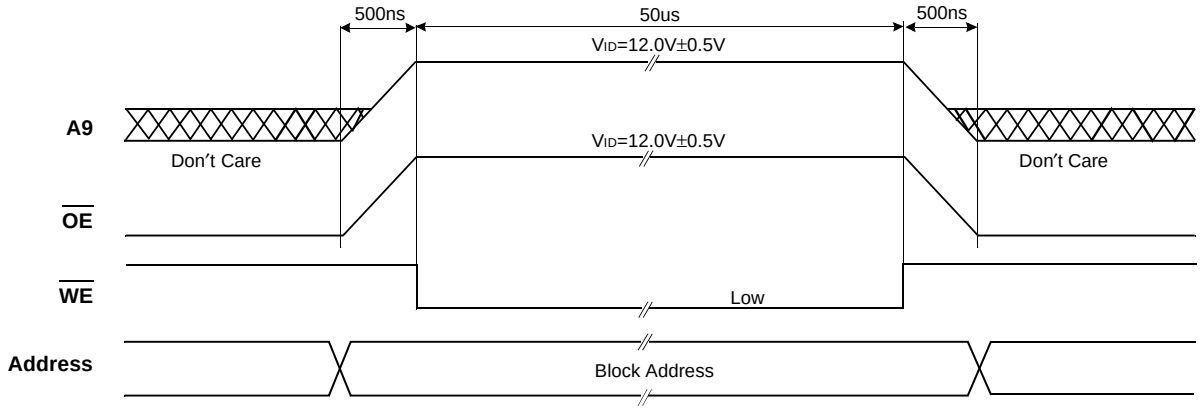


Figure 9. Block Protect Sequence

Temporary Block Unprotect

The protected blocks of the KM28U800 can be temporarily unprotected by applying high voltage (V_{ID} = 12 volt) to the $\overline{RESET}$ pin. In this mode, previously protected blocks can be programmed or erased with the program or erase command routines. When the $\overline{RESET}$ pin goes high ($\overline{RESET}$ = V_{IH}), all the previously protected blocks will be protected again.

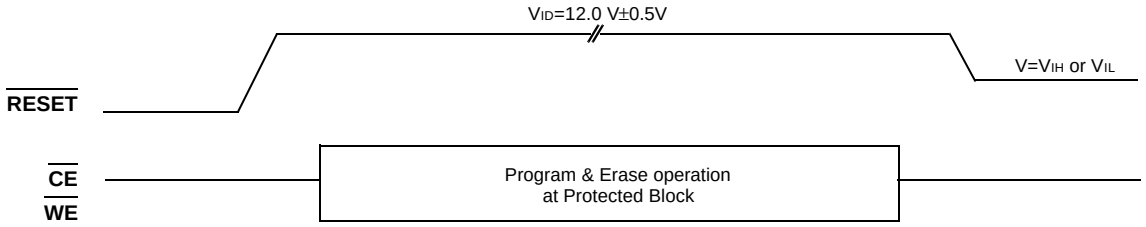


Figure 10. Temporary Block Unprotect Sequence

$\overline{RESET}$

Hardware Reset

The KM28U800 offers a reset feature by driving the $\overline{RESET}$ pin to V_{IL}. The $\overline{RESET}$ pin must be kept low (V_{IL}) for at least 500ns. When the $\overline{RESET}$ pin is driven low, any operation in progress will be terminated and the internal state machine will be reset to the standby mode after 20μs. If a hardware reset occurs during a program operation, the data at that particular location will be lost. Once the $\overline{RESET}$ pin is taken high, the device requires 500ns of wake-up time until outputs are valid for read access. Also, note that all the data output pins are tri-stated for the duration of the $\overline{RESET}$ pulse.
The $\overline{RESET}$ pin may be tied to the system reset pin. If a system reset occurs during the Internal Program and Erase Routine, the device will be automatically reset to the read mode ; this will enable the systems microprocessor to read the boot-up firmware from the Flash memory.

Power-up Protection

To avoid initiation of a write cycle during Vcc Power-up, $\overline{RESET}$ low must be asserted during power-up. After $\overline{RESET}$ goes high, the device is reset to the read mode.

Low Vcc Write Inhibit

To avoid initiation of a write cycle during Vcc power-up and power-down, a write cycle is locked out for Vcc less than 2.3V (typically 2.5V). If Vcc < V_{LKO} (Lock-Out Voltage), the command register and all internal program/erase circuits are disabled. Under this condition the device will reset itself to the read mode. Subsequent writes will be ignored until the Vcc level is greater than V_{LKO}. It is the user's responsibility to ensure that the control pins are logically correct to prevent unintentional writes when Vcc is above 2.3V.

Write Pulse Glitch Protection

Noise pulses of less than 5ns(typical) on $\overline{CE}$, $\overline{OE}$, or $\overline{WE}$ will not initiate a write cycle.

Logical Inhibit

Writing is inhibited under any one of the following conditions : $\overline{OE}$ = V_{IL}, $\overline{CE}$ = V_{IH} or $\overline{WE}$ = V_{IH}. To initiate a write, $\overline{CE}$ and $\overline{WE}$ must be "0", while $\overline{OE}$ is "1".

DEVICE STATUS FLAGS

The KM28U800 has means to indicate its status of operation. The status is indicated by raising the device status flag via corresponding DQ pins or the RY/ $\overline{BY}$ pin. The corresponding DQ pins are DQ7, DQ6, DQ5, and DQ2. The statuses are as follows :

Table 5. Hardware Sequence Flags

	Status		DQ7	DQ6	DQ5	DQ3	DQ2	RY/$\overline{BY}$
In Progress	Programming		$\overline{DQ7}$	Toggle	0	0	1	0
	Block Erase or Chip Erase		0	Toggle	0	1	Toggle	0
	Erase Suspend Read	Erase Suspended	1	1	0	0	Toggle (Note 1)	1
	Erase Suspend Read	Non-Erase Suspended Block	Data	Data	Data	Data	Data	1
	Erase Suspend Program	Non-Erase Suspended Block	$\overline{DQ7}$	Toggle	0	0	1	0
Exceeded Time Limits	Programming		$\overline{DQ7}$	Toggle	1	0	No Toggle	0
	Block Erase or Chip Erase		0	Toggle	1	1	(Note 2)	0
	Erase Suspend Program		$\overline{DQ7}$	Toggle	1	0	No Toggle	0

Notes :
1. DQ2 will toggle when the device performs successive read operations from the erase suspended block.
2. If DQ5 is High (exceeded timing limits), successive reads from a problem block will cause DQ2 to toggle.

DQ7 : $\overline{\text{Data}}$ Polling

When an attempt to read the device is made while executing the Internal Program, the complement of the data is written to DQ7 as an indication of the Routine in progress. When the Routine is completed, however, an attempt to access to the device will produce the true data written to DQ7. When a user attempts to read the device during the Erase operation, DQ7 will be low. If the device is placed in the Erase Suspend Mode, the status can be detected via the DQ7 pin. If the system tries to read an address which belongs to a block that is being erased, DQ7 will be high. If a non-erased block address is read, the device will produce the true data to DQ7. If an attempt is made to program a protected block, DQ7 outputs complements the data for approximately 1μs and the device then returns to the Read Mode without changing data in the block. If an attempt is made to erase a protected block, DQ7 outputs complement data in approximately 100us and the device then returns to the Read Mode without erasing the data in the block.

DQ6 : Toggle Bit

Toggle bit is another option to detect whether an Internal Routine is in progress or completed. Once the device is at a busy state, DQ6 toggles. Toggling DQ6 is halted after the device completes its Internal Routine. If the device is in the Erase Suspend Mode, an attempt to read an address that belongs to a block that is being erased will produce a high output of DQ6. If an address belongs to a block that is not being erased, toggling is halted and valid data is produced at DQ6.
If an attempt is made to program a protected block, DQ6 toggles for approximately 1μs and the device then returns to the Read Mode without changing the data in the block. If an attempt is made to erase a protected block, DQ6 toggles for approximately 100μs and the device then returns to the Read Mode without erasing the data in the block.

DQ5 : Exceed Timing Limits

If the Internal Program/Erase Routine extends beyond the timing limits, DQ5 will go High, indicating program/erase failure.

DQ3 : Block Erase Timer

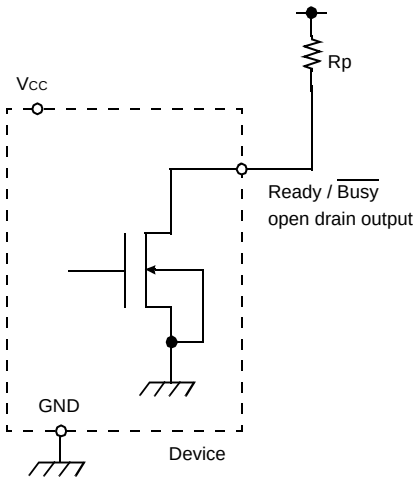
The status of the multi-block erase operation can be detected via the DQ3 pin. DQ3 will go High if 80us of the block erase timer window has expired. In this case, the Internal Erase Routine will initiate the erase operation.Therefore, the device will not accept further write commands until the erase operation is completed. DQ3 is Low if the block erase timer window is not expired. Within the block erase timer window, additional block erase command (30H) can be accepted. To confirm that the block erase command has been accepted, the software may check the status of DQ3 following each block erase command.

DQ2 : Toggle Bit 2

The device generates a toggling pulse in DQ2 only if the Internal Erase Routine or the Erase Suspend is in progress. When the device executes the Internal Erase Routine, DQ2 is toggling only if an erasing block is read. Although the Internal Erase Routine is in the Exceeded Time Limits, DQ2 is toggling only if an erasing block in the Exceeded Time Limits is read. When the device is in the Erase Suspend, DQ2 is toggling only if an address in the erasing block is read. If a non-erasing block address is read during the Erase Suspend, then DQ2 will produce valid data. DQ2 will go High if the user tries to program a non-erase suspend block while the device is in the Erase Suspend. Combination of the status in DQ6 and DQ2 can be used to distinguish the erase operation from the program operation.

RY/$\overline{BY}$: Ready/$\overline{Busy}$

The KM28U800 has a Ready / $\overline{Busy}$ output that indicates either the completion of an operation or the status of Internal Algorithms. If the output is Low, the device is busy with either a program or an erase operation. If the output is High, the device is ready to accept any read/write or erase operation. When the RY/ $\overline{BY}$ pin is low, the device will not accept any additional program or erase commands with the exception of the Erase Suspend command. If the KM28U800 is placed in an Erase Suspend mode, the RY/ $\overline{BY}$ output will be High. For programming, the RY/ $\overline{BY}$ is valid (RY/ $\overline{BY}$ = 0) after the rising edge of the fourth $\overline{WE}$ pulse in the four write pulse sequence. For Chip Erase, RY/ $\overline{BY}$ is also valid after the rising edge of $\overline{WE}$ pulse in the six write pulse sequence. For Block Erase, RY/ $\overline{BY}$ is also valid after the rising edge of the sixth $\overline{WE}$ pulse.
The pin is an open drain output, allowing two or more Ready/ $\overline{Busy}$ outputs to be OR-tied. An appropriate pull-up resistor is required for proper operation.



$$Rp = \frac{Vcc\ (Max.) - V_{OL}\ (Max.)}{I_{OL} + \Sigma I_L} = \frac{3.2\ V}{4.0mA + \Sigma I_L}$$

where ΣI_L is the sum of the input currents of all devices tied to the Ready / $\overline{Busy}$ pin.

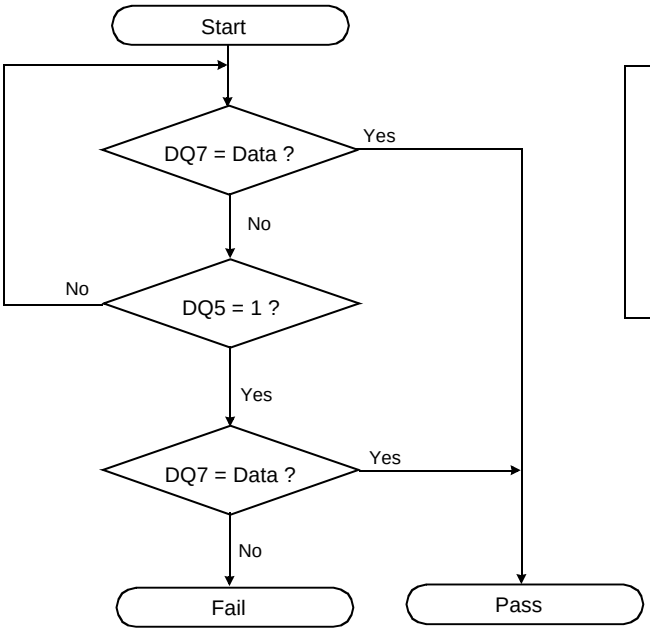


Figure 11. Data Polling Algorithms

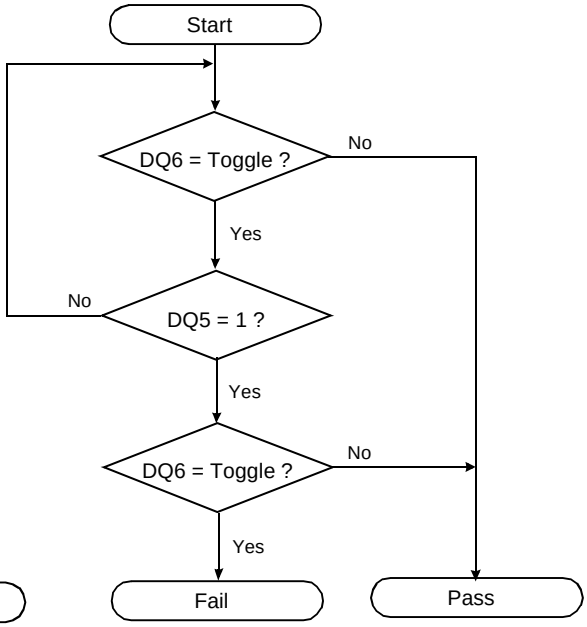
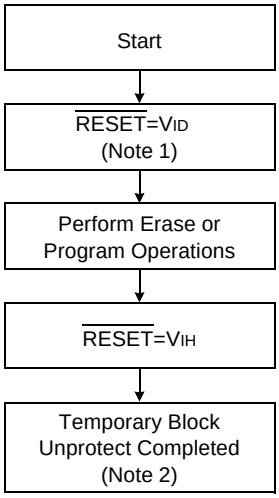


Figure 12. Toggle Bit Algorithms



Notes :
1. All protected blocks are unprotected.
2. All previously protected blocks are protected once again.

Figure 13. Temporary Block Unprotect Routine

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	A9, $\overline{OE}$, $\overline{RESET}$	V_{IN}	-0.6 to +12.5	V
	All Other Pins		-0.6 to +5.5	
Temperature Under Bias	KM28U800	T_{bias}	-10 to +125	°C
	KM28U800I		-40 to +125	
Storage Temperature		T_{stg}	-65 to +150	°C
Short Circuit Output Current		I_{OS}	5	mA
Operating Temperature		T_A (Standard Temp.)	0 to +70	°C
		T_A (Industrial Temp.)	-40 to + 85	°C

Notes :
1. Minimum DC voltage is -0.5V on Input/ Output pins. During transitions, this level may fall to -2.0V for periods <20ns. Maximum DC voltage on input / output pins is Vcc+0.3V which, during transitions, may overshoot to Vcc+2.0V for periods <20ns.
2. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to GND)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V_{CC}	2.7	3.0	3.6	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol		Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}		V_{IN}=V_{SS} to V_{CC}, V_{CC}=V_{CCmax}		-	± 1.0	µA
A9 Input Leakage Current	I_{LIT}		V_{CC}=V_{CC}max, A9=12V		-	35	µA
Output Leakage Current	I_{LO}		V_{OUT}=V_{SS} to V_{CC}, V_{CC}=V_{CCmax}		-	± 1.0	µA
Active Read Current (1)	$I_{CC}1$		$\overline{CE}$=V_{IL}, $\overline{OE}$=V_{IL} All outputs open	5MHz	-	12	mA
				1MHz	-	4	
Active Write Current (2)	$I_{CC}2$		$\overline{CE}$=V_{IL}, $\overline{OE}$=V_{IH}		-	30	mA
Standby Current	$I_{SB}1$	CMOS	V_{CC}=V_{CCmax}, $\overline{CE}$=V_{CC}, $\overline{RESET}$=V_{CC}		-	5	µA
		TTL	V_{CC}=V_{CCmax}, $\overline{CE}$=V_{IH}, $\overline{RESET}$=V_{IH}		-	250	µA
Standby Current During Reset	$I_{SB}2$	CMOS	V_{CC}=V_{CCmax}, $\overline{RESET}$=V_{SS}		-	5	µA
		TTL	V_{CC}=V_{CCmax}, $\overline{RESET}$=V_{IL}		-	250	µA
Automatic Sleep Mode (3)	$I_{SB}3$		V_{IH}=V_{CC} ± 0.3V, V_{IL}=V_{SS}		-	5	µA
Input Low Level	V_{IL}				-0.5	0.8	V
Input High Level	V_{IH}				2.0	V_{CC} + 0.3	V
Voltage for Autoselect and Block Protect	V_{ID}				11.5	12.5	V
Output Low Level	V_{OL}		I_{OL}=4.0mA, V_{CC}=V_{CCmin}		-	0.4	V
Output High Level	$V_{OH}1$		I_{OH}=-2.0mA, Vcc=V_{CCmin}		2.4	-	V
	$V_{OH}2$		I_{OH}=-100 µA, Vcc = V_{CCmin}		V_{CC} - 0.4	-	V
Low VCC Lock-out Voltage (4)	V_{LKO}				2.3	2.5	V

Notes :
1. The ICC current listed includes both the DC operating current and the frequency dependent component(at 5 MHz). The read current is typically 7mA. (@ Vcc 3.0V , f=5MHz , $\overline{OE}$ at VIH)
2. ICC active while Internal Routine(program or erase) is in progress.
3. Automatic sleep mode enables the low power mode when addresses remain stable for 200ns. Typical sleep mode current is 200nA.
4. Not 100% tested.

CAPACITANCE(T_A=25 °C, V_{CC}=3.3V, f=1.0MHz)

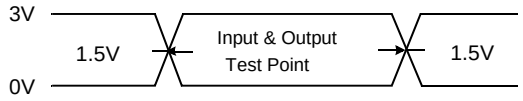
Item	Symbol	Test Condition	Min	Max	Unit
Input/Output Capacitance	$C_{I/O}$	V_{IL}=0V	-	10	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	10	pF

Note : Capacitance is periodically sampled and not 100% tested.

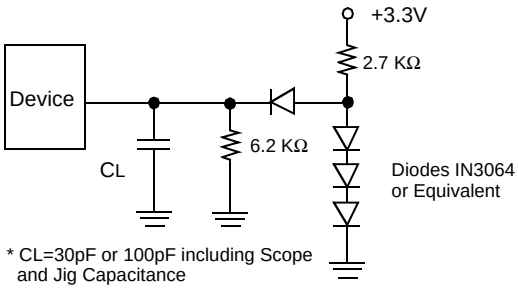
AC TEST CONDITION

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	1TTL and C_L = 30pF or 100pF

Note : T_A=0 °C to + 70 °C, V_{CC}=2.7V - 3.6V, unless otherwise noted.



Input Pulse and Test Point



Output Load

AC CHARACTERISTICS

Read Operations

Parameter	Symbol	CL = 30pF		CL = 100pF						Unit
		-9		-10		-12		-15		
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	90		100		120		150		ns
Address Access Time	t_{AA}		90		100		120		150	ns
Chip Enable Access Time	t_{CE}		90		100		120		150	ns
Output Enable Time	t_{OE}		40		40		50		55	ns
$\overline{CE}$ & $\overline{OE}$ Disable Time	t_{DF} (*)		30		30		30		40	ns
Output Hold Time from Address, $\overline{CE}$ or $\overline{OE}$	t_{OH} (*)	0		0		0		0		ns
$\overline{RESET}$ Pin Low To Read Mode (Note)	tReady(*)		20		20		20		20	µs

***. Note** : Not 100% tested.

AC CHARACTERISTICS
Write(Erase/Program)Operations
Alternate $\overline{WE}$ Controlled Write

Parameter		Symbol	C_L = 30pF		C_L = 100pF						Unit
			-9		-10		-12		-15		
			Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time (1)		t_{WC}	90	-	100	-	120	-	150	-	ns
Address Setup Time		t_{AS}	0	-	0	-	0	-	0	-	ns
Address Hold Time		t_{AH}	50	-	50	-	50	-	65	-	ns
Data Setup Time		t_{DS}	50	-	50	-	50	-	65	-	ns
Data Hold Time		t_{DH}	0	-	0	-	0	-	0	-	ns
Output Enable Setup Time (1)		t_{OES}	0	-	0	-	0	-	0	-	ns
Output Enable Hold	Read (1)	t_{OEH}	0	-	0	-	0	-	0	-	ns
	Toggle and $\overline{Data}$ Polling (1)		10	-	10	-	10	-	10	-	ns
$\overline{CE}$ Setup Time		t_{CS}	0	-	0	-	0	-	0	-	ns
$\overline{CE}$ Hold Time		t_{CH}	0	-	0	-	0	-	0	-	ns
Write Pulse Width		t_{WP}	50	-	50	-	50	-	65	-	ns
Write Pulse Width High		t_{WPH}	30	-	30	-	30	-	35	-	ns
Programming Operation	Word	t_{PGM}	11(typ.)		11(typ.)		11(typ.)		11(typ.)		µs
	Byte		9(typ.)		9(typ.)		9(typ.)		9(typ.)		µs
Block Erase Operation (2)		t_{BERS}	1(typ.)		1(typ.)		1(typ.)		1(typ.)		sec
V_{CC} Set Up Time		t_{VCS}	50	-	50	-	50	-	50	-	µs
Write Recovery Time from RY/$\overline{BY}$		t_{RB}	0	-	0	-	0	-	0	-	ns
$\overline{RESET}$ High Time Before Read		t_{RH}	50	-	50	-	50	-	50	-	ns
$\overline{RESET}$ to Power Down Time		t_{RPD}	20	-	20	-	20	-	20	-	µs
Program/Erase Valid to RY/$\overline{BY}$ Delay		t_{BUSY}	90	-	90	-	90	-	90	-	ns
$\overline{CE}$ to $\overline{BYTE}$ Switching Low or High		t_{ELFL}/ t_{ELFH}		5		5		5		5	ns
$\overline{BYTE}$ Switching Low to Output HIGH-Z		t_{FLQZ}	30	-	30	-	40	-	40	-	ns
$\overline{BYTE}$ Switching High to Output Active		t_{FHQV}	30	-	30	-	40	-	40	-	ns
V_{ID} Rising and Falling Time		t_{VID}	500	-	500	-	500	-	500	-	ns
$\overline{RESET}$ Pulse Width		t_{RP}	500	-	500	-	500	-	500	-	ns
$\overline{RESET}$ Low to RY/BY High		t_{RRB}	-	20	-	20	-	20	-	20	µs
$\overline{CE}$ Setup Time for Block Protection		t_{CESP}	4	-	4	-	4	-	4	-	µs
$\overline{OE}$ Setup Time for Block Protection		t_{OESP}	4	-	4	-	4	-	4	-	µs
$\overline{RESET}$ Setup Time for Temporary Unprotect		t_{RSP}	4	-	4	-	4	-	4	-	µs
$\overline{RESET}$ High to Address Valid		t_{RSTW}	200	-	200	-	200	-	200	-	ns
Read Recovery Time Before Write		t_{GHWL}	0	-	0	-	0	-	0	-	ns

Notes : 1. Not 100% tested.
2. The duration of the Program or Erase operation varies and is calculated in the internal algorithms.

AC CHARACTERISTICS
Write(Erase/Program)Operations
Alternate CE Controlled Writes

Parameter		Symbol	C_L = 30pF		C_L = 100pF						Unit
			-9		-10		-12		-15		
			Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time (1)		t_{WC}	90	-	100	-	120	-	150	-	ns
Address Setup Time		t_{AS}	0	-	0	-	0	-	0	-	ns
Address Hold Time		t_{AH}	50	-	50	-	50	-	65	-	ns
Data Setup Time		t_{DS}	50	-	50	-	50	-	65	-	ns
Data Hold Time		t_{DH}	0	-	0	-	0	-	0	-	ns
Output Enable Setup Time (1)		t_{OES}	0	-	0	-	0	-	0	-	ns
Output Enable HoldTime	Read (1)	t_{OEH}	0	-	0	-	0	-	0	-	ns
	Toggle and $\overline{\text{Data}}$ Polling (1)		10	-	10	-	10	-	10	-	ns
$\overline{WE}$ Setup Time		t_{WS}	0	-	0	-	0	-	0	-	ns
$\overline{WE}$ Hold Time		t_{WH}	0	-	0	-	0	-	0	-	ns
$\overline{CE}$ Pulse Width		t_{CP}	50	-	50	-	50	-	65	-	ns
$\overline{CE}$ Pulse Width High		t_{CPH}	30	-	30	-	30	-	35	-	ns
Programming Operation	Word	t_{PGM}	11(typ.)		11(typ.)		11(typ.)		11(typ.)		µs
	Byte		9(typ.)		9(typ.)		9(typ.)		9(typ.)		µs
Block Erase Operation (2)		t_{BERS}	1(typ.)		1(typ.)		1(typ.)		1(typ.)		sec
$\overline{BYTE}$ Switching Low to Output HIGH-Z		t_{FLQZ}	30	-	30	-	30	-	30	-	ns

Notes : 1. Not 100% tested.
2.This does not include the preprogramming time.

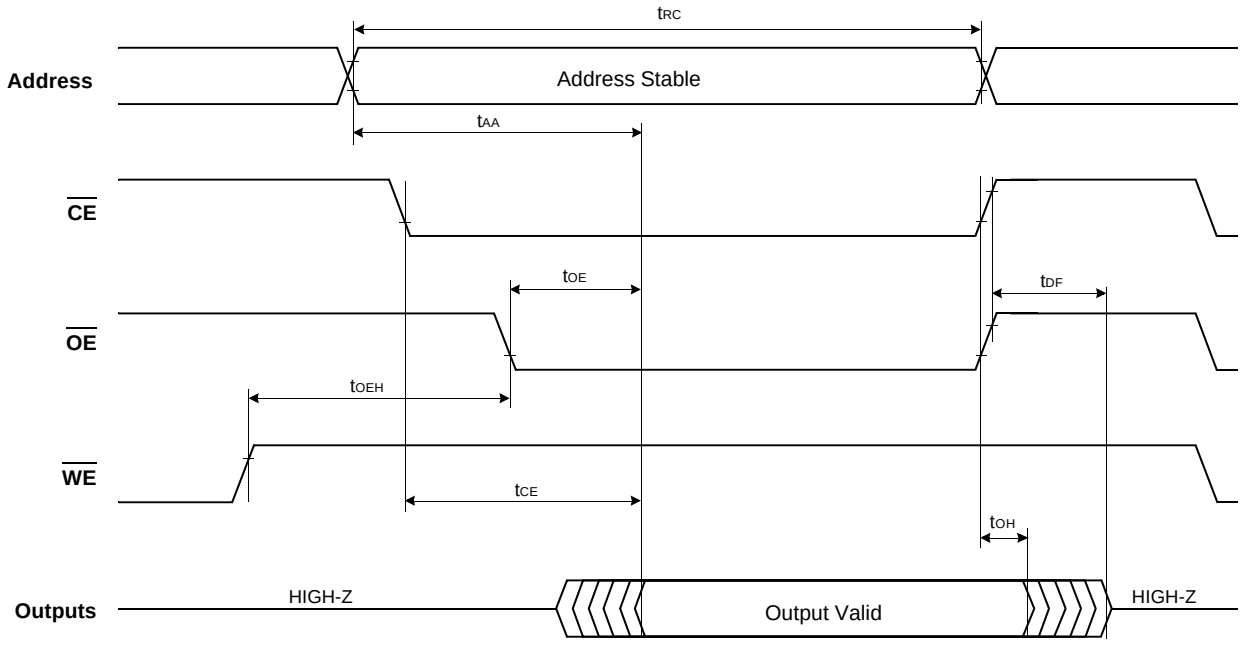
ERASE AND PROGRAM PERFORMANCE

Parameter		Limits		Unit	Comments
		Typ	Max		
Block Erase Time		1	15	sec	Excludes 00H programming prior to erasure
Chip Erase Time		19		sec	
Word Programming Time		11	360	us	Excludes system-level overhead
Byte Programming Time		9	300	us	Excludes system-level overhead
Chip Programming Time	Word Mode	6	17	sec	Excludes system-level overhead
	Byte Mode	9	27	sec	
Erase/Program Endurance		1,000,000		cycles	Minimum 100,000 cycles guaranteed

Notes : 1. 25 °C, V_{CC}=3.0 V 100,000 cycles, typical pattern.
2. System-level overhead is defined as the time required to execute the four bus cycle command necessary to program each byte. In the preprogramming step of the Internal Erase Routine, all bytes are programmed to 00H before erasure.

SWITCHING WAVEFORMS

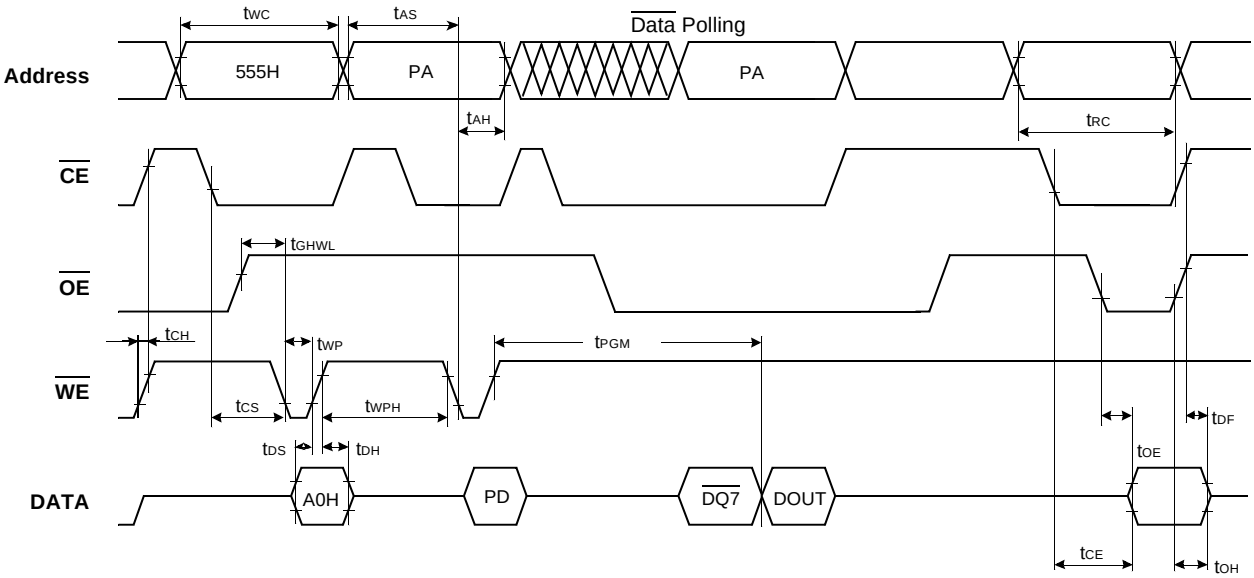
Read Operations



Parameter	Symbol	-9		-10		-12		-15		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	90		100		120		150		ns
Address Access Time	t_{AA}		90		100		120		150	ns
Chip Enable Access Time	t_{CE}		90		100		120		150	ns
Output Enable Time	t_{OE}		40		40		50		55	ns
$\overline{CE}$ & $\overline{OE}$ Disable Time	t_{DF}		30		30		30		40	ns
Output Hold Time from Address, $\overline{CE}$ or $\overline{OE}$	t_{OH}	0		0		0		0		ns
Output Enable Hold Time	t_{OEH}	0		0		0		0		ns

SWITCHING WAVEFORMS

Alternate $\overline{WE}$ Controlled Program Operations

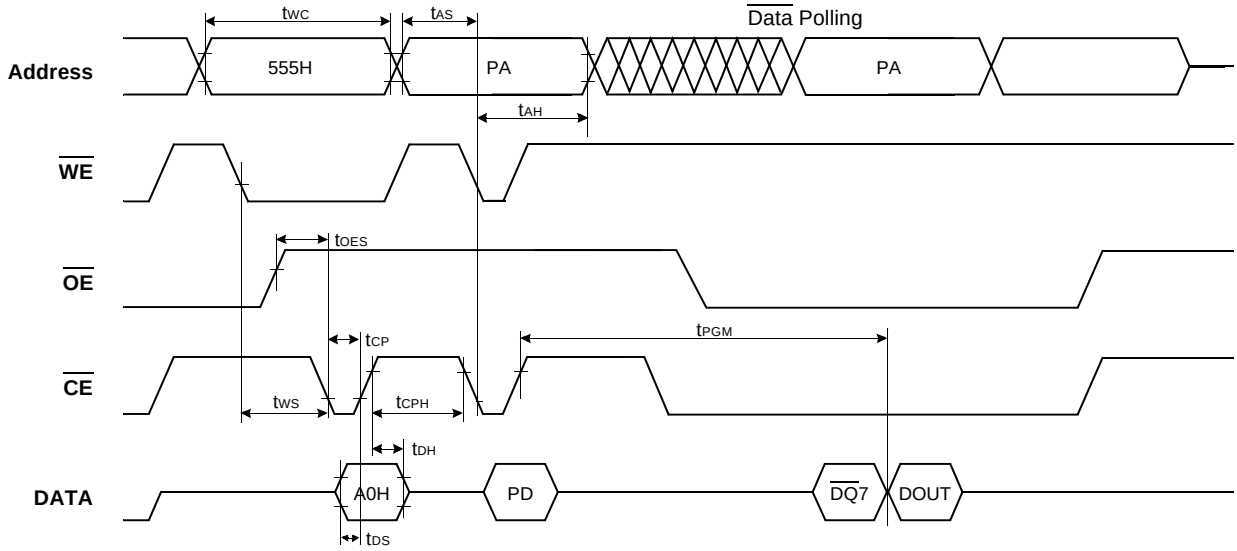


Notes :
1. $\overline{DQ7}$ is the output of the complement of the data written to the device.
2. DOUT is the output of the data written to the device.
3. PA : Program Address, PD : Program Data
4. The illustration shows the last two cycles of the program command sequence.

Parameter		Symbol	-9		-10		-12		-15		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time		tWC	90	-	100	-	120	-	150	-	ns
Address Setup Time		tAS	0	-	0	-	0	-	0	-	ns
Address Hold Time		tAH	50	-	50	-	50	-	65	-	ns
Data Setup Time		tDS	50	-	50	-	50	-	65	-	ns
Data Hold Time		tDH	0	-	0	-	0	-	0	-	ns
$\overline{CE}$ Setup Time		tCS	0	-	0	-	0	-	0	-	ns
$\overline{CE}$ Hold Time		tCH	0	-	0	-	0	-	0	-	ns
Write Pulse Width		tWP	50	-	50	-	50	-	65	-	ns
Write Pulse Width High		tWPH	30	-	30	-	30	-	35	-	ns
Programming Operation	Word	tPGM	11(typ.)		11(typ.)		11(typ.)		11(typ.)		µs
	Byte		9(typ.)		9(typ.)		9(typ.)		9(typ.)		µs
Read Cycle Time		tRC	90	-	100	-	120	-	150	-	ns
Chip Enable Access Time		tCE	-	90	-	100	-	120	-	150	ns
Output Enable Time		tOE	-	40	-	40	-	50	-	55	ns
$\overline{CE}$ & $\overline{OE}$ Disable Time		tDF	-	30	-	30	-	30	-	40	ns
Output Hold Time from Address, $\overline{CE}$ or $\overline{OE}$		tOH	0	-	0	-	0	-	0	-	ns

SWITCHING WAVEFORMS

Alternate $\overline{CE}$ Controlled Program Operations



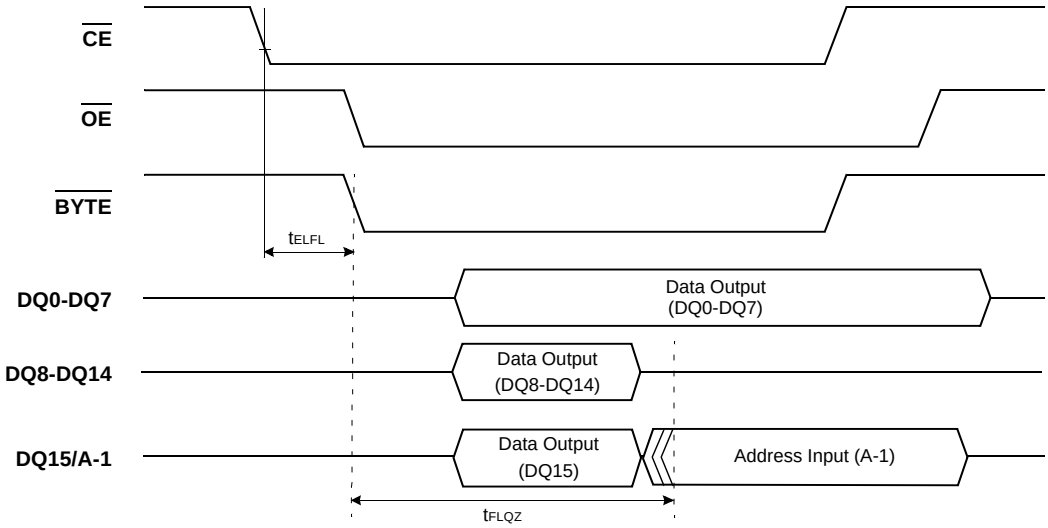
Notes :

1. PA is the address of the memory location to be programmed.
2. PD is the data to be programmed at byte address.
3. DQ7 is the output of the complement of the data written to the device.
4. DOUT is the output of the data written to the device.
5. The figure indicates the last two bus cycles of the four bus cycle sequence.

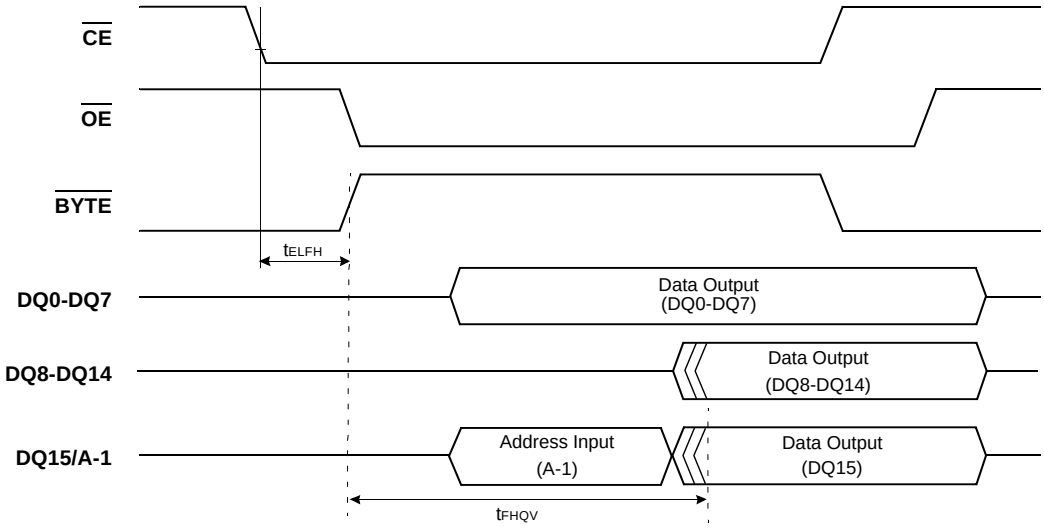
Parameter		Symbol	-9		-10		-12		-15		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time		tWC	90	-	100	-	120	-	150	-	ns
Address Setup Time		tAS	0	-	0	-	0	-	0	-	ns
Address Hold Time		tAH	50	-	50	-	50	-	65	-	ns
Data Setup Time		tDS	50	-	50	-	50	-	65	-	ns
Data Hold Time		tDH	0	-	0	-	0	-	0	-	ns
Output Enable Setup Time		tOES	0	-	0	-	0	-	0	-	ns
$\overline{WE}$ Setup Time		tWS	0	-	0	-	0	-	0	-	ns
$\overline{WE}$ Hold Time		tWH	0	-	0	-	0	-	0	-	ns
$\overline{CE}$ Pulse Width		tCP	50	-	50	-	50	-	65	-	ns
$\overline{CE}$ Pulse Width High		tCPH	30	-	30	-	30	-	35	-	ns
Programming Operation	Word	tPGM	11(typ.)		11(typ.)		11(typ.)		11(typ.)		µs
	Byte		9(typ.)		9(typ.)		9(typ.)		9(typ.)		µs

SWITCHING WAVEFORMS

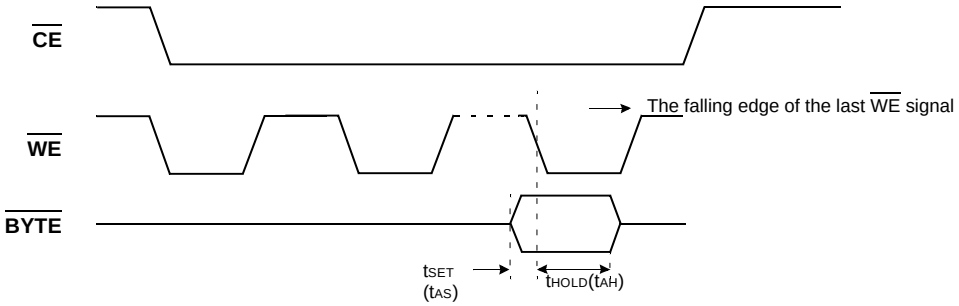
Word to Byte Timing Diagram for Read Operation



Byte to Word Timing Diagram for Read Operation

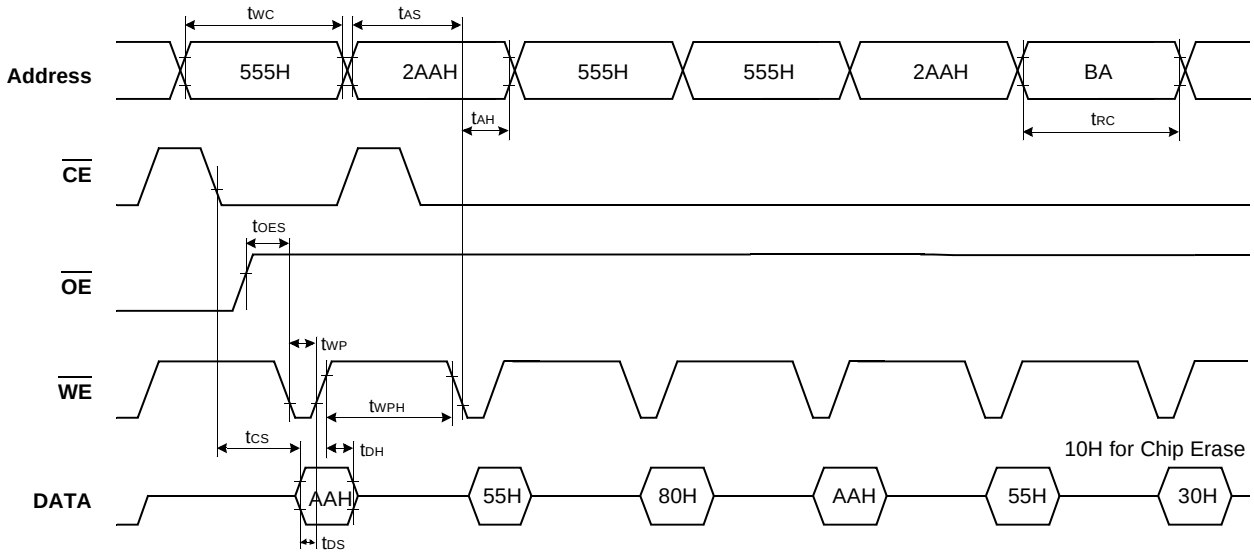


$\overline{\text{BYTE}}$ Timing Diagram for Write Operation



SWITCHING WAVEFORMS

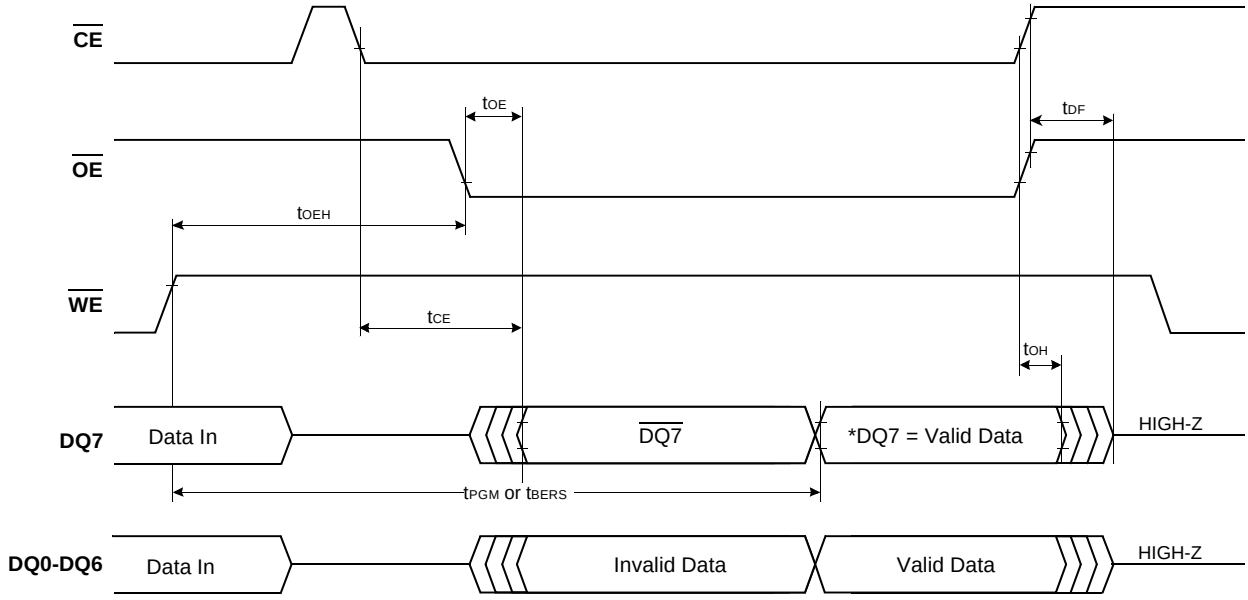
Chip/Block Erase Operations



Parameter	Symbol	-9		-10		-12		-15		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	90	-	100	-	120	-	150	-	ns
Address Setup Time	tAS	0	-	0	-	0	-	0	-	ns
Address Hold Time	tAH	50	-	50	-	50	-	65	-	ns
Data Setup Time	tDS	50	-	50	-	50	-	65	-	ns
Data Hold Time	tDH	0	-	0	-	0	-	0	-	ns
Output Enable Setup Time	tOES	0	-	0	-	0	-	0	-	ns
$\overline{CE}$ Setup Time	tCS	0	-	0	-	0	-	0	-	ns
Write Pulse Width	tWP	50	-	50	-	50	-	65	-	ns
Write Pulse Width High	tWPH	30	-	30	-	30	-	35	-	ns
Read Cycle Time	tRC	90	-	100	-	120	-	150	-	ns

SWITCHING WAVEFORMS

Data Polling During Internal Routine Operation

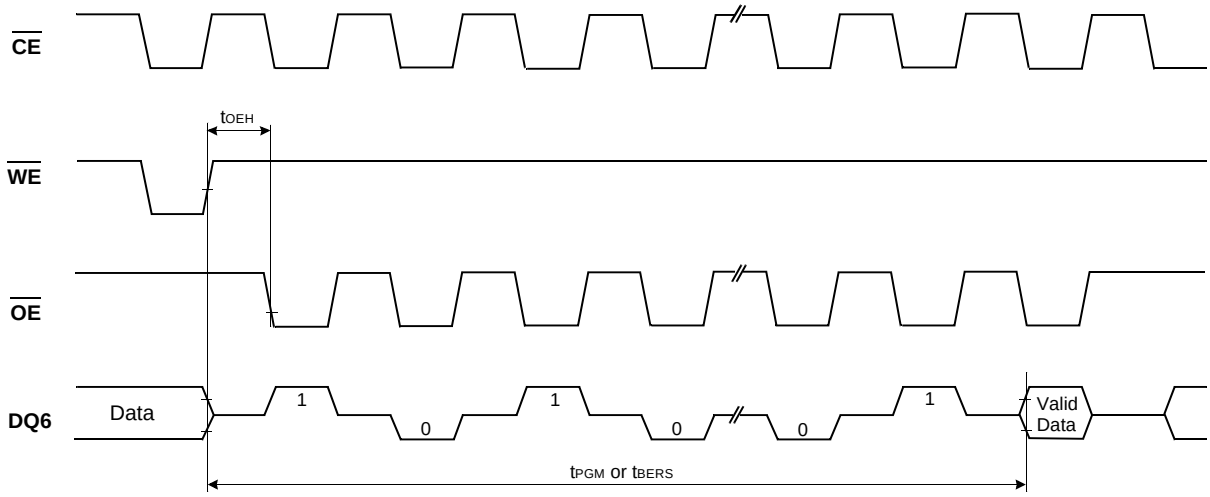


Note :
*DQ7=Vaild Data (The device has completed the internal operation).

Parameter		Symbol	-9		-10		-12		-15		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
Chip Enable Access Time		tCE		90		100		120		150	ns
Output Enable Time		tOE		40		40		50		55	ns
$\overline{CE}$ & $\overline{OE}$ Disable Time		tDF		30		30		30		40	ns
Output Hold Time from Address, $\overline{CE}$ or $\overline{OE}$		tOH	0		0		0		0		ns
Output Enable Hold Time		tOEH	10		10		10		10		ns
Programming Operation	Word	tPGM	11(typ.)		11(typ.)		11(typ.)		11(typ.)		µs
	Byte		9(typ.)		9(typ.)		9(typ.)		9(typ.)		µs
Block Erase Operation		tBERS	1(typ.)		1(typ.)		1(typ.)		1(typ.)		sec

SWITCHING WAVEFORMS

Toggle Bit During Internal Routine Operation

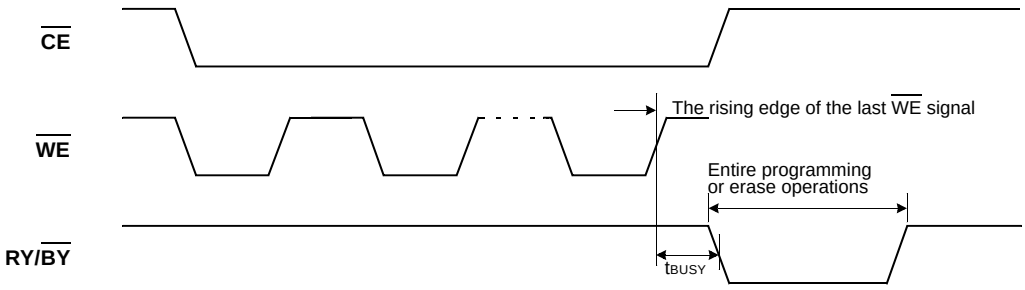


Note : During the write cycle, DQ6 will toggle between "1" and "0"

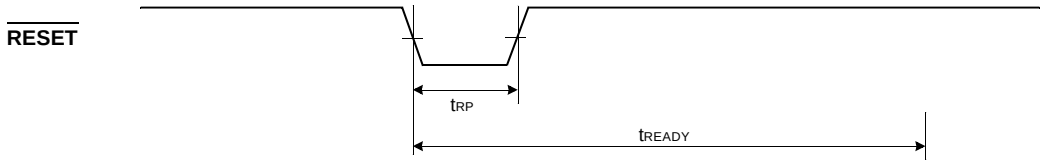
Parameter		Symbol	-9		-10		-12		-15		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
Output Enable Hold Time		t_{OEH}	10	-	10	-	10	-	10	-	ns
Programming Operation	Word	t_{PGM}	11(typ.)		11(typ.)		11(typ.)		11(typ.)		us
	Byte		9(typ.)		9(typ.)		9(typ.)		9(typ.)		us
Block Erase Operation		t_{BERS}	1(typ.)		1(typ.)		1(typ.)		1(typ.)		sec

SWITCHING WAVEFORMS

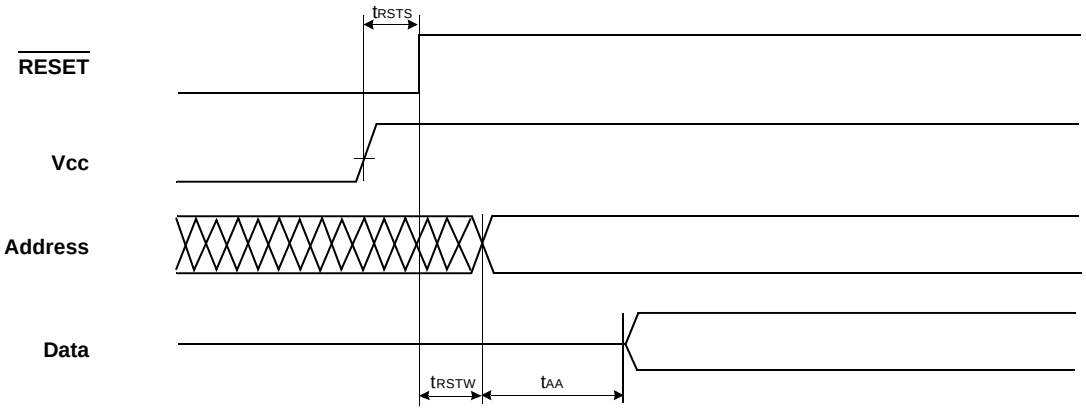
RY/$\overline{BY}$ Timing Diagram During Program/Erase Operation



$\overline{RESET}$ Timing Diagram



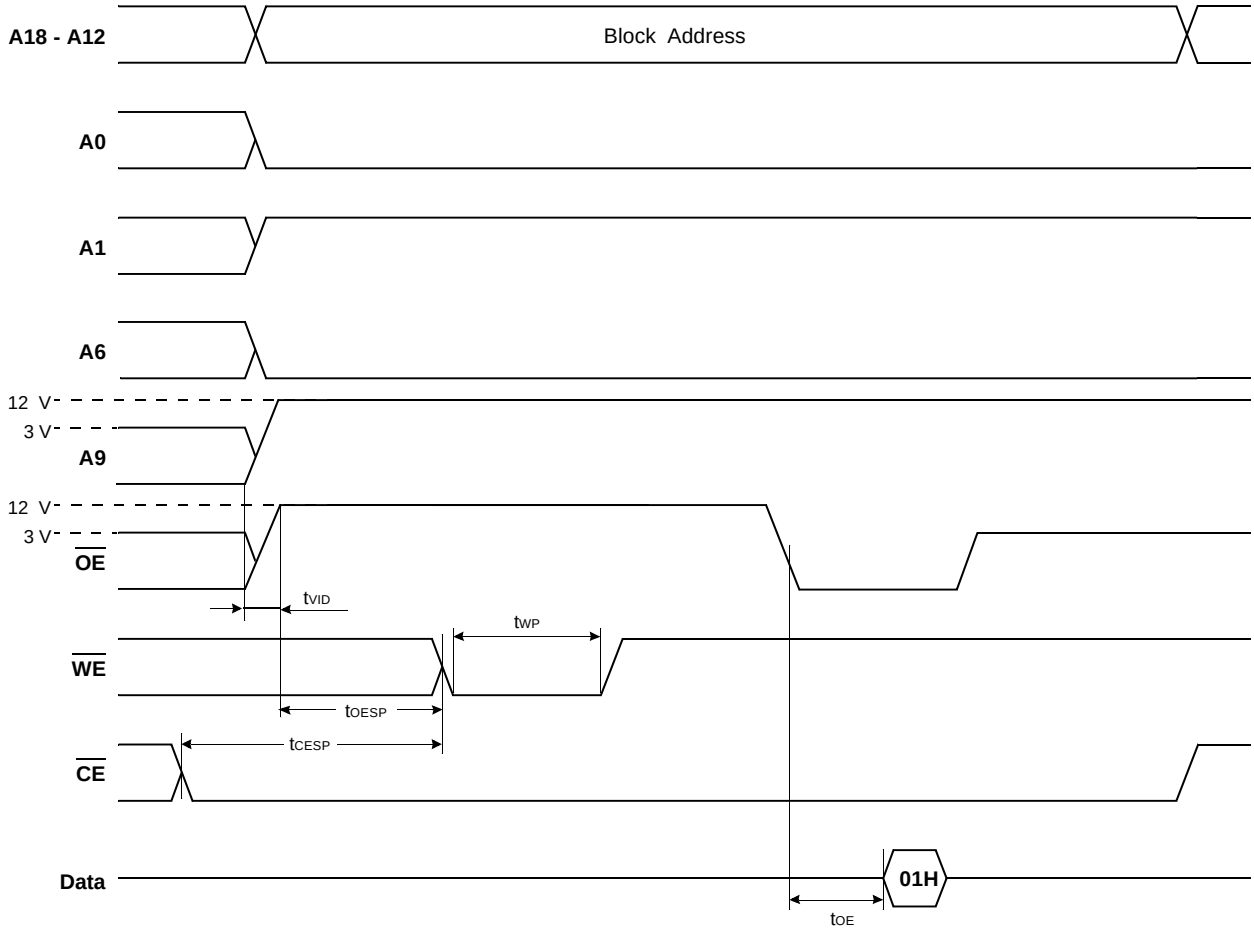
Power-up and $\overline{RESET}$ Timing Diagram



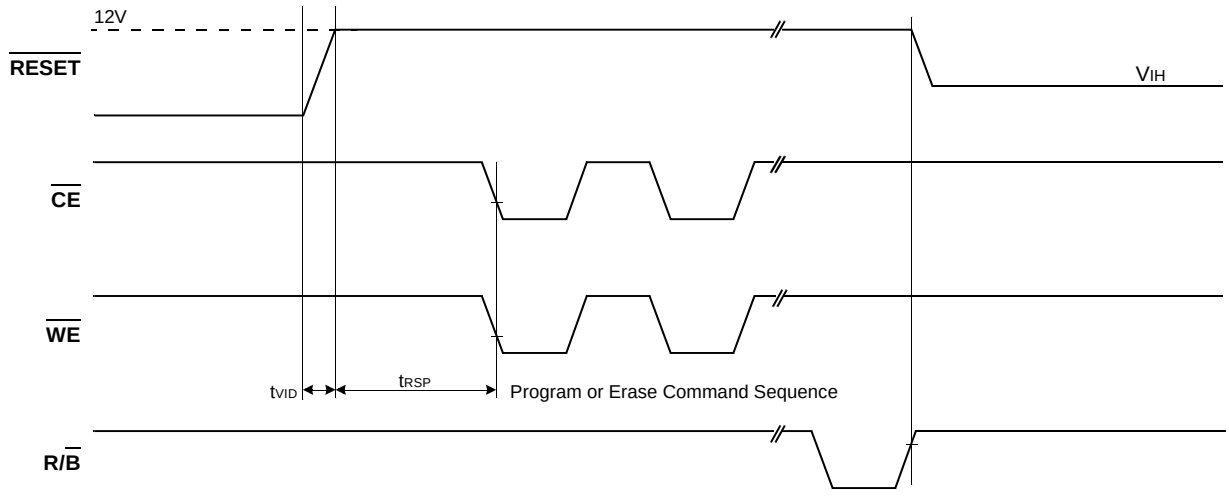
Parameter	Symbol	-9		-10		-12		-15		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Program/Erase Valid to RY/$\overline{BY}$ Delay	t_{BUSY}	90		90		90		90		ns
Reset Pulse Width	t_{RP}	500		500		500		500		ns
Reset Low To Valid Data	t_{READY}		20		20		20		20	us
Reset High to Address Valid	t_{RSTW}	200		200		200		200		ns
Reset Low Set-up Time	t_{RSTS}	500		500		500		500		ns

SWITCHING WAVEFORMS

Block Protection Operations



Temporary Block Unprotect



PACKAGE DIMENSIONS

48-PIN LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(I)

48 - TSOP1 - 1220F

Unit :mm/Inch