

KESTX02

290MHz – 350MHz ASK TRANSMITTER

The KESTX02 is a single chip ASK (Amplitude Shift Key) transmitter IC. It is designed to operate in a variety of low power radio applications including keyless entry, general domestic and industrial remote control RF tagging and local paging systems.

The transmitter offers a high level of integration and performance, which enables the harmonic rejection and fundamental power requirements of the German FTZ, and other governing bodies, to be met.

The basic architecture utilises a crystal reference oscillator, an integrated frequency multiplying PLL and a power output stage. The design is centred around the popular 315MHz operating frequency and particular emphasis has been placed on low current drain, including a power-down feature which greatly increases battery life.

FEATURES

- Low supply Current
- Power down feature
- Adjustable output power level
- Low external part count
- Fully integrated VCO, PLL and Power Amplifier

ABSOLUTE MAXIMUM RATINGS

Junction temperature	-55 to +150°C
Storage temperature	-55 to +150°C
Supply voltage	$V_{EE} -0.5$ to $+8.0$ V
Voltage on any pin	$V_{EE}-0.5$ to $V_{CC}+0.5$ V

Notes:

1. The voltage on pin OUT and OUTB (open collector outputs) can support a higher voltage than this (+14V).

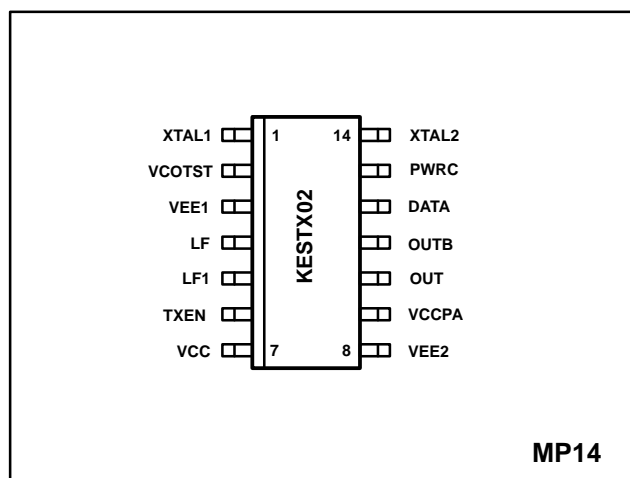
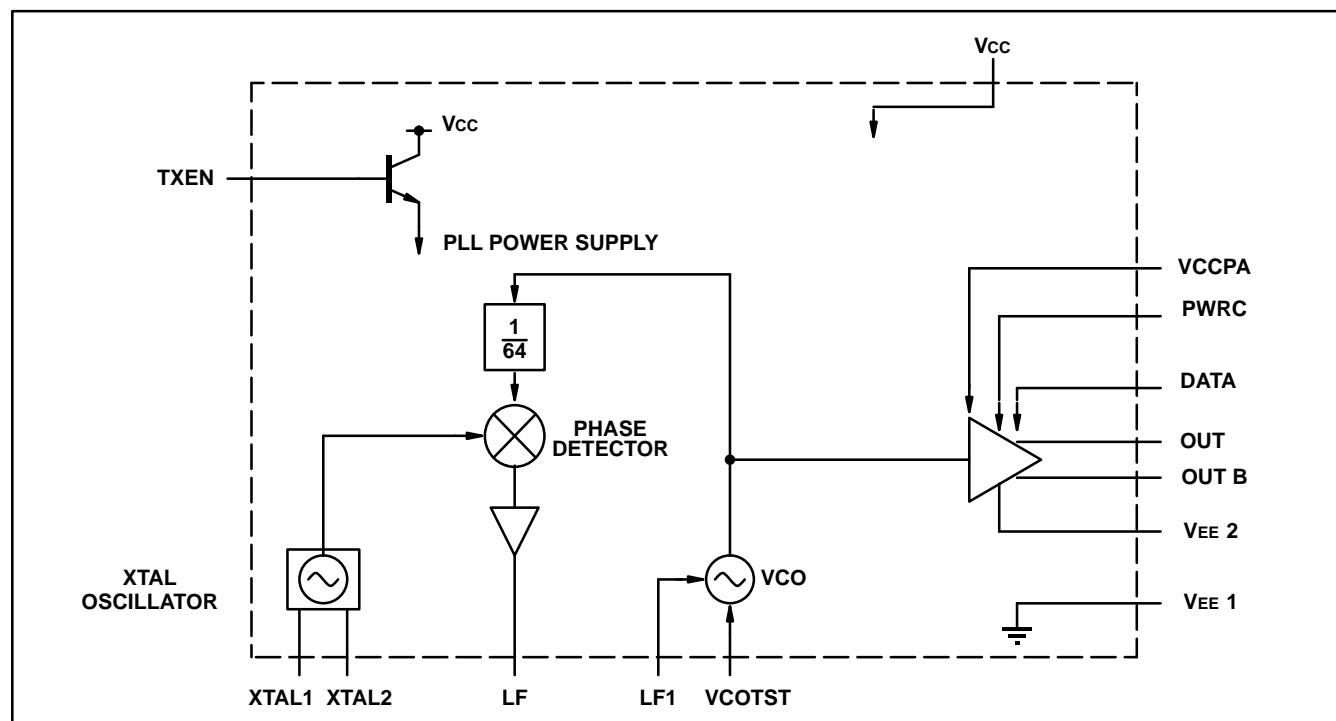


Fig. 1 Pin connections – top view

ORDERING INFORMATION

KESTX02/IG/MP1T (Tape and Reel)
KESTX02/IG/MP1S (Tubes)



KESTX02**ELECTRICAL CHARACTERISTICS Operating conditions**

$T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 3.5\text{V}$ to 7.0V . These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Parameter	Symbol	Value			Units	Conditions
		Min	Typ	Max		
Power supply voltage	V_{CC}	3.5		7.0	V	
Ambient temperature	T_a	-40		+85	$^{\circ}\text{C}$	

Electro static discharge 2kV all pins – human body model

ELECTRICAL CHARACTERISTICS D.C.

$T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 3.5\text{V}$ to 7.0V . These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Parameter	Symbol	Value			Units	Conditions
		Min	Typ	Max		
Supply current stand by mode	I_{CC1}			0.5	μA	$V_{TXEN}=0\text{V}$; $V_{DATA}=0\text{V}$
Supply current PLL enable/transmit space	I_{CC2}		2.50	4	mA	$I_{mod}=150\mu\text{A}$; $V_{CC}=V_{TXEN}=3.5\text{V}$ $V_{DATA}=\text{LOW}$; 315MHz
Supply current PLL enable/transmit space	I_{CC3}		10.5	12.0	mA	$I_{mod}=150\mu\text{A}$; $V_{CC}=V_{TXEN}=3.5\text{V}$ $V_{DATA}=\text{HIGH}$; 315MHz
Supply current PLL enable/transmit space	I_{CC4}		3.25	4	mA	$I_{mod}=150\mu\text{A}$; $V_{CC}=V_{TXEN}=7.0\text{V}$ $V_{Data}=\text{LOW}$; 315MHz
Supply current PLL enable/transmit mark see note 1	I_{CC5}		11.3	14.5	mA	$I_{mod}=150\mu\text{A}$; $V_{CC}=V_{TXEN}=7.0\text{V}$ $V_{DATA}=\text{HIGH}$; 315MHz
TXEN – transmit enable	V_{en}	3.5		$V_{CC}+0.2$	V	
TXEN – transmit disable/stand by	V_{dis}	$V_{EE}-0.2$		0.5	V	
Input bias current TXEN	I_{txen}			150	μA	TXEN = V_{CC} transmit enable
Bias voltage pin PWRC			1.20		V	$I_{mod}=150\mu\text{A}$
Data pin input logic high	V_{ih}	$0.7V_{CC}$		$V_{CC}+0.5$	V	
Data pin input logic low	V_{il}	$V_{EE}-0.5$		$0.3V_{CC}$	V	
Data pin input current – logic low	I_{inl}	-100			μA	
Data pin input current – logic high	I_{inh}			+100	μA	

Notes:– The maximum supply current is directly related to I_{mod} and hence the output power level.

ELECTRICAL CHARACTERISTICS A.C.

$T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 3.5\text{V}$ to 7.0V . These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Parameter	Symbol	Value			Units	Conditions
		Min	Typ	Max		
Output current at fundamental see note 1	IF75	2.1	2.4	2.6	pk-pk mA	$I_{mod}=75\mu\text{A}$, $F_o=315\text{MHz}$ $V_{CC}=3.5\text{V}$
Output current at fundamental see note 1	IF150	2.2	5.3	6.9	pk-pk mA	$I_{mod}=150\mu\text{A}$, $F_o=315\text{MHz}$ $V_{CC}=3.5\text{V}$

ELECTRICAL CHARACTERISTICS (cont.)A.C.

$T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 3.5\text{V}$ to 7.0V . These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Parameter	Symbol	Value			Units	Conditions
		Min	Typ	Max		
Output current fundamental see note 1	IF7150	2.6	5.8	7.5	pk-pk mA	$I_{mod}=150\mu\text{A}$, $F_o=315\text{MHz}$ $V_{CC}=7.0\text{V}$
Output current at 2 x fundamental see note 1&2				-40	dBc	$I_{mod}=150\mu\text{A}$, $F_o=315\text{MHz}$
Output current at 3x fundamental and all other spuri see note 1&2				-11	dBc	$I_{mod}=150\mu\text{A}$, $F_o=315\text{MHz}$
Phase detector gain	PDG		8			$\mu\text{A/rad}$
Extinction ratio see note 2	ER	40	80			dB
VCO gain	G_{VCO}		100			MHz/V
TXEN settling time see note 4	Txe			5.0		ms
Output sidebands due to reference frequency see note 5	SB		-40		dBc	$I_{mod}=150\mu\text{A}$, $F_o=315\text{MHz}$
30dB rise time	T30R		380		ns	
30dB fall time	T30F		430		ns	
VCO operating frequency		290	315	350	MHz	
DATA pulse width mark/space		100			μS	

Notes:

1. Limits can only be established after full characterisation of the part.
2. The spuri are specified relative to the fundamental measured in a 300KHz resolution bandwidth.
3. Extinction ratio is defined as the ratio of the output currents I (space):I(mark) measured at the output operating frequency.
4. Regulatory issues demand that transmission does not take place until the PLL has acquired lock and the VCO is operating at its final output frequency. This requirement demands that pin TXEN is set high at least Txe ms prior to the transmission of any data. This value is dependent on the PLL loop bandwidth and hence on the value of the external loop filter component values. The specification value above is for the loop filter components shown in the applications diagram (Fig. 6)
5. Sidebands on the output due to the PLL reference are a function of the PLL loop bandwidth and the application. This is considered further in a separate application note.

PIN LISTING

Signal	Description
XTAL1	Crystal oscillator
XTAL2	Crystal oscillator
DATA	Input data
TXEN	Transmit enable/stand by
OUT	Power amplifier output/antenna interface
OUTB	Power amplifier output/antenna interface (complementary output)
LF	Phase detector output

Signal	Description
LFI	VCO control input
PWRC	Output power control
VCCPA	Power amplifier positive supply
VEE2	Power amplifier ground
VEE1	PLL ground
VCC	Positive supply
VCOTST	VCO test control input

FUNCTION

When the IC is enabled (TXEN high) a phase locked loop locks the output of the VCO to a multiple of a crystal defined reference input. The output of the VCO operates at the final

output frequency and is the input to a power amplifier stage. The power amplifier directly drives the antenna.

KESTX02

Phase locked loop

Dividers

A divide by 64 prescaler is present in the PLL feedback loop. The final output frequency is then $F_o = 64 \times F_{ref}$.

Phase detector

The phase detector used is a phase frequency detector (PFD) with a current (charge pump) output. This phase detector has a triangular characteristic for an input phase error in the range $-2\pi < \theta_e < 2\pi$. The charge provides an output current in the range $\pm 50\mu A$ and hence gives a phase detector gain of $(50/2\pi) \mu A/rad$ ($\approx 8mA/rad$).

The advantage of the PFD over a pure phase detector is that it is also a frequency discriminator and will always lock the loop irrespective of the initial frequency offset. The PLL loop characteristics such as lock-up time, capture range, loop bandwidth and VCO reference sideband suppression are controlled by the external loop filter.

For certain applications spurious sidebands at the reference frequency must be adequately suppressed and a 3rd order loop is recommended.

VCO

To minimize external component costs the VCO is fully integrated. The frequency of the VCO is controlled by the voltage on pin LF.

Reference crystal oscillator

A differential crystal oscillator provides a reference clock for the PLL. The oscillator is configured for parallel resonant operation in the fundamental mode (typical operating frequency of 3–7MHz) and the crystal used should be specified for parallel resonance. The crystal is connected between pins XTAL1, XTAL2 with external components as shown in Fig.6.

Alternatively, a reference clock can be provided by an external source connected to pin XTAL2.

Output stage (PA)

The input signal at pin DATA produces amplitude shift key (ASK) modulation of the VCO output. This is achieved by

on–off keying of the bias current in the output power amplifier stage. The output of the PA is a balanced output (pin OUT and OUTB) and is current source driven (open collector outputs). The outputs of which should be D.C. referenced to a positive supply voltage (anticipated to be V_{CC} in most applications). The current source outputs can drive a PCB antenna directly (Fig. 5) or if a higher output power is required on limited supply headroom via a simple impedance transforming network.

A balanced output stage is used as it automatically suppresses the even order harmonics of the fundamental. Of particular importance for the European application is suppression of the 2nd harmonic (due to regulatory issues concerning spurious outputs). In order to obtain the benefits of this output stage it is essential to use a balanced antenna.

Power up

In the intended application it is expected that the transmitter will spend a large proportion of time in “stand by” not transmitting data. To maximise battery life it is important that very little quiescent current is taken in this mode.

The “stand by mode” is selected by setting pin TXEN low and similarly the transmitter is enabled by setting TXEN high. To minimize stand-by current TXEN is used to bias an on–chip npn transistor connected in a common collector configuration (Fig. 3). This transistor is used to provide the supply to large portions of the IC. Collapsing the supply when TXEN is set low results in a very low stand by current. The voltage on TXEN therefore should not exceed V_{CC} by more than 0.2V.

From an application standpoint the TXEN pin must be able to source the bias current for the input transistor and should also be decoupled if possible to prevent high frequency noise directly coupling into the IC power supply. The value of the decoupling capacitor and the drive capability of the TXEN source will affect power up delay. Since TXEN enables the PLL it is therefore essential that it is set high prior to any data transmission and that it remains high during the transmission. Therefore three different power drain modes are possible

- (i) Stand by (TXEN low, DATA low)
- (ii) PLL Mode/Transmit SPACE (TXEN high, DATA low)
- (iii) Transmit MARK (TXEN high, DATA high)

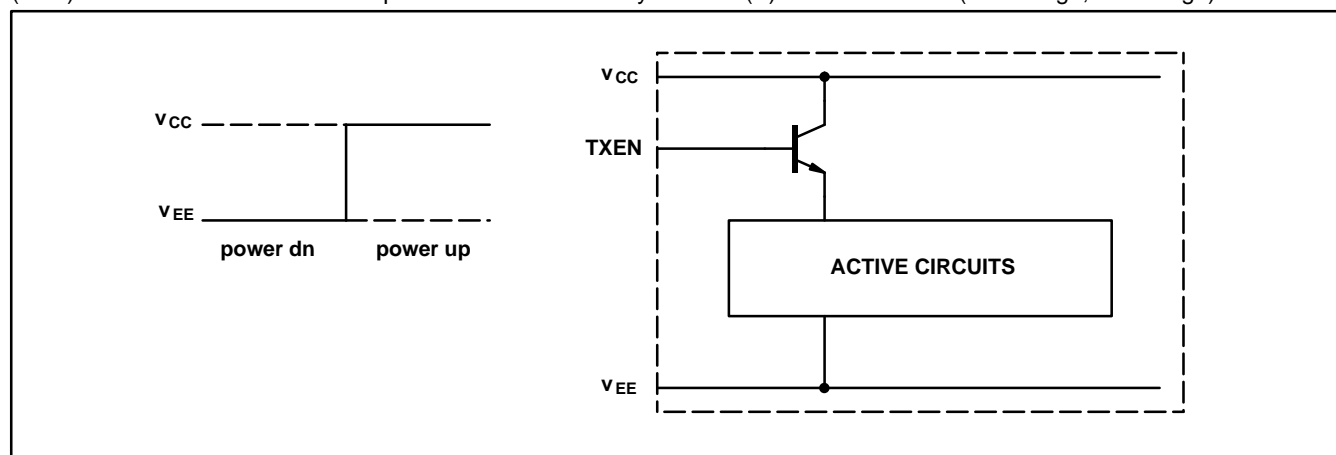


Fig. 3

APPLICATIONS INFORMATION

Power control

The bias current for the power amplifier directly controls the output current (and hence the output power). The bias current

is set by the external resistor connected between PWRC and ground. The bias voltage on pin PWRC is nominally 1.20V and hence the modulation current I_{mod} is given by $1.20/R$.

To a first order neither the linearity (harmonic spuri relative to fundamental) or the amplifier efficiency are affected by

Imod. the graph below shows typical simulation results for the amplifier current output with Imod variation.

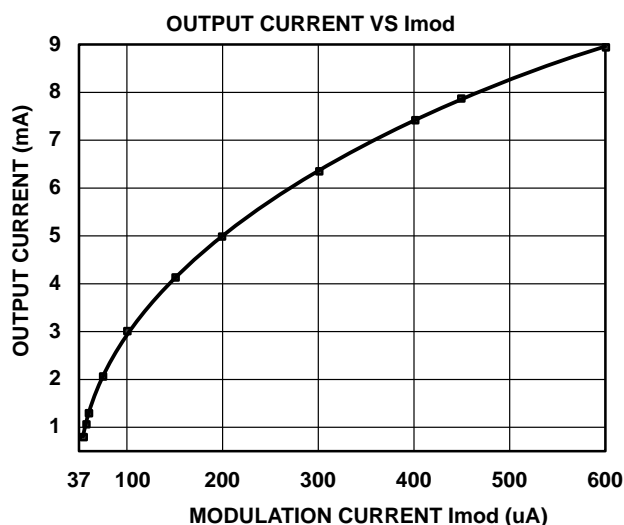


Fig. 4

Frequency accuracy

The stability of the output frequency is equal to that of the crystal referenced oscillator and shift in the VCO frequency during data modulation. To operate with a final output accuracy of $\pm 50\text{KHz}$ at 315MHz (as required for use with the receiver KESRX01) would require a crystal with a tolerance specification of $\pm 150\text{ppm}$. This tolerance should encompass all causes e.g. initial accuracy, temperature stability and ageing.

Operation at a final output frequency of 315MHz requires a crystal specified for operation at 4.92MHz.

Antenna interface

The IC is capable of directly interfacing to a PCB loop antenna as shown in the applications diagram (Fig. 6). However some considerations have to be borne in mind.

The Figure below (Fig. 5) is an equivalent circuit for a PCB loop antenna. The inductance of the loop is Lant and this is in series with two resistors. These represent Rr the radiation resistance and Rs the series resistance of the antenna.

The Q of the antenna is defined as $(\omega_0 \cdot L_{ant} / (R_s + R_r))$ where ω_0 is the resonant frequency (rad/s) of the antenna. At resonance the antenna can be transformed to the equivalent circuit on the right hand side. Here the equivalent parallel

resistance Rp is given by

$$R_p = (R_s + R_r)(Q^2 + 1)$$

For example, $L_s = 55\text{nH}$, $f_0 = 315\text{MHz}$, $R_s + R_r = 2.2\Omega$, $Q = 50$, gives an equivalent parallel resistance of $5.4\text{k}\Omega$.

Typically the antenna will be d.c. referenced to VCC as shown in the applications diagram. The maximum voltage swing across the antenna is therefore limited by the RF saturation voltage of the output PA stage. This is of the order of 0.5V and hence the peak to peak voltage across the antenna will be $2 \cdot (V_{CC} - 0.5V)$ e.g. 9V for $V_{CC} = 5V$. This means that the maximum current that can be driven into the load is 1.7mA (peak-peak at the fundamental) and the external power control resistor should be set accordingly.

If it is necessary to drive more power into the antenna a possible way to accomplish this is to perform an impedance transformation to the antenna.

The antenna also acts as a filter on unwanted harmonic spuri. The use of a balanced output suppresses the 2nd harmonic (and other even order harmonics). The 3rd harmonic of the fundamental is not automatically suppressed. However even a Q as low as 10 will reduce the 3rd harmonic by a further 32dB relative to the fundamental.

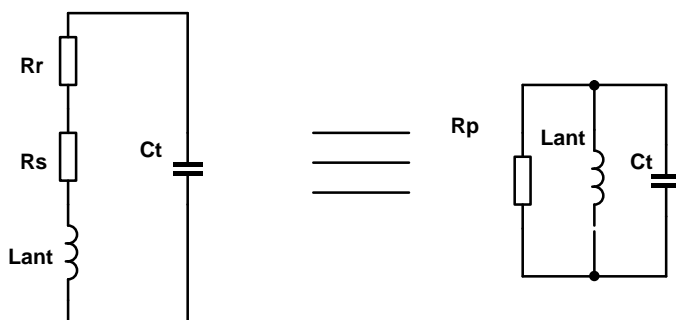


Fig. 5 Loop antenna

Note: The above application diagram is provided to assist the customer in using the IC and no guarantee can be made to its correctness.

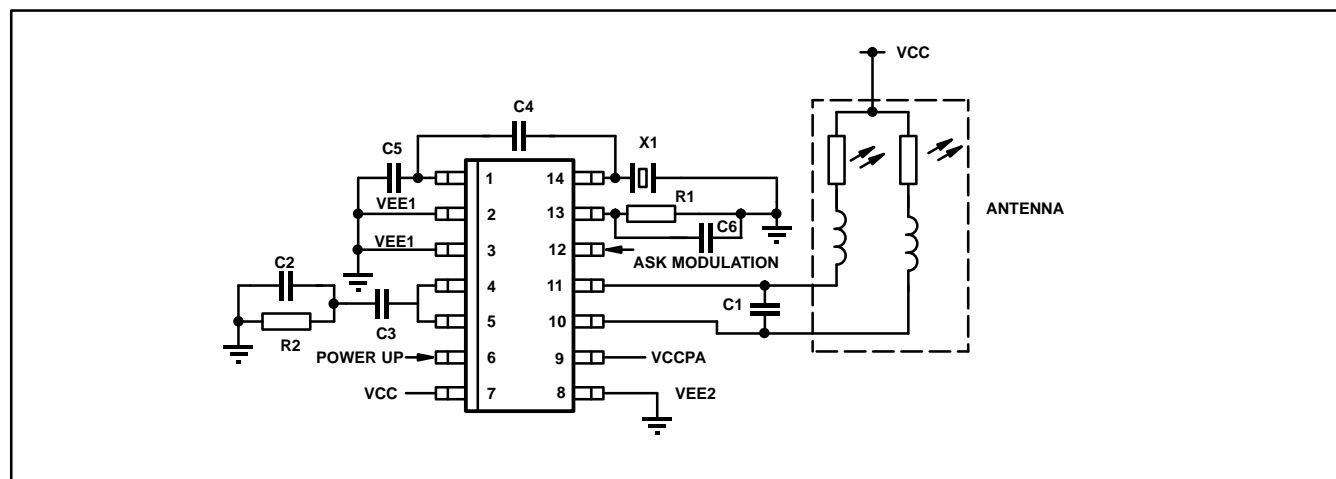


Fig. 6 Application diagram

COMPONENT LIST

COMPONENTS	FUNCTION	VALUE	UNITS
R1	OUTPUT POWER CONTROL	8.2	kΩ
R2	PLL LOOP FILTER	820	Ω
C1	ANTENNA TUNING	APPLICATION DEPENDENT	F
C2	PLL LOOP FILTER	3.9	nF
C3	PLL LOOP FILTER	2.2	nF
X1	PARALLEL RESONANT CRYSTAL	4.92	MHz
C4	CRYSTAL OSCILLATOR	47	pF
C5	CRYSTAL OSCILLATOR	33	pF
C6	PWRC DECOUPLE	100	pF

TESTABILITY REQUIREMENTS

This section is a summary of the observability and controllability requirements identified to simplify the production test requirements of the device.

an external clock source as shown in Fig. 7. Typically a 200mVpk clock signal is AC coupled to produce differential output on OP and OPb to the PFB ($C=10\text{nF}$, R_s (Source) $<5\text{k}\Omega$)

1. Ability to directly drive crystal oscillator from the tester (no Crystal). The XTAL2 pin allows direct drive of the oscillator with

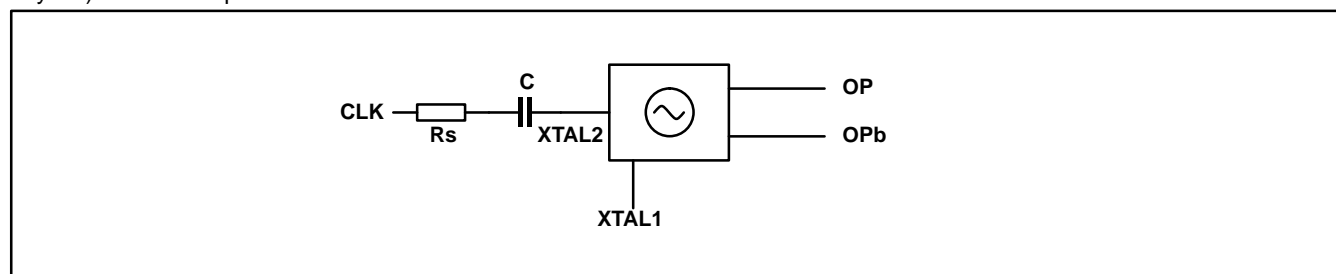


Fig. 7 Direct drive of crystal oscillator

2. Control of the VCO frequency is obtained via the LFI signal pin. The output of the dividers is tested by measuring the DC current output of the charge pump (with XTAL2 held at V_{CC}).

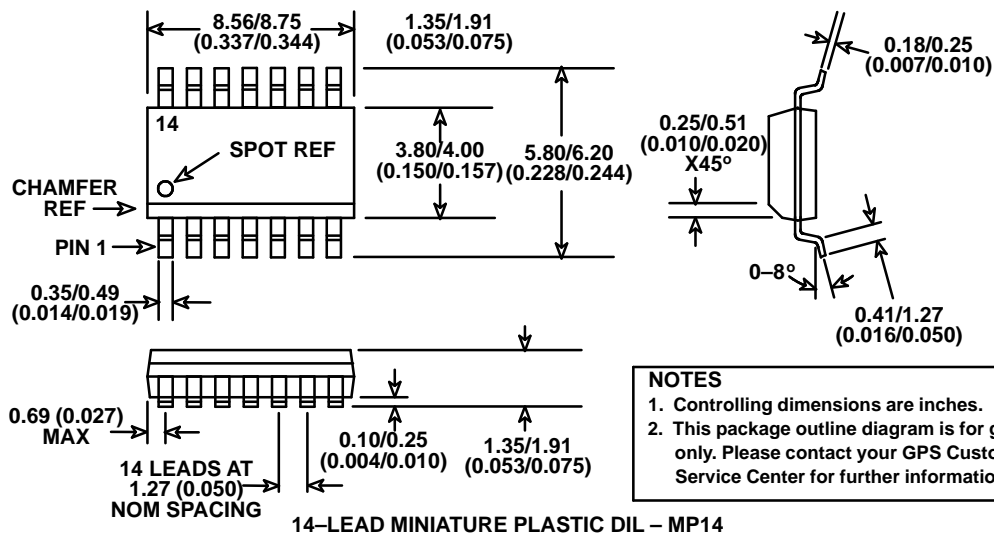
measuring the current through the open collector outputs OUT and OUTB. The VCO input to the power amplifier is disabled with VCOTST tied to V_{CC} and the bias current being measured with DATA tied to V_{CC} . Toggling DATA input will modulate the bias current in the power amplifier.

3. DC operation of the power amplifier is observed by

PACKAGE DETAILS

Dimensions are shown thus: mm (in). For further package information please contact your local Customer Service Centre.

14 LEAD MINIATURE PLASTIC MP14



HEADQUARTERS OPERATIONS

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