GEC PLESSEY SEMICONDUCTORS

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PRELIMINARY INFORMATION
D.S. 3968 1.5

KESRX01

290 – 460MHz ASK RECEIVER

The KESRX01 is a single chip ASK (Amplitude Shift Key) Receiver IC. It is designed to operate in a variety of low power radio applications including keyless entry, general domestic and industrial remote control RF tagging and local paging systems.

The receiver offers an exceptionally high level of integration and performance, which enables the harmonic rejection and fundamental power requirements of the German FTZ, and other governing bodies, to be met. The architecture is a single conversion super–heterodyne receiver. Local oscillator generation is performed by a PLL which utilises a crystal reference oscillator.

The design is centred around the popular 433.92MHz operating frequency, but has a wide operating bandwidth supporting frequencies in the range 290 – 460MHz. Particular emphasis has been placed on low current consumption. The on–chip VCO and IF significantly minimise the external components needed thus reducing any re–radiation effects.

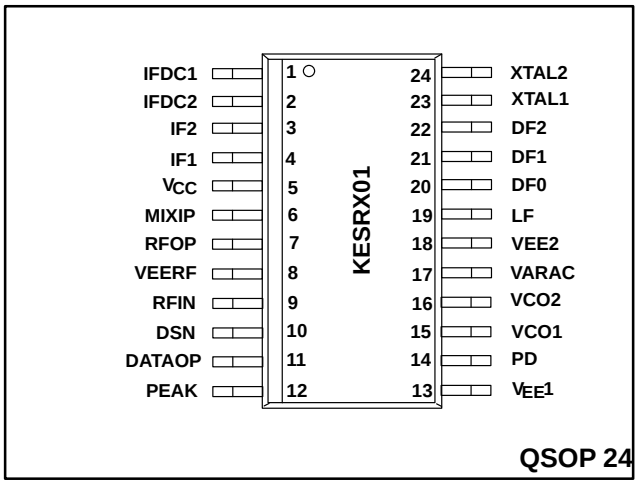


Fig. 1 Pin connections – top view

FEATURES

- Very low supply current (2.25mA typical)
- Low external part count
- –103dBm sensitivity
- Integrated VCO and IF Filters.

ABSOLUTE MAXIMUM RATINGS

All voltages relative to V_{EE} (0V)

Junction temperature, Tj	–55 to +150°C
Storage temperature, Tstg	–55 to +150°C
Supply voltage, V_{CC} max	V_{CC} –0.5 to +8.0 V
Voltage on any pin, Vshort	–0.5 to +8.0V

ORDERING INFORMATION

KESRX01/IG/QPIT (Tape and Reel)
KESRX01/IG/QP1S (Tubes)

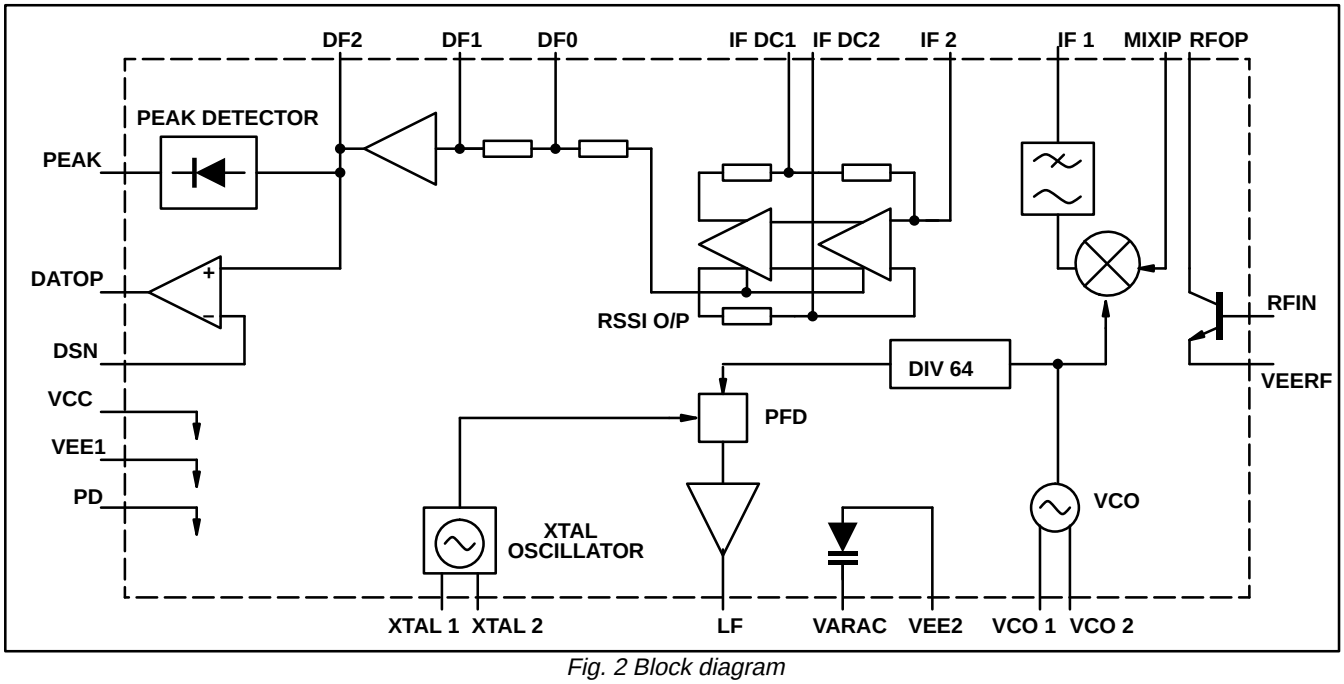


Fig. 2 Block diagram

ELECTRICAL CHARACTERISTICS D.C.

T_{amb}= –40°C to +85°C, V_{CC}= 5V to 7.5V. These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Parameter	Symbol	Value			Units	Conditions
		Min	Typ	Max		
Supply current	I_{CC1}		2.25	2.74	mA	V_{CC}=5V, all
Supply current (PLL powered down)	I_{CC2}		1.83	2.25	mA	V_{CC}=5V, all
Power down pin input logic high	V_{ih}	V_{CC}–0.5		V_{CC}+0.5	V	
Power down pin input logic low	V_{il}	V_{EE}–0.5		V_{EE}+0.5	V	
Peak detector source current	I_{pk}		500		μA	
Peak detector leakage current	I_{lk}			250	nA	
Data output Logic High	V_{oh}	0.7V_{CC}			V	Iload=10μA
Data output Logic Low	V_{ol}			0.3V_{CC}	V	Iload=10μA

Electrostatic discharge (ESD) protection (human body model) 2KV minimum, all pins.

ELECTRICAL CHARACTERISTICS A.C.

T_{amb}= –40°C to +85°C, V_{CC}= 5V to 7.5V. These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Parameter	Symbol	Value			Units	Conditions
		Min	Typ	Max		
Sensitivity see note 1			–103		dBm	R_S=50Ω
Signal handling see note 2			–23.5		dBm	R_S=50Ω
Spurious reverse isolation to RFIN see note 3			100		μV (rms)	Rs=50Ω
Adjacent channel rejection see note 4	ACR		65		dB	

Notes:

1. Sensitivity is defined as the average signal level measured at the input necessary to achieve a bit error rate of 10^{-2} where the input signal is a return to zero pulse (RZ) with an average duty cycle of 50%. The RF input is assumed to be matched into 50Ω as shown in the application diagram.
   The data filter bandwidth is as shown in the application diagram.
2. Signal handling is defined as the maximum input signal capable of being successfully de–modulated. It is assumed the input is ASK modulated with an extinction ratio of at least 40dB. The combination of this specification together with the sensitivity specification give a signal handling dynamic range of > 80dB. The RF input is assumed to be matched into 50Ω as shown in the applications diagram.
3. –67dBm in 50Ω measured with the RF input matching network.
4. Adjacent channel rejection is defined for an interfering tone (ACR)dB above threshold and 10MHz offset from the carrier giving a 3dB reduction in sensitivity i.e. the interfering tone is 4.74mV (rms) @ Fc±10MHz and to achieve the specified sensitivity the wanted signal will have to be increased to 2.1μV (rms).

PIN LISTING

Pin	Symbol	Description
1	IFDC1	IF amplifier – decouple point
2	IFDC2	IF amplifer – decouple point
3	IF1	Mixer output
4	IF2	IF amplifer input
5	VCC	Positive power supply
6	MIXIP	RF mixer input (tank)
7	RFOP	RF amplifier output (tank)
8	VEERF	RF amplifier ground
9	RFIN	RF input (antenna)
10	DSN	Bit slicer comparator negative input
11	DATAOP	Bit slicer comparator output
12	PEAK	Peak detector output
13	VEE	Negative power supply (0V)

Pin	Symbol	Description
14	PD	PLL power down
15	VCO1	VCO maintaining amplifer
16	VCO2	VCO maintaining amplifier
17	VARAC	Varactor, positive biase
18	VEE2	Varactor ground
19	LF	PLL loop filter O/P output
20	DF0	Data filter – external connection
21	DF1	Data filter – external connection
22	DF2	Data filter – external connection
23	XTAL1	Crystal oscillator
24	XTAL2	Crystal oscillator

FUNCTION

Phase locked loop

The phase locked loop generates the local oscillator by frequency multiplication of a crystal referenced oscillator.

Dividers

A divide by 64 prescaler is present in the PLL feedback loop. The local oscillator frequency is then $Fo=64xF_{ref}$. For the system operating at 433.92MHz (RFIN) with a 270KHz IF frequency would require a reference of 6.77578MHz (assuming mixer low side injection). Alternative choice of crystal and tank components permit operation at specific frequencies in the range 290 – 460MHz.

Phase detector

The phase detector used is a phase frequency detector (PFD) with a current (charge pump) output. This phase detector has a triangular characteristic for an input phase error in the range $-2\pi < \theta e +2\pi$ and has the benefit of being a true frequency detector (as well as a phase detector) and hence will always achieve lock for any initial VCO frequency.

The charge pump provides an output current in the range $\pm 30\mu A$ and hence gives a phase detector gain of $4.8\mu A/rad$.

The PLL loop characteristics such as lock–up time, capture range, loop bandwidth and VCO reference sideband suppression are controlled by the external loop filter.

For the intended application a 2nd order loop should be sufficient as shown in the application diagram Fig. 6.

VCO

A balanced configuration is used with the LC tank connected externally across VCO1 and VCO2 Fig.3.

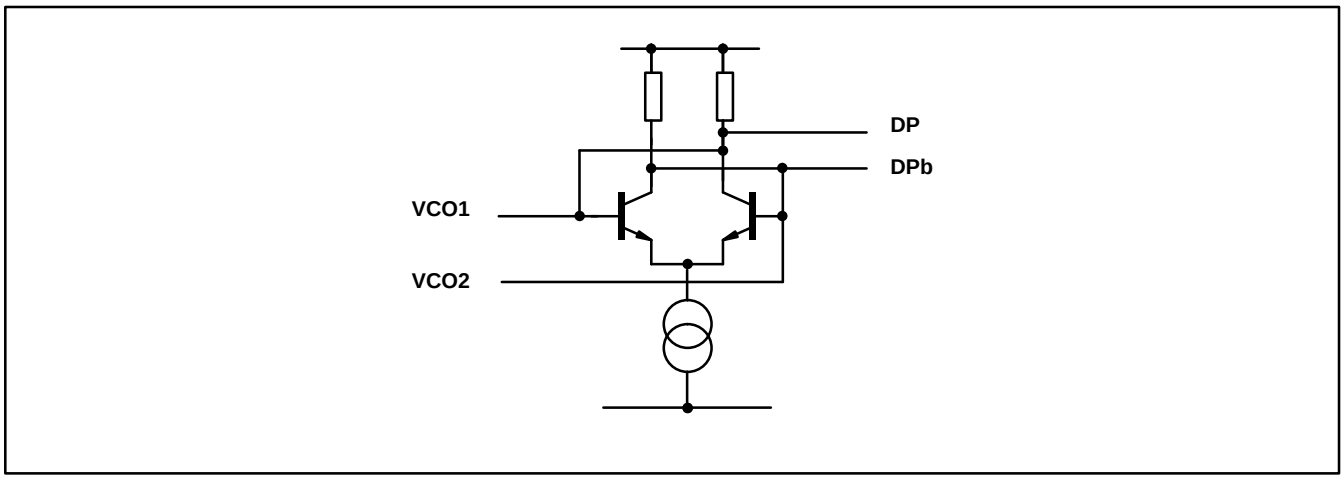


Fig. 3 Input circuit of VCO and divider chain.

External SAW resonator

For reduced power the PLL based oscillator can be replaced by a SAW based oscillator. If pin PD is tied low (VEE) the crystal oscillator, dividers and phase detector/charge pump are powered down. The VCO can then be used as a maintaining amplifier for an external SAW based oscillator. The normal mode of operation is with PD set high (VCC) or alternatively left unconnected. Note: the power down facility is intended to be hard wired (either to VCC or VEE and hence the PD pin is not specified for operation with normal CMOS or TTL logic levels.

PD	MODE
V_{CC}/NC	PLL Enable
V_{EE}	PLL Disable

Reference crystal oscillator

A crystal stabilised oscillator provides a reference clock for the PLL. The oscillator is configured for parallel resonant operation in the fundamental mode (typical operating frequency of 3–7MHz). The crystal is connected between pins XTAL1, XTAL2 with external components as shown in Fig. 6. Note that the external load capacitors depend on the choice of crystal.

RF amplifier

The RF amplifier consists of a low noise transistor in a common emitter configuration. A separate emitter connection is provided (VEERF) to reduce sensitivity to any common impedance in this path. The amplifier is current source biased so the signal (RFIN) should be a.c. coupled.
The collector is open circuit so that the gain can be set with an external tuned load. Fig. 6.

Down converting mixer

The RF input to the mixer is a.c. coupled from the tank (this also allows an impedance transform to be used as shown in Fig. 6). A doubly balanced mixer configuration is used.

IF filtering

The IF filter has a (nominal) bandpass response from 25KHz to 650KHz. The single high pass section is provided by the combination of the external a.c. coupling capacitor between IF1 and IF2 and an on chip resistor (nominal value 12kΩ.) The low pass section is entirely on chip and to meet the selectivity requirements (adjacent channel rejection) this filter has 4 low pass poles with a Butterworth response.

IF amplifiers and demodulator

The majority of the receiver gain is provided in the form of an IF limiting strip. These amplifiers are all d.c. coupled and hence differential d.c. feedback is required. This is decoupled externally at pins IFDC1 and IFDC2. The IF amplifier stages also combine a Received Signal Strength Indicator (RSSI) function. Since the modulation is ASK and the RSSI output has a linear output for a logarithmic change on its input then the RSSI output is the demodulated data. The only uncertainty is the d.c. level.

Data filter

Prior to the data slicer the demodulated data passes through a low pass filter. This filter is a 2nd order Sallen–Key section using an on chip voltage follower. External capacitors set the cutoff frequency and filter Q. The value of the on chip resistors is 100kΩ (nominal). See Fig. 4.

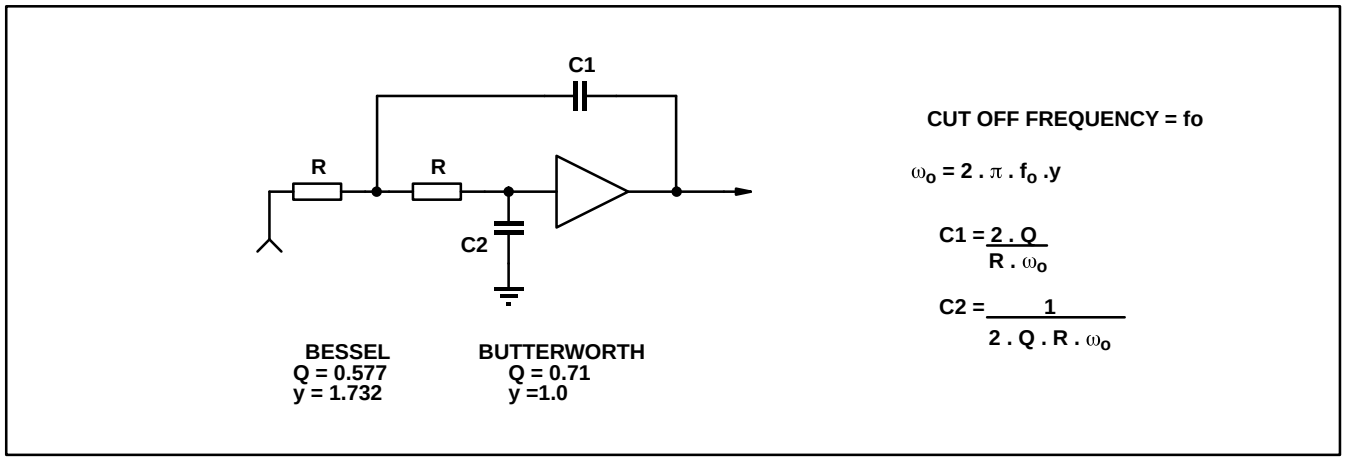


Fig. 4 Choosing data filter components

Example

To implement a Bessel response filter with a 10KHz 3dB cutoff

C1 = 106pF C2 = 80pF

Bit slicer and Peak Detector

To provide maximum flexibility an independent data comparator is provided. External circuitry must be provided to obtain the bit slicer threshold level. Two basic approaches are supported.

1. For coding schemes with no d.c. content (e.g. Manchester coding or 33% / 66% pulse width encoding) this can be based on the integrated d.c. level (as shown in the applications diagram)

2. For coding schemes with d.c. content (e.g. low duty cycle pulse width modulation) an active peak detector is included. The output at pin PEAK represents the peak level at the data filter output (as shown in Fig.5). An external RC time constant at this pin determines the maximum attack and decay times of the peak detector. Typical values for the leakage and diode current source capability are shown in the specifications.

The comparator has relatively low drive capability (push/pull current source output of 20μA) and hence DATOP

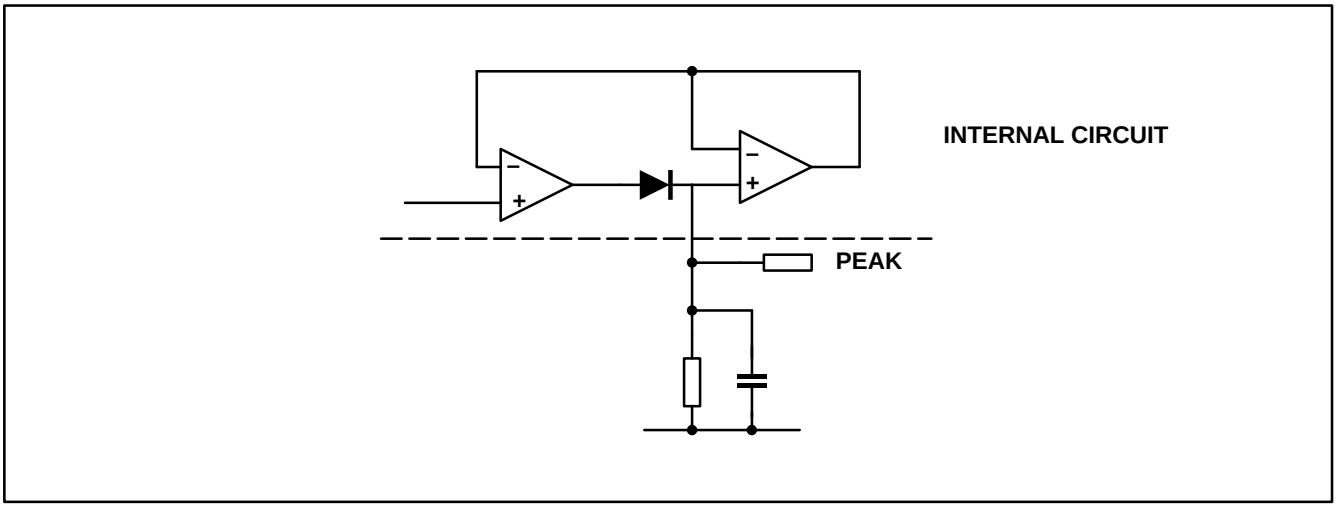


Fig. 5 Peak detector output

should not be excessively loaded. On chip positive feedback around the comparator provides a nominal hysteresis level of 20mV.

SENSITIVITY

In digital radio systems, sensitivity is often defined as the lowest signal level at the receiver input that will achieve a specified Bit Error Rate (BER) at the output. The sensitivity of the KESRX01 receiver, when used in the 315MHz application shown in Fig. 6, is typically –105dBm average power (ASK modulated with 2kHz, 50% duty cycle square wave) to achieve a 0.01 BER. The input was matched for a 50Ω signal source. At 434MHz–103dBm average power is typically achievable. The component values for the 315MHz application are given in Table 1 and, where they differ, the values for the 433MHz application are given in brackets. The circuit shown is a simple example provided to assist in evaluating the device; a detailed Application note will be published with more system, block level and circuit information to aid the design and optimise sensitivity in other applications.

Choice of IF frequency and IF bandwidth

The IF frequency is selected to be nominally 270KHz with the low frequency cutoff at 25KHz and the high frequency cutoff at 650KHz (nominal).

The suggested (see transmitter design specification application notes) accuracy of the transmitter is 433.92MHz ±100KHz. i.e from 433.82MHz to 434.02MHz.

The local oscillator frequency is set at 433.65MHz with a required accuracy of at least ±100kHz (see section below) i.e 433.55MHz to 433.75MHz.

This guarantees that the IF (70KHz to 470KHz) falls within the acceptance bandwidth of the IF filter.

The frequency of operation for such products in Europe is 433.05MHz to 434.79MHz. The choice of such a low IF frequency ensures that any image falls within the regulatory band. This in turn ensures that the receiver cannot be blocked by the image response of an unwanted signal outside of this band.

Frequency Accuracy

The stability of the local oscillator is equal to that of the crystal referenced oscillator. Therefore to obtain a final output accuracy of ±100KHz at 433MHz would require a crystal with a tolerance specification of ±230ppm. This tolerance should encompass all causes e.g. initial accuracy, temperature stability and ageing.

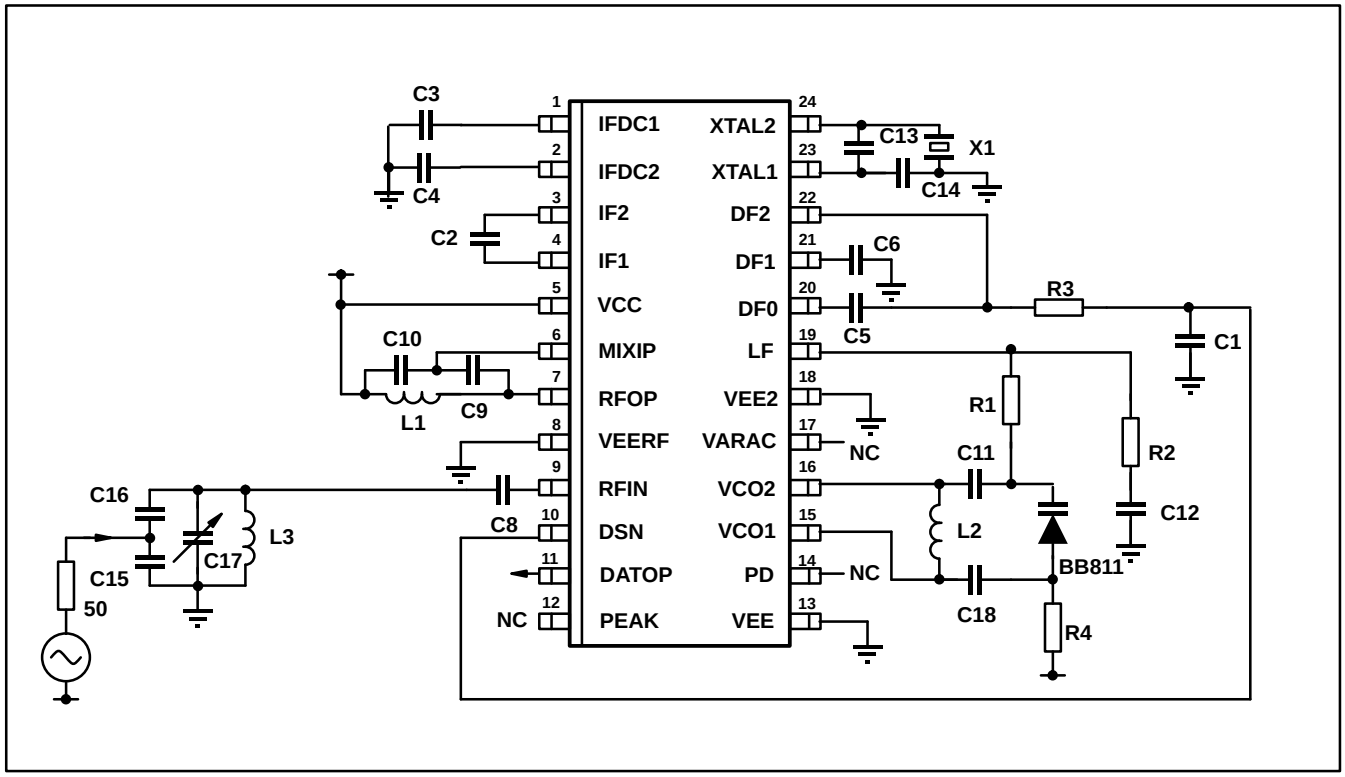


Fig. 6 Application diagram for 433MHz

Component	Function	Value	Units
C1	Data slicer threshold time constant	10	nF
C2	IF filter high pass	470	pF
C3	IF amplifier decouple	100	nF
C4	IF amplifier decouple	100	nF
C5	Data filter	100	pF
C6	Data filter	82	pF
C8	RF amplifier input	100	pF
C9	RF amplifier load	7	pF
C10	RF amplifier load	8	pF
C11	VCO decouple	33	pF
C12	PLL loop filter	560	nF
C13	Crystal oscillator	39	pF
C14	Crystal oscillator	39	pF
C15	RF Input matching network	5	pF
C16	RF Input matching network	2	pF
C17	RF Input matching network (variable)	1.5 – 3.0	pF
C18	VCO decouple	33	pF
L1	RF amplifier load	39 (22)	nH
L2	VCO tank circuit	39 (18)	nH
L3	RF Input matching network	27 (18)	nH
R1	Varactor bias	47	kΩ
R2	PLL loop filter	18	kΩ
R3	Data slicer threshold time constant	100	kΩ
R4	Varactor bias	47	kΩ
X1	Parallel resonant crystal	4.91766 (6.77578)	MHz

Table 1

If required, the reference signal to the PLL can be driven externally from a stable signal source as shown in Fig. 7. Typically a 200mVp clock signal is ac coupled to produce differential output on OP and OPb. (C=10nF, Rs (source) < 5kΩ)

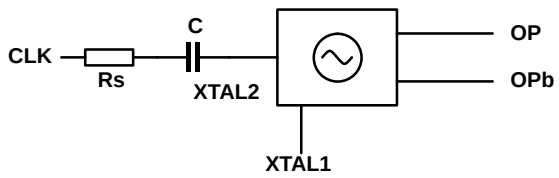
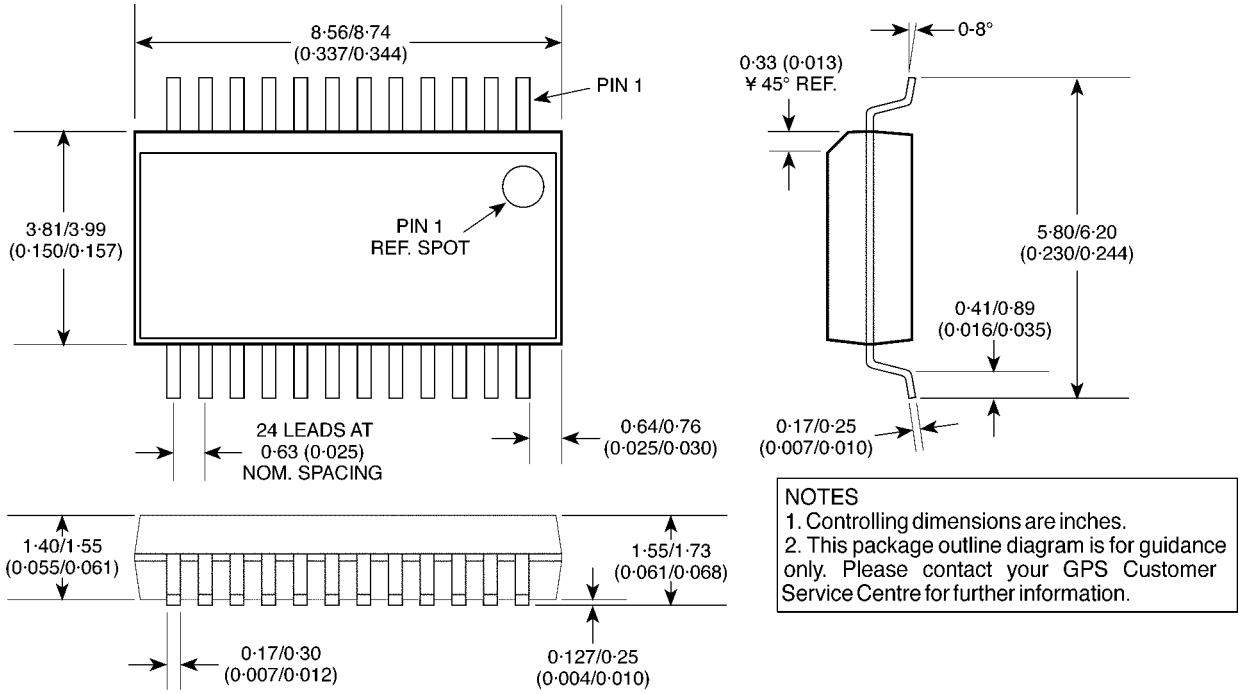


Fig. 7 Direct drive of crystal oscillator

PACKAGE DETAILS

Dimensions are shown thus: mm (in). For further package information please contact your local Customer Service Centre.



NOTES
1. Controlling dimensions are inches.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

24-LEAD SUBMINIATURE CERAMIC DIL - QPA24

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