

KA9258D(KA9258CD)

4-Channel Motor Driver

Features

- 4-CH Balanced Transformerless(BTL) Driver
- Output Gain Adjustable
- Built in OP-Amplifier
- Built in Mute Function
- Built in Thermal Shutdown Circuit (TSD)
- Operating Range 6 ~ 13.2V

Description

The KA9258D is a monolithic integrated circuit, suitable for 4-CH motor driver which drives tracking actuator, focus actuator, sled motor and spindle motor of compact disk player system.

28-SSOPH-375



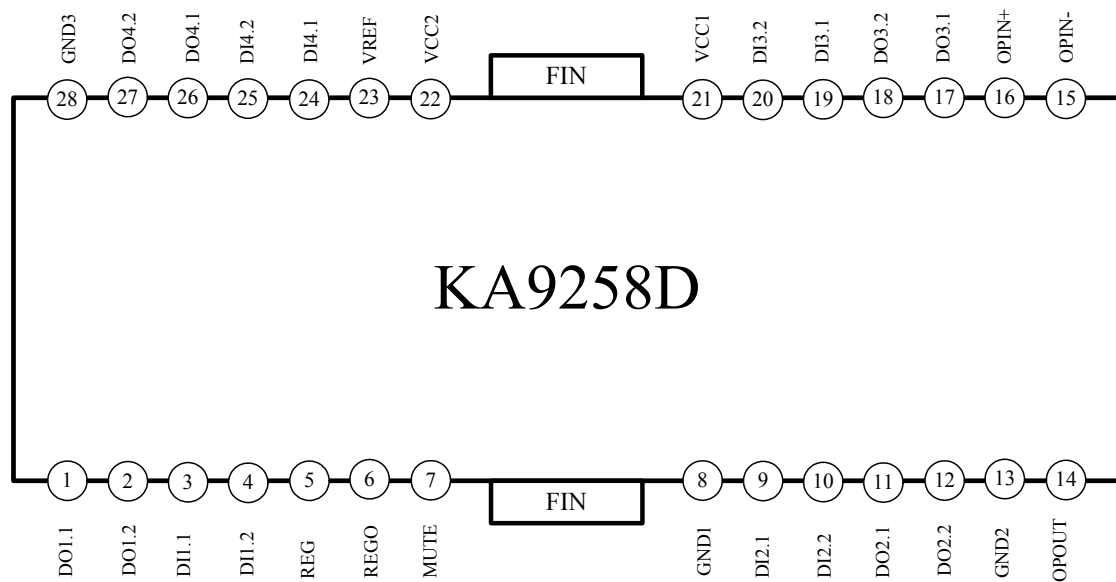
Typical Applications

- Compact Disk Player (CDP)
- Video Compact Disk Player (VCD)
- Automotive Compact Disk Player
- Other Compact Disk Media

Ordering Information

Device	Package	Operating Temp.
KA9258CD	28-SSOPH-375	-40°C ~ +85°C
KA9258CDTF	28-SSOPH-375	-40°C ~ +85°C

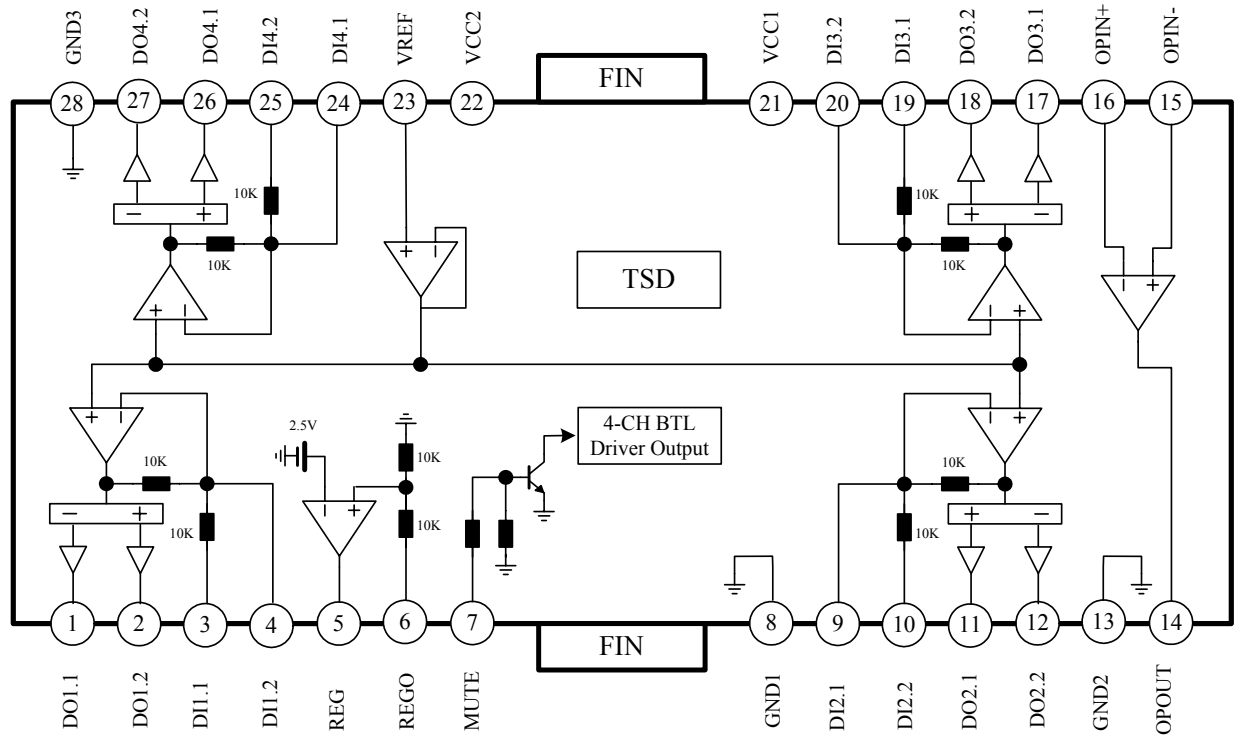
Pin Assignments



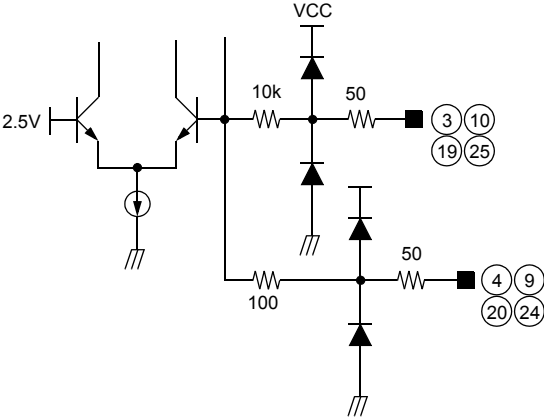
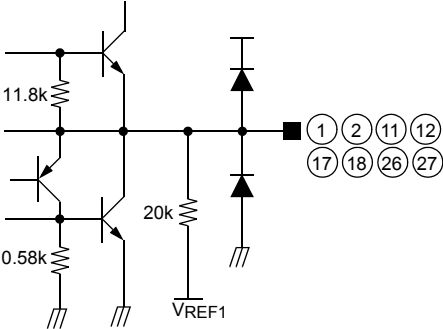
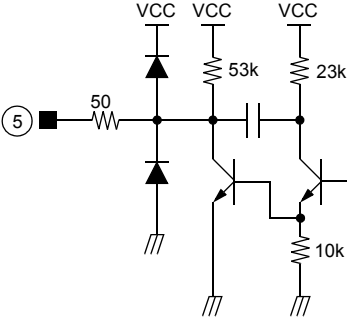
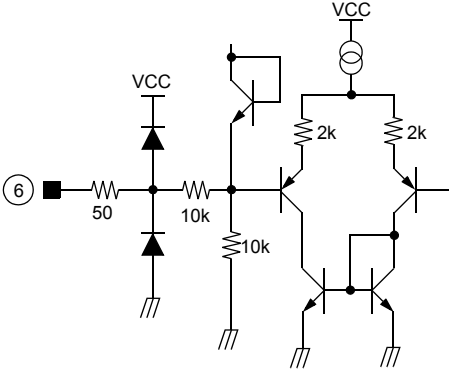
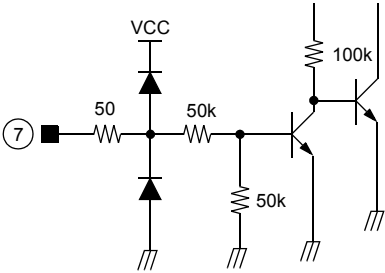
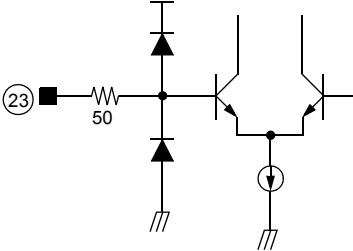
Pin Definitions

Pin Number	Pin Name	I/O	Pin Function Description
1	DO1.1	O	Channel 1 output 1
2	DO1.2	O	Channel 1 output 2
3	DI1.1	I	Channel 1 input 1
4	DI1.2	I	Channel 1 input 2
5	REG	O	External transistor base drive output
6	REO	O	Regulator output
7	MUTE	I	Mute signal input
8	GND1	-	Ground 1
9	DI2.1	I	Channel 2 output 1
10	DI2.2	I	Channel 2 output 2
11	DO2.1	O	Channel 2 input 1
12	DO2.2	O	Channel 2 input 2
13	GND2	-	Ground 2
14	OPOUT	O	OP-amplifier output
15	OPIN(-)	I	OP-amplifier negative input
16	OPIN(+)	I	OP-amplifier positive input
17	DO3.1	O	Channel 3 output 1
18	DO3.2	O	Channel 3 output 2
19	DI3.1	I	Channel 3 input 1
20	DI3.2	I	Channel 3 input 2
21	VCC1	-	Power supply voltage 1
22	VCC2	-	Power supply voltage 2
23	VREF	I	Bias Voltage
24	DI4.1	I	Channel 4 input 1
25	DI4.2	I	Channel 4 input 2
26	DO4.1	O	Channel 4 output 1
27	DO4.2	O	Channel 4 output 2
28	GND3	-	Ground 3

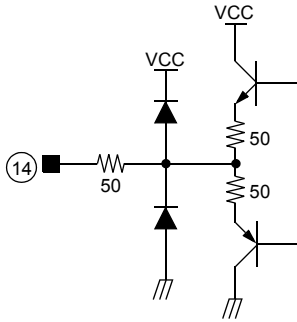
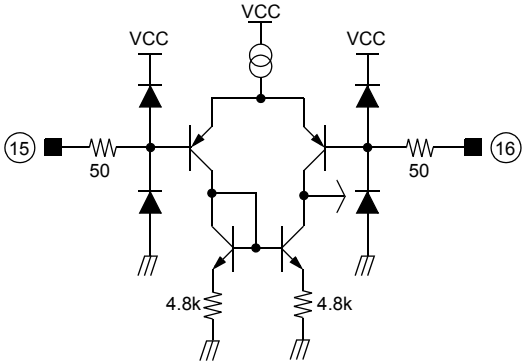
Internal Block Diagram



Equivalent Circuits

Driver Input	Driver Output
 The Driver Input circuit diagram shows a 2.5V source connected to a differential pair of transistors. The base of the left transistor is grounded. The base of the right transistor is connected to a 10k resistor, which is in turn connected to a VCC source through a 50 resistor. The emitter of the right transistor is connected to ground through a 100 resistor. The collector of the right transistor is connected to a 50 resistor, which is in turn connected to a VCC source through a 50 resistor. The output is taken from the collector of the right transistor, which is connected to pins 3, 10, 19, and 25. The output is also connected to pins 4, 9, 20, and 24 through a 50 resistor.	 The Driver Output circuit diagram shows a differential pair of transistors. The base of the left transistor is connected to a 11.8k resistor, which is in turn connected to a VCC source. The base of the right transistor is connected to a 0.58k resistor, which is in turn connected to ground. The emitter of the right transistor is connected to ground through a 20k resistor. The collector of the right transistor is connected to a VREF1 source. The output is taken from the collector of the right transistor, which is connected to pins 1, 2, 11, 12, 17, 18, 26, and 27.
Regulator	Regulator Output
 The Regulator circuit diagram shows a differential pair of transistors. The base of the left transistor is connected to a 50 resistor, which is in turn connected to a VCC source. The base of the right transistor is connected to a 53k resistor, which is in turn connected to a VCC source. The emitter of the right transistor is connected to ground through a 10k resistor. The collector of the right transistor is connected to a 23k resistor, which is in turn connected to a VCC source. The output is taken from the collector of the right transistor, which is connected to pin 5.	 The Regulator Output circuit diagram shows a differential pair of transistors. The base of the left transistor is connected to a 50 resistor, which is in turn connected to a VCC source. The base of the right transistor is connected to a 10k resistor, which is in turn connected to a VCC source. The emitter of the right transistor is connected to ground through a 10k resistor. The collector of the right transistor is connected to a 2k resistor, which is in turn connected to a VCC source. The output is taken from the collector of the right transistor, which is connected to pin 6.
Mute Input	Bias Input
 The Mute Input circuit diagram shows a differential pair of transistors. The base of the left transistor is connected to a 50 resistor, which is in turn connected to a VCC source. The base of the right transistor is connected to a 50k resistor, which is in turn connected to a VCC source. The emitter of the right transistor is connected to ground through a 50k resistor. The collector of the right transistor is connected to a 100k resistor, which is in turn connected to a VCC source. The output is taken from the collector of the right transistor, which is connected to pin 7.	 The Bias Input circuit diagram shows a differential pair of transistors. The base of the left transistor is connected to a 50 resistor, which is in turn connected to a VCC source. The base of the right transistor is connected to a VCC source. The emitter of the right transistor is connected to ground. The collector of the right transistor is connected to a VCC source. The output is taken from the collector of the right transistor, which is connected to pin 23.

Equivalent Circuits (Continued)

OP-AMP Output	OP-AMP Input
 The diagram shows the equivalent circuit for the OP-AMP output. It features a central node connected to a 50 ohm resistor, which is in turn connected to a square symbol labeled (14). This central node is also connected to two diodes: one pointing towards VCC and another pointing towards ground. Additionally, there are two 50 ohm resistors connected to this node, each leading to a transistor. The transistors are configured with their emitters to ground and their bases connected to the resistors. The collectors of these transistors are connected to VCC.	 The diagram shows the equivalent circuit for the OP-AMP input. It features a central node connected to a 50 ohm resistor, which is in turn connected to a square symbol labeled (15). This central node is also connected to two diodes: one pointing towards VCC and another pointing towards ground. Additionally, there are two 4.8k resistors connected to this node, each leading to a transistor. The transistors are configured with their emitters to ground and their bases connected to the resistors. The collectors of these transistors are connected to VCC. The entire circuit is symmetric, with a second identical branch on the right side connected to a square symbol labeled (16).

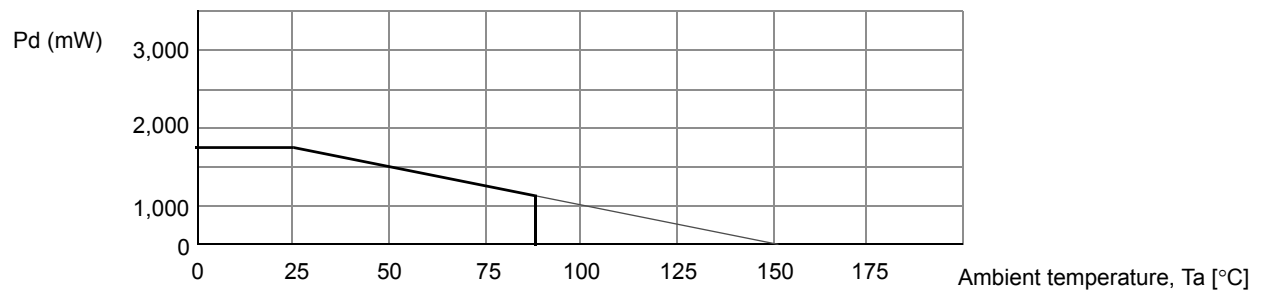
Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Value	Unit
Supply Voltage	VCC	15	V
Power Dissipation	PD	1.7 ^{note}	W
Operating Temperature	TOPR	-40 ~ +85	°C
Storage Temperature	TSTG	-55 ~ +150	°C
Maximum Output Current	IOMAX	1	A

Note:

1. When mounted on 76.2mm × 114mm × 1.57mm PCB (Phenolic resin material).
2. Power dissipation reduces 13.6mW/°C for using above Ta=25°C
3. Do not exceed Pd and SOA (Safe Operating Area).

Power Dissipation Curve



Recommended Operating Condition (Ta = 25°C)

Parameter	Symbol	Value	Unit
Operating Supply Voltage	VOPR	6 ~ 13.2	V

Electrical Characteristics (Ta = 25°C)

(Ta=25°C, VCC=8V, RL=8Ω, f=1kHz, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
REGULATOR PART						
Regulator Output Voltage	VREG	IL=100mA	4.75	5	5.25	V
Load Regulation	ΔVRL	IL=0 ~ 200mA	-40.0	0	10.0	mV
Line Regulation	ΔVCC	IL=200mA, VCC=6 ~ 9V	-10.0	0	20.0	mV
DRIVER PART (EXCEPT FOR LOADING MOTOR DRIVER)						
Quiescent Circuit Current	ICCQ	VI = 0	5.5	9.5	13.5	mA
Input Offset Voltage (Note1)	VOF	-	-5.0	0	5.0	mV
Output Offset Voltage	VOO	VCC= 13V	-50	0	50	
Maximum Sink Current	ISINK	RL= 4Ω, VCC	0.5	0.8	-	A
Maximum Source Current	ISOURCE	RL= 4Ω, GND	0.5	0.8	-	
Maximum Output Voltage	VOM	VI = 2VRMS, 1kHz	2.5	3.0	-	V
Closed Loop Voltage Gain	AvF	VI = 0.1VRMS, 1kHz	4.5	6.5	7.5	dB
Ripple Rejection Ratio (Note1)	RR	VI = -20dB, 120Hz	60.0	80.0	-	
Slew Rate (Note1)	SR	100Hz, Square wave	1.0	2.0	-	V/μs
LOADING MOTOR DRIVER PART (UNLESS OTHERWISE SPECIFIED, VCTL=OPENED)						
Input Offset Voltage	VOF1	-	-5	-	+5	mA
Input Bias Current	IB1	-	-	-	300	nA
High Level Output Voltage	VOH1	-	6	-	-	V
Low Level Output Voltage	VOL1	-	-	-	1.8	V
Output Sink Current	ISINK1	RL= 50Ω, GND	10	40	-	mA
Output Source Current	ISOURCE1	RL= 50Ω, VCC	10	50	-	mA
Open Loop Voltage Gain	GVO1	VIN = -75dB, f =1kHz	65	78	-	dB
Ripple Rejection Ratio (Note1)	RR1	VIN = -20dB, f =120kHz	50	70	-	dB
Slew Rate (Note1)	SR1	Square, VOUT = 2Vp-p, f = 120kHz	0.5	1	-	V/μs
Common Mode Rejection Ratio	CMRR1	VIN = -20dB, f =1kHz	70	84	-	dB

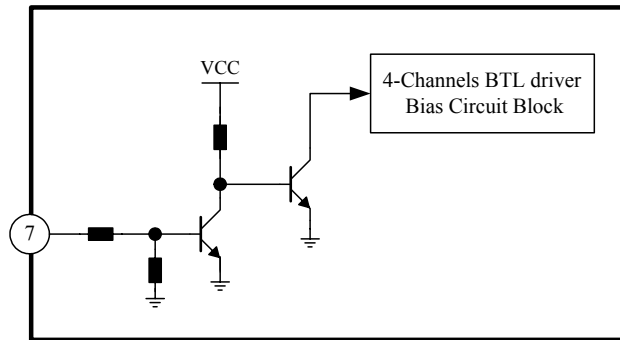
Note :

1. Guaranteed Design Value

Application Information

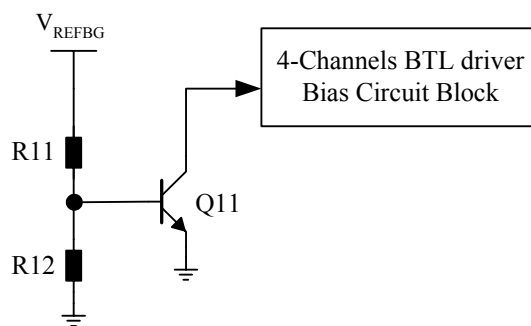
1. Mute Function

Pin 7	Mute circuit
High	Mute-off
Low	Mute-on
Open	Mute-on



- When the mute (pin 7) is high level, the bias circuit of BTL driver is activated. On the other hand, when the mute (pin7) is open or low level, the bias circuit of BTL driver is disabled. So that the 4-channels BTL driver output circuit will be muted.

2. TSD (Thermal Shutdown) Function



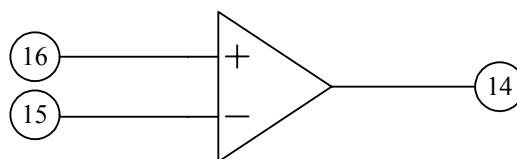
- The V_{REFBG} is the output voltage of the band-gap-referenced biasing circuit and acts as the input voltage of the TSD circuit.
- The base-emitter voltage of the transistor, Q11 is designed to turn-on at below voltage.

$$V_{BE} = \frac{V_{REFBG} \times R12}{R11 + R12} = 460[mV]$$

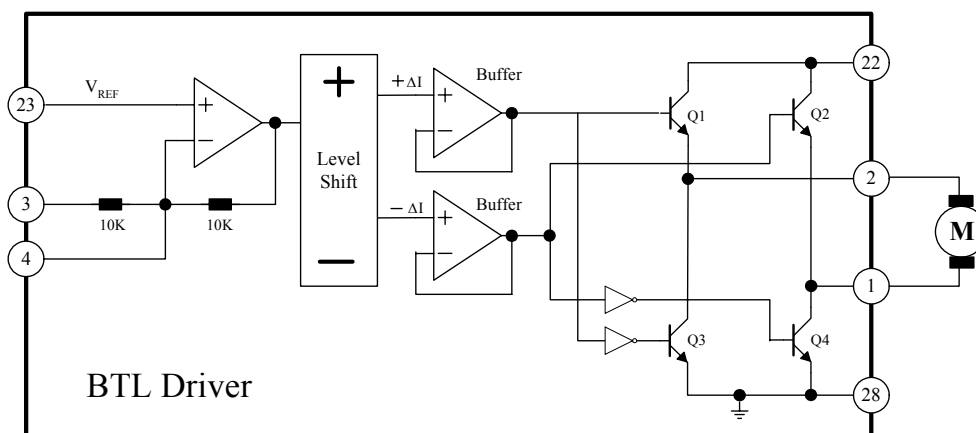
- When the chip temperature rises up to 175°C, then the turn-on voltage of the Q11 would drop down to 460mV. Hence, the Q11 would turn on so the output circuit will be muted. The TSD circuit has the hysteresis temperature of 25°C.

3. OP-AMP

- General OP-amplifier is integrated in the IC for user's convenience.

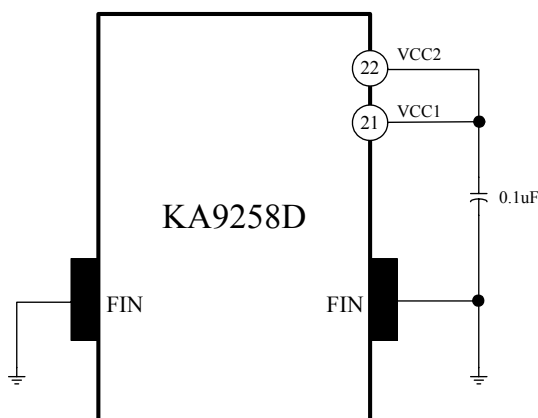


4. Balanced Transformerless(BTL) Driver



- The voltage, V_{REF} , is the reference voltage given by the bias voltage of the pin #23.
- The input signal through the pin #3 is amplified by 10K/10K times and then fed to the level shift.
- The level shift produces the current due to the difference between the input signal and the arbitrary reference signal. The current produced as $+\Delta I$ and $-\Delta I$ is fed into the driver buffer.
- Driver Buffer operates the power transistor of the output stage according to the state of the input signal.
- The output stage is the BTL driver and the motor is rotating in forward direction by operating transistor Q1 and Q4. On the other hand, if transistor Q2 and Q3 is operating, the motor is rotating in reverse direction
- When the input voltage through the pin #3 is below the V_{REF} , then the direction of the motor in forward direction.
- When the input voltage through the pin #3 is above the V_{REF} , then the direction of the motor in reverse direction.
- If it is desired to change the gain, then the pin #4 or #24 can be used.

5. Connect a by-pass capacitor, $0.1\mu F$ between the supply voltage source.



- Radiation FIN is connecting to the internal GND of the package. Connect the FIN to the external GND.

Typical Performance Characteristics

- Test contrions: $V_{REF}=2.5[V]$, Mute : OFF

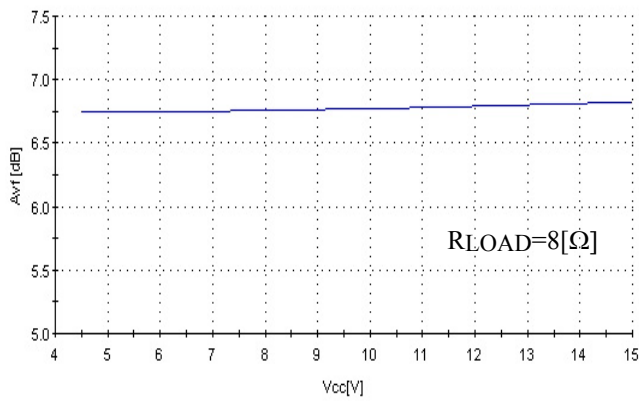


Figure 1. Vcc vs. AVF

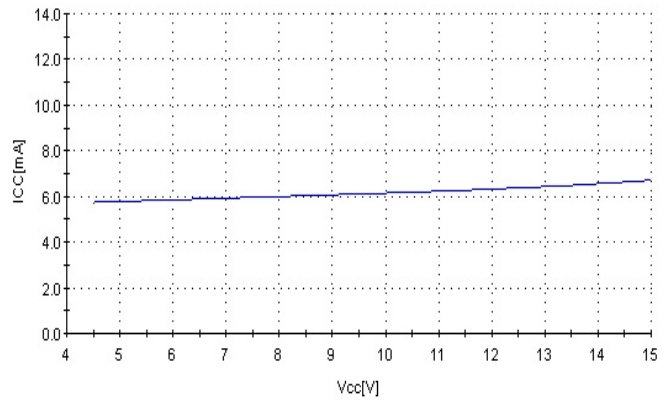


Figure 2. Vcc vs. Icc

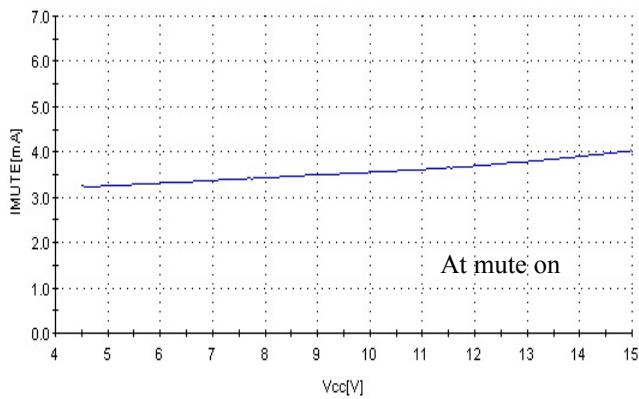


Figure 3. Vcc vs. IMUTE

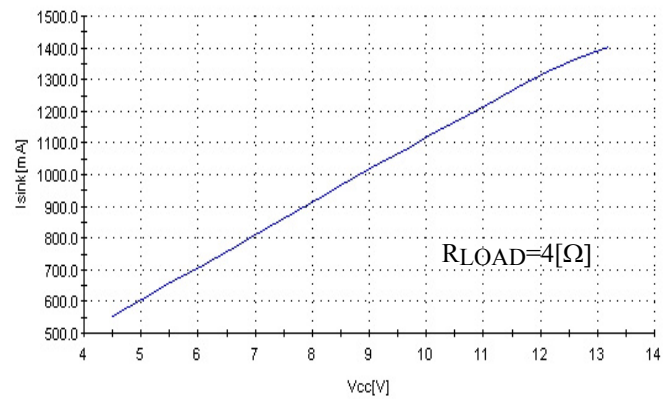


Figure 4. Vcc vs. ISINK

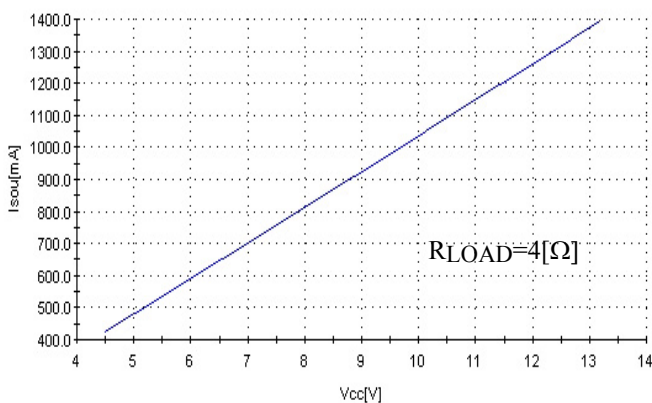


Figure 5. Vcc vs. ISOU

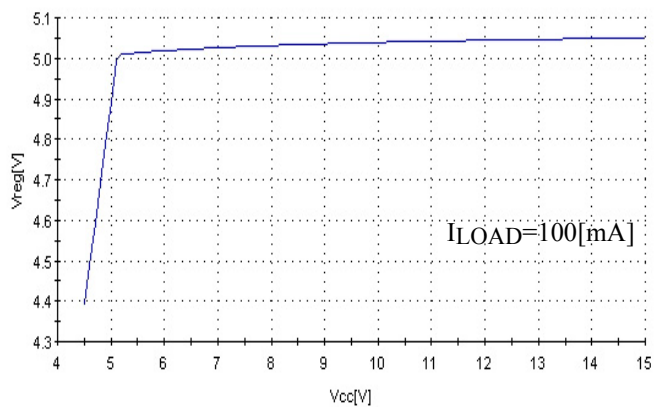
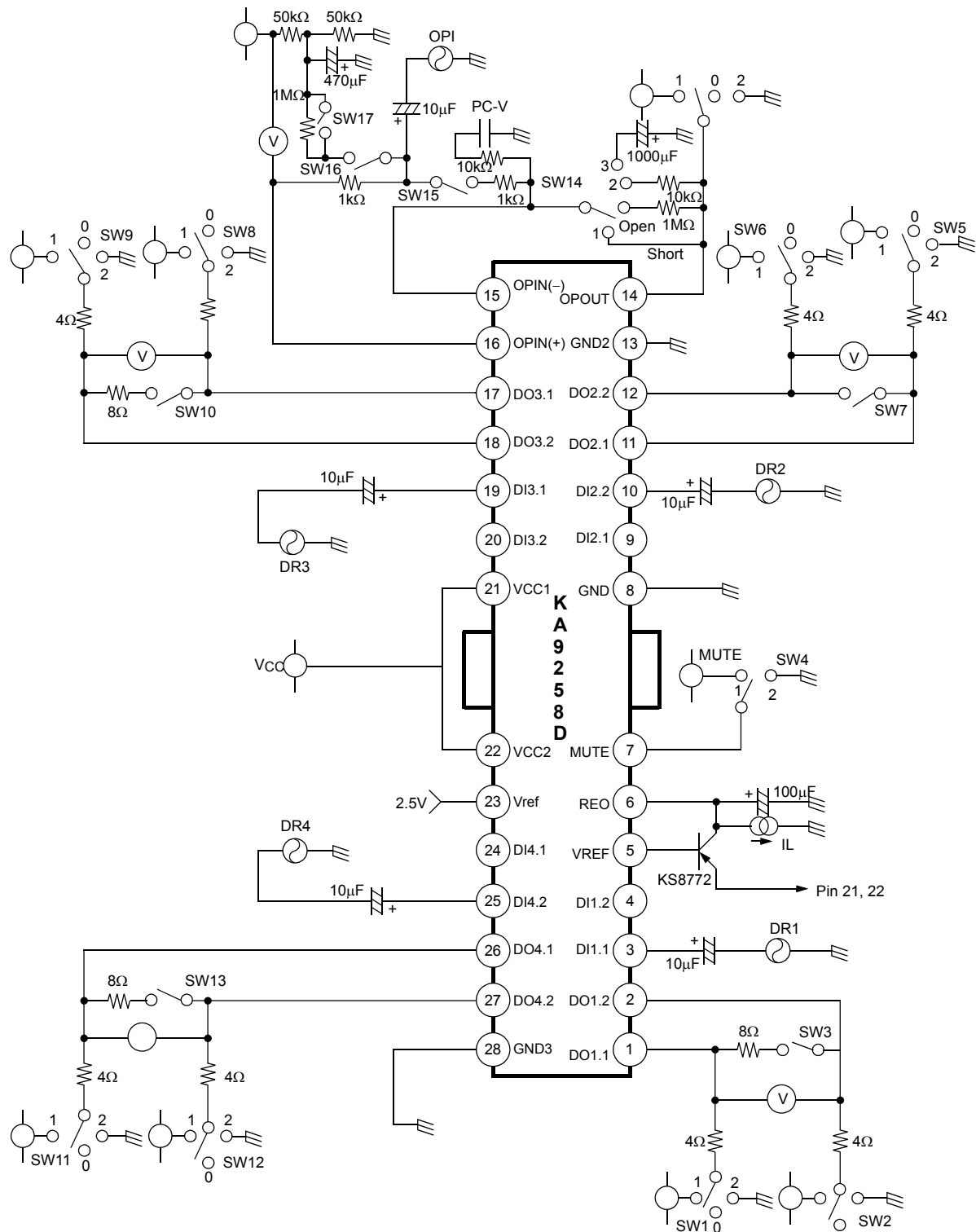
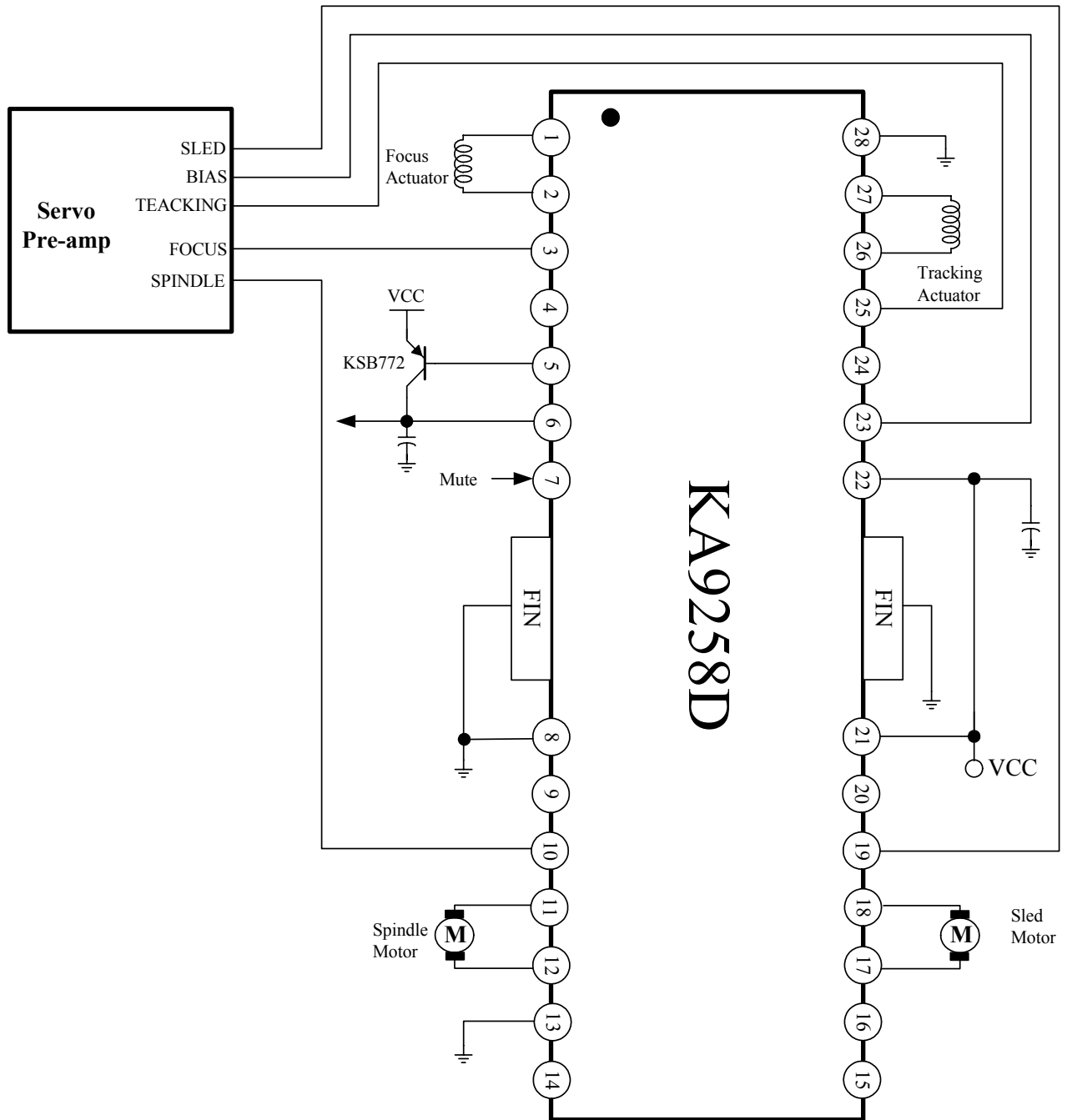


Figure 6. Vcc vs. VREG

Test Circuits



Application Circuits



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