ChipCorder®
TECHNOLOGY BY ISD

ISD33120/150/180/240 Products

Single-Chip Voice Record/Playback Devices
2-, 2.5-, 3-, and 4-Minute Durations

GENERAL DESCRIPTION

The ISD33120/150/180/240 ChipCorder® Products provide high-quality, 3-volt, single-chip Record/Playback solutions for 2- to 4-minute messaging applications which are ideal for cellular phones and other portable products. The CMOS devices include an on-chip oscillator, antialiasing filter, smoothing filter, AutoMute™ feature, audio amplifier, and high density, multilevel storage array. The ISD33000 series is designed to be used in a microprocessor- or microcontroller-based system. Address and control are accomplished through a Serial Peripheral Interface (SPI) or Microwire Serial Interface to minimize pin count.

Recordings are stored in on-chip nonvolatile memory cells, providing zero-power message storage. This unique, single-chip solution is made possible through ISD's patented multilevel storage technology. Voice and audio signals are stored directly into memory in their natural form, providing high-quality, solid-state voice reproduction.

FEATURES

- Single-chip voice Record/Playback solution
- Single +3 volt supply
- Low-power consumption
  - Operating current:
    I_{CC} Play = 25 mA (typical)
    I_{CC} Rec = 30 mA (typical)
  - Standby current: 1 μA (typical)
- Single-chip durations of 2 to 4 minutes
- High-quality, natural voice/audio reproduction
- AutoMute™ feature provides background noise attenuation during periods of silence
- No algorithm development required
- Microcontroller SPI or Microwire™ Serial Interface
- Fully addressable to handle multiple messages

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Table 2-76: ISD33120/150/180/240 Product Summary

Part Number	Duration	Input Sample Rate (KHz)	Typical Filter Pass Band (KHz)
ISD33120	2.0 Min.	8.0	3.4
ISD33150	2.5 Min.	6.4	2.7
ISD33180	3.0 Min.	5.3	2.3
ISD33240	4.0 Min.	4.0	1.7

- Nonvolatile message storage
- Power consumption controlled by SPI or Microwire control register
- 100-year message retention (typical)
- 100K record cycles (typical)
- On-chip clock source
- Available in die form, PDIP, SOIC, TSOP and chip scale packaging (CSP)
- Extended temperature (–20°C to +70°C) and industrial temperature (–40°C to +85°C) versions available

DETAILED DESCRIPTION

Speech/Sound Quality

The ISD33000 ChipCorder Series includes devices offered at 4.0, 5.3, 6.4, and 8.0 KHz sampling frequencies, allowing the user a choice of speech quality options. Increasing the duration within a product series decreases the sampling frequency and bandwidth, which affects sound quality. Please refer to the ISD33120/150/180/240 Product Summary table on the cover to compare filter pass band and product durations.

The speech samples are stored directly into on-chip nonvolatile memory without the digitization and compression associated with other solutions. Direct analog storage provides a true, natural sounding reproduction of voice, music, tones, and sound effects not available with most solid-state solutions.

Duration

To meet end system requirements, the ISD33120/150/180/240 Products are single-chip solutions at 2, 2.5, 3, and 4 minutes. One- to two-minute durations are addressed in the ISD33060/075/090/120-4 Products datasheet. More than one device can be controlled by one microcontroller for longer durations.

EEPROM Storage

One of the benefits of ISD's ChipCorder technology is the use of on-chip nonvolatile memory, providing zero-power message storage. The message is retained for up to 100 years typically without power. In addition, the device can be re-recorded typically over 100,000 times.

Figure 2-33: ISD33000 Series Block Diagram

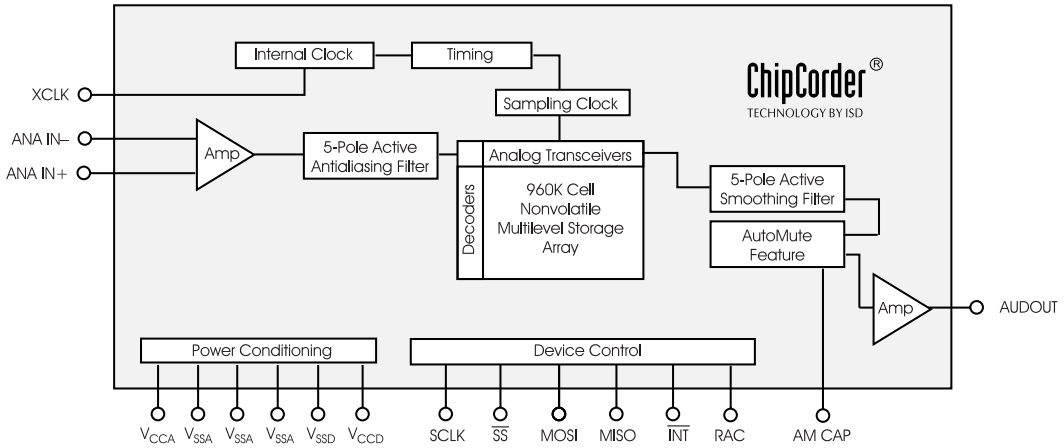
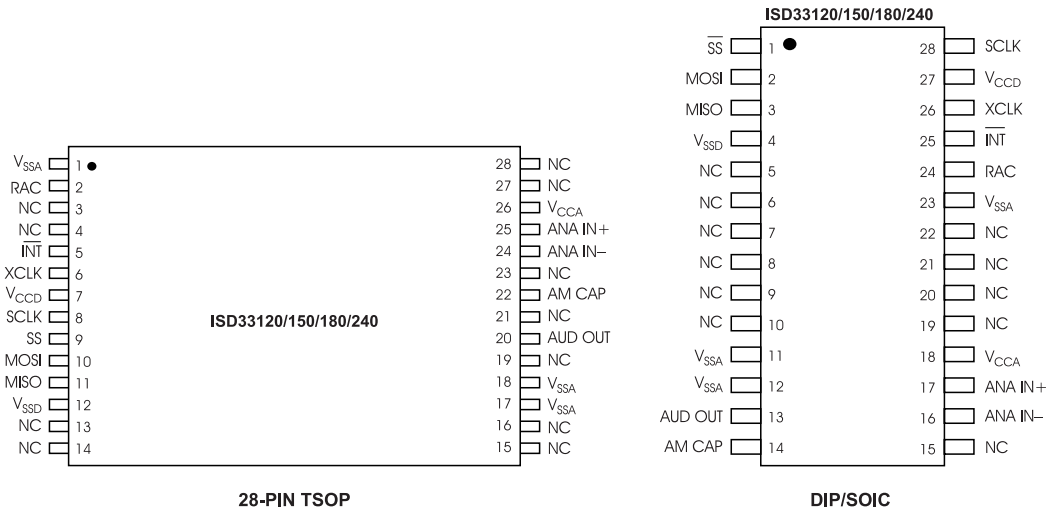


Figure 2-34: ISD33000 TSOP and DIP/SOIC Pinouts



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Microcontroller Interface

A four-wire (SCLK, MOSI, MISO, $\overline{SS}$) SPI interface is provided for ISD33000 control and addressing functions. The ISD33000 is configured to operate as a peripheral slave device, with a microcontroller-based SPI bus interface. Read/Write access to all the internal registers is provided through this SPI interface. An interrupt signal ($\overline{INT}$) and internal read-only Status Register are provided for handshake purposes.

Programming

The ISD33000 Series is also ideal for playback-only applications, where single or multiple message Playback is controlled through the SPI port. Once the desired message configuration is created, duplicates can easily be generated via an ISD programmer.

PIN DESCRIPTIONS

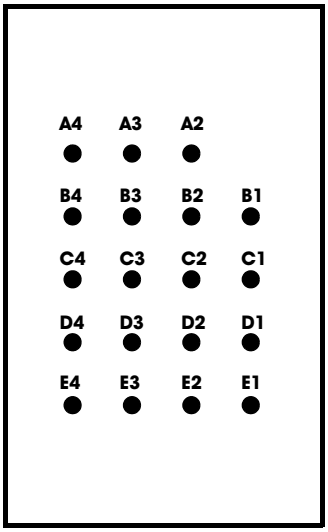
Voltage Inputs (V_{CCA}, V_{CCD})

To minimize noise, the analog and digital circuits in the ISD33000 devices use separate power busses. These +3V busses are brought out to separate pins and should be tied together as close to the supply as possible. In addition, these supplies should be decoupled as close to the package as possible.

Ground Inputs (V_{SSA}, V_{SSD})

The ISD33000 Series utilizes separate analog and digital ground busses. The analog ground (V_{SSA}) pins should be tied together as close to the package as possible and connected through a low-impedance path to power supply ground. The digital ground (V_{SSD}) pin should be connected through a separate low-impedance path to power supply ground. These ground paths should be large enough to ensure that the impedance between the V_{SSA} pins and the V_{SSD} pin is less than 3 ohms. The backside of the die is connected to V_{SS} through the substrate resistance. In a chip-on-board design the die attach area must be connected to V_{SS} or left floating.

Figure 2-35: ISD33000 CSP Pinout



Name	Ball Location	TSOP Pin #
V_{SSA}	A2	18
AMCAP	A3	22
ANAIN+	A4	25
V_{SSA}	B1	17
AUDOUT	B2	20
ANAIN–	B3	24
V_{CCA}	B4	26
V_{SSD}	C1	12
NC	C2	
NC	C3	
V_{SSA}	C4	1

Name	Ball Location	TSOP Pin #
MOSI	D1	10
SCLK	D2	8
XCLK	D3	6
RAC	D4	2
MISO	E1	11
SS	E2	9
V_{CCD}	E3	7
INT	E4	5

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Non-Inverting Analog Input (ANA IN+)

This pin is the non-inverting analog input that transfers the signal to the device for recording. The analog input amplifier can be driven single ended or differentially. In the single-ended input mode, a 32 mVp-p for optional sound quality (peak-to-peak) maximum signal should be capacitively connected to this pin for optimal signal quality. This capacitor value, together with the 3 KΩ input impedance of ANA IN+, is selected to give cutoff at the low frequency end of the voice passband. In the differential-input mode, the max. input signal at ANA IN+ should be 16 mVp-p for optional sound quality. The circuit connections for the two modes are shown in the ISD33000 Series ANA IN Modes figures above.

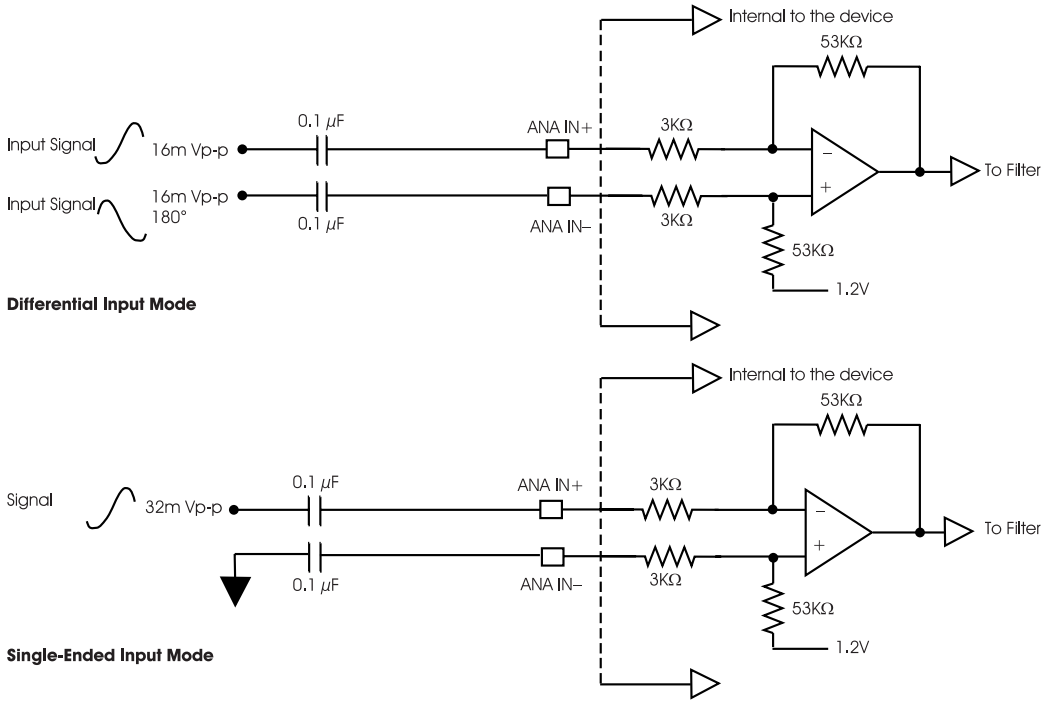
Inverting Analog Input (ANA IN–)

This pin is the inverting analog input that transfers the signal to the device for recording in the differential-input mode. In this differential-input mode, a 16 mVp-p max. input signal at ANA IN– should be capacitively coupled to this pin for optimal sound quality (as shown in the ISD33000 Series ANA IN Modes figure). This capacitor value should be equal to the coupling capacitor used on the ANA IN+ pin. The input impedance at ANA IN– is nominally 56 KΩ. In the single-ended mode, ANA IN– should be capacitively coupled to V_{SSA} through a capacitor equal to that used on the ANA IN+ input.

Audio Output (AUD OUT)

This pin provides the audio output to the user. It is capable of driving a 5 KΩ impedance.

Figure 2-36: ISD33000 Series ANA IN Modes



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NOTE *The AUD OUT pin is biased up to approximately 1.2 volts unless the ISD33000 is actively recording or the device is in the power down state. When the device is actively recording or powered down, the pin is in a high-impedance state. This means that there is a transition from high-impendance to 1.2 volts under the following conditions:*

- *When a SPI cycle is executed to initially set the PU bit and thus power up the device.*
- *When a SPI cycle is executed to clear the RUN bit during a RECORD operation, and thus stop recording.*
- *When the device goes into OVERFLOW during a RECORD operation both ending the recording and setting the OVF interrupt.*

  There is a transition from 1.2 volts to high-impendance under the following condition:

- *When a SPI cycle is executed to begin a RECORD operation and in power down mode.*

Slave Select ($\overline{SS}$)

This input, when LOW, will select the ISD33000 device.

Master Out Slave In (MOSI)

This is the serial input to the ISD33000 device. The master microcontroller places data on the MOSI line one half-cycle before the rising clock edge to be clocked in by the ISD33000 device.

Master In Slave Out (MISO)

This is the serial output of the ISD33000 device. This output goes into a high-impedance state if the device is not selected.

Serial Clock (SCLK)

This is the clock input to the ISD33000. It is generated by the master device (microcontroller) and is used to synchronize data transfers in and out of the device through the MISO and MOSI lines. Data is latched into the ISD33000 on the rising edge of SCLK and shifted out of the device on the falling edge of SCLK.

Interrupt ($\overline{INT}$)

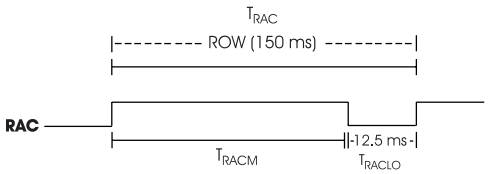
The ISD33000 interrupt pin goes LOW and stays LOW when an Overflow (OVF) or End of Message (EOM) marker is detected. This is an open drain output pin. Each operation that ends in an EOM or Overflow will generate an interrupt including the message cueing cycles. The interrupt will be cleared the next time an SPI cycle is initiated. The interrupt status can be read by an RINT instruction.

Overflow Flag (OVF)—The Overflow flag indicates that the end of the ISD33000's analog memory has been reached during a record or playback operation. There are six EOM flag position options per row.

End of Message (EOM)—The End-of-Message flag is set only during playback operation when an EOM is found.

Row Address Clock (RAC)

This is an open drain output pin that provides a signal with a 150 ms period at the 8 KHz sampling frequency. (This represents a single row of memory and there are 800 rows of memory in the ISD33120/150/180/240 devices. This signal stays HIGH for 137.5 ms and stays LOW for 12.5 ms when it reaches the end of a row.



The RAC pin stays HIGH for 172 μsec and stays LOW for 15.62 μsec in Message Cueing mode (see "Message Cueing" on page 171.). Refer to the AC Parameters table for RAC timing information on other sample rate products.

External Clock Input (XCLK)

The external clock input for the ISD33000 products has an internal pull-down device. These products are configured at the factory with an internal sampling clock frequency centered to $\pm$1% of specification. The frequency is then maintained to a variation of $\pm$2.25% over the entire commercial temperature and operating voltage ranges. The internal clock has a –6/+4% tolerance over the extended temperature, industrial temperature, and voltage ranges. A regulated power supply is recommended for industrial temperature range parts. If greater precision is required, the device can be clocked through the XCLK pin as follows:

Table 2-77: External Clock Input Precision Power Regulation

Part Number	Sample Rate	Required Clock
ISD33120	8.0 KHz	1024 KHz
ISD33150	6.4 KHz	819.2 KHz
ISD33180	5.3 KHz	682.7 KHz
ISD33240	4.0 KHz	512 KHz

These recommended clock rates should not be varied because the antialiasing and smoothing filters are fixed. Thus, aliasing problems can occur if the sample rate differs from the one recommended. The duty cycle on the input clock is not critical, as the clock is immediately divided by two internally. ***If the XCLK is not used, this input should be connected to ground.***

AutoMute™ Feature (AM CAP)

This pin is used in controlling the AutoMute feature. The AutoMute feature attenuates the signal when it drops below an internally set threshold. This helps to eliminate noise (with 6 dB of attenuation) when there is no signal (i.e., during periods of silence). A 1 μF capacitor to ground should be connected to the AMCAP pin. This capacitor becomes a part of an internal peak detect circuit which senses the signal level. This peak level is compared to an internally set threshold to determine the AutoMute trip point. For large signals the AutoMute attenuation is set to 0 dB while 6 dB of attenuation occurs for silence. The 1 μF capacitor also affects the rate at which the AutoMute feature changes with the signal amplitude. The Automute feature can be disabled by connecting the AMCAP pin to V_{CCA}.

SERIAL PERIPHERAL INTERFACE (SPI) DESCRIPTION

The ISD33000 series operates from an SPI serial interface. The SPI interface operates with the following protocol.

The data transfer protocol assumes that the microcontroller's SPI shift registers are clocked on the falling edge of the SCLK. With the ISD33000, data is clocked in on the MOSI pin on the rising clock edge. Data is clocked out on the MISO pin on the falling clock edge.

1. All serial data transfers begin with the falling edge of $\overline{SS}$ pin.
2. $\overline{SS}$ is held LOW during all serial communications and held HIGH between instructions.
3. Data is clocked in on the rising clock edge and data is clocked out on the falling clock edge.
4. Play and Record operations are initiated by enabling the device by asserting the $\overline{SS}$ pin LOW, shifting in an opcode and an address field to the ISD33000 device (refer to the Opcode Summary table on the next page).
5. The opcodes and address fields are as follows: <5 control bits> and <11 address bits>. It should be noted that the ISD33120/150/180/240 devices only need 10 bits of address but the 11th bit is reserved for longer duration products. For clarity, the control bits and the address bits will be displayed in binary and "X" means Don't Care.
6. Each operation that ends in an EOM or Overflow will generate an interrupt, including the Message Cueing cycles. The Interrupt will be cleared the next time an SPI cycle is initiated.
7. As Interrupt data is shifted out of the ISD33000 MISO pin, control and address data is simultaneously being shifted into the MOSI pin. Care should be taken such that the data shifted in is compatible with current system operation. It is possible to read interrupt data and start a new operation within the same SPI cycle.
8. An operation begins with the RUN bit set and ends with the RUN bit reset.
9. All operations begin with the rising edge of $\overline{SS}$.

Message Cueing

Message cueing allows the user to skip through messages, without knowing the actual physical location of the message. This operation is used during playback. In this mode, the messages are skipped 800 times faster than in normal playback mode. It will stop when an EOM (end of message) marker is reached. Then, the internal address counter will point to the next message.

Table 2-78: Opcode Summary

Instruction	Opcode <5 bits> Address <10 bits>	Operational Summary
POWERUP	00100 <XXXXXXXXXX>	Power Up: Device will be ready for an operation after T_{PUD}.
SETPLAY	11100 <X A9–A0>	Initiates Playback from address <A9–A0>. Must be followed by a PLAY command to continue playback.
PLAY	11110 <XXXXXXXXXX>	Play back from the current address (until EOM or OVF).
SETREC	10100 <X A9–A0>	Initiates a Record operation from address <A9–A0>. Must be followed by a REC command to continue recording.
REC	10110 <XXXXXXXXXX>	Records from current address until OVF is reached.
SETMC	11101 <X A9–A0>	Initiates Message Cueing (MC) from address <A9–A0>. Must be followed by a MC command to continue Message Cueing.
MC(1)	11111 <XXXXXXXXXX>	Performs a Message Cue. Proceeds to the end of the current message (EOM) or enters OVF condition if no more messages are present.
STOP	0X110 <XXXXXXXXXX>	Stops current operation.
STOPPWRDN	0X01X <XXXXXXXXXX>	Stops current Operation and enters stand-by (power down) mode.
RINT(2)	0X110 <XXXXXXXXXX>	Read Interrupt status bits: Overflow and EOM.

1. *Message Cueing can be selected only at the beginning of a play operation.*
2. *As the Interrupt data is shifted out of the ISD33000, control and address data is being shifted in. Care should be taken such that the data shifted in is compatible with current system operation. It is possible to read interrupt data and start a new operation at the same time.*

See pages 1-17 and 1-18 for Opcode format.

Power Up Sequence

The ISD33000 will be ready for an operation after T_{PUD} (25 ms approx. for 8 KHz sample rate). The user needs to wait T_{PUD} before issuing an operational command. For example, to play from address 00 the following programing cycle should be used.

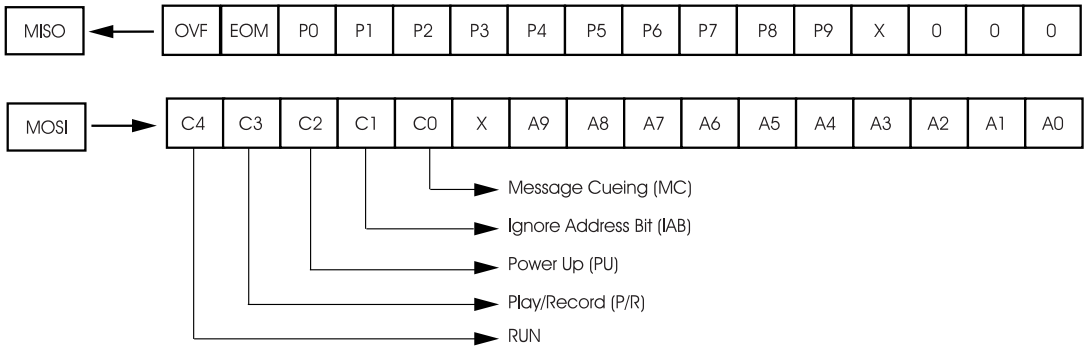
1. Send POWERUP command.
2. Wait T_{PUD} (power up delay).
3. Send SETPLAY command with address 00.
4. Send PLAY command.

The device will start Playback at address 00 and it will generate an interrupt when an EOM (End of Message) is reached. It will then stop Playback.

SPI Port

The following diagram describes the SPI port and the control bits associated with it.

Figure 2-37: SPI Port



SPI Control Register

The SPI control register provides control of individual device functions such as Play, Record, Message Cueing, Power-Up and Power-Down, Start and Stop operations, and Ignore Address pointers.

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Table 2-79: SPI Control Register

Control Register	Bit	Device Function	Control Register	Bit	Device Function
RUN		Enable or Disable an operation	PU		Master power control
=	1	Start	=	1	Power-Up
=	0	Stop	=	0	Power-Down
P/$\overline{R}$		Selects Play or Record operation	IAB[1]		Ignore address control bit
=	1	Play	=	1	Ignore input address register (A9–A0)
=	0	Record	=	0	Use the input address register contents for an operation (A9–A0)
MC		Enable or Disable Message Cueing	P9–P0		Output of the row pointer register
=	1	Enable Message Cueing	A9–A0		Input address register
=	0	Disable Message Cueing			

1. *When IAB (Ignore Address Bit) is set to 0, a Playback or Record operation starts from address (A9–A0). For consecutive Playback or Record, IAB should be changed to a 1 before the end of that row (see RAC timing). Otherwise the ISD33000 will repeat the operation from the same row address. For memory management, the Row Address Clock (RAC) pin and IAB can be used to move around the memory segments.*

Figure 2-38: SPI Interface Simplified Block Diagram

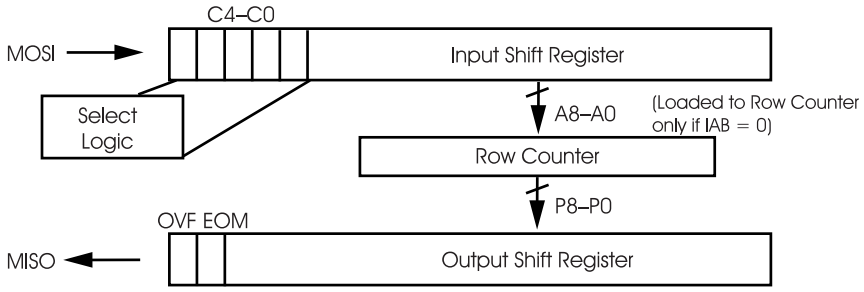

Table 2-80: Absolute Maximum Ratings (Packaged Parts)[1]

Condition	Value
Junction temperature	150°C
Storage temperature range	–65°C to +150°C
Voltage applied to any pin	(V_{SS} – 0.3 V) to (V_{CC} + 0.3 V)
Voltage applied to any pin (Input current limited to ±20 mA)	(V_{SS} – 1.0 V) to (V_{CC} + 1.0 V)
Voltage applied to MOSI, SLK, and $\overline{SS}$ pins (Input current limited to ±20 mA)	(V_{SS} – 1.0 V) to (V_{CC} + 2.5 V)
Lead temperature (soldering – 10 seconds)	300°C
$V_{CC} – V_{SS}$	–0.3 V to + 7.0 V

1. *Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability. Functional operation is not implied at these conditions.*

Table 2-81: Operating Conditions (Packaged Parts)

Condition	Value
Commercial operating temperature range[1]	0°C to +70°C
Extended operating temperature[1]	–20°C to +70°C
Industrial operating temperature[1]	–40°C to +85°C
Supply voltage (V_{CC})[2]	+2.7 V to + 3.3 V
Ground voltage (V_{SS})[3]	0 V

1. *Case temperature.*
2. $V_{CC} = V_{CCA} = V_{CCD}$.
3. $V_{SS} = V_{SSA} = V_{SSD}$.

Table 2-82: DC Parameters (Packaged Parts)

Symbol	Parameters	Min[2]	Typ[1]	Max[2]	Units	Conditions
V_{IL}	Input Low Voltage			V_{CC} x 0.2	V	
V_{IH}	Input High Voltage	V_{CC} x 0.8			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 10 µA
V_{OL1}	RAC, $\overline{INT}$ Output Low Voltage			0.4	V	I_{OL} = 1 mA
V_{OH}	Output High Voltage	V_{CC} – 0.4			V	I_{OH} = –10 µA
I_{CC}	V_{CC} Current (Operating) Playback Record		 25 30	 30 40	 mA mA	 $R_{EXT} = \infty$[3] $R_{EXT} = \infty$[3]
I_{SB}	V_{CC} Current (Standby)		1	10	µA	3, 4
I_{IL}	Input Leakage Current			±1	µA	
I_{HZ}	MISO Tristate Current		1	10	µA	
R_{EXT}	Output Load Impedance	5			KΩ	
$R_{ANA\ IN+}$	ANA IN+ Input Resistance	2.2	3.0	3.8	KΩ	
$R_{ANA\ IN-}$	ANA IN– Input Resistance	40	55.8	71	KΩ	
A_{ARP}	ANA IN+ or ANA IN– to AUD OUT Gain		25		dB	5

1. *Typical values @ T_A = 25°C and 3.0 V.*

2. *All min/max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100% tested.*

3. *V_{CCA} and V_{CCD} connected together.*

4. *$\overline{SS}$ = V_{CCA} = V_{CCD}, XCLK = MOSI = V_{SSA}= V_{SSD} and all other pins floating.*

5. *Measured with AutoMute feature disabled.*

Table 2-83: AC Parameters (Packaged Parts)

Symbol	Characteristic		Min[2]	Typ[1]	Max[2]	Units	Conditions
F_S	Sampling Frequency	ISD33120		8.0		KHz	[5]
		ISD33120D		8.0		KHz	[5]
		ISD33120I		8.0		KHz	[5]
		ISD33150		6.4		KHz	[5]
		ISD33150D		6.4		KHz	[5]
		ISD33150I		6.4		KHz	[5]
		ISD33180		5.3		KHz	[5]
		ISD33180D		5.3		KHz	[5]
		ISD33180I		5.3		KHz	[5]
		ISD33240		4.0		KHz	[5]
		ISD33240D		4.0		KHz	[5]
		ISD33240I		4.0		KHz	[5]
F_{CF}	Filter Pass Band	ISD33120		3.4		KHz	3-dB Roll-Off Point [3,7]
		ISD33120D		3.4		KHz	3-dB Roll-Off Point [3,7]
		ISD33120I		3.4		KHz	3-dB Roll-Off Point [3,7]
		ISD33150		2.7		KHz	3-dB Roll-Off Point [3,7]
		ISD33150D		2.7		KHz	3-dB Roll-Off Point [3,7]
		ISD33150I		2.7		KHz	3-dB Roll-Off Point [3,7]
		ISD33180		2.3		KHz	3-dB Roll-Off Point [3,7]
		ISD33180D		2.3		KHz	3-dB Roll-Off Point [3,7]
		ISD33180I		2.3		KHz	3-dB Roll-Off Point [3,7]
		ISD33240		1.7		KHz	3-dB Roll-Off Point [3,7]
		ISD33240D		1.7		KHz	3-dB Roll-Off Point [3,7]
		ISD33240I		1.7		KHz	3-dB Roll-Off Point [3,7]
T_{REC}	Record Duration	ISD33120	115.1		124.4	sec	Commercial [6]
		ISD33120D	112.7		125.7	sec	Extended[6]
		ISD33120I	112.7		125.7	sec	Industrial[6]
		ISD33150	143.8		155.5	sec	Commercial [6]
		ISD33150D	140.8		157.1	sec	Extended[6]
		ISD33150I	140.8		157.1	sec	Industrial[6]
		ISD33180	172.6		186.6	sec	Commercial [6]
		ISD33180D	169.0		188.5	sec	Extended[6]
		ISD33180I	169.0		188.5	sec	Industrial[6]
		ISD33240	229.3		249.9	sec	Commercial [6]
		ISD33240D	224.5		259.4	sec	Extended[6]
		ISD33240I	224.5		259.4	sec	Industrial[6]
T_{PLAY}	Playback Duration	ISD33120	115.1		124.4	sec	Commercial [6]
		ISD33120D	112.7		125.7	sec	Extended[6]
		ISD33120I	112.7		125.7	sec	Industrial[6]
		ISD33150	143.8		155.5	sec	Commercial [6]
		ISD33150D	140.8		157.1	sec	Extended[6]
		ISD33150I	140.8		157.1	sec	Industrial[6]
		ISD33180	172.6		186.6	sec	Commercial [6]
		ISD33180D	169.0		188.5	sec	Extended[6]
		ISD33180I	169.0		188.5	sec	Industrial[6]
		ISD33240	229.3		249.9	sec	Commercial [6]
		ISD33240D	224.5		259.4	sec	Extended[6]
		ISD33240I	224.5		259.4	sec	Industrial[6]

Table 2-83: AC Parameters (Packaged Parts)

Symbol	Characteristic		Min[2]	Typ[1]	Max[2]	Units	Conditions
T_{PUD}	Power-Up Delay	ISD33120	23.9		26.0	msec	Commercial
		ISD33120D	23.4		26.2	msec	Extended
		ISD33120I	23.4		26.2	msec	Industrial
		ISD33150	29.9		32.4	msec	Commercial
		ISD33150D	29.3		32.8	msec	Extended
		ISD33150I	29.3		32.8	msec	Industrial
		ISD33180	35.9		38.9	msec	Commercial
		ISD33180D	35.2		39.3	msec	Extended
		ISD33180I	35.2		39.3	msec	Industrial
		ISD33240	47.7		52.1	msec	Commercial
		ISD33240D	46.7		54.1	msec	Extended
		ISD33240I	46.7		54.1	msec	Industrial
T_{STOP} or T_{PAUSE}	Stop or Pause in Record or Play	ISD33120		25.0		msec	
		ISD33150		31.25		msec	
		ISD33180		37.5		msec	
		ISD33240		50.0		msec	
T_{RAC}	RAC Clock Period	ISD33120	143.8		155.5	msec	
		ISD33120D	140.8		152.5	msec	
		ISD33120I	140.8		152.5	msec	
		ISD33150	179.7		194.4	msec	
		ISD33150D	176.0		190.6	msec	
		ISD33150I	176.0		190.6	msec	
		ISD33180	215.6		233.2	msec	
		ISD33180D	211.1		228.7	msec	
		ISD33180I	211.1		228.7	msec	
		ISD33240	286.6		312.3	msec	
		ISD33240D	280.6		306.3	msec	
		ISD33240I	280.6		306.3	msec	
T_{RACLO}	RAC Clock Low Time	ISD33120	11.9		13.0	msec	Commercial
		ISD33120D	11.7		12.8	msec	Extended
		ISD33120I	11.7		12.8	msec	Industrial
		ISD33150	14.9		16.2	msec	Commercial
		ISD33150D	14.6		15.9	msec	Extended
		ISD33150I	14.6		15.9	msec	Industrial
		ISD33180	17.9		19.5	msec	Commercial
		ISD33180D	17.6		19.1	msec	Extended
		ISD33180I	17.6		19.1	msec	Industrial
		ISD33240	23.8		26.1	msec	Commercial
		ISD33240D	23.3		25.6	msec	Extended
		ISD33240I	23.3		25.6	msec	Industrial
T_{RACM}	RAC Clock Period in Message Cueing Mode	ISD33120		187.5		msec	
		ISD33150		234.4		msec	
		ISD33180		281.3		msec	
		ISD33240		375.0		msec	
T_{RACML}	RAC Clock Low Time in Message Cueing Mode	ISD33120		15.6		µsec	
		ISD33150		19.5		µsec	
		ISD33180		23.4		µsec	
		ISD33240		31.3		µsec	

Table 2-83: AC Parameters (Packaged Parts)

Symbol	Characteristic	Min[2]	Typ[1]	Max[2]	Units	Conditions
THD	Total Harmonic Distortion		1	2	%	@ 1 KHz
V_{IN}	ANA IN Input Voltage			32	mV	Peak-to-Peak[4,8,9]

1. *Typical values @ T_A = 25°C and 3.0 V.*
2. *All min/max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100% tested.*
3. *Low-frequency cut off depends upon the value of external capacitors (see Pin Descriptions).*
4. *Single-ended input mode. In the differential input mode, V_{IN} max. for ANA IN+ and ANA IN– is 16 mV peak-to-peak.*
5. *Sampling Frequency can vary as much as ±2.25% over the commercial temperature and voltage ranges, and –6/+4% over the extended temperature, industrial temperature and voltage ranges. For greater stability, an external clock can be utilized (see Pin Descriptions).*
6. *Playback and Record Duration can vary as much as ±2.25% over the commercial temperature and voltage ranges and voltage ranges and –4/+6% over the extended temperature, industrial temperature and voltage ranges. For greater stability, an external clock can be utilized (see Pin Descriptions).*
7. *Filter specification applies to the antialiasing filter and to the smoothing filter.*
8. *The typical output voltage will be approximately 570 mV peak-to-peak with V_{IN} at 32 mV peak-to-peak.*
9. *For optimal signal quality, this maximum limit is recommended.*

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Table 2-84: Absolute Maximum Ratings (Die)[1]

Condition	Value
Junction temperature	150°C
Storage temperature range	–65°C to +150°C
Voltage applied to any pad	(V_{SS} – 0.3 V) to (V_{CC} + 0. V)
Voltage applied to any pad (Input current limited to ±20 mA)	(V_{SS} – 1.0V) to (V_{CC} + 1.0V)
Voltage applied to MOSI, SLK, and $\overline{SS}$ pins (Input current limited to ±20 mA)	(V_{SS} – 1.0 V) to (V_{CC} + 2.5 V)
$V_{CC} – V_{SS}$	–0.3 V to +7.0 V

1. *Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability. Functional operation is not implied at these conditions.*

Table 2-85: Operating Conditions (Die)

Condition	Value
Commercial operating temperature range	0°C to +50°C
Supply voltage (V_{CC})[1]	+2.7 V to +3.3 V
Ground voltage (V_{SS})[2]	0 V

1. *$V_{CC} = V_{CCA} = V_{CCD}$*
2. *$V_{SS} = V_{SSA} = V_{SSD}$.*

Table 2-86: DC Parameters (Die)

Symbol	Parameters	Min[2]	Typ[1]	Max[2]	Units	Conditions
V_{IL}	Input Low Voltage			V_{CC} x 0.2	V	
V_{IH}	Input High Voltage	V_{CC} x 0.8			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 10 µA
V_{OL1}	RAC, $\overline{INT}$ Output Low Voltage			0.4	V	I_{OL} = 1 mA
V_{OH}	Output High Voltage	V_{CC} – 0.4			V	I_{OH} = –10 µA
I_{CC}	V_{CC} Current Operating) — Playback — Record		 25 30	 30 40	 mA mA	 $R_{EXT} = \infty$[3] $R_{EXT} = \infty$[3]
I_{SB}	V_{CC} Current (Standby)		1	10	µA	[3,4]
I_{IL}	Input Leakage Current			±1	µA	
I_{HZ}	MISO Tristate Current		1	10	µA	
R_{EXT}	Output Load Impedance	5			KΩ	
$R_{ANA\ IN+}$	ANA IN+ Input Resistance	2.2	3.0	3.8	KΩ	
$R_{ANA\ IN-}$	ANA IN– Input Resistance	40	56	71	KΩ	
A_{ARP}	ANA IN+ or ANA IN– to AUD OUT Gain		25		dB	[5]

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1. *Typical values @ T_A = 25°C and 3.0 V.*

2. *All min/max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100% tested.*

3. *V_{CCA} and V_{CCD} connected together.*

4. *$\overline{SS}$ = V_{CCA}= V_{CCD}, XCLK = MOSI = V_{SSA} = V_{SSD} and all other pins floating.*

5. *Measured with AutoMute feature disabled.*

Table 2-87: AC Parameters (Die)

Symbol	Characteristic		Min[2]	Typ[1]	Max[2]	Units	Conditions
F_S	Sampling Frequency	ISD33120		8.0		KHz	[5]
		ISD33150		6.4		KHz	[5]
		ISD33180		5.3		KHz	[5]
		ISD33240		4.0		KHz	[5]
F_{CF}	Filter Pass Band	ISD33120		3.4		KHz	3dB Roll-Off Point [3,6]
		ISD33150		2.7		KHz	3dB Roll-Off Point [3,6]
		ISD33180		2.3		KHz	3dB Roll-Off Point [3,6]
		ISD33240		1.7		KHz	3dB Roll-Off Point [3,6]
T_{REC}	Record Duration	ISD33120	115.1		124.4	sec	[5]
		ISD33150	143.8		155.5	sec	[5]
		ISD33180	172.6		186.6	sec	[5]
		ISD33240	229.3		249.9	sec	[5]

Table 2-87: AC Parameters (Die)

Symbol	Characteristic		Min[2]	Typ[1]	Max[2]	Units	Conditions
T_{PLAY}	Playback Duration	ISD33120	115.1		124.4	sec	5
		ISD33150	143.8		155.5	sec	5
		ISD33180	172.6		186.6	sec	5
		ISD33240	229.3		249.9	sec	5
T_{PUD}	Power-Up Delay	ISD33120	23.9		26.0	msec	
		ISD33150	29.9		32.4	msec	
		ISD33180	35.9		38.9	msec	
		ISD33240	47.7		52.1	msec	
T_{STOP} or T_{PAUSE}	Stop or Pause in Record or Play	ISD33120		25.0		msec	
		ISD33150		31.25		msec	
		ISD33180		37.5		msec	
		ISD33240		50.0		msec	
T_{RAC}	RAC Clock Period	ISD33120	143.8		155.5	msec	
		ISD33150	179.7		194.4	msec	
		ISD33180	215.6		233.2	msec	
		ISD33240	286.6		312.3	msec	
T_{RACLO}	RAC Clock Low Time	ISD33120		12.50		msec	
		ISD33150		15.63		msec	
		ISD33180		18.75		msec	
		ISD33240		25.0		msec	
T_{RACM}	RAC Clock Period in Message Cueing Mode	ISD33120		187.5		µsec	
		ISD33150		234.4		µsec	
		ISD33180		281.3		µsec	
		ISD33240		375.0		µsec	
T_{RACML}	RAC Clock Low Time in Message Cueing Mode	ISD33120		15.6		µsec	
		ISD33150		19.5		µsec	
		ISD33180		23.4		µsec	
		ISD33240		31.3		µsec	
THD	Total Harmonic Distortion			1	2	%	@ 1 KHz
V_{IN}	ANA IN Input Voltage				32	mV	Peak-to-Peak[4,7,8]

1. *Typical values @ T_A = 25°C and 3.0 V.*

2. *All min/max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100% tested.*

3. *Low-frequency cut off depends upon the value of external capacitors (see Pin Descriptions).*

4. *Single-ended input mode. In the differential input mode, V_{IN} max. for ANA IN+ and ANA IN– is 16 mV peak-to-peak.*

5. *Sampling Frequency and Duration can vary as much as ±2.25% over the commercial temperature and voltage ranges. For greater stability, an external clock can be utilized. See "PIN DESCRIPTIONS" on page 167.*

6. *Filter specification applies to the antialiasing filter and to the smoothing filter.*

7. *The typical output voltage will be approximately 570 mV peak-to-peak with V_{IN} at 32 mV peak-to-peak.*

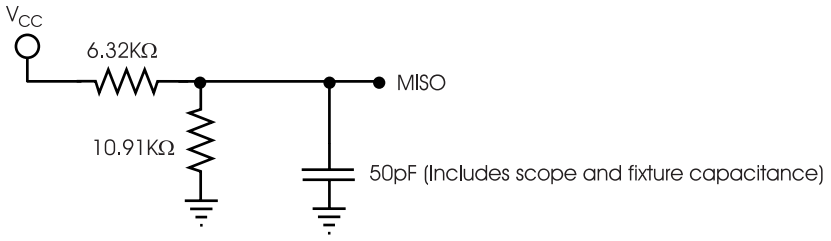
8. *For optimal signal quality, this maximum limit is recommended.*

Table 2-88: SPI AC Parameters[1]

Symbol	Characteristics	Min	Max	Units	Conditions
T_{SSS}	$\overline{SS}$ Setup Time	500		nsec	
T_{SSH}	$\overline{SS}$ Hold Time	500		nsec	
T_{DIS}	Data in Setup Time	200		nsec	
T_{DIH}	Data in Hold Time	200		nsec	
T_{PD}	Output Delay		500	nsec	
T_{DF}[(2)]	Output Delay to hiZ		500	nsec	
T_{SSmin}	$\overline{SS}$ HIGH	1		µsec	
T_{SCKhi}	SCLK High Time	400		nsec	
T_{SCKlow}	SCLK Low Time	400		nsec	
F_0	CLK Frequency		1,000	KHz	

1. *Typical values @T_A = 25°C and 3.0 V. Timing measured at 50% of the V_{CC} level.*

2. *Tristate test condition.*



2

TIMING DIAGRAMS

Figure 2-39: Timing Diagram

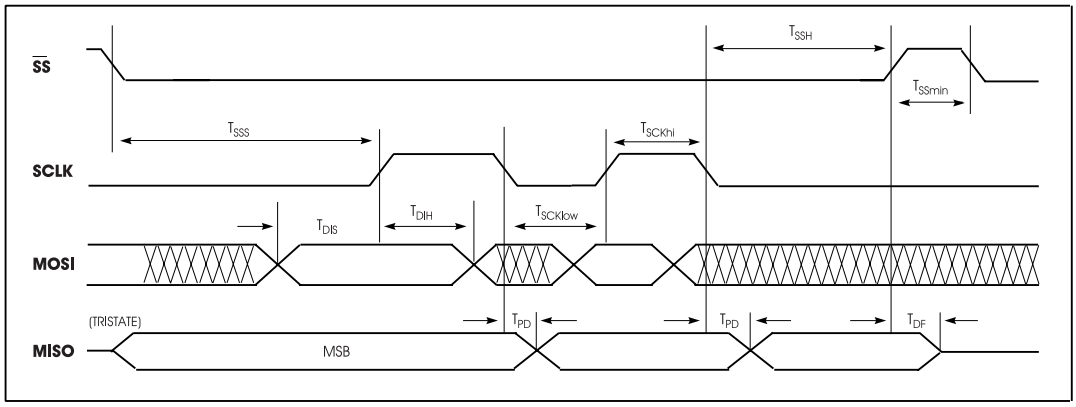


Figure 2-40: 8-Bit Command Format

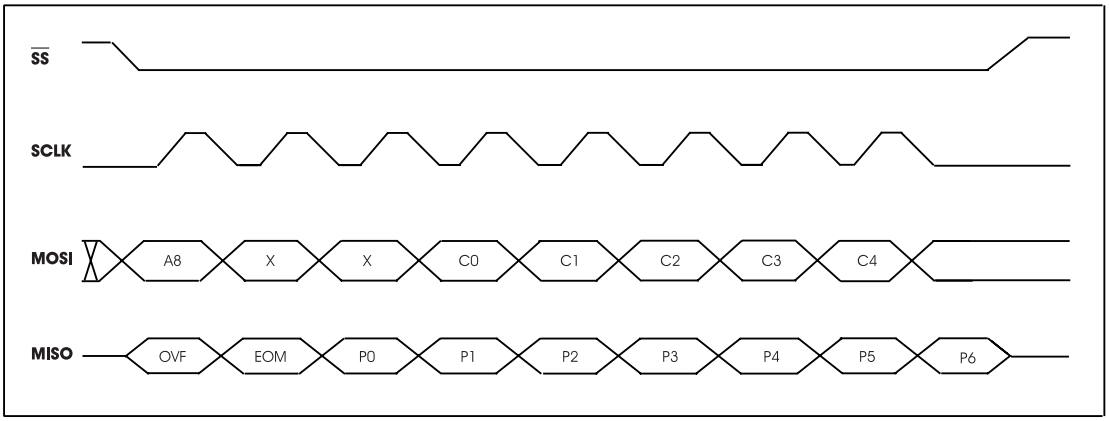


Figure 2-41: 16-Bit Command Format

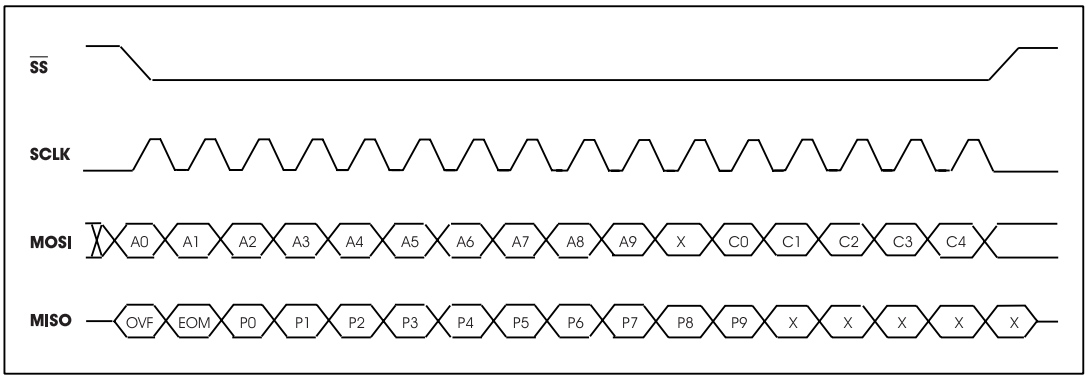


Figure 2-42: Playback/Record and Stop Cycle

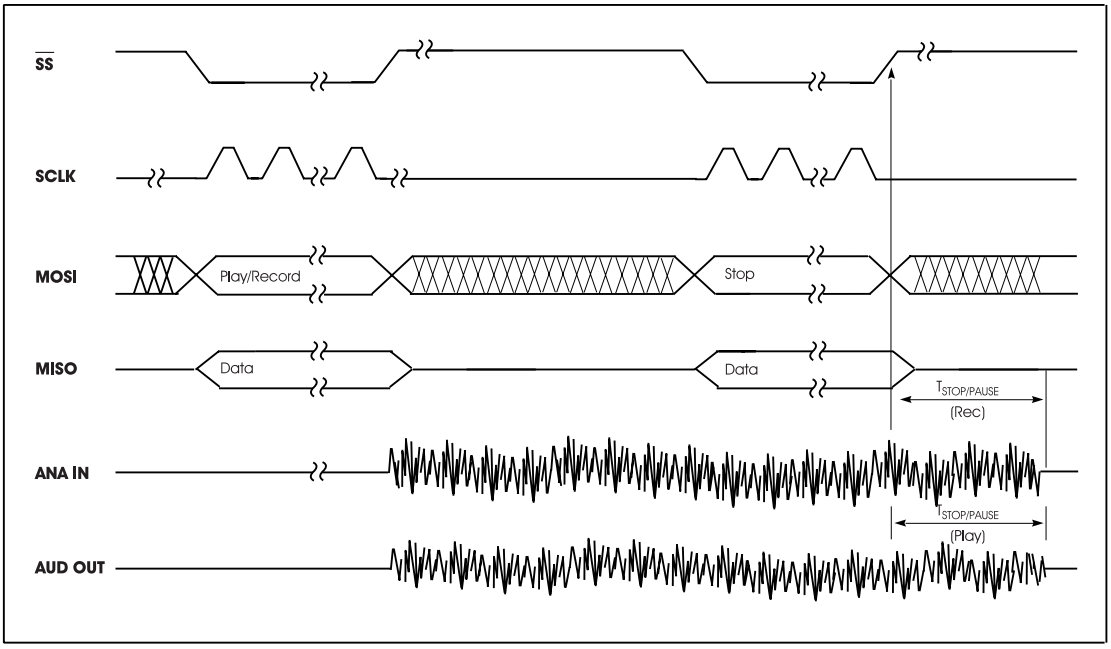
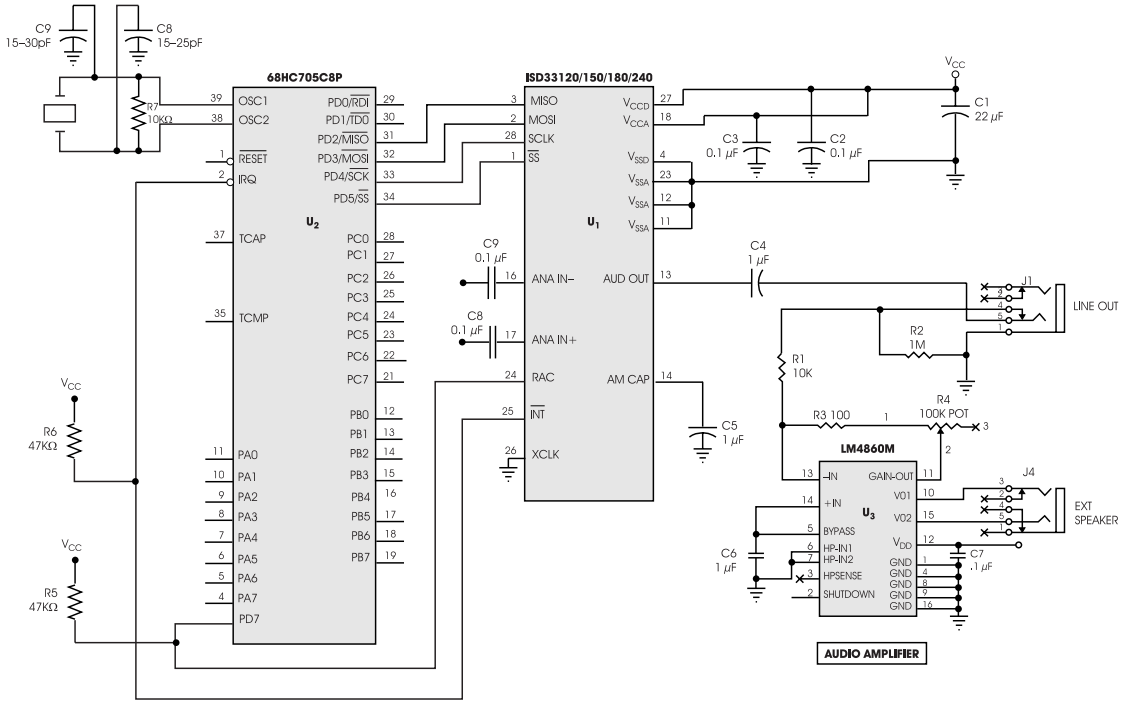
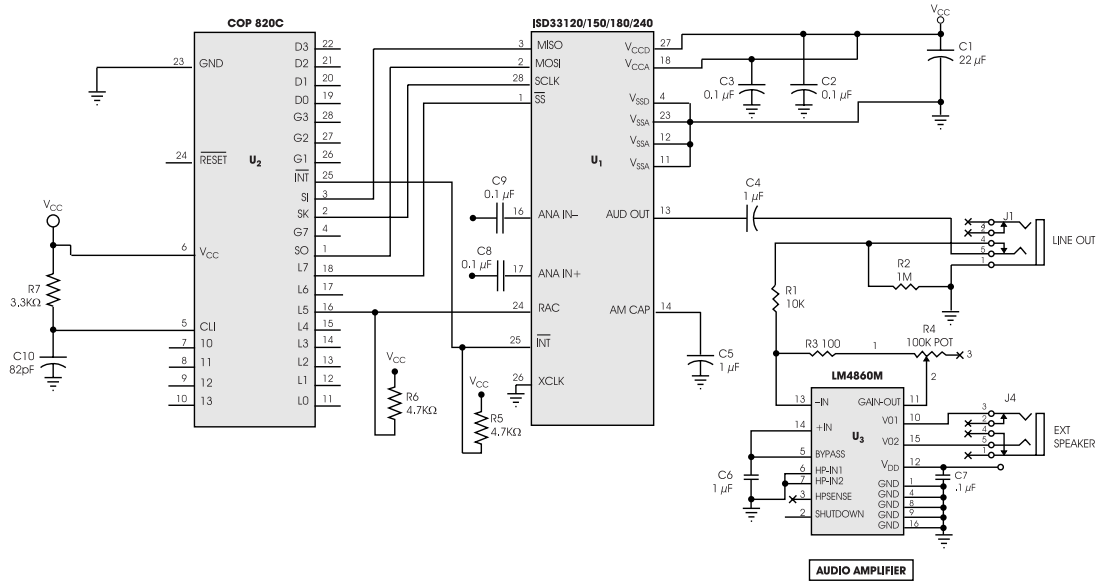


Figure 2-43: Application Example Using SPI



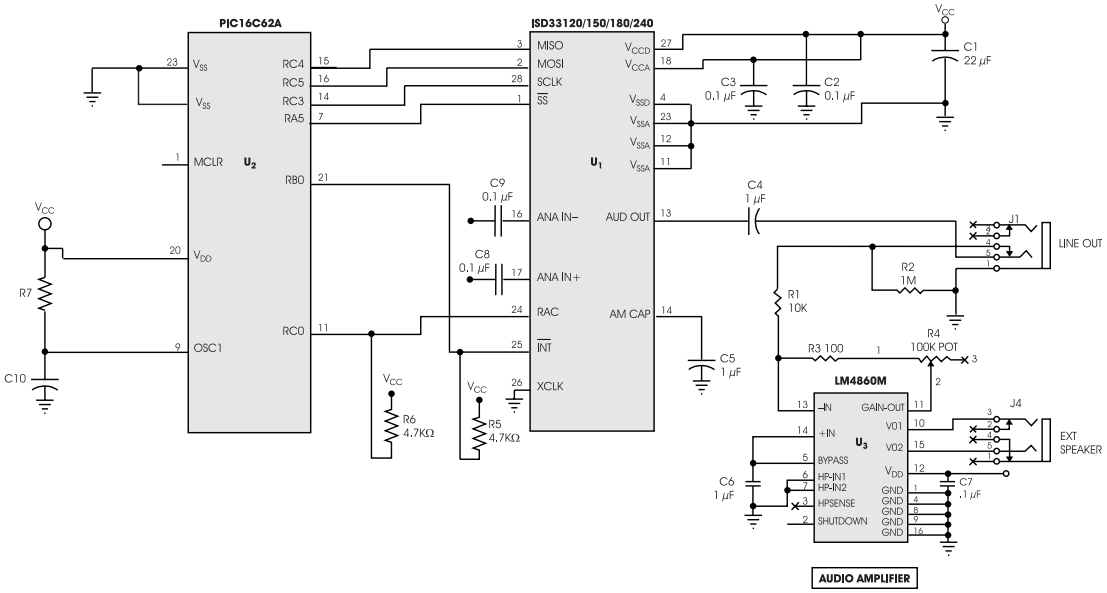
NOTE: *This application example is for illustration purposes only. ISD makes no representation or warranty that such application will be suitable for production.*

Figure 2-44: Application Example Using Microwire



1. *This application example is for illustration purposes only. ISD makes no representation or warranty that such application will be suitable for production.*

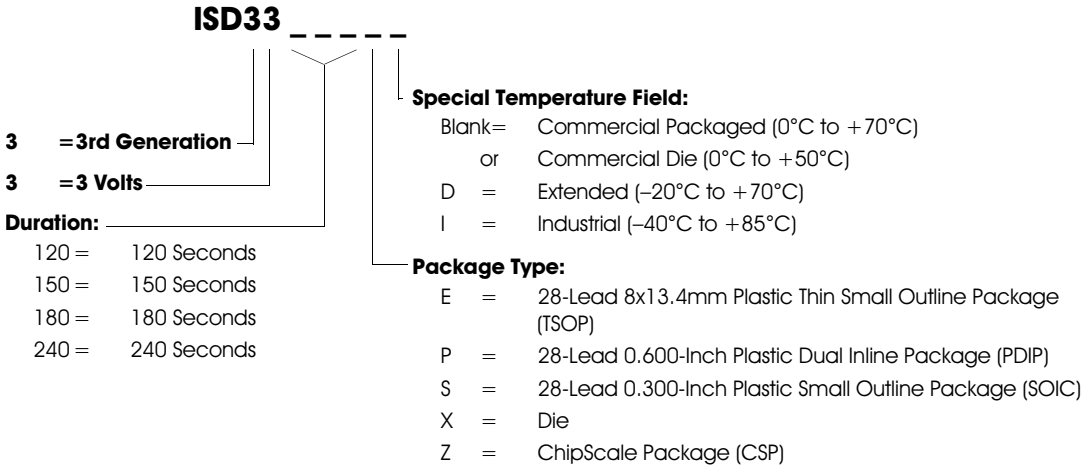
Figure 2-45: Application Example using SPI Port on Microcontroller



NOTE: *This application example is for illustration purposes only. ISD makes no representation or warranty that such application will be suitable for production.*

ORDERING INFORMATION

Product Number Descriptor Key



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When ordering ISD33000 Series devices, please refer to the following part numbers, which are planned to be supported in volume for this product series. Consult the local ISD Sales Representative or Distributor for availability information.

Part Number	Part Number	Part Number	Part Number
ISD33120E	ISD33150E	ISD33180E	ISD33240E
ISD33120ED	ISD33150ED	ISD33180ED	ISD33240ED
ISD33120EI	ISD33150EI	ISD33180EI	ISD33240EI
ISD33120P	ISD33150P	ISD33180P	ISD33240P
ISD33120PD	ISD33150PD	ISD33180PD	ISD33240S
ISD33120PI	ISD33150PI	ISD33180PI	ISD33240X
ISD33120S	ISD33150S	ISD33180S	ISD33240Z
ISD33120SD	ISD33150SD	ISD33180SD	ISD33240ZD
ISD33120SI	ISD33150SI	ISD33180SI	ISD33240ZI
ISD33120X	ISD33150X	ISD33180X	
ISD33120Z	ISD33150Z	ISD33180Z	
ISD33120ZD	ISD33150ZD	ISD33180ZD	
ISD33120ZI	ISD33150ZI	ISD33180ZI	

For the latest product information, access ISD's worldwide website at http://www.isd.com.