ChipCorder®
TECHNOLOGY BY ISD

ISD1606 Product

Single-Chip, Single- or Dual-Message Voice Record/Playback Device 4.8- to 9.6-Second Durations with Beep Tone Generator

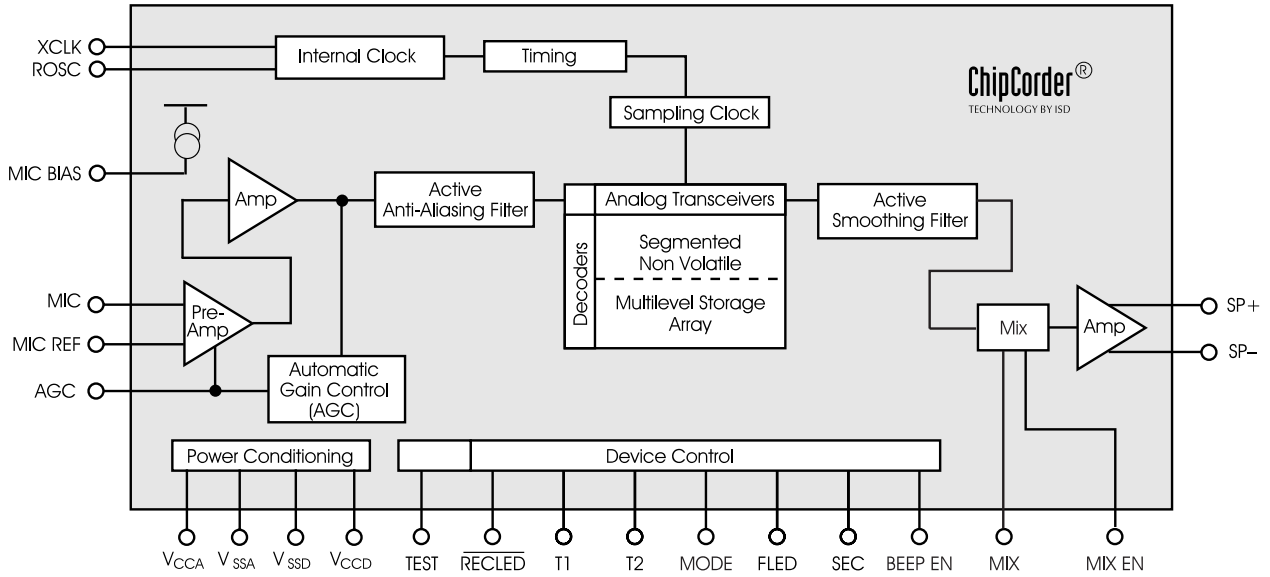
Advanced Information

GENERAL DESCRIPTION

Information Storage Devices' ISD1606 ChipCorder product provides a high quality, single chip, segmentable-message, audio record/playback solution with user selectable durations from 4.8 to 9.6 seconds. On-chip beep tone generator and LED drivers enables unique user interface options as well as additional audio and visual effects to be created. Available auxiliary audio mixing, microphone biasing and amplifier capabilities allow the simple integration of the ISD1606 with other system audio components, thus, minimizing total system costs. The CMOS device includes ISD's ChipCorder multilevel storage array, automatic gain control, anti-aliasing and smoothing filters, microphone preamplifier, speaker amplifier, auxiliary input, audio mixing circuitry, oscillator (with external resistor control), LED drivers, and beep tone generator. A minimum record/playback subsystem can be configured with a microphone, a speaker, several passive components, two push-buttons, and a power source.

Recordings are stored in on-chip, nonvolatile, memory cells, providing zero-power message storage. This unique, single-chip solution is made possible through ISD's patented multilevel storage technology. Voice and audio signals are stored directly into memory in their natural form, providing high-quality, solid-state voice reproduction.

Figure: ISD1606 Product Block Diagram



MAY 1998

FEATURES

- Easy-to-use single-chip, single or dual message voice record/playback solution
- High-quality, natural voice/audio reproduction
- Variable record/playback duration controlled by external resistor selection which sets sample rate.
- Segmented array
  - 6 seconds (2 x 3 sec) for the ISD1606
- AUX/MIX capability
- Beep tone before record operation and after overflow is reached
- 3 Hz flashing LED during playback
- A microphone biasing source
- Push-button interface
  - Playback can be edge- or level-activated
- On-chip 8 Ω speaker driver
- Automatic power-down mode
  - Enters standby mode immediately following a record or playback cycle
  - 0.5 μA standby current (typical)
- Zero-power message storage
  - Eliminates battery backup circuits
- 100-year message retention (typical)
- 10K record cycles (typical)
- On-chip oscillator
- No algorithm development required
- Single +5 volt power supply
- 0°C to 50°C Operation
- Available in wafer form, die form, and 28-pin 600 mil. PDIP (for sampling only)

Table : ISD1606 Product Summary

Playback and Record Duration	ISD1606 Duration
8.0 KHz sample rate (R_{OSC} = 80 KΩ)	4.8 sec
6.4 KHz sample rate (R_{OSC} = 100 KΩ)	6.0 sec
5.3 KHz sample rate (R_{OSC} = 120 KΩ)	7.2 sec
4.0 KHz sample rate (R_{OSC} = 160 KΩ)	9.6 sec

1. *The ISD1606 products are only tested at the 6.4 KHz sample.*

Table of Contents

FIGURES, GRAPHS, AND TABLES IN THE ISD1606 DATASHEET

DETAILED DESCRIPTION

SPEECH/SOUND QUALITY

ISD's patented ChipCorder technology provides natural record and playback. The input voice signals are stored directly in nonvolatile EEPROM cells and are reproduced without the synthetic effect often heard with digital solid-state speech solutions. A complete sample is stored in a single cell, minimizing the memory necessary to store a single message.

DURATION

The ISD1606 device offers single-chip solutions with 4.8 to 9.6 seconds of record/playback duration capacity. Sampling rate and duration are determined by an external resistor connected to the ROSC pin. These specifications apply with the required resistor value for 6-second minimum playback duration.

NOTE *Only the 6 second duration is guaranteed and tested.*

EEPROM STORAGE

One of the benefits of ISD's ChipCorder technology is the use of on-chip non-volatile memory, providing zero-power message storage. The message is retained for up to 100 years without power. In addition, the device can be re-recorded typically over 10,000 times.

BASIC OPERATION

The ISD1606 product ChipCorder device is controlled by the MODE pin, and either of two trigger pins, T1 or T2. The ISD1606 product parts are configured for design simplicity in a dual-message application. Device operation is explained under "Functional Description Example" on page 8.

AUTOMATIC POWER-DOWN MODE

At the end of a playback or record cycle, the ISD1606 device automatically returns to a low-power standby mode, consuming typically 0.5 μA, provided that MODE, T1, T2, XCLK, and TEST pins are LOW (see Table 5 on page 5). During a playback cycle, the device powers down automatically at the end of the message. During a record cycle, the device powers down immediately after T1 or T2 is released LOW.

PIN DESCRIPTIONS

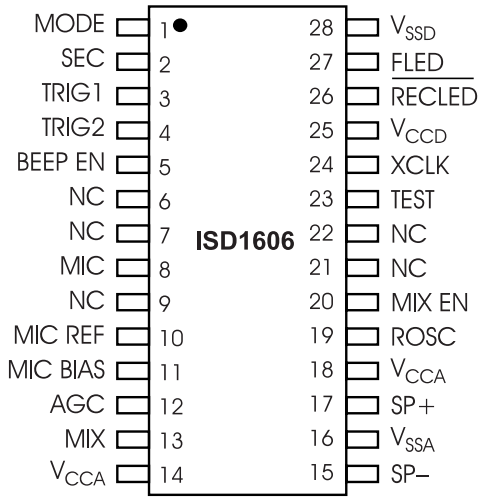
VOLTAGE SUPPLIES (V_{CCA} , V_{CCD})

Analog and digital circuits internal to the ISD1606 device use separate power buses to minimize noise on the chip. These power buses are brought out to separate pins on the device and should be tied together as close to the supply as possible. It is important that the power supply be decoupled as close as possible to the device.

GROUND SUPPLIES (V_{SSA}, V_{SSD})

Similar to V_{CCA} and V_{CCD}, the analog and digital circuits internal to the ISD1606 device use separate ground buses to minimize noise. These pins should be tied together as close as possible to the device.

Figure 1: ISD1606 Product Pinouts—For Sampling Only



PDIP

MODE PIN

This pin configures the T1 and T2 pins. MODE pin set at 0, the T1 and T2 pin will be configured as edge sensitive play pins. MODE set to 1, T1 and T2 pins will be configured as record pins. The MODE pin floating, T1 an T2 pins will be configured as level sensitive play pins.

SEC PIN

The security pin prevents recording on Seg 1 when it is set to 1. Recording on Seg 1 is allowed when SEC pin is set at 0.

T1 AND T2 PINS

T1 and T2 as Record Pins

T1 and T2 are trigger pins which play and record both segments independently or combined as a single message. Triggering T1 pin will initiate recording on segment one. Triggering T2 pin will begin recording on segment two. Triggering both T1 and T2 together (during debounce period) will record a single message. Segment one overflow will be ignored and beep tone at the end of segment one will be disabled. Once a record operation has been initiated all further transition on T1 and T2 pins will be ignored until the end of the record operation. The record operation ends when the trigger pins are returned LOW or the end of the message is reached.

T1 and T2 as Play Pins

Table 1 and Table 2 describe the operation of the T1 and T2 pins in edge and level modes.

Table 1: Play Edge Triggering Conditions

Condition	Action
T1 Pulsed	Playback Seg 1 until EOM or OVF of Seg 1 is reached.
T2 Pulsed	Playback Seg 2 until EOM or OVF of Seg 2 is reached
T1 and T2 Pulsed	Playback Seg 1 and then Seg 2 messages until EOM or OVF of Seg 2 is reached.
T2 pulsed while Seg 1 in Playback	Jump to beginning of Seg 2 and continue playback until EOM or OVF of Seg 2 is reached.
T1 pulsed while Seg 2 in Playback	Jump to beginning of Seg 1 and continue playback until EOM or OVF of Seg 1 is reached.

Table 2: Play Level Conditions

Play Level Conditions	Action
T1 is set HIGH	Playback Seg 1 until T1 pin is pulled LOW or EOM or OVF of Seg 1 is reached
T2 is set HIGH	Playback Seg 2 until T2 pin is pulled LOW or EOM or OVF of Seg 2 is reached.
T1 and T2 are both set HIGH during debounce time	Playback Seg 1 and then Seg 2 until T1 and T2 pins are both pulled LOW or EOM or OVF of Seg 2 is reached.

MIX PIN

Input pin for an auxiliary audio signal. During playback auxiliary input will mix with the playing message.

MIX EN PIN

An input pin that enables the AUX/MIX function when set to 1. Disables the AUX/MIX function when set to 0.

FLED PIN

An output pin that will drive an LED to flash approximately at 3 Hz. The LED needs to be connected between the positive power supply and the FLED pin.

BEEP EN PIN

An input pin that will enable the beep tone function.

MIC BIAS PIN

A constant voltage source pin that provides preset bias to the microphone.

RECORD LED OUTPUT ($\overline{\text{RECLED}}$)

The $\overline{\text{RECLED}}$ output is LOW during a record cycle. It can be used to drive a LED to provide feedback that a record cycle is in progress. In addition, $\overline{\text{RECLED}}$ pulses LOW momentarily when an end-of-message or end-of-memory marker is encountered in a playback cycle.

MICROPHONE INPUT (MIC)

The microphone input transfers its signal to the on-chip preamplifier. An on-chip Automatic Gain Control (AGC) circuit controls the gain of the preamplifier. An external microphone should be AC-coupled to this pin via a series capacitor. The capacitor value, together with the internal 10 Kohm resistance on this pin, determine the low-frequency cutoff for the ISD1606 product pass-band. Internal AC-coupling connects the preamplifier to the amplifier.

MICROPHONE REFERENCE (MIC REF)

The MIC REF input is the inverting input to the microphone preamplifier. This provides input noise-cancellation, or common-mode rejection, when the microphone is connected differentially to the device (this is the preferred connection).

AUTOMATIC GAIN CONTROL (AGC)

The AGC dynamically adjusts the gain of the preamplifier to compensate for the wide range of microphone input levels. The AGC allows the full range of sound, from whispers to loud sounds, to be recorded with minimal distortion. The "attack" time is determined by the time constant of a 5 KΩ internal resistance and an external capacitor (C6 on the schematic on Figure 2 on page 8) connected from the AGC pin to V_{SSA} analog ground. The "release" time is determined by the time constant of an external resistor (R5) and an external capacitor (C6) connected in parallel between the AGC pin and V_{SSA} analog ground. Nominal values of 470 KΩ and 4.7 μF give satisfactory results in most cases.

SPEAKER OUTPUTS (SP+, SP–)

The SP+ and SP– pins provide direct drive for loudspeakers with impedances as low as 8 ohms. A single output may be used, however, for direct-drive loudspeakers the two opposite-polarity outputs provide an improvement in output power of up to four times over a single-ended connection. Furthermore, when SP+ and SP– are used, a speaker coupling capacitor is not required. A single-ended connection will require an AC-coupling capacitor between the SP pin and the speaker.

The SP+ pin and the SP– pin are internally connected through a 50 KΩ resistance. When not in playback mode, they are floating.

EXTERNAL CLOCK (XCLK)

The external clock input for the ISD1606 device has an internal pull-down resistor. This pin is used for test purposes only. Do not bond this pad.

TEST (TEST)

The test input for the ISD1606 device has an internal pull-down resistor. This pin is used for test purposes only. Do not bond this pad.

RESISTOR CONTROLLED OSCILLATOR (ROSC)

The resistor-controlled oscillator input enables the user to vary the ISD1606 device record and playback duration. The resistor connected between the ROSC pin and V_{SS}, R2 (R_{OSC}), determines the sample frequency and the filter upper pass band for the ISD1606 device. ISD recommends an R_{OSC} resistor value of 100 KΩ.

SPECIFICATIONS

Table 3: Absolute Maximum Ratings(1)

Condition	Value
Junction temperature	150°C
Storage temperature range	–65°C to +150°C
Voltage applied to any pin	(V_{SS} – 0.3 V) to (V_{CC} + 0.3 V)
Lead temperature (soldering—10 seconds)	300°C
V_{CC} – V_{SS}	–0.3 V to +7.0 V

1. *Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability. Functional operation is not implied at these conditions.*

Table 4: Operating Conditions

Condition	Value
Die operating temperature range(1)	0°C to +50°C
Supply voltage (V_{CC})(2)	+4.5 V to +6.5 V
Ground voltage (V_{SS})(3)	0 V

1. *Case Temperature*
2. $V_{CC} = V_{CCA} = V_{CCD}$.
3. $V_{SS} = V_{SSA} = V_{SSD}$.

Table 5: DC Parameters

Symbol	Parameters	Min(2)	Typ(1)	Max(2)	Conditions
V_{BIAS}	Microphone Bias Output Voltage		3.2 V		I_{SOURCE} = 1 mA Applies to MIC BIAS pin
V_F	Floating Output Voltage		2.0 V		Applies to MODE pin
V_{IH1}	Input High Voltage	2.0 V			Applies to: T1, T2, SEC, BEEP EN, and MIX EN pins
V_{IH2}	Input High Voltage	3.5 V			Applies to MODE pin
V_{IL1}	Input Low Voltage			0.8 V	Applies to: T1, T2, SEC, BEEP EN, and MIX EN pins.
V_{IL2}	Input Low Voltage			0.8 V	Applies to MODE pin
V_{OL}	Output Low Voltage			0.4 V	I_{OL} = 4.0 mA(3) Applies to: $\overline{\text{RECLED}}$ and FLED pins
V_{OH}	Output High Voltage	2.4 V			I_{OH} = – 1.6 mA(3) Applies to: $\overline{\text{RECLED}}$ and FLED pins
I_{CC}	V_{CC} Current (Operating)		15 mA	30 mA	R_{EXT}∞ (4)
I_{SB}	V_{CC} Current (Standby)		0.5 µA	10 µA	(4) (5)
I_{ILPD1}	Input Leakage Current			1 µA	Force V_{SS} Applies to: T1, T2, SEC, BEEP EN, and MIX EN pins

Table 5: DC Parameters

Symbol	Parameters	Min(2)	Typ(1)	Max(2)	Conditions
I_{ILPD2}	Input Current HIGH			130 µA	Force V_{CC} Applies to: T1, T2, SEC, BEEP EN, and MIX EN pins
I_{ILPD3}	Input Current HIGH			100 µA	Force V_{CC} Applies to the MODE pin during record and playback
I_{ILPD4}	Input Current HIGH	–100 µA			Force V_{CC} Applies to the MODE pin during record and playback
R_{EXT}	Output Load Impedance	8 Ω			Speaker Load, SP+ to SP–
R_{MIC}, R_{MICREF}	Preamp Input Resistance		10 KΩ		
A_{MSP}	MIC SP+/– Gain		45 dB		AGC = 0.0 V; input signal driven balanced to MIC and MIC REF pins
R_{AGC}	AGC Output Resistance		5 KΩ		
R_{MIX}	AUX/MIX Input Resistance		27 KΩ		

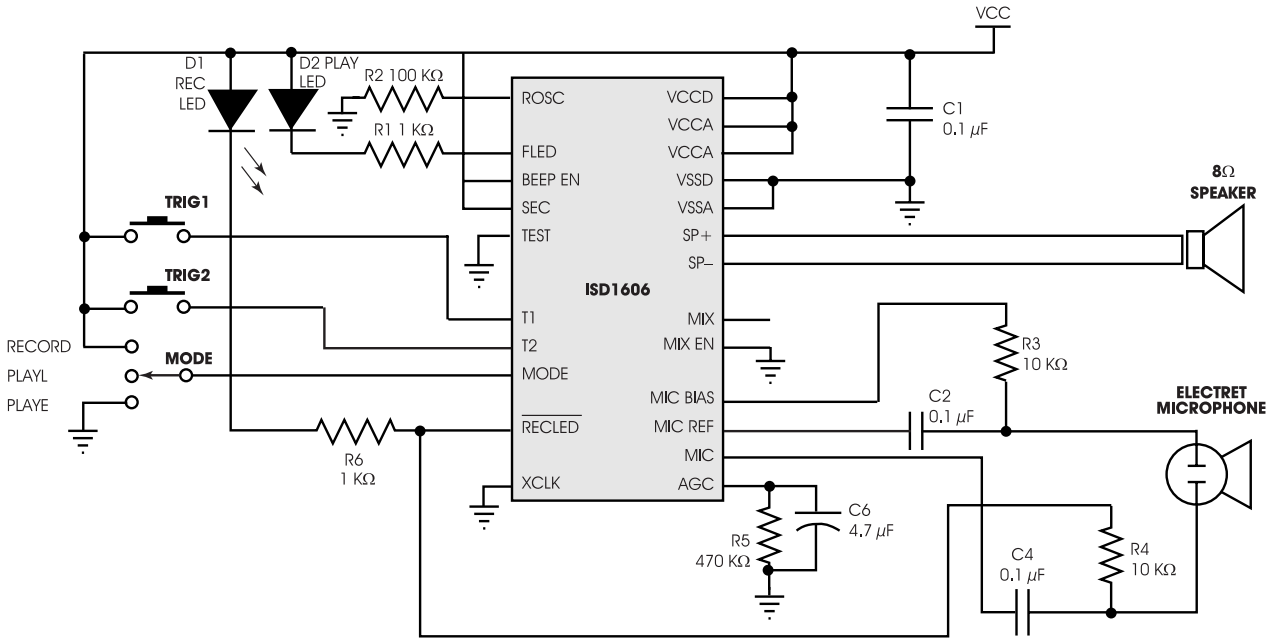
1. *Typical values: T_A = 25°C and 5.0 V.*
2. *All minimum and maximum limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100 percent tested.*
3. *Record LED output, $\overline{RECLED}$ and FLED.*
4. *V_{CCA} and V_{CCD} connected together.*
5. *T1, T2, SEC, BEEP EN, MIX EN, XCLK, and TEST must be at V_{SSD}.*

Table 6: AC Parameters[1]

Symbol	Characteristic	Min[3]	Typ[2]	Max[3]	Conditions
F_S	Sampling Frequency			6.4 KHz	[4]
F_{CF}	Filter Pass Band		2.6 KHz		3 dB Roll-Off Point[5] [6]
T_{REC}, T_{PLAY}	Record Duration —ISD1606	6 sec		6.6 sec	[4]
T_{EOM}	EOM Pulse Width (Wink)		84 msec		
T_{DB}	Debounce Time		84 msec		
THD	Total Harmonic Distortion		1 %		@ 500 Hz, 15 mV Peak to Peak
P_{OUT}	Speaker Output Power		24.4 mW		R_{EXT} = 8 Ω
V_{OUT}	Voltage Across Speaker Pins		1.25 Vp–p	2.5 Vp–p	R_{EXT} = 600 Ω
V_{IN}	MIC Input Voltage		150 mVp–p	300 mVp–p	Input level of MIC to MIC REF when driven balanced[7]
	Oscillator Stability			±5.0 %	

1. *These specifications apply with R_{OSC} equaling 100 KΩ. The ISD1606 product is only tested at the 6.4 KHz sample rate.*
2. *Typical values: T_A = 25°C and 5.0 V.*
3. *All minimum and maximum limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100 percent tested.*
4. *Oscillator stability may vary as much as ±5 percent over the operating temperature and voltage ranges.*
5. *Low-frequency cutoff depends upon value of external capacitors (see Pin Descriptions)*
6. *Filter specification applies to the anti-aliasing filter and to the smoothing filter.*
7. *Balanced input signal applied between MIC and MIC REF as shown in the application example. Single-ended MIC or MIC REF recommended to be less than 100 mV peak to peak.*

Figure 2: ISD1606 Product Application Example—Design Schematic



FUNCTIONAL DESCRIPTION EXAMPLE

The following example operating sequences demonstrate the functionality of the ISD1606 device.

1. Record a message filling the memory.

   Taking the MODE switch HIGH, then pressing T1 and T2 pins HIGH simultaneously, will initiate a recording that will fill both segments of the device. The $\overline{\text{RECLED}}$ pin will go LOW to activate the record LED and will remain LOW until the device is filled.

   If, instead, only T1 or T2 is pressed HIGH, then the message will be in the first or second segment of the device. If either trigger pin is released before the segment is filled, the message will end at that point.

2. Edge-activated playback.

   With the MODE switch set LOW and momentarily pressing either T1 or T2 HIGH will result in the corresponding segment being played completely. If both T1 and T2 are pressed simultaneously then the entire device will be played through.

3. Level-activated playback.

   With the MODE switch OPEN (floating), then pressing and holding either T1 or T2 play the selected segment completely.

4. Level-activated playback (truncated).

   If one of the trigger pins is released (LOW) before the entire message is played, as in the level-activated playback step detailed above, then the playback will stop immediately.

5. Record (interrupting playback).

   The record function takes precedence over playback. If, while the device is playing a message, the MODE pin is taken HIGH and T1 or T2 is taken HIGH, the device will stop playing and begin to record at the beginning of the selected message segment.

6. Record a message, partially filling the memory.

   A record operation does not necessarily need to fill the entire device. Releasing one of the trigger pins LOW before filling the message space causes the recording to stop, an EOM marker to be placed, and the device to automatically power-down.

7. Play back a message partially filling the memory.

   As in the edge-activated playback sequence, when the MODE pin is LOW and T1 or T2 is pressed, the message will play until the EOM marker is reached and the device powers down.

8. $\overline{\text{RECLED}}$ operation.

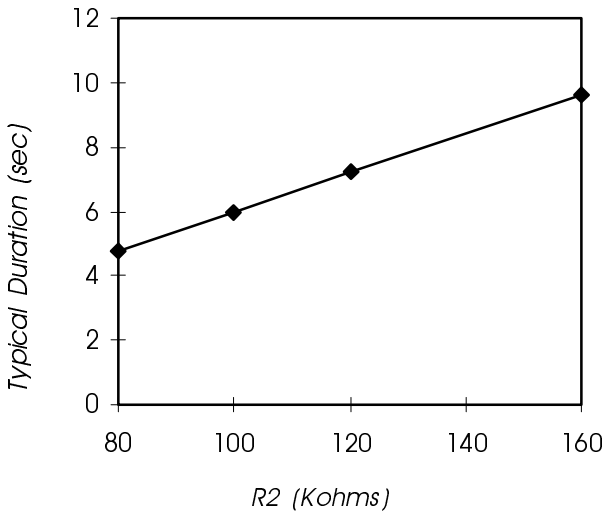
   The $\overline{\text{RECLED}}$ output pin provides an active-LOW signal which can be used to drive an LED as a "record-in-progress" indicator. It returns to a HIGH state when one of the trigger pins are released LOW or when the recording is completed due to the memory being filled. This pin also pulses LOW to indicate the end of a message has been played.

9. ROSC operation.

   The duration of the device can be varied by changing the value of R2 (R_{OSC}). This means the ISD1606 device can actually be between 4.8 to 9.6 seconds duration. See Graph 1 which charts typical durations when the R2 is varied from 80 KΩ to 160 KΩ.

   ROSC allows frequency shifting where a recorded voice or sound can be played back faster or slower than normal for special effects. For example, use a 100 KΩ resistor to make the recording and then playback with either an 80 KΩ resistor for faster "chipmunk" talk or a 120 KΩ resistor for a slower, lower voice.

Graph 1: ISD1606 Product Duration versus R2 (R_{OSC}) at T_A = 25°C and 5.0 V



TIMING DIAGRAMS

Figure 3: Record Message Until T1/T2 Goes LOW

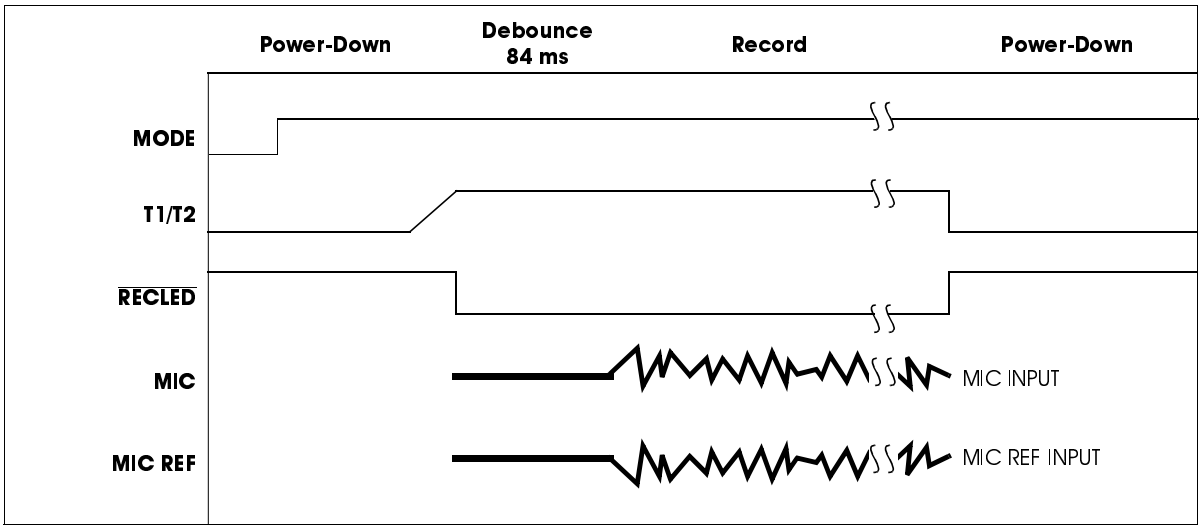


Figure 4: Record Message Until Array is Full

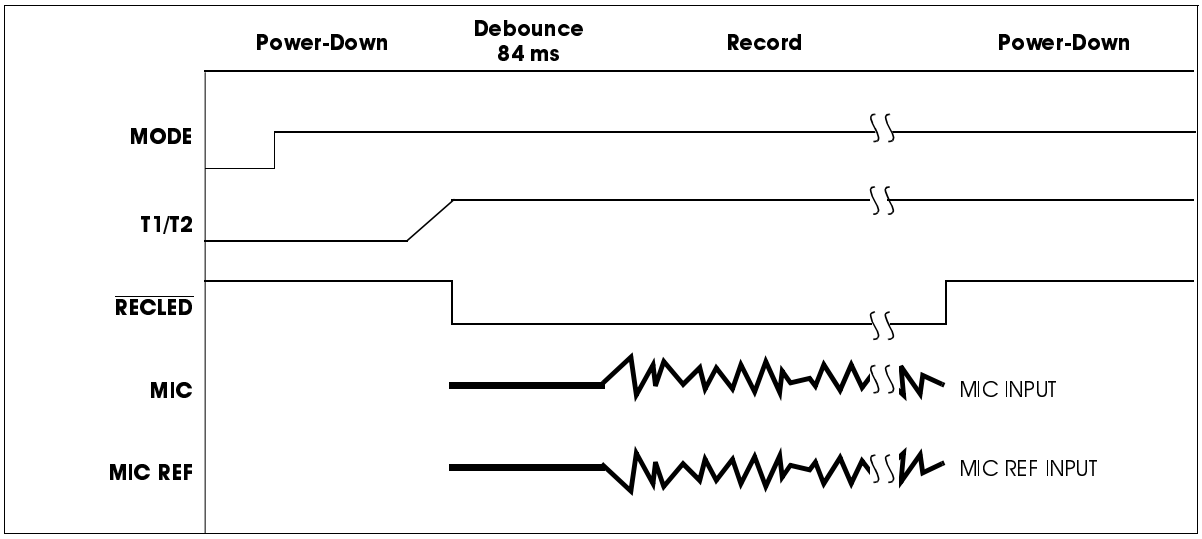


Figure 5: Play Edge Mode Timing Diagram—Edge Sensitive Playback Mode for Seg 1 to Seg 2 Transition, and Seg 2 to Seg 1

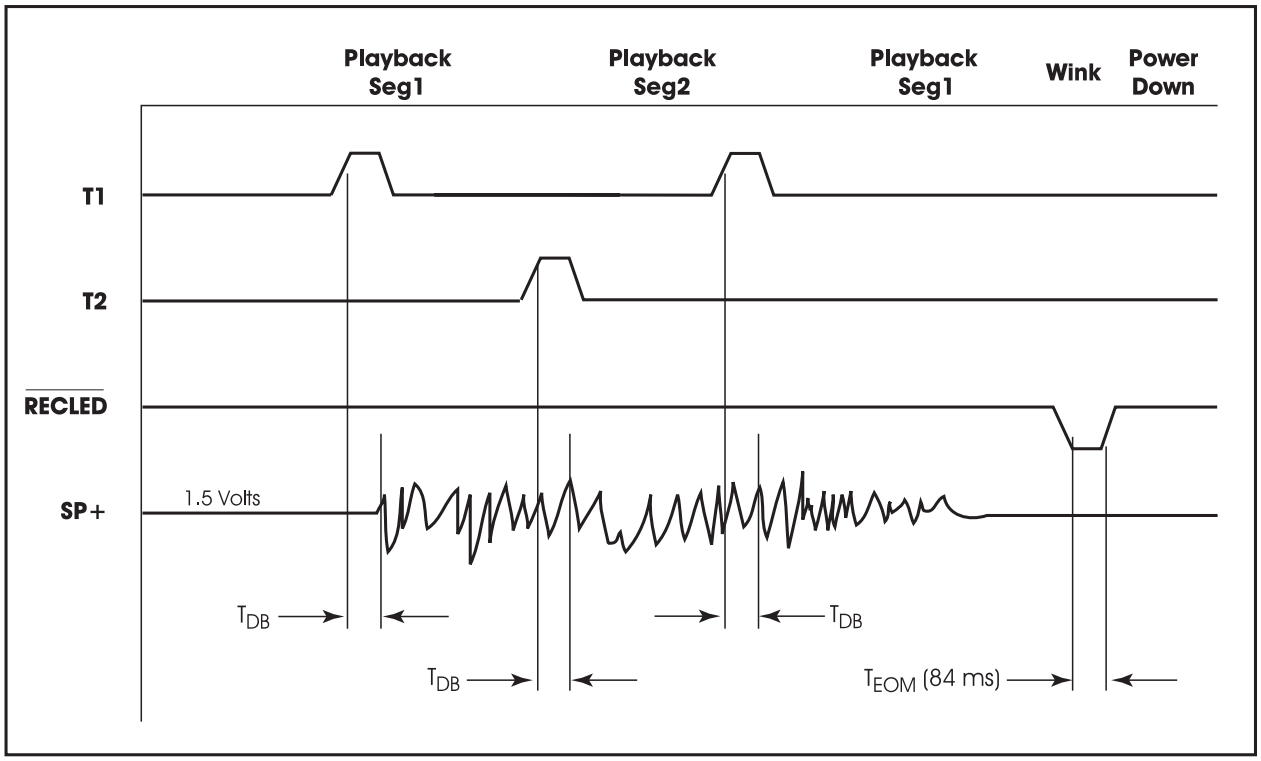
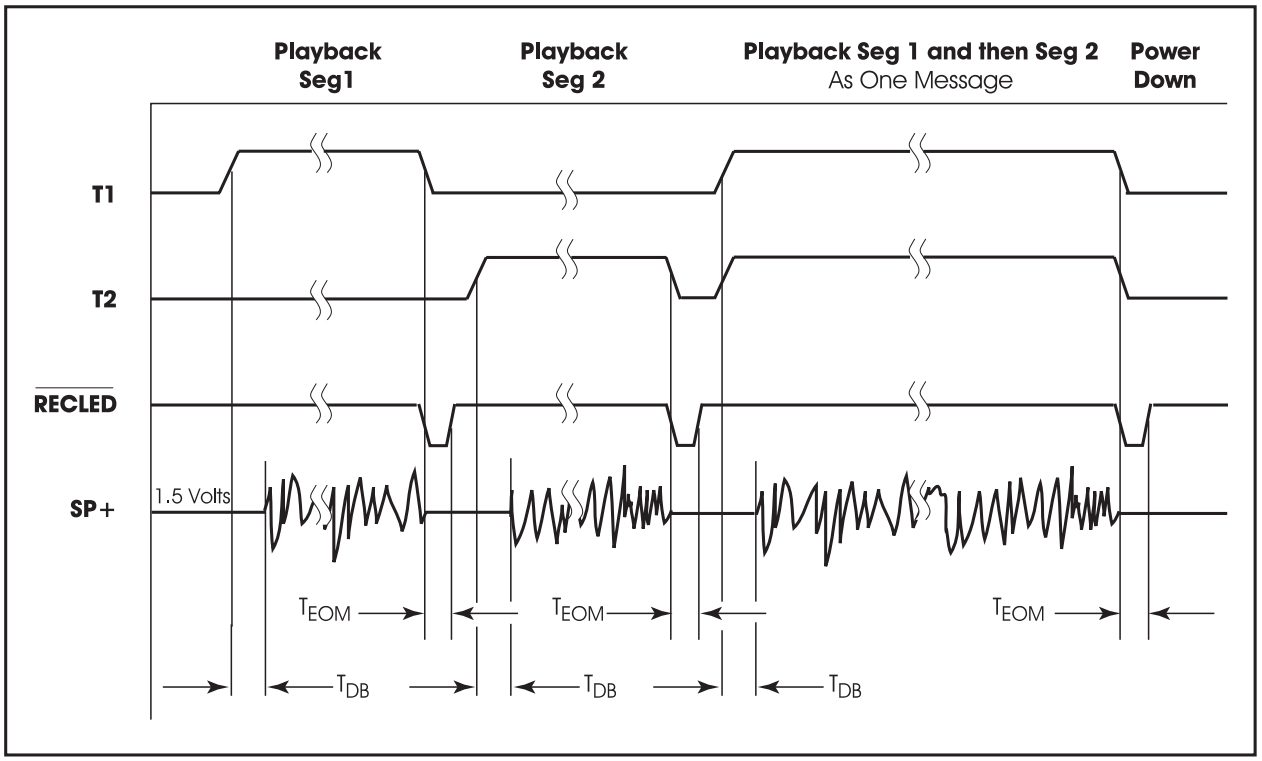


Figure 6: Play Level Mode Timing Diagram



DEVICE PHYSICAL DIMENSIONS

Figure 7: ISD1606 Bonding Physical Layout[1] (Unpackaged Die)

ISD1606

I. Die Dimensions

X: 2730 ±25.4 microns
107.5 ±1 mil

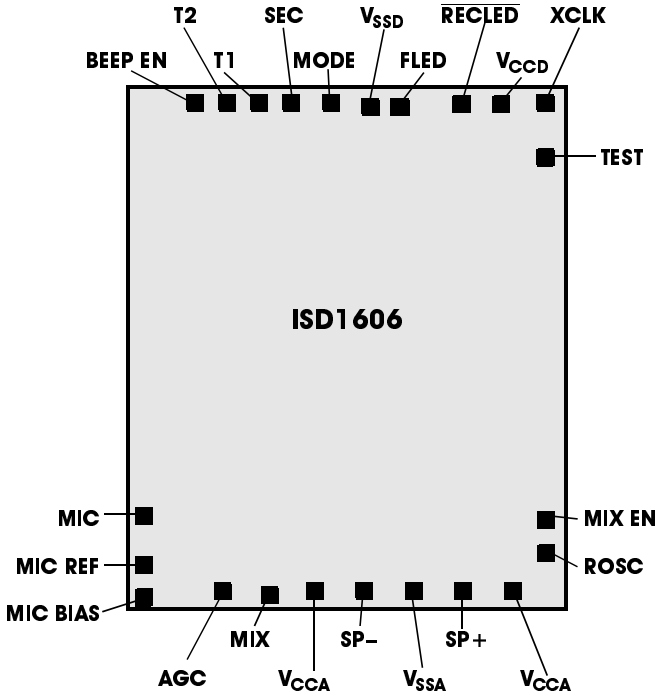
Y: 3230 ±25.4 microns
127.1 ±1 mil

II. Die Thickness[2]

16 ±1 mil (typ)

III. Pad Opening

100 microns
3.9 mils



1. *The backside of die is internally connected to V_{SS}. It **MUST NOT** be connected to any other potential or damage may occur.*
2. *Die thickness is subject to change, please contact ISD factory for status and availability.*

Table 7: ISD1606 Pin/Pad Designations with Respect to Die Center

Pin	Pin Name	X Axis (um)	Y Axis (um)	X Axis (mil)	Y Axis (mil)
1	MODE	–151.60	1464.20	–5.97	57.65
2	SEC	–385.00	1464.20	–15.16	57.65
3	T1	–568.55	1464.20	–22.38	57.65
4	T2	–746.65	1464.20	–29.40	57.65
5	BEEP EN	–929.40	1464.20	–36.59	57.65
6	N/C				
7	N/C				
8	MIC	–1207.60	–1012.20	–47.54	–39.85
9	N/C				
10	MIC REF	–1196.80	–1273.00	–47.12	–50.12
11	AGC	–770.55	–1447.60	–30.34	–56.99
12	MIC BIAS	–1196.80	–1468.05	–47.12	–57.80
13	MIX	–523.00	–1468.00	–20.59	–57.80
14	V_{CCA}	–253.80	–1454.40	–9.99	–57.26
15	SP–	66.00	–1454.40	2.60	–57.26
16	V_{SSA}	385.80	–1454.40	15.19	–57.26
17	SP+	705.60	–1454.40	27.78	–57.26
18	V_{CCA}	1025.40	–1454.40	40.37	–57.26
19	ROSC	1203.00	–1202.20	47.36	–47.33
20	MIX EN	1203.00	–1029.00	47.36	–40.51
21	N/C				
22	N/C				
23	TEST	1203.00	1154.35	47.36	45.45
24	XCLK	1184.20	1460.60	46.62	57.50
25	V_{CCD}	860.80	1449.20	33.89	57.06
26	$\overline{\text{RECLED}}$	627.60	1451.60	24.71	57.15
27	FLED	270.00	1449.20	10.63	57.06
28	V_{SSD}	60.20	1449.20	2.37	57.06

Figure 8: 28-Lead 0.600-Inch Plastic Dual Inline Package (PDIP) (P)—For Sampling Only

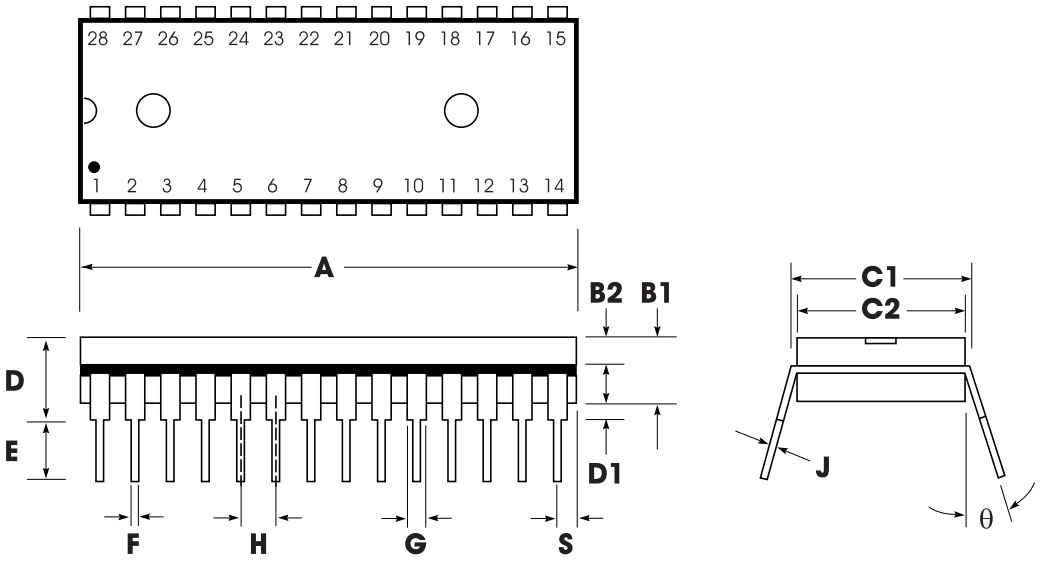
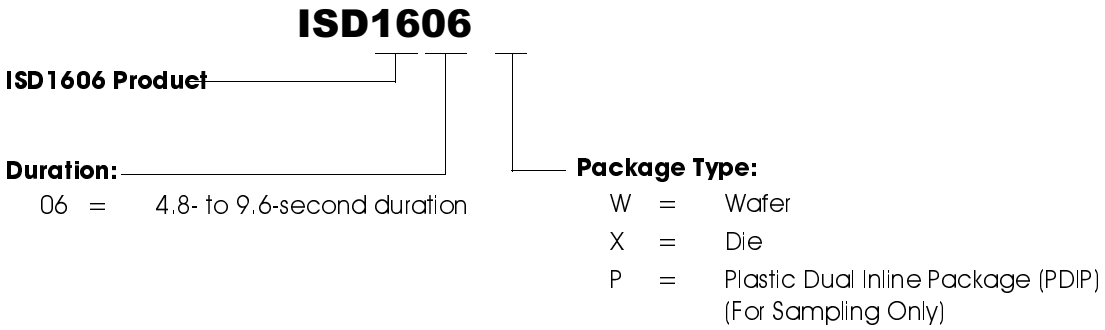


Table 8: Plastic Dual Inline Package (PDIP) (P) Dimensions—For Sampling Only

	INCHES			MILLIMETERS		
	Min	Nom	Max	Min	Nom	Max
A	1.445	1.450	1.455	36.70	36.83	36.96
B1		0.150			3.81	
B2	0.065	0.070	0.075	1.65	1.78	1.91
C1	0.600		0.625	15.24		15.88
C2	0.530	0.540	0.550	13.46	13.72	13.97
D			0.19			4.83
D1	0.015			0.38		
E	0.125		0.135	3.18		3.43
F	0.015	0.018	0.022	0.38	0.46	0.56
G	0.055	0.060	0.065	1.40	1.52	1.65
H		0.100			2.54	
J	0.008	0.010	0.012	0.20	0.25	0.30
S	0.070	0.075	0.080	1.78	1.91	2.03
q	0°		15°	0°		15°

ORDERING INFORMATION

Product Number Descriptor Key



When ordering, please refer to the following part numbers which are supported in volume for this product series. Consult the local ISD Sales Representative or Distributor for availability information.

Part Number
ISD1606W
ISD1606X
ISD1606P (For Sampling Only)

For the latest product information, access ISD's worldwide website at http://www.isd.com.

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The warranty for each product of ISD (Information Storage Devices, Inc.), is contained in a written warranty which governs sale and use of such product. Such warranty is contained in the printed terms and conditions under which such product is sold, or in a separate written warranty supplied with the product. Please refer to such written warranty with respect to its applicability to certain applications of such product.

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The 100-year retention and 100K record cycle projections are based upon accelerated reliability tests, as published in the ISD Reliability Report, and are neither warranted nor guaranteed by ISD.

Information contained in this ISD ChipCorder data sheet supersedes all data for the ISD ChipCorder products published by ISD prior to May, 1998.

This data sheet and any future addendum to this data sheet is (are) the complete and controlling ISD ChipCorder product specifications. In the event any inconsistencies exist between the information in this and other product documentation, or in the event that other product documentation contains information in addition to the information in this, the information contained herein supersedes and governs such other information in its entirety.

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Part No. 2200598D1606