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ISD1200 Series

Single-Chip Voice Record/Playback Devices
10- and 12-Second Durations

FIGURES, CHARTS, AND TABLES IN THE ISD1200 SERIES DATASHEET

Winbond Electronics Corporation America

ChipCorder®
TECHNOLOGY BY ISD

ISD1200 Series

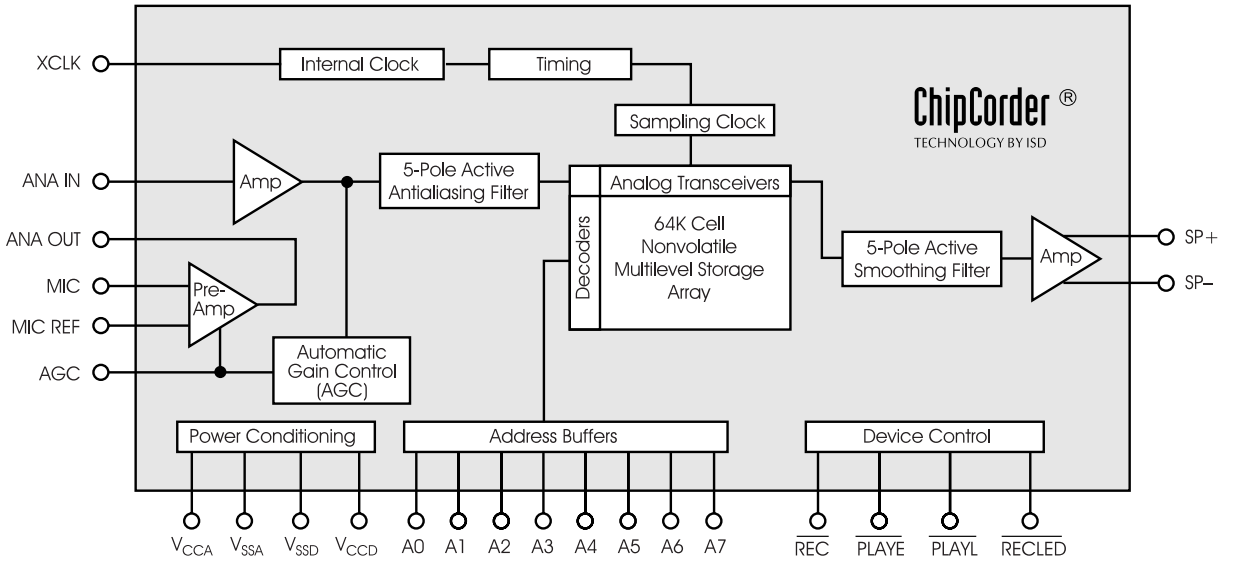
Single-Chip Voice Record/Playback Devices
10- and 12-Second Durations

GENERAL DESCRIPTION

Information Storage Devices' ISD1200 ChipCorder® series provides high-quality, single-chip record/playback solutions to 10- and 12-second messaging applications. The CMOS devices include an on-chip oscillator, microphone preamplifier, automatic gain control, antialiasing filter, smoothing filter, and speaker amplifier. A minimum Record/Playback subsystem can be configured with a microphone, a speaker, several passives, two push-buttons, and a power source.

Recordings are stored in on-chip nonvolatile memory cells, providing zero-power message storage. This unique, single-chip solution is made possible through ISD's patented multilevel storage technology. Voice and audio signals are stored directly into memory in their natural form, providing high-quality, solid-state voice reproduction.

Figure i: ISD1200 Series Block Diagram



FEATURES

- Easy-to-use single-chip voice record/playback solution
- High-quality, natural voice/audio reproduction
- Push-button interface
  - Playback can be edge- or level-activated
- Single-chip durations of 10 and 12 seconds
- Automatic power-down mode
  - Enters standby mode immediately following a record or playback cycle
  - Standby current 0.5 μA (typical)
- Zero-power message storage
  - Eliminates battery backup circuits
- Fully addressable to handle multiple messages
- 100-year message retention (typical)
- 100,000 record cycles (typical)
- On-chip clock source
- No programmer or development system needed
- Single +5 volt power supply
- Available in die form, DIP, and SOIC packaging

Table i: ISD1200 Series Summary

Part Number	Minimum Duration (Seconds)	Input Sample Rate (KHz)	Typical Filter Pass Band (KHz)
ISD1210	10	6.4	2.6
ISD1212	12	5.3	2.2

DETAILED DESCRIPTION

SPEECH/SOUND QUALITY

ISD's patented ChipCorder technology provides natural record and playback. The ISD1200 series includes devices offered at 5.3 and 6.4 KHz sampling frequencies allowing the user a choice of speech quality options. The input voice signals are stored directly in nonvolatile EEPROM cells, and reproduced without the synthetic effect often heard with digital solid-state speech solutions. A complete sample is stored in a single cell, minimizing the memory necessary to store a recording of a given duration.

DURATION

To meet end system requirements, the ISD1200 series offers single-chip solutions at 10 and 12 seconds.

EEPROM STORAGE

One of the benefits of ISD's ChipCorder technology is the use of on-chip nonvolatile memory, providing zero-power message storage. The message is retained for up to 100 years typically without power. In addition, the device can be re-recorded typically over 100,000 times.

BASIC OPERATION

The ISD1200 ChipCorder series devices are controlled by a single record signal, $\overline{REC}$, and either of two push-button control playback signals, $\overline{PLAYE}$ (edge-activated playback), and $\overline{PLAYL}$ (level-activated playback). The ISD1200 parts are configured for simplicity of design in a single-message application. Using the address lines will allow multiple message applications. Device operation is explained on page 4.

AUTOMATIC POWER-DOWN MODE

At the end of a playback or record cycle, the ISD1200 series devices automatically return to a low-power standby mode, consuming typically 0.5 μA. During a playback cycle, the device powers down automatically at the end of the message. During a record cycle, the device powers down immediately after $\overline{REC}$ is released HIGH.

ADDRESSING (OPTIONAL)

In addition to providing simple message playback, the ISD1200 series provides a full addressing capability.

The ISD1200 series storage array has 80 distinct addressable segments, providing the following resolutions. See Application Information in this book for ISD1200 address tables.

Table 1: Device Playback/Record Durations

Part Number	Minimum Duration (Seconds)
ISD1210	125 ms
ISD1212	150 ms

PIN DESCRIPTIONS

NOTE *The $\overline{REC}$ signal is denounced for 50 ms on the rising edge to prevent a false retriggering from a push-button switch.*

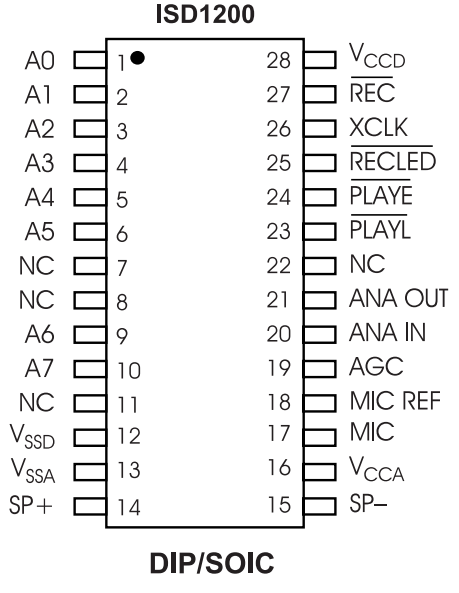
VOLTAGE INPUTS (V_{CCA}, V_{CCD})

Analog and digital circuits internal to the ISD1200 series use separate power buses to minimize noise on the chip. These power buses are brought out to separate pins on the package and should be tied together as close to the supply as possible. It is important that the power supply be decoupled as close as possible to the package.

GROUND INPUTS (V_{SSA}, V_{SSD})

Similar to V_{CCA} and V_{CCD}, the analog and digital circuits internal to the ISD1200 series use separate ground buses to minimize noise. These pins should be tied together as close as possible to the device.

Figure 1: ISD1200 Series Pinouts



NOTE: *NC means must Not Connect.*

RECORD ($\overline{REC}$)

The $\overline{REC}$ input is an active-LOW record signal. The device records whenever $\overline{REC}$ is LOW. This signal must remain LOW for the duration of the recording. $\overline{REC}$ takes precedence over either playback ($\overline{PLAYE}$ or $\overline{PLAYL}$) signal. If $\overline{REC}$ is pulled LOW during a playback cycle, the playback immediately ceases and recording begins. A record cycle is completed when $\overline{REC}$ is pulled HIGH or the memory space is filled.

An end-of-message marker (EOM) is internally recorded, enabling a subsequent playback cycle to terminate appropriately. The device automatically powers down to standby mode when $\overline{REC}$ goes HIGH.

PLAYBACK, EDGE-ACTIVATED ($\overline{PLAYE}$)

When a LOW-going transition is detected on this input signal, a playback cycle begins. Playback continues until an EOM marker is encountered or the end of the memory space is reached. Upon completion of the playback cycle, the device automatically powers down into standby mode. Taking $\overline{PLAYE}$ HIGH during a playback cycle will not terminate the current cycle.

PLAYBACK, LEVEL-ACTIVATED ($\overline{PLAYL}$)

When this input signal transitions from HIGH to LOW, a playback cycle is initiated. Playback continues until $\overline{PLAYL}$ is pulled HIGH, an EOM marker is detected, or the end of the memory space is reached. The device automatically powers down to standby mode upon completion of the playback cycle.

NOTE *In playback, if either $\overline{PLAYE}$ or $\overline{PLAYL}$ is held LOW during EOM or OVF, the device will still enter standby and the internal oscillator and timing generator will stop. However, the rising edge of $\overline{PLAYE}$ and $\overline{PLAYL}$ are not denounced and any subsequent falling edge (particularly switch bounce) present on the input pins will initiate another playback.*

RECORD LED OUTPUT ($\overline{\text{RECLED}}$)

The output $\overline{\text{RECLED}}$ is LOW during a record cycle. It can be used to drive an LED to provide feedback that a record cycle is in progress. In addition, $\overline{\text{RECLED}}$ pulses LOW momentarily when an EOM marker is encountered in a playback cycle.

MICROPHONE INPUT (MIC)

The microphone input transfers its signal to the on-chip preamplifier. An on-chip Automatic Gain Control (AGC) circuit controls the gain of this preamplifier from –15 to 24 dB. An external microphone should be AC coupled to this pin via a series capacitor. The capacitor value, together with the internal 10 KΩ resistance on this pin, determine the low-frequency cutoff for the ISD1200 series passband. See the ISD Application Information in this book for additional information on low-frequency cutoff calculations.

MICROPHONE REFERENCE (MIC REF)

The MIC REF input is the inverting input to the microphone preamplifier. This provides a noise-canceling or common-mode rejection input to the device when connected differentially to a microphone.

AUTOMATIC GAIN CONTROL (AGC)

The AGC dynamically adjusts the gain of the preamplifier to compensate for the wide range of microphone input levels. The AGC allows the full range of sound, from whispers to loud sounds, to be recorded with minimal distortion. The "attack" time is determined by the time constant of a 5 KΩ internal resistance and an external capacitor (C6 on the schematic in Figure 4) connected from the AGC pin to V_{SSA} analog ground. The "release" time is determined by the time constant of an external resistor (R5) and an external capacitor (C6) connected in parallel between the AGC Pin and V_{SSA} analog ground. Nominal values of 470 KΩ and 4.7 μF give satisfactory results in most cases.

ANALOG OUTPUT (ANA OUT)

This pin provides the preamplifier output to the user. The voltage gain of the preamplifier is determined by the voltage level at the AGC pin.

ANALOG INPUT (ANA IN)

The ANA IN pin transfers the input signal to the chip for recording. For microphone inputs, the ANA OUT pin should be connected via an external capacitor to the ANA IN pin. This capacitor value, together with the 3.0 KΩ input impedance of ANA IN, is selected to give additional cutoff at the low-frequency end of the voice passband. If the desired input is derived from a source other than a microphone, the signal can be fed, capacitively coupled, into the ANA IN pin directly.

EXTERNAL CLOCK INPUT (XCLK)

The external clock input for the ISD1200 devices has an internal pull-down device. The ISD1200 is configured at the factory with an internal sampling clock frequency that guarantees its minimum nominal record/playback time. For instance, an ISD1210 operating within specification will be observed to always have a minimum of 10 seconds of recording time. The sampling frequency is then maintained to a variation of ±2.25 percent over the commercial temperature and operating voltage ranges while still maintaining the minimum specified recording duration. This will result in some devices having a few percent more than nominal recording time. If greater precision is required, the device can be clocked through the XCLK pin as follows:

Table 2: External Clock Sample Rates

Part Number	Sample Rate	Required Clock
ISD1210	6.4 KHz	819.2 KHz
ISD1212	5.3 KHz	682.7 KHz

These recommended clock rates should not be varied because the antialiasing and smoothing filters are fixed, and aliasing problems can occur if the sample rate differs from the one recommended. The duty cycle on the input clock is not critical, as the clock is immediately divided by two internally. **If the XCLK is not used, this input should be connected to ground.**

SPEAKER OUTPUTS (SP+, SP–)

The SP+ and SP– pins provide direct drive for loudspeakers with impedances as low as 16 Ω. A single output may be used, but, for direct-drive loudspeakers, the two opposite-polarity outputs provide an improvement in output power of up to four times over a single-ended connection. Furthermore, when SP+ and SP– are used, a speaker-coupling capacitor is not required. A single-ended connection will require an AC-coupling capacitor between the SP pin and the speaker. The speaker outputs are in a high-impedance state during a record cycle, and held at V_{SSA} during power-down.

ADDRESS INPUTS (A0–A7)

The Address Inputs have two functions, depending upon the level of the two Most Significant Bits (MSB) of the address.

If either of the two MSBs is LOW, the inputs are all interpreted as address bits and are used as the start address for the current record or playback cycle. The address pins are inputs only and do not output internal address information as the operation progresses. Address inputs are latched by the falling edge of $\overline{\text{PLAYE}}$, $\overline{\text{PLAYL}}$, or $\overline{\text{REC}}$.

OPERATIONAL MODES

The ISD1200 series is designed with several built-in operational modes provided to allow maximum functionality with a minimum of additional components, described in detail below. The operational modes use the address pins on the ISD1200 devices, but are mapped outside the valid address range. When the two Most Significant Bits (MSBs) are HIGH (A6 and A7), the remaining address signals are interpreted as mode bits and not as address bits. Therefore, operational modes and direct addressing are not compatible and cannot be used simultaneously.

There are two important considerations for using operational modes. First, all operations begin initially at address 0, which is the beginning of the ISD1200 address space. Later operations can begin at other address locations, depending on the operational mode(s) chosen. In addition, the address pointer is reset to 0 when the device is changed from record to playback but not from playback to record when A4 is HIGH in Operational Mode.

Second, an Operational Mode is executed when any of the control inputs, $\overline{\text{PLAYE}}$, $\overline{\text{PLAYL}}$, or $\overline{\text{REC}}$, go LOW and the two MSBs are HIGH. This Operational Mode remains in effect until the next LOW-going control input signal, at which point the current address/mode levels are sampled and executed.

NOTE *The two MSBs are on pins 9 and 10 for each ISD1200 series device.*

OPERATIONAL MODES DESCRIPTION

The Operational Modes can be used in conjunction with a microcontroller, or they can be hard-wired to provide the desired system operation.

A0 — MESSAGE CUEING

Message Cueing allows the user to skip through messages, without knowing the actual physical addresses of each message. Each control input LOW pulse causes the internal address pointer to skip to the next message. This mode should be used for playback only, and is typically used with the A4 Operational Mode.

A1 — DELETE $\overline{\text{EOM}}$ MARKERS

The A1 Operational Mode allows sequentially recorded messages to be combined into a single message with only one EOM marker set at the end of the final message. When this operational mode is configured, messages recorded sequentially are played back as one continuous message.

A2 — UNUSED

A3 — MESSAGE LOOPING

The A3 Operational Mode allows for the automatic, continuously repeated playback of the message located at the beginning of the address space.

A message can completely fill the ISD1200 device and will loop from beginning to end. Pulsing $\overline{\text{PLAYE}}$ will start the playback and pulsing $\overline{\text{PLAYL}}$ will end the playback.

A4 — CONSECUTIVE ADDRESSING

During normal operations, the address pointer will reset when a message is played through to an EOM marker. The A4 Operational Mode inhibits the address pointer reset, allowing messages to be recorded or played back consecutively. When the device is in a static state; i.e., not recording or playing back, momentarily taking this pin LOW will reset the address counter to zero.

A5 — UNUSED

Table 3: Operational Modes Table

Address Crtl. (HIGH)	Function	Typical Use	Jointly Compatible*
A0	Message cueing	Fast-forward through messages	A4
A1	Delete EOM markers	Position EOM marker at the end of the last message	A3, A4
A2	Unused		
A3	Looping	Continuous playback from Address 0	A1
A4	Consecutive addressing	Record/play multiple consecutive messages	A0, A1
A5	Unused		

NOTE: *An asterisk (*) indicates additional operational modes that can be used simultaneously with the given mode.*

TIMING DIAGRAMS

Figure 2: Record

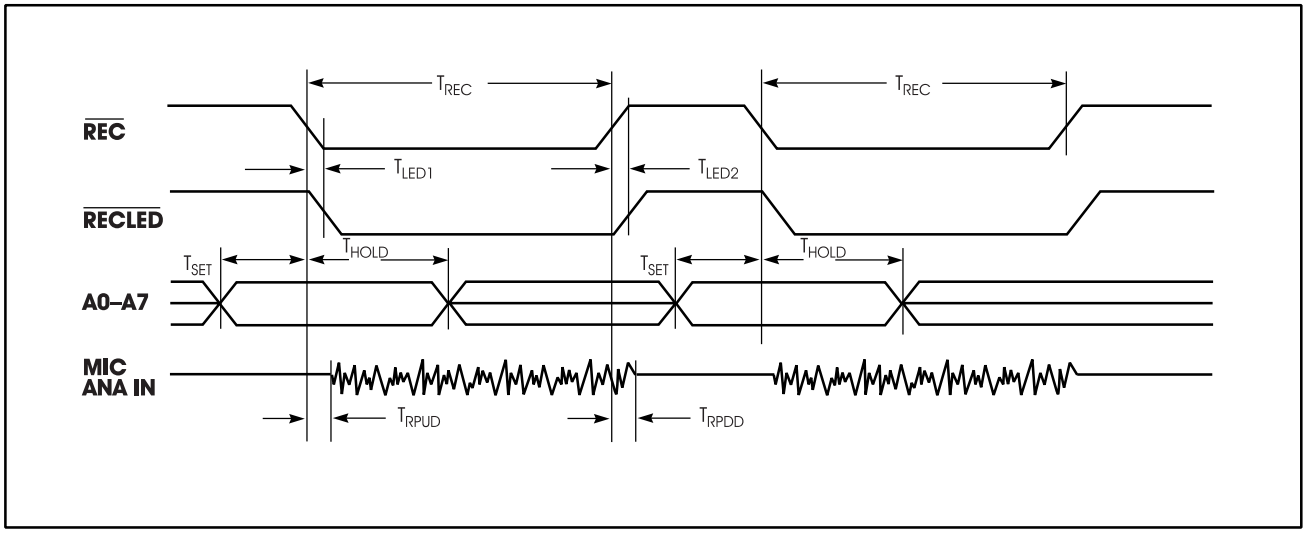
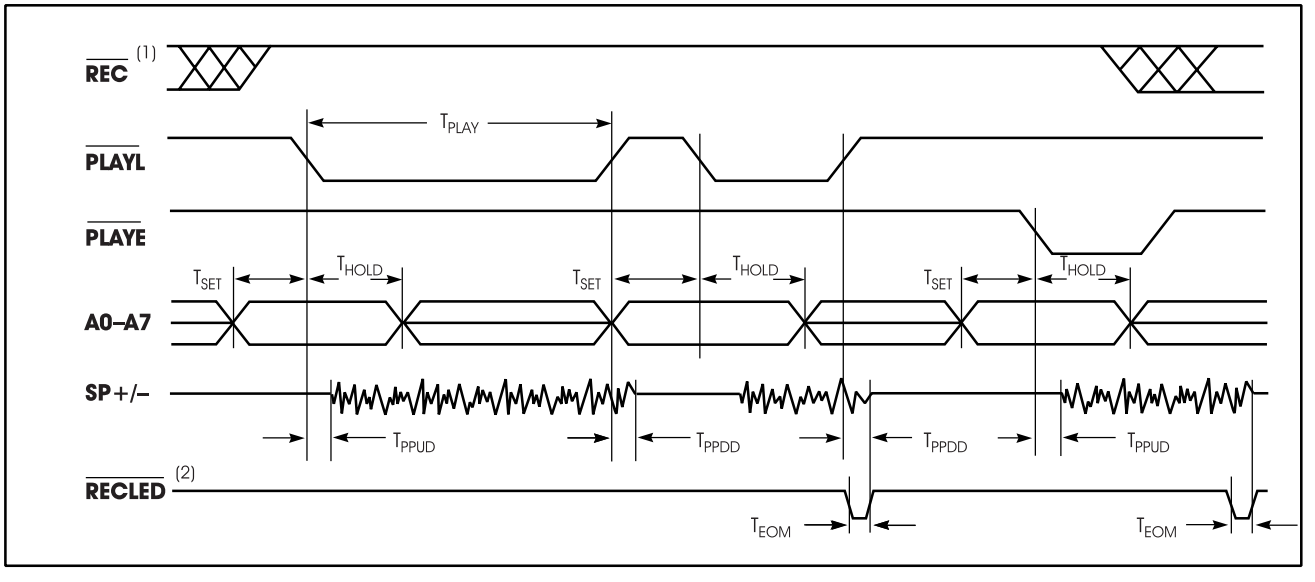


Figure 3: Playback



1. *$\overline{REC}$ must be HIGH for the entire duration of a playback cycle.*

2. *$\overline{RECLED}$ functions as an EOM during playback.*

Table 4: Absolute Maximum Ratings (Packaged Parts)[1]

Condition	Value
Junction temperature	150°C
Storage temperature range	–65°C to +150°C
Voltage applied to any pin	(V_{SS} – 0.3 V) to (V_{CC} + 0.3 V)
Voltage applied to any pin (Input current limited to ±20 mA)	(V_{SS} – 1.0 V) to (V_{CC} + 1.0 V)
Lead temperature (soldering – 10 seconds)	300°C
V_{CC} – V_{SS}	–0.3 V to +7.0 V

1. *Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability. Functional operation is not implied at these conditions.*

Table 5: Operating Conditions (Packaged Parts)

Condition	Value
Commercial operating temperature range[1]	0°C to +70°C
Supply voltage (V_{CC})[2]	+4.5 V to +5.5 V
Ground voltage (V_{SS})[3]	0 V

1. *Case temperature.*
2. $V_{CC} = V_{CCA} = V_{CCD}$.
3. $V_{SS} = V_{SSA} = V_{SSD}$.

Table 6: DC Parameters (Packaged Parts)

Symbol	Parameters	Min[2]	Typ [1]	Max[2]	Units	Conditions
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.4			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 4.0 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = –1.6 mA
I_{CC}	V_{CC} Current (Operating)		15	30	mA	V_{CC} = 5.5 V [3], R_{EXT} = ∞
I_{SB}	V_{CC} Current (Standby)		0.5	10	µA	[3] [4]
I_{IL}	Input Leakage Current			±1	µA	
I_{ILPD}	Input Current HIGH w/Pull Down			130	µA	Force V_{CC} [5]
R_{EXT}	Output Load Impedance	16			Ω	Speaker Load
R_{MIC}	Preamp In Input Resistance		10		KΩ	Pins 17, 18
$R_{ANA\ IN}$	ANA IN Input Resistance		3		KΩ	
A_{PRE1}	Preamp Gain 1		24		dB	AGC = 0.0 V
A_{PRE2}	Preamp Gain 2		–45	–15	dB	AGC = 2.5 V

Table 6: DC Parameters (Packaged Parts)

Symbol	Parameters	Min(2)	Typ (1)	Max(2)	Units	Conditions
A_{ARP}	ANA IN to SP+/– Gain		22		dB	
R_{AGC}	AGC Output Resistance		5		KΩ	
I_{PREH}	Preamp Out Source		–2		mA	@ V_{OUT} = 1.0 V
I_{PREL}	Preamp In Sink		0.5		mA	@ V_{OUT} = 2.0 V

1. *Typical values @ T_A = 25°C and 5.0 V.*
2. *All Min/Max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100 percent tested.*
3. *V_{CCA} and V_{CCD} connected together.*
4. *$\overline{REC}$, $\overline{PLAYL}$, and $\overline{PLAYE}$ must be at V_{CCD} .*
5. *Pin 26.*

Table 7: AC Parameters (Packaged Parts)

Symbol	Characteristic		Min(2)	Typ (1)	Max(2)	Units	Conditions
F_S	Sampling Frequency	ISD1210 ISD1212			6.4 5.3	KHz KHz	(5) (5)
F_{CF}	Filter Pass Band	ISD1210 ISD1212		2.6 2.2		KHz KHz	3 dB Roll-Off Point (3)(6) 3 dB Roll-Off Point (3)(6)
T_{REC}	Record Duration	ISD1210 ISD1212	10 12			sec sec	
T_{PLAY}	Playback Duration	ISD1210 ISD1212	10 12			sec sec	(5) (5)
T_{LED1}	$\overline{RECLED}$ ON Delay			5		msec	
T_{LED2}	$\overline{RECLED}$ OFF Delay	ISD1210 ISD1212	40 50	48.6 58.3	100 105	msec msec	
T_{SET}	Address Setup Time		300			nsec	
T_{HOLD}	Address Hold Time		0			nsec	
T_{RPUD}	Record Power-Up Delay	ISD1210 ISD1212		32 39		msec msec	
T_{RPDD}	Record Power-Down Delay	ISD1210 ISD1212		32 39		msec msec	
T_{PPUD}	Play Power-Up Delay	ISD1210 ISD1212		32 39		msec msec	

Table 7: AC Parameters (Packaged Parts)

Symbol	Characteristic		Min(2)	Typ (1)	Max(2)	Units	Conditions
T_{PPDD}	Play Power-Down Delay	ISD1210 ISD1212		8.1 9.7		msec msec	
T_{EOM}	EOM Pulse Width	ISD1210 ISD1212		15.625 18.75		msec msec	
THD	Total Harmonic Distortion			1		%	@ 1 KHz
P_{OUT}	Speaker Output Power			12.2		mW	R_{EXT} = 16 Ω
V_{OUT}	Voltage Across Speaker Pins			1.25	2.5	V p–p	R_{EXT} = 600 Ω
V_{IN1}	MIC Input Voltage				20	mV	Peak-to-Peak (4)
V_{IN2}	ANA IN Input Voltage				50	mV	Peak-to-Peak

1. *Typical values @ T_A = 25°C, 5.0 V, and 6.4 KHz sample rate.*
2. *All Min/Max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100 percent tested.*
3. *Low-frequency cutoff depends upon value of external capacitors (see Pin Descriptions).*
4. *With 5.1 KΩ series resistor at ANA IN.*
5. *Sampling frequency and playback duration will vary as much as ±2.25 percent over the commercial temperature and voltage ranges. All devices will meet the maximum sampling frequency and minimum playback duration parameters. For greater stability, an external clock can be utilized (see Pin Descriptions).*
6. *Filter specification applies to the antialiasing filter and to the smoothing filter.*

TYPICAL PARAMETER VARIATION WITH VOLTAGE AND TEMPERATURE (PACKAGED PARTS)

Chart 1: Record Mode Operating Current (I_{CC})

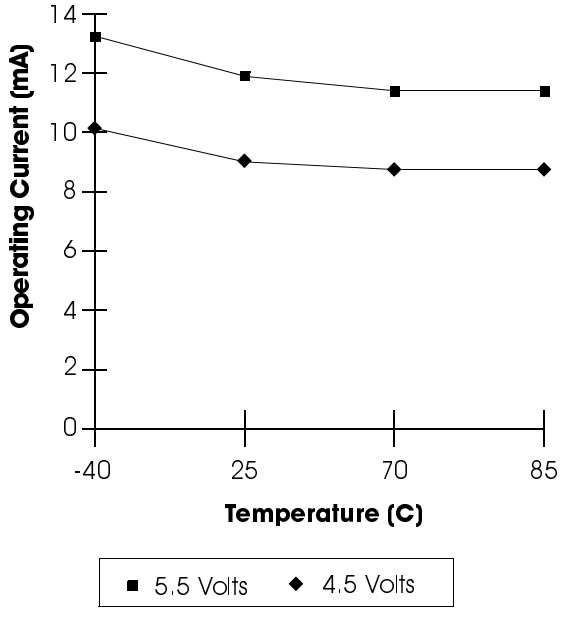


Chart 2: Total Harmonic Distortion

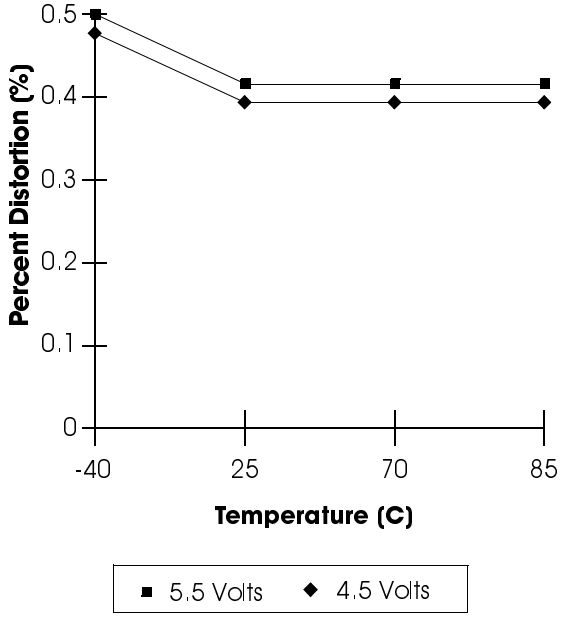


Chart 3: Standby Current (I_{SB})

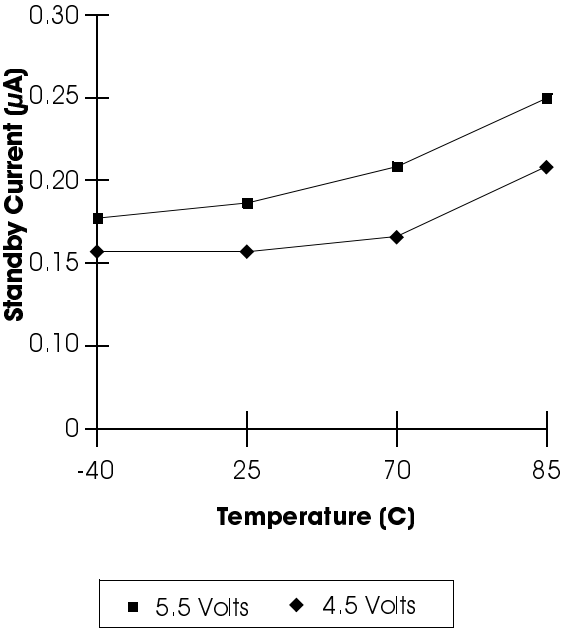


Chart 4: Oscillator Stability

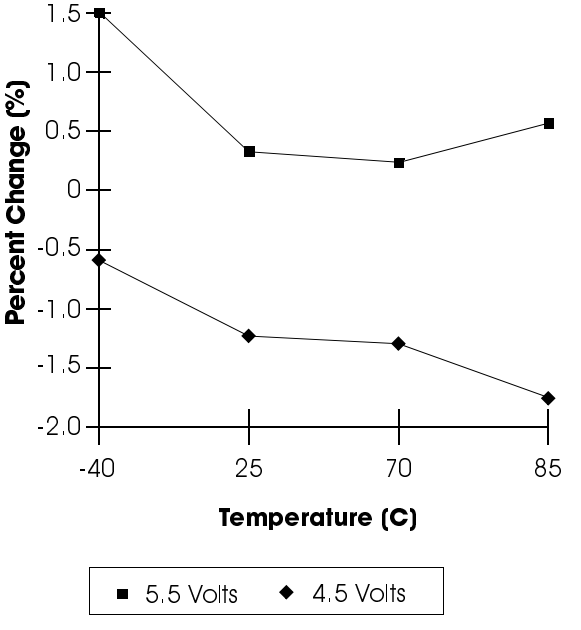


Table 8: Absolute Maximum Ratings (Die)[1]

Condition	Value
Junction temperature	150°C
Storage temperature range	–65°C to +150°C
Voltage applied to any pad	(V_{SS} – 0.3 V) to (V_{CC} + 0.3 V)
Voltage applied to any pad (Input current limited to ±20 mA)	(V_{SS} – 1.0 V) to (V_{CC} + 1.0 V)
V_{CC} – V_{SS}	–0.3 V to +7.0 V

1. *Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability. Functional operation is not implied at these conditions.*

Table 9: Operating Conditions (Die)

Condition	Value
Commercial operating temperature range	0°C to +50°C
Supply voltage (V_{CC})[1]	+4.5 V to +6.5 V
Ground voltage (V_{SS})[2]	0 V

1. $V_{CC} = V_{CCA} = V_{CCD}$.
2. $V_{SS} = V_{SSA} = V_{SSD}$.

Table 10: DC Parameters (Die)

Symbol	Parameters	Min[2]	Typ [1]	Max[2]	Units	Conditions
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.4			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 4.0 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = – 1.6 mA
I_{CC}	V_{CC} Current (Operating)		15	30	mA	V_{CC} = 5.5 V [3], R_{EXT} = ∞
I_{SB}	V_{CC} Current (Standby)		0.5	10	µA	[3] [4]
I_{IL}	Input Leakage Current			±1	µA	
I_{ILPD}	Input Current HIGH w/Pull Down			130	µA	Force V_{CC} [5]
R_{EXT}	Output Load Impedance	16			Ω	Speaker Load
R_{MIC}	Preamp In Input Resistance		10		KΩ	Pins 17, 18
$R_{ANA\ IN}$	ANA IN Input Resistance		3		KΩ	
A_{PRE1}	Preamp Gain 1		24		dB	AGC = 0.0 V
A_{PRE2}	Preamp Gain 2		–45	–15	dB	AGC = 2.5 V

Table 10: DC Parameters (Die)

Symbol	Parameters	Min(2)	Typ (1)	Max(2)	Units	Conditions
A_{ARP}	ANA IN to SP+/– Gain		22		dB	
R_{AGC}	AGC Output Resistance		5		KΩ	
I_{PREH}	Preamp Out Source		–2		mA	@ V_{OUT} = 1.0 V
I_{PREL}	Preamp In Sink		0.5		mA	@ V_{OUT} = 2.0 V

1. *Typical values @ T_A = 25°C and 5.0 V.*
2. *All Min/Max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100 percent tested.*
3. *V_{CCA} and V_{CCD} connected together.*
4. *$\overline{REC}$, $\overline{PLAYL}$, and $\overline{PLAYE}$ must be at V_{CCD} .*
5. *Pin 26.*

Table 11: AC Parameters (Die)

Symbol	Characteristic		Min(2)	Typ (1)	Max(2)	Units	Conditions
F_S	Sampling Frequency	ISD1210 ISD1212			6.4 5.3	KHz KHz	(5) (5)
F_{CF}	Filter Pass Band	ISD1210 ISD1212		2.6 2.2		KHz KHz	3 dB Roll-Off Point (3)(6) 3 dB Roll-Off Point (3)(6)
T_{REC}	Record Duration	ISD1210 ISD1212	10 12			sec sec	
T_{PLAY}	Playback Duration	ISD1210 ISD1212	10 12			sec sec	(5) (5)
T_{LED1}	$\overline{RECLED}$ ON Delay			5		msec	
T_{LED2}	$\overline{RECLED}$ OFF Delay	ISD1210 ISD1212	40 50	48.6 58.3	100 105	msec msec	
T_{SET}	Address Setup Time		300			nsec	
T_{HOLD}	Address Hold Time		0			nsec	
T_{RPUD}	Record Power-Up Delay	ISD1210 ISD1212		32 39		msec msec	
T_{RPDD}	Record Power-Down Delay	ISD1210 ISD1212		32 39		msec msec	
T_{PPUD}	Play Power-Up Delay	ISD1210 ISD1212		32 39		msec msec	
T_{PPDD}	Play Power-Down Delay	ISD1210 ISD1212		8.1 9.7		msec msec	

Table 11: AC Parameters (Die)

Symbol	Characteristic	Min(2)	Typ (1)	Max(2)	Units	Conditions
T_{EOM}	EOM Pulse Width ISD1210 ISD1212		15.625 18.75		msec msec	
THD	Total Harmonic Distortion		1		%	@ 1 KHz
P_{OUT}	Speaker Output Power		12.2		mW	R_{EXT} = 16 Ω
V_{OUT}	Voltage Across Speaker Pins		1.25	2.5	V p-p	R_{EXT} = 600 Ω
V_{IN1}	MIC Input Voltage			20	mV	Peak-to-Peak (4)
V_{IN2}	ANA IN Input Voltage			50	mV	Peak-to-Peak

1. *Typical values @ T_A = 25°C, 5.0 V, and 6.4 KHz sample rate.*
2. *All Min/Max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100 percent tested.*
3. *Low-frequency cutoff depends upon value of external capacitors (see Pin Descriptions).*
4. *With 5.1 KΩ series resistor at ANA IN.*
5. *Sampling frequency and playback duration will vary as much as ±2.25 percent over the commercial temperature and voltage ranges. All devices will meet the maximum sampling frequency and minimum playback duration parameters. For greater stability, an external clock can be utilized (see Pin Descriptions).*
6. *Filter specification applies to the antialiasing filter and to the smoothing filter.*

TYPICAL PARAMETER VARIATION WITH VOLTAGE AND TEMPERATURE (DIE)

Chart 5: Record Mode Operating Current (I_{CC})

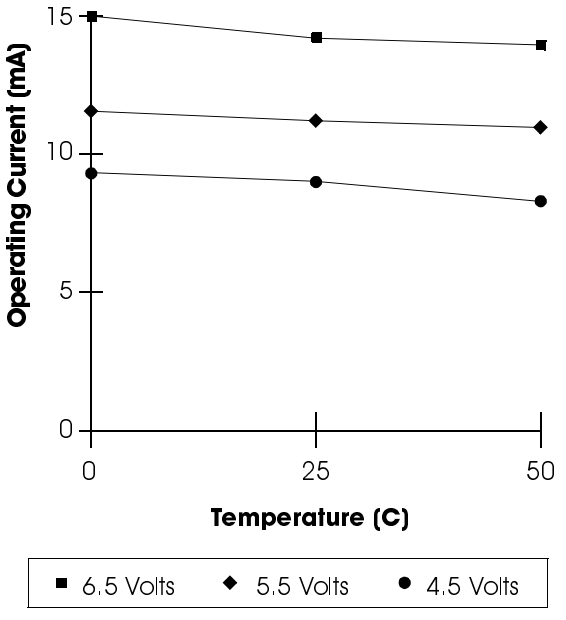


Chart 6: Total Harmonic Distortion

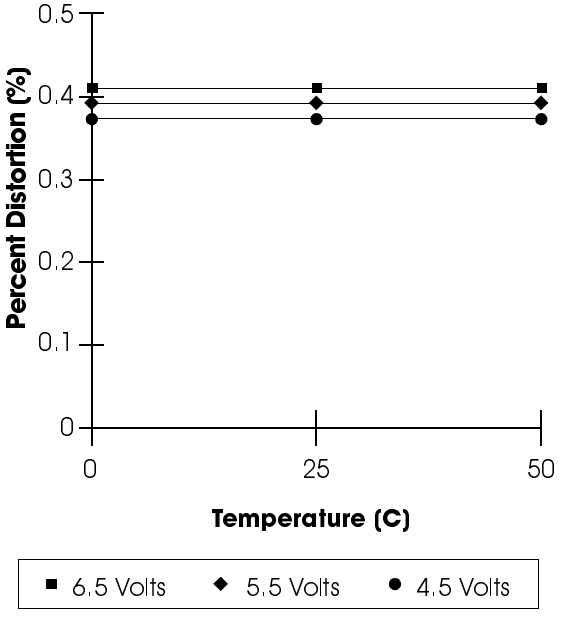


Chart 7: Standby Current (I_{SB})

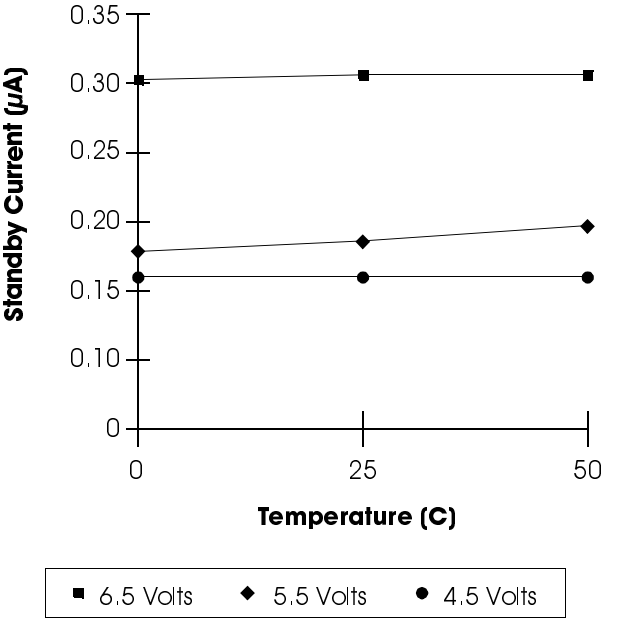


Chart 8: Oscillator Stability

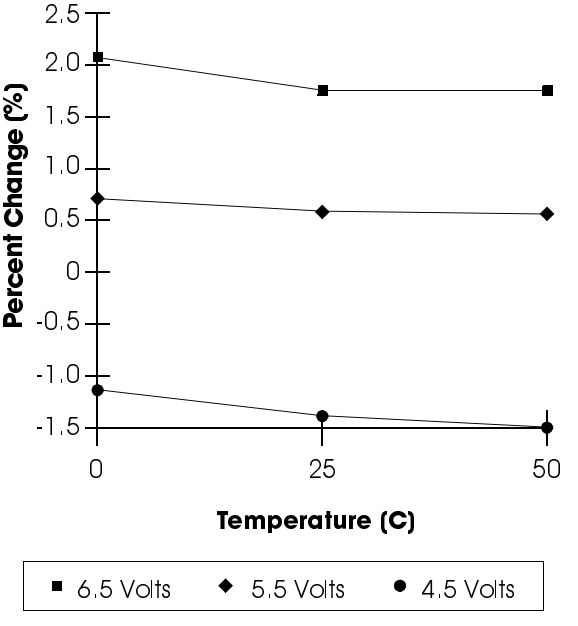
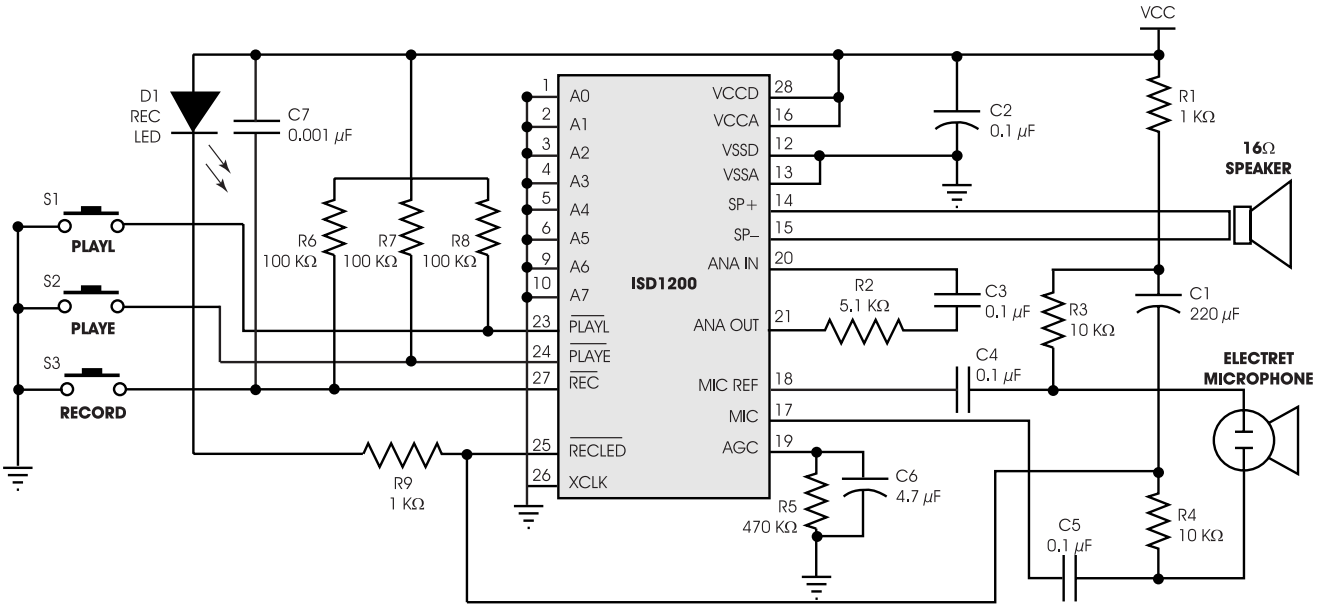


Figure 4: Application Example



FUNCTIONAL DESCRIPTION EXAMPLE

The following example operating sequence demonstrates the functionality of the ISD1200 series devices.

1. Record a message filling the address space.

   Pulling the $\overline{\text{REC}}$ signal LOW initiates a record cycle from the beginning of the message space. If $\overline{\text{REC}}$ is held LOW, the recording continues until the message space has been filled. Once the message space is filled, recording ceases. The device will automatically power down after $\overline{\text{REC}}$ is pulled HIGH.

2. Edge-activated playback.

   Pulling the $\overline{\text{PLAYE}}$ signal LOW initiates a playback cycle from the beginning of the message space or at a selected location. The rising edge of $\overline{\text{PLAYE}}$ has no effect on operation. If a recording has filled the message space, the entire message is played. When the device reaches the EOM marker, it automatically powers down. A subsequent falling edge on $\overline{\text{PLAYE}}$ initiates a new play cycle from the start address.

3. Level-activated playback.

   Pulling the $\overline{\text{PLAYL}}$ signal LOW initiates a playback cycle from the beginning of the message space or a selected location. If recording has filled the message space, the entire message is played. When the device reaches the EOM marker, it automatically powers down. A subsequent falling edge on $\overline{\text{PLAYL}}$ initiates a new play cycle from the starting address.

4. Level-activated playback (truncated).

   If $\overline{\text{PLAYL}}$ is pulled HIGH any time during the playback cycle, the device stops playing and enters the power-down mode. A subsequent falling edge on $\overline{\text{PLAYL}}$ initiates a new play cycle from the start address.

5. Record (interrupting playback).

   The $\overline{REC}$ signal takes precedence over other operations. Any LOW-going transition on $\overline{REC}$ initiates a new record operation from the beginning of the start address or at a selected location, regardless of any current operation in progress.

6. Record a message, partially filling the address space.

   A record operation need not fill the entire message space. Releasing the $\overline{REC}$ signal HIGH before filling the message space causes the recording to stop and an EOM to be placed. The device powers down automatically.

7. Play back a message, partially filling the address space.

   Pulling the $\overline{PLAYE}$ or $\overline{PLAYL}$ signal LOW initiates a playback cycle which is then completed when the EOM marker is encountered. Playback ceases and the device powers down.

8. $\overline{RECLED}$ operation.

   The $\overline{RECLED}$ output pin provides an active-LOW signal which can be used to drive an LED as a "record-in-progress" indicator. It returns to a HIGH state when the $\overline{REC}$ pin is released HIGH or when the recording is completed due to the message space being filled. This pin also pulses LOW to indicate an EOM at the end of a message being played.

APPLICATIONS NOTE

Some users may experience an unexpected recording taking place when their circuit is powered up, or the batteries are changed and V_{CC} rises faster than $\overline{REC}$. This undesired recording prevents playback of the previously recorded message. A spurious End Of Message (EOM) marker appears at the very beginning of the memory, preventing access to the original message, and nothing is played.

To prevent this occurrence, place a capacitor (approx. 0.001 μF) between the control pin ($\overline{REC}$) and V_{CC}. This pulls the control pin voltage up with V_{CC} as it rises. Once the voltage is HIGH, the pull-up device will keep the pin HIGH until intentionally pulled LOW, preventing the false EOM marker.

Since this anomaly depends on factors such as the capacitance of the user's printed circuit board, not all circuit designs will exhibit the spurious marker. However, it is recommended that the capacitor is included for design reliability. A more detailed explanation and resolution of this occurrence is described in Application Information.

ISD1200 SERIES PHYSICAL DIMENSIONS

Figure 5: 28-Lead 0.600-Inch Plastic Dual Inline Package (PDIP) (P)

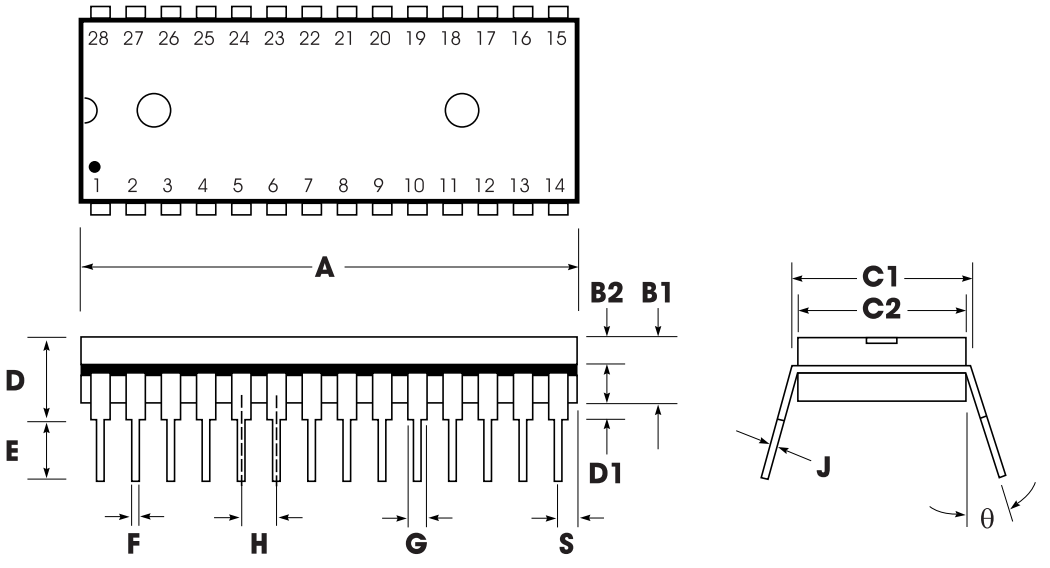


Table 12: Plastic Dual Inline Package (PDIP) (P) Dimensions

	INCHES			MILLIMETERS		
	Min	Nom	Max	Min	Nom	Max
A	1.445	1.450	1.455	36.70	36.83	36.96
B1		0.150			3.81	
B2	0.065	0.070	0.075	1.65	1.78	1.91
C1	0.600		0.625	15.24		15.88
C2	0.530	0.540	0.550	13.46	13.72	13.97
D			0.19			4.83
D1	0.015			0.38		
E	0.125		0.135	3.18		3.43
F	0.015	0.018	0.022	0.38	0.46	0.56
G	0.055	0.060	0.065	1.40	1.52	1.65
H		0.100			2.54	
J	0.008	0.010	0.012	0.20	0.25	0.30
S	0.070	0.075	0.080	1.78	1.91	2.03
q	0°		15°	0°		15°

NOTE: *Lead coplanarity to be within 0.005 inches.*

Figure 6: 28-Lead 0.300-Inch Plastic Small Outline Integrated Circuit (SOIC) (S)

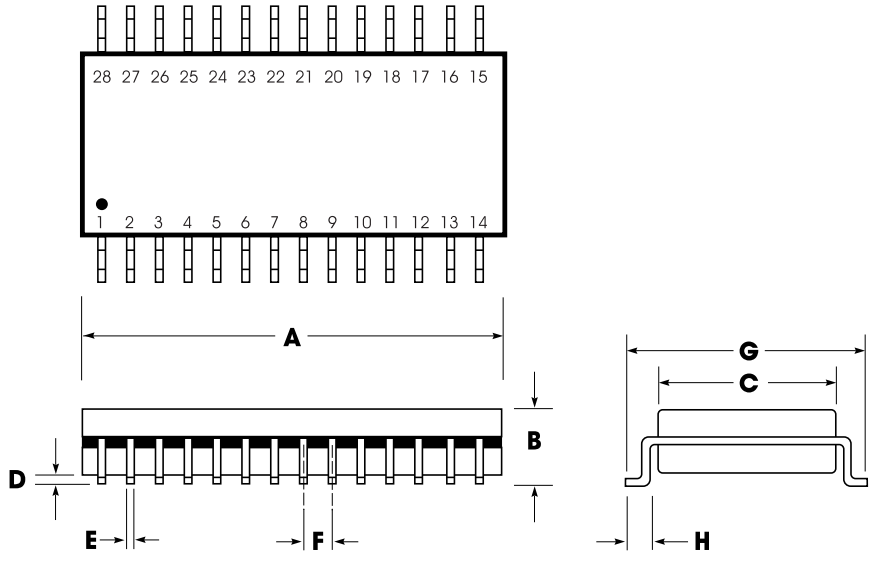


Table 13: Plastic Small Outline Integrated Circuit (SOIC) (S) Dimensions

	INCHES			MILLIMETERS		
	Min	Nom	Max	Min	Nom	Max
A	0.701	0.706	0.711	17.81	17.93	18.06
B	0.097	0.101	0.104	2.46	2.56	2.64
C	0.292	0.296	0.299	7.42	7.52	7.59
D	0.005	0.009	0.0115	0.127	0.22	0.29
E	0.014	0.016	0.019	0.35	0.41	0.48
F		0.050			1.27	
G	0.400	0.406	0.410	10.16	10.31	10.41
H	0.024	0.032	0.040	0.61	0.81	1.02

NOTE: *Lead coplanarity to be within 0.004 inches.*

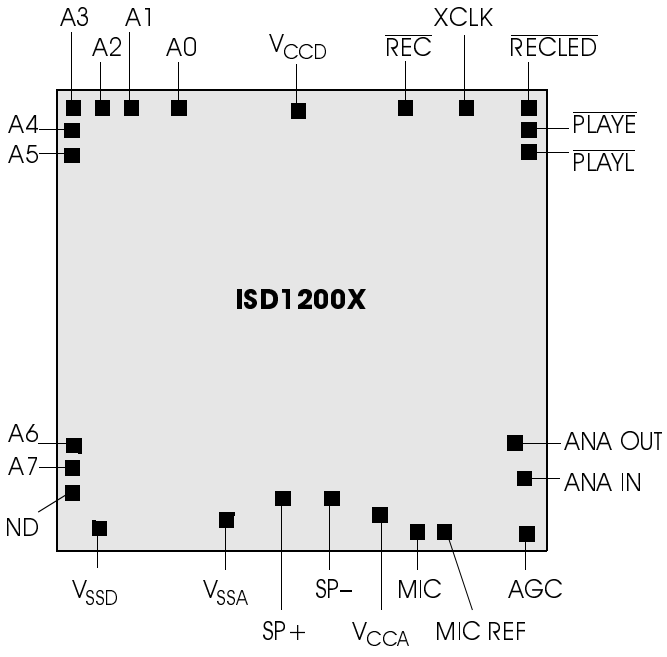
Figure 7: ISD1200 Series Bonding Physical Layout[1]

ISD1200X

I. Die Dimensions
X: 172.2 ±1 mils
Y: 138.2 ±1 mils

II. Die Thickness[2]
17.5 ±1 mils

III. Pad Opening
88 x 112 microns
3.46 x 4.41 mils



1. *The backside of die is internally connected to V_{SS}. It **MUST NOT** be connected to any other potential or damage may occur.*
2. *Die thickness is subject to change please contact ISD factory for status.*

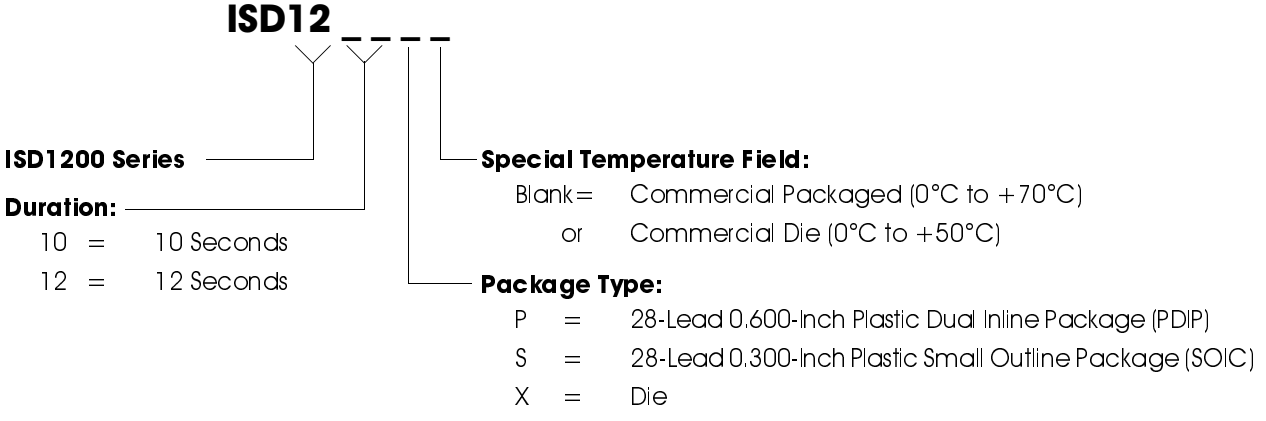
Table 14: ISD1200 Series PIN/PAD Designations, with Respect to Die Center (µm)

Pin	Pin Name	X Axis	Y Axis
A0	Address 0	–1364.0	1589.6
A1	Address 1	–1648.4	1589.6
A2	Address 2	–1816.4	1589.6
A3	Address 3	–2013.6	1515.6
A4	Address 4	–2013.6	1337.6
A5	Address 5	–2013.6	1129.6
A6	Address 6	–2013.6	–831.2
A7	Address 7	–2013.6	–1022.0
NC	No Connect	–2013.6	–1361.6
V_{SSD}	V_{SS} Digital Power Supply	–1893.6	–1588.0
V_{SSA}	V_{SS} Analog Power Supply	–357.6	–1588.0
SP+	Speaker Output +	–17.2	–1512.8
SP–	Speaker Output –	412.4	–1512.8
V_{CCA}	V_{CC} Analog Power Supply	780.0	–1552.4
MIC	Microphone Input	992.0	–1590.0
MIC REF	Microphone Reference	1169.2	–1590.0
AGC	Automatic Gain Control	1978.4	–1590.0
ANA IN	Analog Input	2005.6	–1196.4
ANA OUT	Analog Output	1991.2	–995.2
$\overline{\text{PLAYL}}$	Level-Activated Playback	2014.4	1224.4
$\overline{\text{PLAYE}}$	Edge-Activated Playback	2014.4	1392.8
$\overline{\text{RECLED}}$	Record LED Output	2012.4	1587.6
XCLK	No Connect (optional)	1581.2	1589.6
$\overline{\text{REC}}$	Record	752.8	1589.6
V_{CCD}	V_{CC} Digital Power Supply	–48.0	1545.2

NOTE: *Die dimensions and pin/pad positions may be subject to change. Please contact ISD Sales Offices or Representatives to verify current or future specifications.*

ORDERING INFORMATION

Product Number Descriptor Key



When ordering ISD1200 series devices, please refer to the following valid part numbers.

Part Number	Part Number
ISD1210P	ISD1212P
ISD1210S	ISD1212S
ISD1210X	ISD1212X

For the latest product information, access ISD's worldwide website at http://www.isd.com.