ChipCorder®
TECHNOLOGY BY ISD

ISD1000A Series

Single-Chip Voice Record/Playback Devices
16- and 20-Second Durations

GENERAL DESCRIPTION

Information Storage Devices' ISD1000A ChipCorder® Series provides high-quality, single-chip record/playback solutions for 16- and 20-second messaging applications. The CMOS devices include an on-chip oscillator, microphone preamplifier, automatic gain control, antialiasing filter, smoothing filter, and speaker amplifier. In addition, the ISD1000A Series is fully microprocessor-compatible, allowing complex messaging and addressing to be achieved.

Recordings are stored in on-chip nonvolatile memory cells, providing zero-power message storage. This unique, single-chip solution is made possible through ISD's patented multilevel storage technology. Voice and audio signals are stored directly into memory in their natural form, providing high-quality, solid-state voice reproduction.

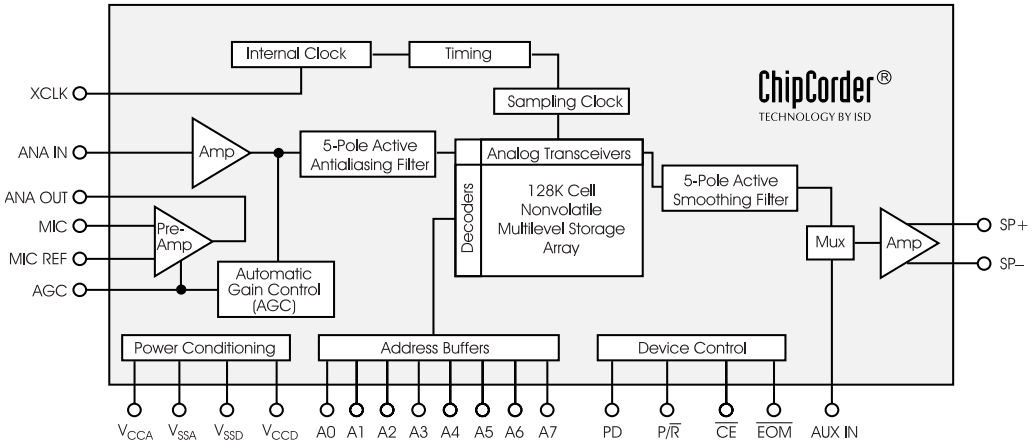
FEATURES

- Easy-to-use single-chip voice Record/ Playback solution
- High-quality, natural voice/audio reproduction
- Manual switch or microcontroller compatible
  - Playback can be edge- or level-activated
- Single-chip durations of 16 and 20 seconds
- Directly cascadable for longer durations
- Power-down mode
  - 1 μA standby current (typical)
- Zero-power message storage
  - Eliminates battery backup circuits
- Fully addressable to handle multiple messages
- 100-year message retention (typical)
- 100K record cycles (typical)
- On-chip clock source
- On-chip Automatic Gain Control (AGC)
- Single +5 volt supply
- Available in die form, DIP, and SOIC packaging
- Industrial temperature (–40°C to +85°C) version available

Table 2-1: ISD1000A Series Summary

Part Number	Duration (Seconds)	Input Sample Rate (KHz)	Typical Filter Pass Band (KHz)
ISD1016A	16	8	3.4
ISD1020A	20	6.4	2.7

Figure 2-1: ISD1000A Series Block Diagram

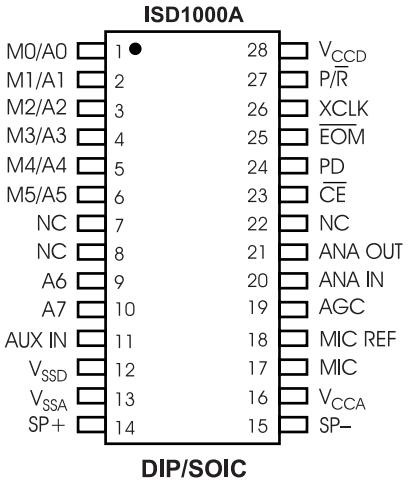


2 DETAILED DESCRIPTION

The ISD1000A ChipCorder Series devices are designed to record and play back audio and voice information in a single chip with a minimum of circuit complexity. This compact, easy-to-use, nonvolatile, low-power solution has been made possible by ISD's multilevel storage technology—a breakthrough in storage technology in EEPROM. ISD's multilevel storage technology results in a density that is eight times greater than digital memory. The ISD1000A nonvolatile analog array consists of 128K cells—the equivalent of 1 Mbit of digital storage.

The ISD1000A Series eliminates the need for digital conversion, digital compression, and voice synthesis techniques which often compromise voice quality and are more complicated to use. The ISD1000A Series includes signal conditioning circuits and control functions which enable a complete, high-quality recording and playback system in a single device. The ISD1000A is available in two versions which store voice in 16- or 20-second arrays. Additional devices may be cascaded to achieve longer recording durations. The nonvolatile storage array is based on production-proven, low-power CMOS EEPROM technology.

Figure 2-2: ISD1000A Series Pinouts



The highly integrated ISD1000A Series contains all the basic functions required for high-quality voice recording and playback. The noise-cancelling Microphone Preamplifier and Automatic Gain Control (AGC) record both low-volume and high-

volume sounds. The AGC attack and release times are adjusted by an external resistor and capacitor. Antialiasing is performed by a continuous fifth-order Chebyshev filter, requiring no external components or clocks to give toll-quality reproduction. The low corner of the passband is user-settable by two external capacitors. The devices contain their own temperature-stabilized timebase oscillator.

The ISD1000A devices drive a speaker directly through differential outputs. This boosts power by four times and eliminates the need for a series capacitor or an output amplifier. The device will operate from a single power supply or from batteries. The device also includes a power down function for applications where minimum power consumption is critical. The CMOS-based design, combined with the nonvolatile storage array, assures the lowest possible overall power consumption.

On-chip control functions make the ISD1000A Series easy to use in a wide array of applications. Each device offers a variety of operating modes and interface options. The devices may be used in applications that require little more than a few switches and a battery. The devices may also be integrated into electronic systems where digital addresses can be provided for more sophisticated message addressing and control. The ISD1000A array is organized into 160 segments. Addresses A0 through A7 provide access to each segment in the array for message addressing. Addressing provides the capability of constructing messages by combining stored phrases and sounds.

PIN DESCRIPTIONS

Voltage Inputs (V_{CCA}, V_{CCD})

To minimize noise, the analog and digital circuits in the ISD1000A Series devices use separate power busses. These voltage busses are brought out to separate pins and should be tied together as close to the supply as possible. In addition, these supplies should be decoupled as close to the package as possible.

Ground Inputs (V_{SSA}, V_{SSD})

The ISD1000A Series of devices utilizes separate analog and digital ground busses. These pins should be tied together as close to the package as possible and connected through a low-impedance path to power supply ground. The backside of the die is connected to V_{SS} through the substrate resistance. In a chip-on-board design the die attach area must be connected to V_{SS} or left floating.

Power Down Input (PD)

When not recording or playing back, the PD pin should be pulled HIGH to place the part in an extremely low power mode (see I_{SB} specification). When $\overline{EOM}$ pulses LOW for an overflow condition, PD should be brought HIGH to reset the address pointer back to the beginning of the Record/Playback space.

Chip Enable Input ($\overline{CE}$)

The $\overline{CE}$ pin is taken LOW to enable all playback and record operations. The address inputs and Playback/Record input (P/$\overline{R}$) are latched by the falling edge of $\overline{CE}$. When $\overline{CE}$ is taken HIGH, the ISD1000A is unselected, the P/$\overline{R}$ is HIGH, and the auxiliary input is directed into the speaker amplifier.

Playback/Record Input (P/$\overline{R}$)

The P/$\overline{R}$ input is latched by the falling edge of the $\overline{CE}$ pin. A HIGH level selects a playback cycle while a LOW level selects a record cycle. For a record cycle, the address inputs provide the starting address and recording continues until PD or $\overline{CE}$ is pulled HIGH or an overflow is detected (i.e. the chip is full). When a Record cycle is terminated by pulling PD or $\overline{CE}$ HIGH, an End-Of-Message (EOM) marker is stored at the current address in memory. For a playback cycle, the address inputs provide the starting address and the device will play until an EOM marker is encountered. The device can continue past an EOM marker in an operational mode, or if $\overline{CE}$ is held LOW in address mode. (See "Operational Modes" on page 2-5).

End-Of-Message Output ($\overline{EOM}$)

A nonvolatile marker is automatically inserted at the end of each recorded message. It remains there until the message is recorded over. During playback, the $\overline{EOM}$ output pulses LOW for a period of T_{EOM} at the end of each message or in the event of a message overflow (device full).

In addition, the ISD1000A Series has an internal V_{CC} detect circuit to maintain message integrity should V_{CC} fall below 3.5V. In this case, $\overline{EOM}$ goes LOW and the device is fixed in playback-only mode. The EOM marker provides a convenient handshake signal for a processor and also facilitates the cascading of devices.

Microphone Input (MIC)

The microphone input transfers its signal to the on-chip preamplifier. An on-chip Automatic Gain Control (AGC) circuit controls the gain of this preamplifier from –15 to 24 dB. An external microphone should be AC coupled to this pin via a series capacitor. The capacitor value, together with the internal 10 Kohm resistance on this pin, determines the low-frequency cutoff for the ISD1000A Series passband. See ISD Application Information, Chapter 5, for additional information on low-frequency cutoff calculation.

Microphone Reference Input (MIC REF)

The MIC REF input is the inverting input to the microphone preamplifier. This provides a noise-canceling or common-mode rejection input to the device when connected to a differential microphone. ***If this input is unused, it must be left disconnected.***

Automatic Gain Control Input (AGC)

The AGC dynamically adjusts the gain of the preamplifier to compensate for the wide range of microphone input levels. The AGC allows the full range, from whispers to loud sounds, to be recorded with minimal distortion. The "attack" time is determined by the time constant of a 5 KΩ internal resistance and an external capacitor (C2) connected from the AGC pin to V_{SSA} analog ground. The "release" time is determined by the time constant of an external resistor (R2) and an external capacitor (C2 on the schematic on page 2-16) connected in parallel between the AGC Pin and V_{SSA} analog ground. Nominal values of 470 KΩ and 4.7 μF give satisfactory results, in most cases. For AGC voltages of 1.5V and below, the preamplifier is at its maximum gain of 24 dB. Reduction in preamplifier gain occurs for voltages of approximately 1.8V.

Analog Output (ANA OUT)

This pin provides the preamplifier output to the user. The voltage gain of the preamplifier is determined by the voltage level at the AGC pin. It has a maximum gain of about 24 dB for small input signal levels.

Analog Input (ANA IN)

The analog input pin transfers its signal to the chip for recording. For microphone inputs, the ANA OUT pin should be connected via an external capacitor to the ANA IN pin. This capacitor value, together with the 2.7 KΩ input impedance of ANA IN, is selected to give additional cutoff at the low-frequency end of the voice passband. If the desired input is derived from a source other than a microphone, the signal can be fed, capacitively coupled, into the ANA IN pin directly.

Optional External Clock Input (XCLK)

ISD1000A devices are configured at the factory with an internal sampling clock frequency centered to ±1% of specification. The frequency is maintained to a total variation of ±2.25% tolerance over the entire commercial temperature and 4.5 to 5.5 voltage ranges. The internal clock has a ±5% tolerance over the industrial temperature range and 4.5 to 5.5 voltage range. A regulated power supply is recommended for industrial-temperature-range parts. If greater precision is required, the device can be clocked through the XCLK pin as follows.

Table 2-2: External Clock Sample Rates

Part Number	Sample Rate	Required Clock
ISD1016A	8.0 KHz	1024 KHz
ISD1020A	6.4 KHz	819.2 KHz

These recommended clock rates should not be varied because the antialiasing and smoothing filters are fixed, and aliasing problems can occur if the sample rate differs from the one recommended. The duty cycle on the input clock is not critical, as the clock is immediately divided by two. ***If the XCLK is not used, this input must be connected to ground.***

Speaker Outputs (SP+/SP–)

All devices in the ISD1000A Series include an on-chip differential speaker driver, capable of driving 50 milliwatts into 16 Ω from AUX IN (12.2 mW from memory).

The speaker outputs are held at V_{SSA} levels during record and power down. It is therefore not possible to parallel speaker outputs of multiple ISD1000A devices or the outputs of other speaker drivers.

NOTE *Connection of speaker outputs in parallel may cause damage to the device.*

While a single output may be used alone (including a coupling capacitor between the SP pin and the speaker), these outputs may also be used individually with the output signal taken from either pin. Using the differential outputs results in a 4:1 improvement in output power.

NOTE *Never ground or drive an output.*

Auxiliary Input (AUX IN)

The Auxiliary Input is multiplexed through to the output amplifier and speaker output pins when $\overline{CE}$ is HIGH and Playback has ended, or if the device is in overflow. When cascading multiple ISD1000A devices, the AUX IN pin is used to connect a Playback signal from a following device to the previous output speaker drivers. For noise consideration, it is suggested that the Auxiliary Input not be driven when the storage array is active.

Address/Mode Inputs (Ax/Mx)

The Address/Mode Inputs provide two functions in the ISD1000A Series: 1. Message address (either A6 or A7 = LOW) and 2. ISD1000A Series Operational Mode Options (A6 and A7 = HIGH).

Operational mode options are shown in the Operational Modes table. There are a maximum of 160 message addresses (or segments). Each segment corresponds to one of 160 rows in the analog storage array. The message addresses (segments) are in locations 0 through 159 contiguous. The playback/record duration of each segment depends upon the device and is as follows:

Table 2-3: Device Playback/Record Durations

Part Number	Segment Playback/Record Duration
ISD1016A	100 milliseconds
ISD1020A	125 milliseconds

An operation may be started at any address, as defined by address pins A0-A7. Record or playback continues with automatic incrementing of the internal on-chip address until either $\overline{CE}$ is brought HIGH (Record), an end of message marker is encountered (Playback with $\overline{CE}$ HIGH), or an overflow (device full) condition results.

OPERATIONAL MODES

The ISD1000A Series is designed with several built-in operational modes provided to allow maximum functionality with a minimum of additional components, described in detail below. The operational modes use the address pins on the ISD1000A devices, but are mapped outside the valid address range. When the two Most Significant Bits (MSBs) are HIGH (A6 = A7=1), the remaining address signals are interpreted as mode bits and **not** as address bits. Therefore, operational modes and direct addressing are not compatible and cannot be used simultaneously.

There are two important considerations for using operational modes. First, all operations begin initially at address 0, which is the beginning of the ISD1000A address space. Later operations can begin at other address locations, depending on the operational mode(s) chosen. In addition, the address pointer is reset to 0 when the device is changed from Record to Playback, or when a Power-Down cycle is executed.

Second, an Operational Mode is executed when $\overline{CE}$ goes LOW and the two MSBs are HIGH. This Operational Mode remains in effect until the next LOW-going $\overline{CE}$ signal, at which point the current address/mode levels are sampled and executed.

NOTE *The two MSBs are on pins 9 and 10 for each ISD1000A Series member.*

Table 2-4: Operational Modes

Control Mode	Function	Typical Use	Jointly Compatible[1]
M0	Message cueing	Fast-forward through messages	M4, M5
M1	Delete EOM markers	Position EOM marker at the end of the last message	M3, M4, M5
M2	Cascading	Adding devices to extend message	
M3	Looping	Continuous playback from Address 0	M1, M5
M4	Consecutive addressing	Record/Play multiple consecutive messages	M0, M1, M5
M5	$\overline{CE}$ level-activated	Allow message pausing	M0, M1, M3, M4

1. *Indicates additional operational modes which can be used simultaneously with the given mode.*

OPERATIONAL MODES DESCRIPTION

The Operational Modes can be used in conjunction with a microcontroller, or they can be hardwired to provide the desired system operation.

M0 — Message Cueing

Message Cueing allows the user to skip through messages, without knowing the actual physical addresses of each message. Each $\overline{CE}$ LOW pulse causes the internal address pointer to skip to the next message. This mode should be used for Playback only, and is typically used with the M4 Operational Mode.

M1 — Delete EOM Markers

The M1 Operational Mode allows sequentially recorded messages to be combined into a single message with only one EOM marker set at the end of the combined message. When this operational mode is configured, messages recorded sequentially are played back as one continuous message.

M2 — Used for Cascading

During playback, $\overline{EOM}$ goes LOW at array overflow only. Normal EOM pulses are turned off.

M3 — Message Looping

The M3 Operational Mode allows for the automatic, continuously repeated playback of the message located at the beginning of the address space. A message **cannot** completely fill the ISD1000A device and loop.

M4 — Consecutive Addressing

During normal operations, the address pointer will reset when a message is played through to an EOM marker. The M4 Operational Mode inhibits the address pointer reset on EOM, allowing messages to be played back consecutively.

M5 — $\overline{CE}$ Level Activated

The default mode for ISD1000A devices is for $\overline{CE}$ to be edge-activated on Playback and level-activated on Record. The M5 Operational Mode causes the $\overline{CE}$ pin to be interpreted as level-activated as opposed to edge-activated during Playback. This is specifically useful for terminating Playback operations using the $\overline{CE}$ signal. In this mode, $\overline{CE}$ LOW begins a Playback cycle at the beginning of device memory.

TIMING DIAGRAMS

Figure 2-3: Record

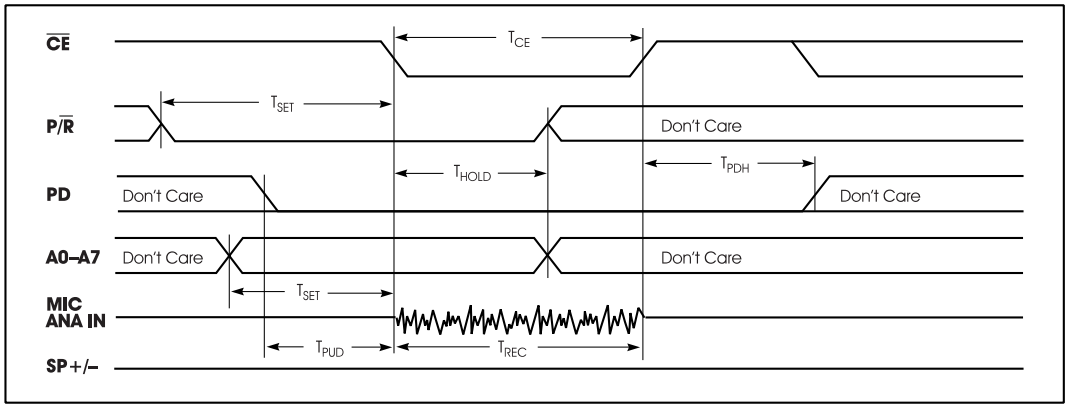


Figure 2-4: Playback

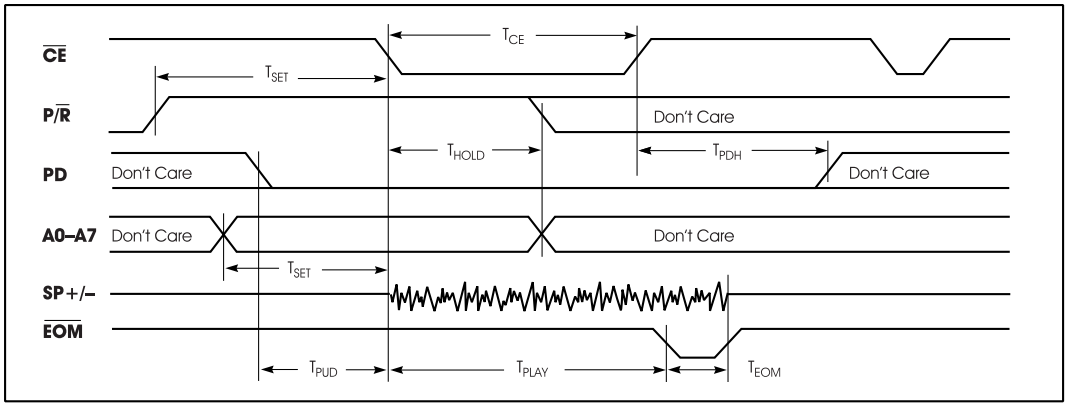


Table 2-5: Absolute Maximum Ratings (Packaged Parts)[1]

Condition	Value
Junction temperature	150°C
Storage temperature range	–65°C to +150°C
Voltage applied to any pin	(V_{SS} – 0.3 V) to (V_{CC} + 0.3 V)
Voltage applied to any pin (Input current limited to ±20 mA)	(V_{SS} – 1.0 V) to (V_{CC} + 1.0 V)
Lead temperature (soldering – 10 seconds)	300°C
$V_{CC} - V_{SS}$	– 0.3 V to +7.0 V

1. *Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability. Functional operation is not implied at these conditions.*

Table 2-6: Operating Conditions (Packaged Parts)

Condition	Value
Commercial operating temperature range[1]	0°C to +70°C
Industrial operating temperature[1]	–40°C to +85°C
Supply voltage (V_{CC})[2]	+4.5 V to +5.5 V
Ground voltage (V_{SS})[3]	0 V

1. *Case temperature.*
2. *$V_{CC} = V_{CCA} = V_{CCD}$.*
3. *$V_{SS} = V_{SSA} = V_{SSD}$.*

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Table 2-7: DC Parameters (Packaged Parts)

Symbol	Parameters	Min[2]	Typ [1]	Max[2]	Units	Conditions
V_{IL}	Input Low Voltage			0.8	V	V_{CC} = 4.5 V to 5.5 V
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 4.0 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = –1.6 mA, V_{CC} = 4.5 V to 5.5 V
V_{OH1}	Output High Voltage	V_{CC} – 0.4			V	I_{OH} = – 10 µA
I_{CC}	V_{CC} Current (Operating)		25	30	mA	$R_{EXT} = \infty$[3]
I_{SB}	V_{CC} Current (Standby)		1	10	µA	[3]
I_{IL}	Input Leakage Current			±1	µA	
R_{EXT}	Output Load Impedance	16			Ω	Speaker Load
R_{MIC}	Preamp In Input Resistance		10		KΩ	Pins 17, 18
R_{AUX}	AUX Input Resistance		10		KΩ	V_{CC} = 4.5 V to 5.5 V
$R_{ANA\ IN}$	ANA IN Input Resistance		3.0		KΩ	
A_{PRE1}	Preamp Gain 1		24		dB	AGC = 0.0 V, V_{CC} = 4.5 V to 5.5 V

Table 2-7: DC Parameters (Packaged Parts)

Symbol	Parameters	Min[2]	Typ [1]	Max[2]	Units	Conditions
A_{PRE2}	Preamp Gain 2		–45	15	dB	AGC = 2.5 V
A_{AUX}	AUX IN/ SP+ Gain	0.9			V/V	V_{CC} = 4.5 V to 5.5 V
A_{ARP}	ANA IN to SP+/- Gain		22		dB	
R_{AGC}	AGC Output Resistance		5		KΩ	
I_{PREH}	Preamp Out Source		–1		mA	@ V_{OUT} = 1.0 V, V_{CC} = 4.5 V to 5.5 V
I_{PREL}	Preamp In Sink		0.8		mA	@ V_{OUT} = 2.0 V, V_{CC} = 4.5 V to 5.5 V

1. *Typical values @ T_A = 25°C and 5.0 V.*

2. *All Min/Max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100% tested.*

3. *V_{CCA} and V_{CCD} connected together.*

Table 2-8: AC Parameters (Packaged Parts)

Symbol	Characteristic		Min[2]	Typ[1]	Max[2]	Units	Conditions
F_S	Internal Clock Sampling Frequency	ISD1016A ISD1020A		8 6.4		KHz KHz	[9] [9]
F_{CF}	Filter Pass Band	ISD1016A ISD1020A		3.4 2.7		KHz KHz	3 dB Roll-Off Point[3,10] 3 dB Roll-Off Point[3,10]
T_{REC}	Record Duration	ISD1016A ISD1020A		16 20		sec sec	
T_{PLAY}	Playback Duration	ISD1016A ISD1020A		16 20		sec sec	[9] [9]
T_{CE}	CE Pulse Width	ISD1016A ISD1020A	100 100			nsec nsec	
T_{SET}	Control/Address Setup Time	ISD1016A ISD1020A	300 300			nsec nsec	
T_{HOLD}	Control/Address Hold Time	ISD1016A ISD1020A	0 0			nsec nsec	
T_{PUD}	Power-Up Delay	ISD1016A ISD1020A	18.7 5 31.2 5			msec msec	
T_{PDR}	PD Pulse Width—Record	ISD1016A ISD1020A		25 31.25		msec msec	[6] [6]

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Table 2-8: AC Parameters (Packaged Parts)

Symbol	Characteristic		Min[2]	Typ[1]	Max[2]	Units	Conditions
T_{PDP}	PD Pulse Width—Play	ISD1016A ISD1020A		12.5 15.62 5		msec msec	[7] [7]
T_{PDS}	PD Pulse Width—Static	ISD1016A ISD1020A		100 100		nsec nsec	[8] [8]
T_{PDH}	Power Down Hold	ISD1016A ISD1020A	0 0			nsec nsec	
T_{EOM}	EOM Pulse Width	ISD1016A ISD1020A		12.5 15.6		msec msec	
THD	Total Harmonic Distortion	ISD1016A ISD1020A		1 1		% %	@ 1 KHz @ 1 KHz
P_{OUT}	Speaker Output Power	ISD1016A ISD1020A		12.5 12.5	50 50	mW mW	R_{EXT} = 16 Ω[4] R_{EXT} = 16 Ω[4]
V_{OUT}	Voltage Across Speaker Pins	ISD1016A ISD1020A			2.5 2.5	V p–p V p–p	R_{EXT} = 600 Ω R_{EXT} = 600 Ω
V_{IN1}	MIC Input Voltage	ISD1016A ISD1020A			20 20	mV mV	Peak-to-Peak[5] Peak-to-Peak[5]
V_{IN2}	ANA IN Input Voltage	ISD1016A ISD1020A			50 50	mV mV	Peak-to-Peak Peak-to-Peak
V_{IN3}	AUX IN Input Voltage	ISD1016A ISD1020A			1.25 1.25	V p–p V p–p	R_{EXT} = 16 Ω R_{EXT} = 16 Ω

2

1. *Typical values @ T_A = 25°C and 5.0 V.*

2. *All Min/Max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100% tested.*

3. *Low-frequency cutoff depends upon value of external capacitors (see Pin Descriptions).*

4. *From AUX IN; if ANA IN is driven at 50 mV p-p, the POUT= 12.2 mW, typical.*

5. *With 5.1 KΩ series resistor at ANA IN.*

6. *This is the minimum pulse width required to guarantee that a Record cycle will be interrupted. A LOW-going PD pulse of less than this interval during Record may be ignored.*

7. *This is the minimum pulse width required to guarantee that a Playback cycle will be interrupted. A LOW-going PD pulse of less than this interval during Playback may be ignored.*

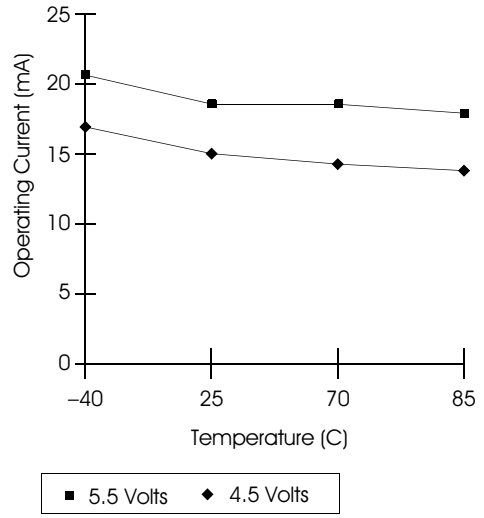
8. *This is the minimum pulse width required to reset the device when in a static condition; i.e., not actively recording or playing back.*

9. *Sampling Frequency and Playback Duration will vary as much as ±2.25% over the commercial temperature and voltage range and ±5% over the industrial temperature and voltage range. For greater stability, an external clock can be utilized (see Pin Descriptions).*

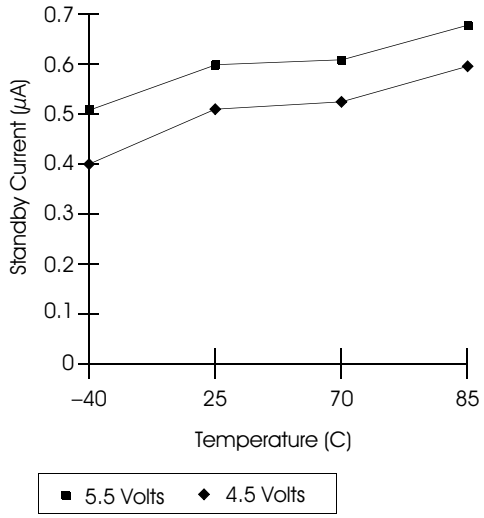
10. *Filter specification applies to the antialiasing filter and to the smoothing filter.*

TYPICAL PARAMETER VARIATION WITH VOLTAGE AND TEMPERATURE (PACKAGED PARTS)

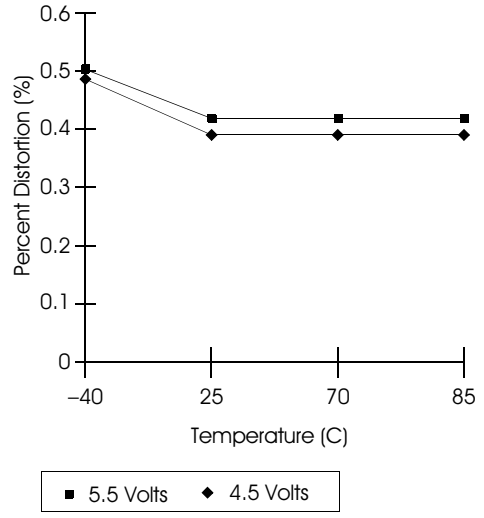
Graph 2-1: Record Mode Operating Current (I_{CC})



Graph 2-3: Standby Current (I_{SB})



Graph 2-2: Total Harmonic Distortion



Graph 2-4: Oscillator Stability

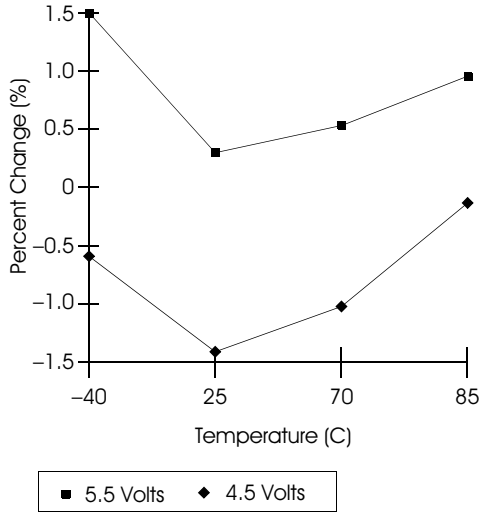


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Table 2-9: Absolute Maximum Ratings (Die)[1]

Condition	Value
Junction temperature	150°C
Storage temperature range	–65°C to +150°C
Voltage applied to any pad	(V_{SS} – 0.3 V) to (V_{CC} + 0.3 V)
Voltage applied to any pad (Input current limited to ±20 mA)	(V_{SS} – 1.0 V) to (V_{CC} + 1.0 V)
$V_{CC} - V_{SS}$	– 0.3 V to +7.0 V

1. *Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability. Functional operation is not implied at these conditions.*

Table 2-10: Operating Conditions (Die)

Condition	Value
Commercial operating temperature range [1]	0°C to +50°C
Supply voltage (V_{CC})[2]	+4.5 V to +6.5 V
Ground voltage (V_{SS})[3]	0 V

1. *Case temperature.*
2. *$V_{CC} = V_{CCA} = V_{CCD}$.*
3. *$V_{SS} = V_{SSA} = V_{SSD}$.*

2

Table 2-11: DC Parameters (Die)

Symbol	Parameters	Min[2]	Typ[1]	Max[2]	Units	Conditions
V_{IL}	Input Low Voltage			0.8	V	V_{CC} = 4.5 V to 5.5 V
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 4.0 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = –1.6 mA, V_{CC} = 4.5 V to 5.5 V
V_{OH1}	Output High Voltage	V_{CC} – 0.4			V	I_{OH} = –10 µA
I_{CC}	V_{CC} Current (Operating)		25	30	mA	$R_{EXT} = \infty$[3]
I_{SB}	V_{CC} Current (Standby)		1	10	µA	[3]
I_{IL}	Input Leakage Current			±1	µA	
R_{EXT}	Output Load Impedance	16			Ω	Speaker Load
R_{MIC}	Preamp In Input Resistance		10		KΩ	Pins 17, 18
R_{AUX}	AUX Input Resistance		10		KΩ	V_{CC} = 4.5 V to 5.5 V
$R_{ANA\ IN}$	ANA IN Input Resistance		3.0		KΩ	
A_{PRE1}	Preamp Gain 1		24		dB	AGC = 0.0 V, V_{CC} = 4.5 V to 5.5 V
A_{PRE2}	Preamp Gain 2		–45	15	dB	AGC = 2.5 V
A_{AUX}	AUX IN/ SP+ Gain	0.9			V/V	V_{CC} = 4.5 V to 5.5 V

Table 2-11: DC Parameters (Die)

Symbol	Parameters	Min[2]	Typ[1]	Max[2]	Units	Conditions
A_{ARP}	ANA IN to SP+/– Gain		22		dB	
R_{AGC}	AGC Output Resistance		5		KΩ	
I_{PREH}	Preamp Out Source		–1		mA	@ V_{OUT} = 1.0 V, V_{CC} = 4.5 V to 5.5 V
I_{PREL}	Preamp In Sink		0.8		mA	@ V_{OUT} = 2.0 V, V_{CC} = 4.5 V to 5.5 V

1. *Typical values @ T_A = 25°C and 5.0 V.*

2. *All Min/Max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100% tested.*

3. *V_{CCA} and V_{CCD} connected together.*

Table 2-12: AC Parameters (Die)

Symbol	Characteristic		Min[2]	Typ [1]	Max[2]	Units	Conditions
F_S	Internal Clock Sampling Frequency	ISD1016A ISD1020A		8 6.4		KHz KHz	9 9
F_{CF}	Filter Pass Band	ISD1016A ISD1020A		3.4 2.7		KHz KHz	3 dB Roll-Off Point[3,10] 3 dB Roll-Off Point[3,10]
T_{REC}	Record Duration	ISD1016A ISD1020A		16 20		sec sec	
T_{PLAY}	Playback Duration	ISD1016A ISD1020A		16 20		sec sec	9 9
T_{CE}	CE Pulse Width	ISD1016A ISD1020A	100 100			nsec nsec	
T_{SET}	Control/Address Setup Time	ISD1016A ISD1020A	300 300			nsec nsec	
T_{HOLD}	Control/Address Hold Time	ISD1016A ISD1020A	0 0			nsec nsec	
T_{PUD}	Power-Up Delay	ISD1016A ISD1020A	18.7 5 31.2 5			msec msec	
T_{PDR}	PD Pulse Width - Record	ISD1016A ISD1020A		25 31.25		msec msec	6 6
T_{PDP}	PD Pulse Width - Play	ISD1016A ISD1020A		12.5 15.625		msec msec	7 7

Table 2-12: AC Parameters (Die)

Symbol	Characteristic		Min[2]	Typ [1]	Max[2]	Units	Conditions
T_{PDS}	PD Pulse Width - Static	ISD1016A ISD1020A		100 100		nsec nsec	[8] [8]
T_{PDH}	Power Down Hold	ISD1016A ISD1020A	0 0			nsec nsec	
T_{EOM}	EOM Pulse Width	ISD1016A ISD1020A		12.5 15.6		msec msec	
THD	Total Harmonic Distortion	ISD1016A ISD1020A		1 1		% %	@ 1 KHz @ 1 KHz
P_{OUT}	Speaker Output Power	ISD1016A ISD1020A		12.5 12.5	50 50	mW mW	R_{EXT} = 16 Ω[4] R_{EXT} = 16 Ω[4]
V_{OUT}	Voltage Across Speaker Pins	ISD1016A ISD1020A			2.5 2.5	V p–p V p–p	R_{EXT} = 600 Ω R_{EXT} = 600 Ω
V_{IN1}	MIC Input Voltage	ISD1016A ISD1020A			20 20	mV mV	Peak-to-Peak[5] Peak-to-Peak[5]
V_{IN2}	ANA IN Input Voltage	ISD1016A ISD1020A			50 50	mV mV	Peak-to-Peak Peak-to-Peak
V_{IN3}	AUX IN Input Voltage	ISD1016A ISD1020A			1.25 1.25	V p–p V p–p	R_{EXT} = 16 Ω R_{EXT} = 16 Ω

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1. *Typical values @ T_A = 25°C and 5.0 V.*

2. *All Min/Max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100% tested.*

3. *Low-frequency cutoff depends upon value of external capacitors (see Pin Descriptions).*

4. *From AUX IN; if ANA IN is driven at 50 mV p-p, the POUT= 12.2 mW, typical.*

5. *With 5.1 KΩ series resistor at ANA IN.*

6. *This is the minimum pulse width required to guarantee that a Record cycle will be interrupted. A LOW-going PD pulse of less than this interval during Record may be ignored.*

7. *This is the minimum pulse width required to guarantee that a Playback cycle will be interrupted. A LOW-going PD pulse of less than this interval during Playback may be ignored.*

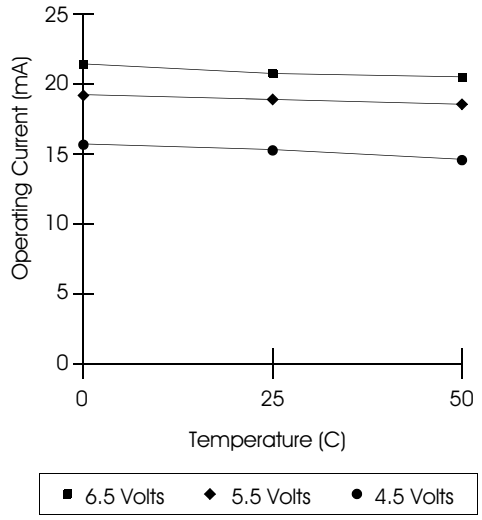
8. *This is the minimum pulse width required to reset the device when in a static condition; i.e., not actively recording or playing back.*

9. *Sampling frequency and Playback duration will vary as much as ±2.25% over the commercial temperature and voltage range. For greater stability, an external clock can be utilized (see Pin Descriptions).*

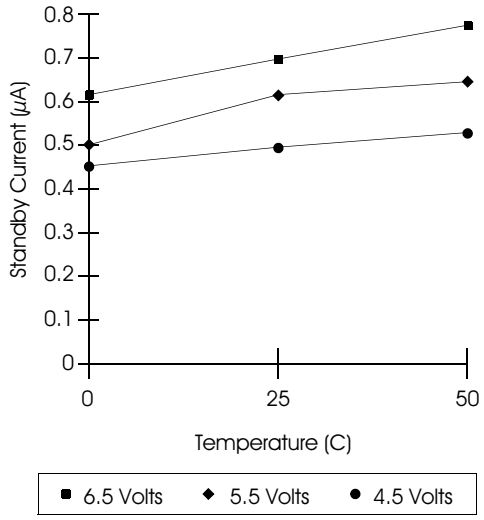
10. *Filter specification applies to the antialiasing filter and to the smoothing filter.*

TYPICAL PARAMETER VARIATION WITH VOLTAGE AND TEMPERATURE (DIE)

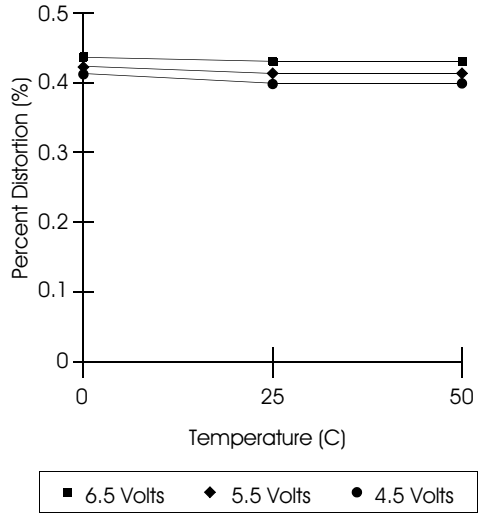
Graph 2-5: Record Mode Operating Current (I_{CC})



Graph 2-7: Standby Current (I_{SB})



Graph 2-6: Total Harmonic Distortion



Graph 2-8: Oscillator Stability

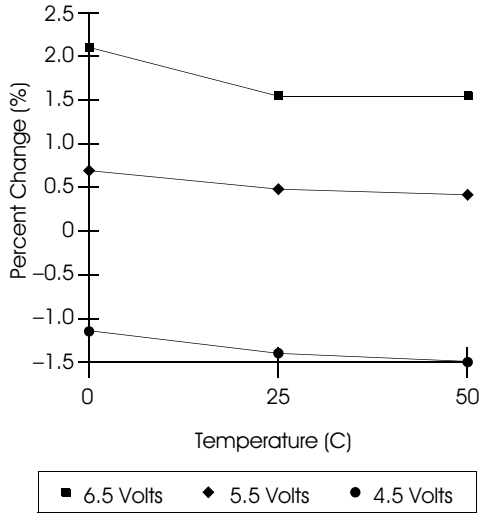


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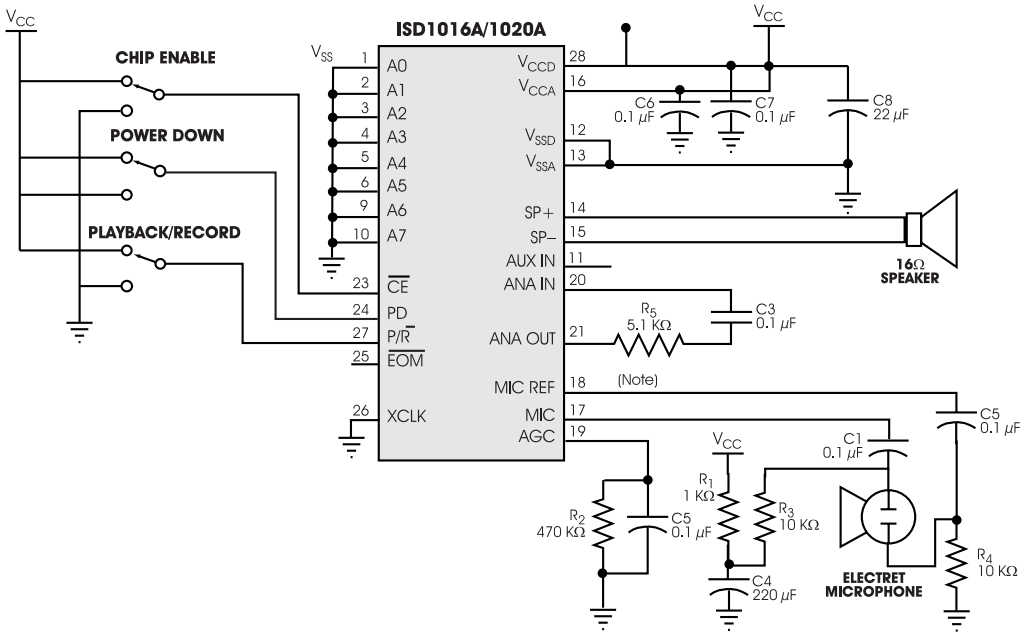
Figure 2-5: Application Example—Design Schematic



NOTE: *If desired, pin 18 may be left unconnected (microphone preamplifier noise will be higher). In this case, pin 18 must not be tied to any other signal or voltage. Additional design example schematics are provided in Chapter 5, "Application Information."*

Table 2-13: Application Example—Basic Device Control

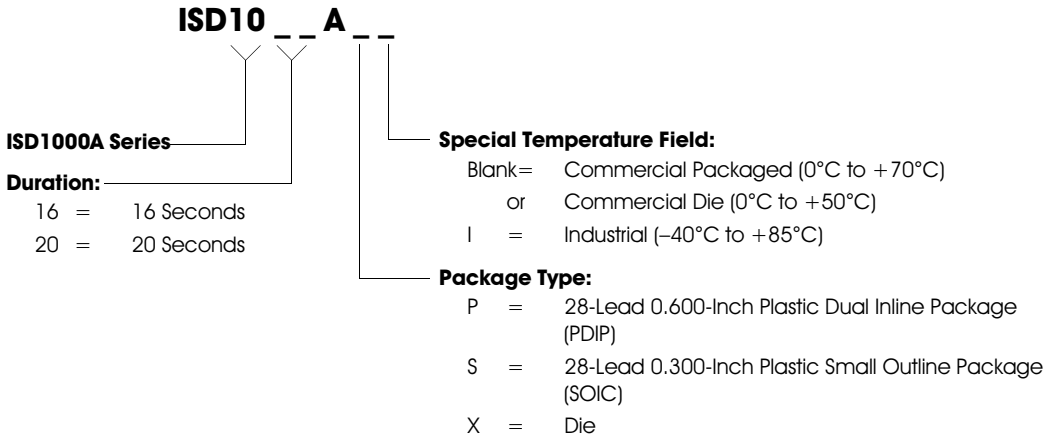
Control Step	Function	Action
1	Power up chip and select record/playback mode	1. PD = LOW 2. P/$\overline{R}$ = As desired
2	Set message address for record/playback	Set addresses A0–A7
3	Begin playback/record	$\overline{CE}$ = Pulsed LOW (Playback) $\overline{CE}$ = Held LOW (Record)
4	End cycle	$\overline{CE}$ = HIGH and EOM reached

Table 2-14: Application Example—Passive Component Functions

Part	Function	Comments
R1	Microphone power supply decoupling	Reduces power supply noise
R2	Release time constant	Sets release time for AGC
R3, R4	Microphone biasing resistors	Provides biasing for microphone operation
R5	Series limiting resistor	Reduces level at high supply voltages
C1, C5	Microphone DC–blocking capacitor Low-frequency cutoff	Decouples microphone bias from chip. Provides single-pole low-frequency cutoff and common-mode noise rejection
C2	Attack/Release time constant	Sets attack/release time for AGC
C3	Low-frequency cutoff capacitor	Provides additional pole for low-frequency cutoff
C4	Microphone power supply decoupling	Reduces power supply noise
C6, C7, C8	Power supply capacitors	Filter and bypass of power supply

ORDERING INFORMATION

Product Number Descriptor Key



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When ordering ISD1000A Series devices, please refer to the following valid part numbers.

Part Number	Part Number
ISD1016AP	ISD1020AP
ISD1016API	ISD1020API
ISD1016AS	ISD1020AS
ISD1016ASI	ISD1020ASI
ISD1016AX	ISD1020AX

For the latest product information, access ISD's worldwide website at http://www.isd.com.