Advanced Power MOSFET

IRFR/U234A

FEATURES

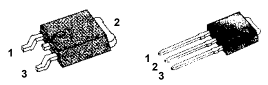
- Avalanche Rugged Technology
- Rugged Gate Oxide Technology
- Lower Input Capacitance
- Improved Gate Charge
- Extended Safe Operating Area
- Lower Leakage Current : 10 μA (Max.) @ V_{DS} = 250V
- Lower $R_{DS(ON)}$: 0.327 Ω (Typ.)

BV_{DSS} = 250 V

$R_{DS(on)}$ = 0.45 Ω

I_D = 6.6 A

D-PAK **I-PAK**



1. Gate 2. Drain 3. Source

Absolute Maximum Ratings

Symbol	Characteristic	Value	Units
V_{DSS}	Drain-to-Source Voltage	250	V
I_D	Continuous Drain Current (T_C=25℃)	6.6	A
	Continuous Drain Current (T_C=100℃)	4.2	
I_{DM}	Drain Current-Pulsed ①	26	A
V_{GS}	Gate-to-Source Voltage	±30	V
E_{AS}	Single Pulsed Avalanche Energy ②	191	mJ
I_{AR}	Avalanche Current ①	6.6	A
E_{AR}	Repetitive Avalanche Energy ①	4.9	mJ
dv/dt	Peak Diode Recovery dv/dt ③	4.8	V/ns
P_D	Total Power Dissipation (T_A=25℃) *	2.5	W
	Total Power Dissipation (T_C=25℃)	49	W
	Linear Derating Factor	0.39	W/℃
T_J , T_{STG}	Operating Junction and Storage Temperature Range	- 55 to +150	℃
T_L	Maximum Lead Temp. for Soldering Purposes, 1/8? from case for 5-seconds	300	

Thermal Resistance

Symbol	Characteristic	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	--	2.54	℃/W
$R_{\theta JA}$	Junction-to-Ambient *	--	50	
$R_{\theta JA}$	Junction-to-Ambient	--	110	

* When mounted on the minimum pad size recommended (PCB Mount).

SAMSUNG ELECTRONICS

Electrical Characteristics (T_C=25℃ unless otherwise specified)

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
BV_{DSS}	Drain-Source Breakdown Voltage	250	--	--	V	V_{GS}=0V,I_D=250μA
$\Delta BV/\Delta T_J$	Breakdown Voltage Temp. Coeff.	--	0.29	--	V/℃	I_D=250μA ***See Fig 7***
$V_{GS(th)}$	Gate Threshold Voltage	2.0	--	4.0	V	V_{DS}=5V,I_D=250μA
I_{GSS}	Gate-Source Leakage , Forward	--	--	100	nA	V_{GS}=30V
	Gate-Source Leakage , Reverse	--	--	-100		V_{GS}=-30V
I_{DSS}	Drain-to-Source Leakage Current	--	--	10	μA	V_{DS}=250V
		--	--	100		V_{DS}=200V,T_C=125℃
$R_{DS(on)}$	Static Drain-Source On-State Resistance	--	--	0.45	Ω	V_{GS}=10V,I_D=3.3A ④
g_{fs}	Forward Transconductance	--	4.83	--	℧	V_{DS}=40V,I_D=3.3A ④
C_{iss}	Input Capacitance	--	730	950	pF	V_{GS}=0V,V_{DS}=25V,f =1MHz ***See Fig 5***
C_{oss}	Output Capacitance	--	110	130		
C_{rss}	Reverse Transfer Capacitance	--	50	60		
$t_{d(on)}$	Turn-On Delay Time	--	13	40	ns	V_{DD}=125V,I_D=8.1A, R_G=12Ω ***See Fig 13*** ④ ⑤
t_r	Rise Time	--	14	40		
$t_{d(off)}$	Turn-Off Delay Time	--	53	120		
t_f	Fall Time	--	21	50		
Q_g	Total Gate Charge	--	30	40	nC	V_{DS}=200V,V_{GS}=10V, I_D=8.1A ***See Fig 6 & Fig 12*** ④ ⑤
Q_{gs}	Gate-Source Charge	--	5.8	--		
Q_{gd}	Gate-Drain(밧iller? Charge	--	13.5	--		

Source-Drain Diode Ratings and Characteristics

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
I_S	Continuous Source Current	--	--	6.6	A	Integral reverse pn-diode in the MOSFET
I_{SM}	Pulsed-Source Current ①	--	--	26		
V_{SD}	Diode Forward Voltage ④	--	--	1.5	V	T_J=25℃,I_S=6.6A,V_{GS}=0V
t_{rr}	Reverse Recovery Time	--	190	--	ns	T_J=25℃,I_F=8.1A di_F/dt=100A/μs ④
Q_{rr}	Reverse Recovery Charge	--	1.28	--	μC	

Notes ;

① Repetitive Rating : Pulse Width Limited by Maximum Junction Temperature
② L=7mH, I_{AS}=6.6A, V_{DD}=50V, R_G=27Ω, Starting T_J =25℃
③ I_{SD}≤8.1A, di/dt≤210A/μs, V_{DD}≤BV_{DSS} , Starting T_J =25℃
④ Pulse Test : Pulse Width = 250μs, Duty Cycle ≤ 2%
⑤ Essentially Independent of Operating Temperature

Fig 1. Output Characteristics

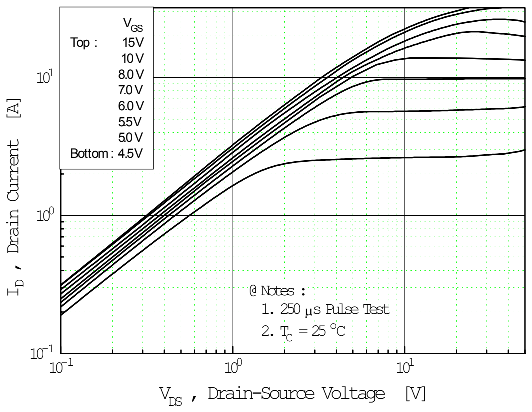


Fig 2. Transfer Characteristics

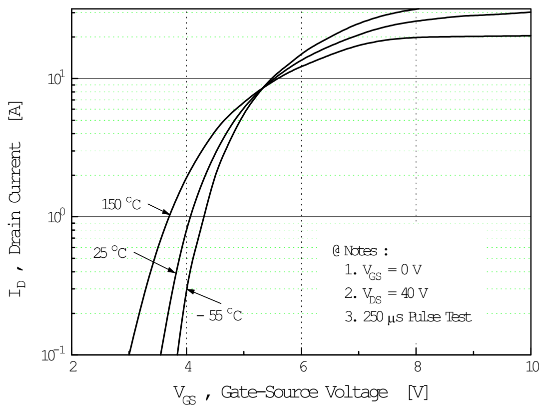


Fig 3. On-Resistance vs. Drain Current

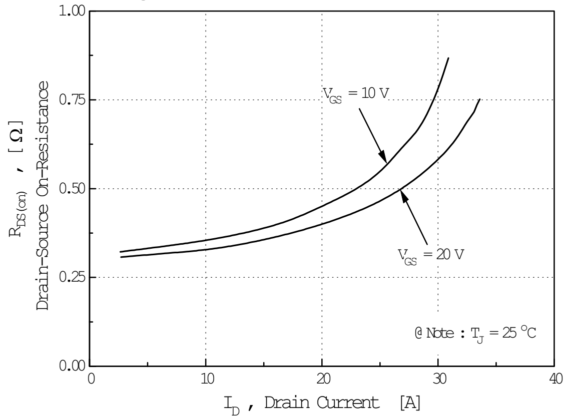


Fig 4. Source-Drain Diode Forward Voltage

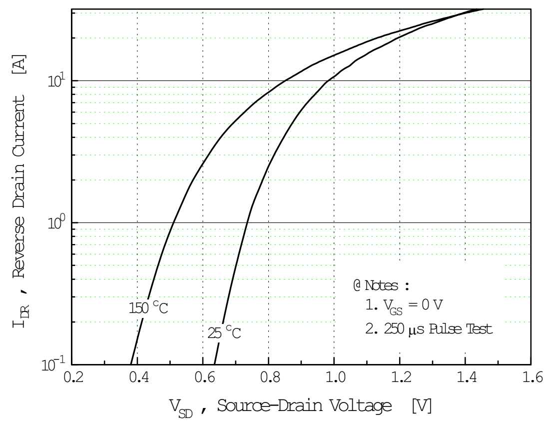


Fig 5. Capacitance vs. Drain-Source Voltage

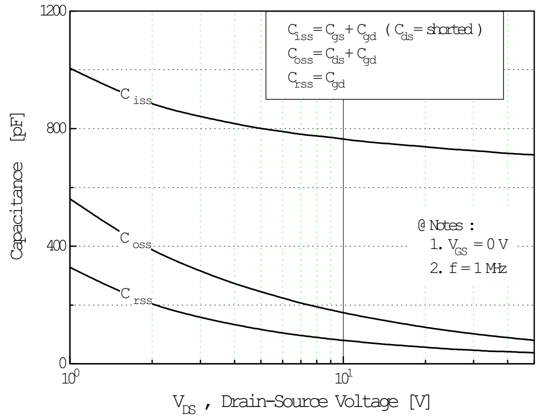


Fig 6. Gate Charge vs. Gate-Source Voltage

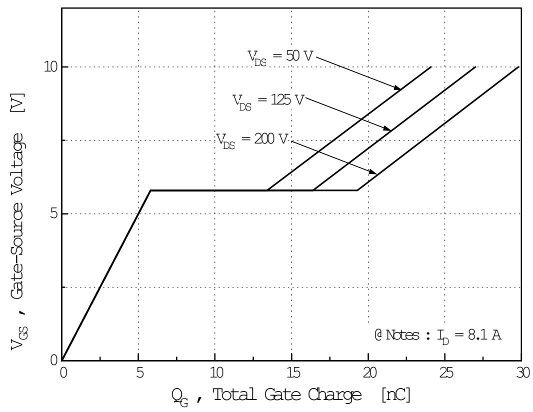


Fig 7. Breakdown Voltage vs. Temperature

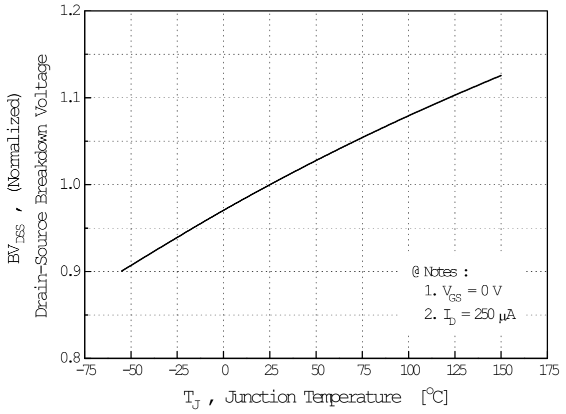


Fig 8. On-Resistance vs. Temperature

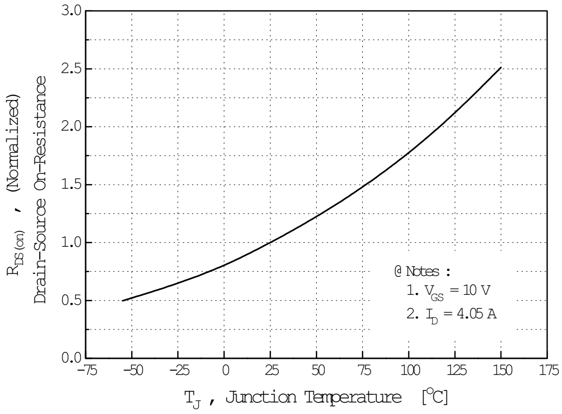


Fig 9. Max. Safe Operating Area

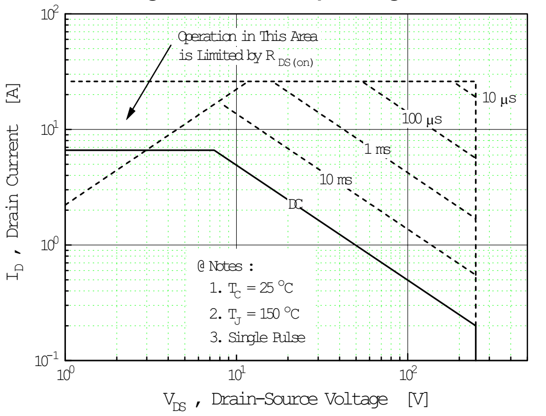


Fig 10. Max. Drain Current vs. Case Temperature

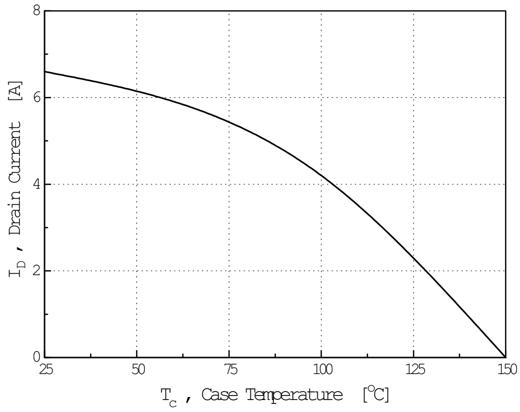


Fig 11. Thermal Response

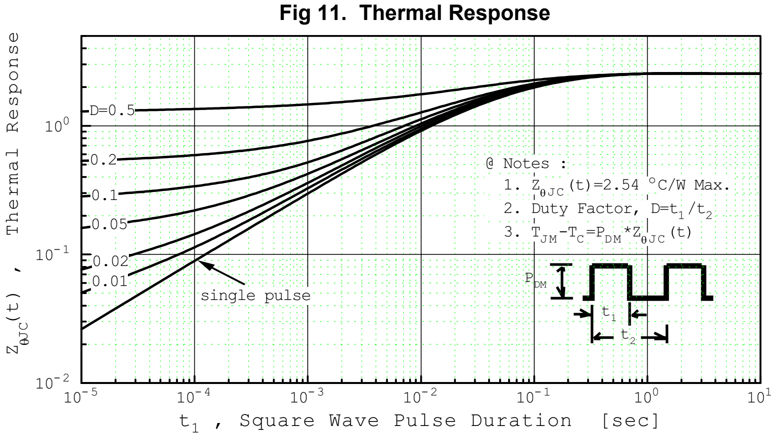


Fig 12. Gate Charge Test Circuit & Waveform

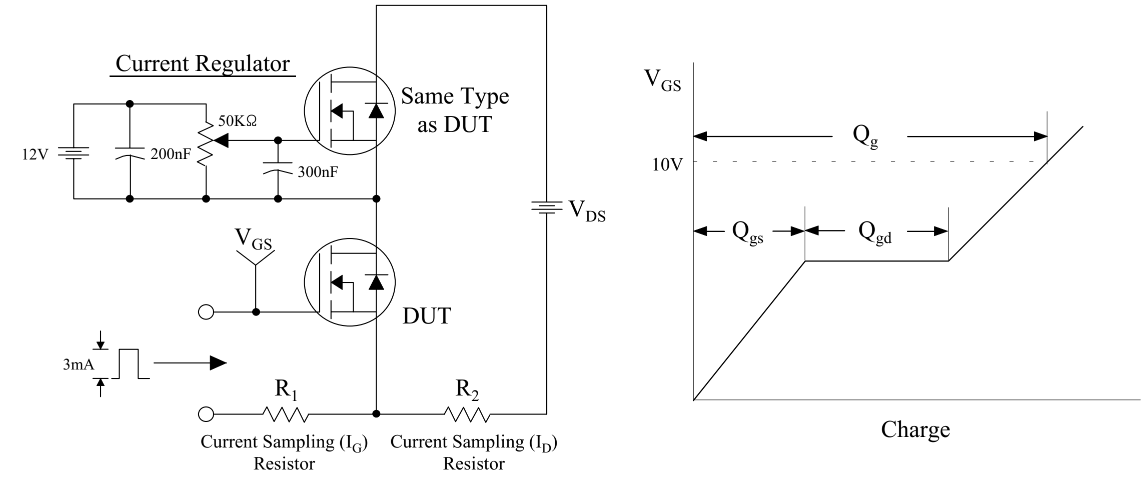


Fig 13. Resistive Switching Test Circuit & Waveforms

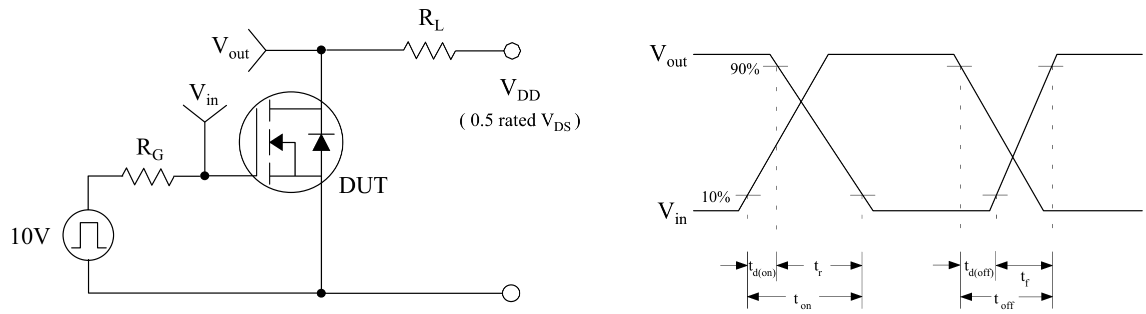


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

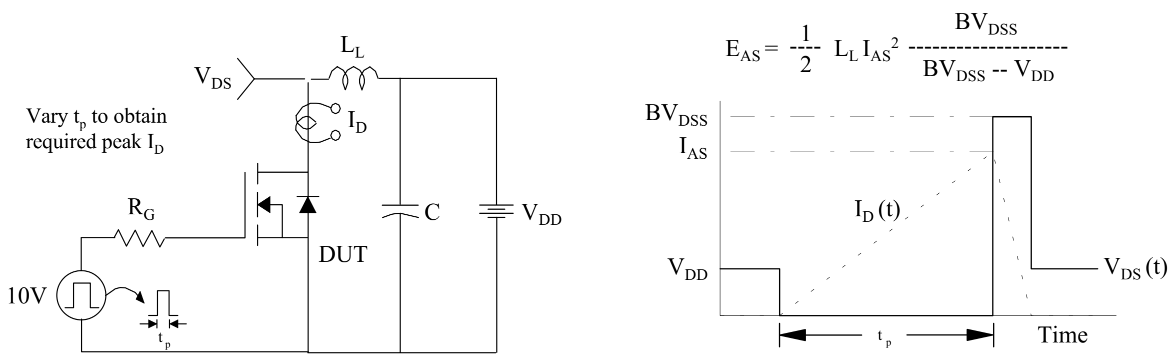


Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms