

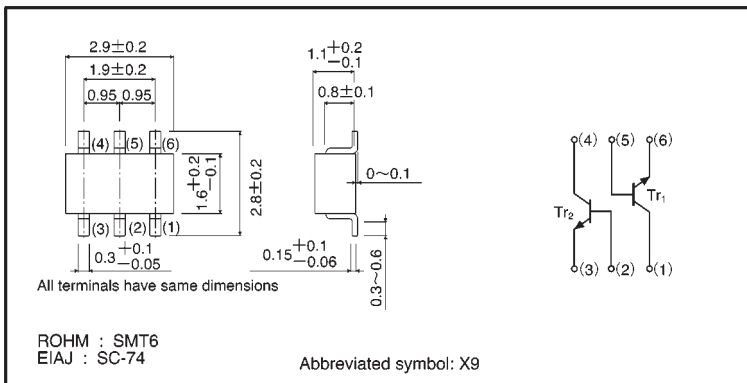
IMX9

- 1) Two 2SD2114K chips in a SMT package.
- 2) Mounting possible with SMT3 automatic mounting machine.
- 3) Transistor elements are independent, eliminating interference.
- 4) Mounting cost and area can be cut in half.

Epitaxial planar type
NPN silicon transistor

The following characteristics apply to both Tr_1 and Tr_2 .

● External dimensions (Units: mm)



●Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Limits	Unit
Collector-base voltage	V_{CBO}	60	V
Collector-emitter voltage	V_{CEO}	50	V
Emitter-base voltage	V_{EBO}	5	V
Collector current	I_C	500	mA
Power dissipation	P_d	300 (TOTAL)	mW *
Junction temperature	T_j	150	°C
Storage temperature	T_{stg}	-55~+150	°C

* 200mW per element must not be exceeded.

●Electrical characteristics (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Collector-base breakdown voltage	BV_{CBO}	60	—	—	V	$I_C=100\mu A$
Collector-emitter breakdown voltage	BV_{CEO}	50	—	—	V	$I_C=1mA$
Emitter-base breakdown voltage	BV_{EBO}	5	—	—	V	$I_E=100\mu A$
Collector cutoff current	I_{CBO}	—	—	0.1	μA	$V_{CB}=30V$
Emitter cutoff current	I_{EBO}	—	—	0.1	μA	$V_{EB}=4V$
Collector-emitter saturation voltage	$V_{CE(sat)}$	—	—	0.6	V	$I_C/I_E=500mA/50mA$
DC current transfer ratio	h_{FE}	120	—	390	—	$V_{CE}=3V, I_C=100mA$ *
Transition frequency	f_T	—	250	—	MHz	$V_{CE}=5V, I_E=-20mA, f=100MHz$
Output capacitance	C_{ob}	—	7	—	pF	$V_{CB}=10V, I_E=0A, f=1MHz$

* Measured using pulse current.

●Packaging specifications

Part No.	Packaging type	Taping
	Code	T110
	Basic ordering unit (pieces)	3000
IMX17		

●Electrical characteristic curves

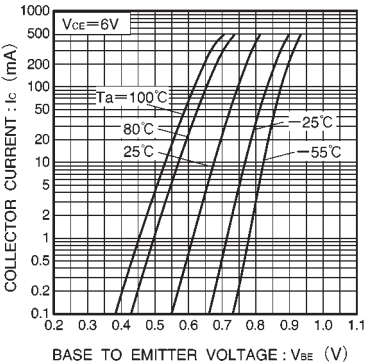


Fig.1 Grounded emitter propagation characteristics

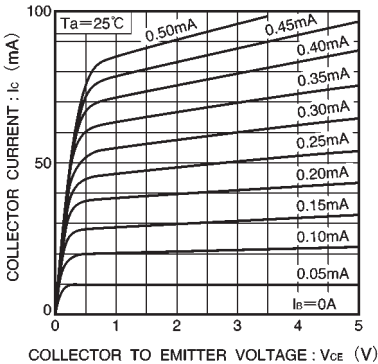


Fig.2 Grounded emitter output characteristics (I)

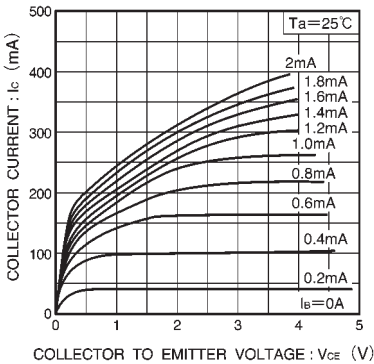


Fig.3 Grounded emitter output characteristics (II)

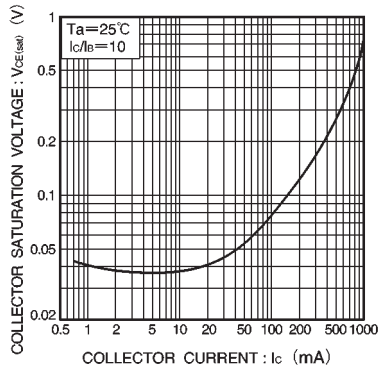


Fig.4 Collector-emitter saturation voltage vs. collector current

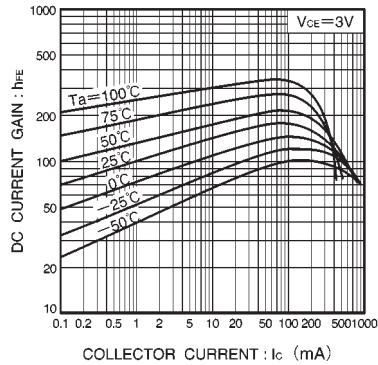


Fig.5 DC current gain vs. collector current

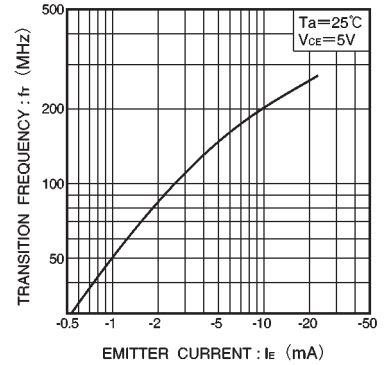


Fig.6 Gain bandwidth product vs. emitter current

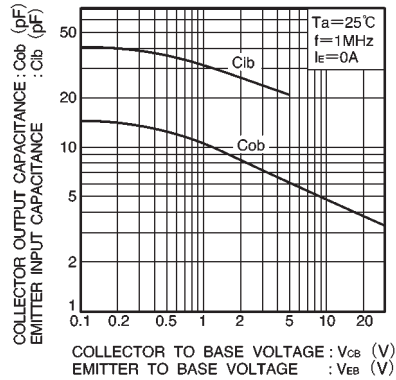


Fig.7 Input/output capacitance vs. voltage