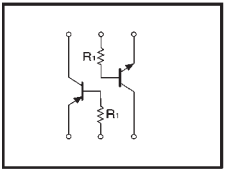
Power management (dual digital transistors)

IMD1A

●Features

1） Both the DTA124T and DTC124T chips in a SMT package.

●Circuit diagram



●Absolute maximum ratings（Ta=25℃）

Parameter	Symbol	Limits	Unit
Collector-base voltage	V_{CBO}	50	V
Collector-emitter voltage	V_{CEO}	50	V
Emitter-base voltage	V_{EBO}	5	V
Collector current	I_C	100	mA
Collector power dissipation	Pc	300（TOTAL）	mW ＊
Junction temperature	Tj	150	℃
Storage temperature	Tstg	−55～+150	℃

＊ 200mW per element must not be exceeded. PNP type negative symbols have been omitted.

●Package, marking, and packaging specifications

Type	IMD1A
Package	SMT6
Marking	D1
Code	T108
Basic ordering unit (pieces)	3000

●Electrical characteristics（Ta=25℃）

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Collector-base breakdown voltage	BV_{CBO}	50	—	—	V	I_C=50 μA
Collector-emitter breakdown voltage	BV_{CEO}	50	—	—	V	I_C=1mA
Emitter-base breakdown voltage	BV_{EBO}	5	—	—	V	I_E=50 μA
Collector cutoff current	I_{CBO}	—	—	0.5	μA	V_{CB}=50V
Emitter cutoff current	I_{EBO}	—	—	0.5	μA	V_{EB}=4V
Collector-emitter saturation voltage	$V_{CE(sat)}$	—	—	0.3	V	I_C/I_B=5mA/0.5mA
DC current transfer ratio	h_{FE}	100	250	600	—	V_{CE}=5V, I_C=1mA
Transition frequency	f_T	—	250	—	MHz	V_{CE}=10V, I_E=−5mA , f=100MHz ＊
Input resistance	R_1	15.4	22	28.6	kΩ	—

＊ Transition frequency of mounted transistor. PNP type negative symbols have been omitted.