HT48CA0
8-bit Microcontroller

HT48CA0 SPECIFICATION

Features

- 10 bidirectional I/O lines

- 6 schmitt trigger input lines

- One carrier output (1/2 or 1/3 duty)

- On-chip crystal and RC oscillator

- Watch dog timer

- 1K×14 program ROM

- 32×8 data RAM

- Operating voltage: 2.2V~3.6V

- Low voltage reset function

- Halt function to reduce power consumption and wake-up feature

- 62 powerful instructions

- Up to 1μs instruction cycle with 4MHz system clock

- All instructions in 1 or 2 machine cycles

- 14-bit table read instructions

- One-level subroutine nesting

- Bit manipulation instructions

General Description

The HT48CA0 is an 8-bit high performance RISC-like microcontroller specifically designed for multiple I/O product applications. The device is particularly suitable for use in products such as remote controllers, fan/light controllers, washing machine controllers, scales, toys and various subsystem controllers. A halt feature is included to reduce power consumption.

Block Diagram
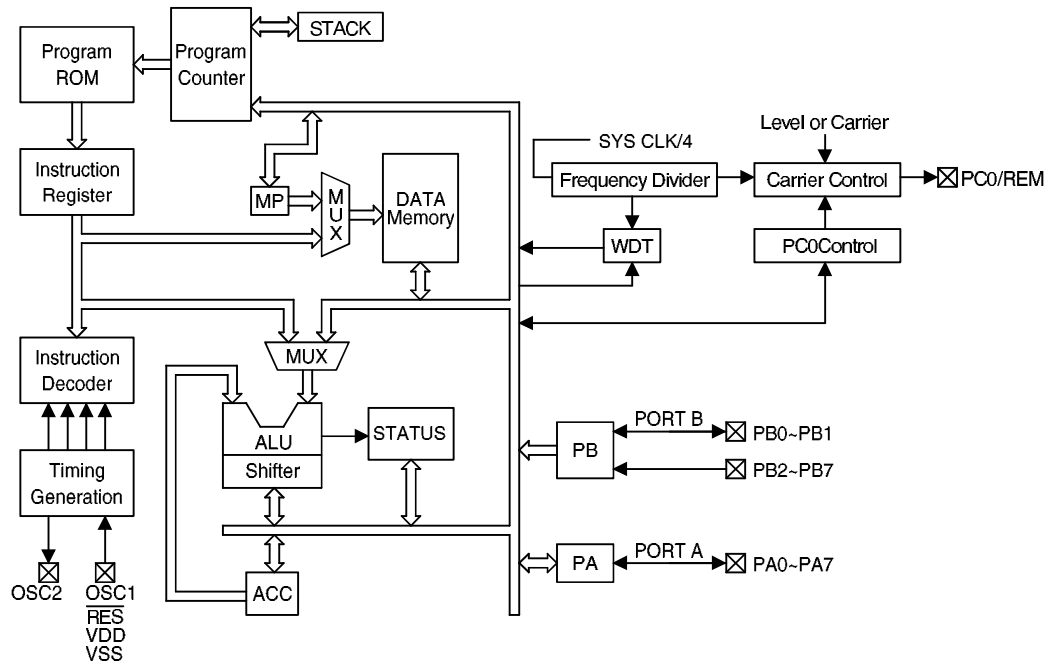
Pad Description

Pad No.	Pad Name	I/O	Mask Option	Function
1, 22	PB0, PB1	I/O	Wake-up or none	2-bit bidirectional input/output lines with pull-high resistors. Each bit can be determined to be the NMOS output or schmitt trigger input by software instructions. Each bit also can be configured as a wake-up input by a mask option.
2	PC0/REM	O	Level or Carrier	Level or carrier output pin. PC0 can be set as CMOS output pin or carrier output pin by mask option.
3	VDD	—	—	Positive power supply.
6	VSS	—	—	Negative power supply, GND.
7	$\overline{\text{RES}}$	I	—	Schmitt trigger reset input. Active low.
13~8	PB2~PB7	I	Wake-up or none	6-bit schmitt trigger input lines with pull-high resistors. Each bit can be configured as a wake-up input by a mask option.
21~14	PA0~PA7	I/O	—	Bidirectional 8-bit input/output port with pull-high resistors. Each bit can be determined to be the NMOS output or schmitt trigger input by software instructions.

24th Dec '97

Pad Coordinates
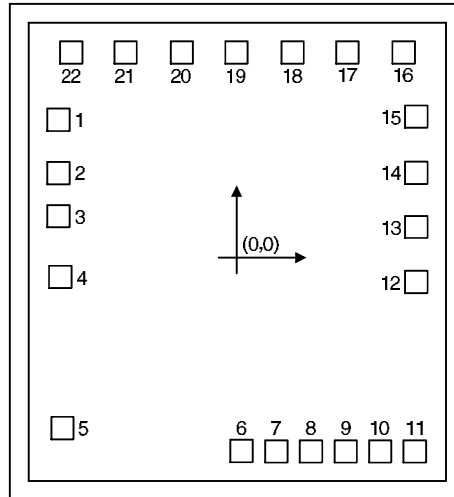
* The IC substrate should be connected to VSS in the PCB layout artwork.
* The TMR pad must be bonded to VDD or VSS if the TMR pad is not used.

Package & Pin Assignment

20SOP-A

20DIP-A

24SOP-A

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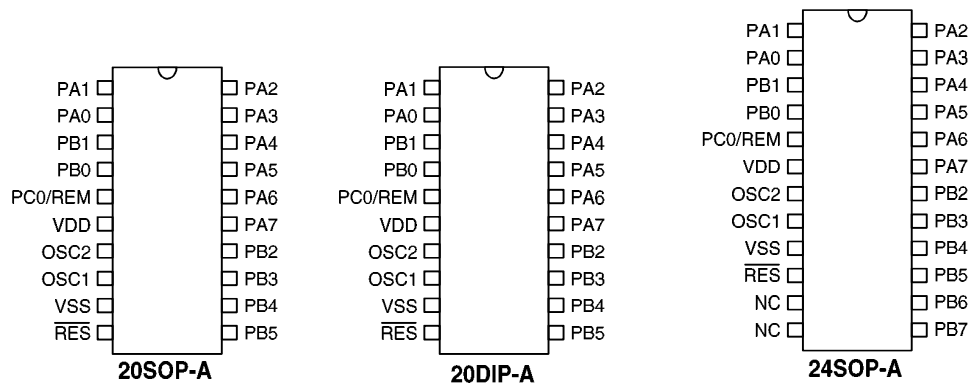
Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Unit
Supply Voltage	V_{DD}	−0.3	4.0	V
Input Voltage	V_I	VSS−0.3	V_{DD}+0.3	V
Storage Temperature	T_{STG}	−50	125	°C
Operating Temperature	T_{OP}	−25	70	°C

D.C. Characteristics

(Ta=25°C)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Operating voltage	—	—	2.2	—	3.6	V
I_{DD}	Operating current	3V	No load, f_{SYS}=4MHz	—	0.7	1.5	mA
I_{STB}	Standby current	3V	No load, System HALT	—	—	1	μA
V_{IL1}	Input low voltage for I/O ports	3V	—	0	—	1.05	V
V_{IH1}	Input high voltage for I/O ports	3V	—	1.95	—	3	V
V_{IL2}	Input low voltage ($\overline{RES}$)	3V	—	—	1.5	—	V
V_{IH2}	Input high voltage ($\overline{RES}$)	3V	—	—	2.4	—	V
I_{OL}	I/O ports sink current	3V	V_{OL}=0.3V	1.5	2.5	—	mA
I_{OH}	I/O ports source current	3V	V_{OH}=2.7V	−1	−1.5	—	mA
R_{PH1}	Pull-high resistance of PA port, PB0~PB1 & $\overline{RES}$	3V	—	—	60	—	kΩ
R_{PH2}	Pull-high resistance of PB2~PB7	3V	—	—	60	—	kΩ
V_{LVR}	Low voltage reset	3V	—	1.8	2.0	2.2	V

A.C Characteristics

(Ta=25°C)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
f_{SYS}	System clock	3V	—	400	—	4000	kHz
t_{RES}	External reset low pulse width	—	—	1	—	—	μs
t_{SST}	System start-up timer period	—	Power-up or wake-up from halt	—	1024	—	t_{SYS}

Note: t_{SYS}=1/(f_{SYS})

Application Circuit
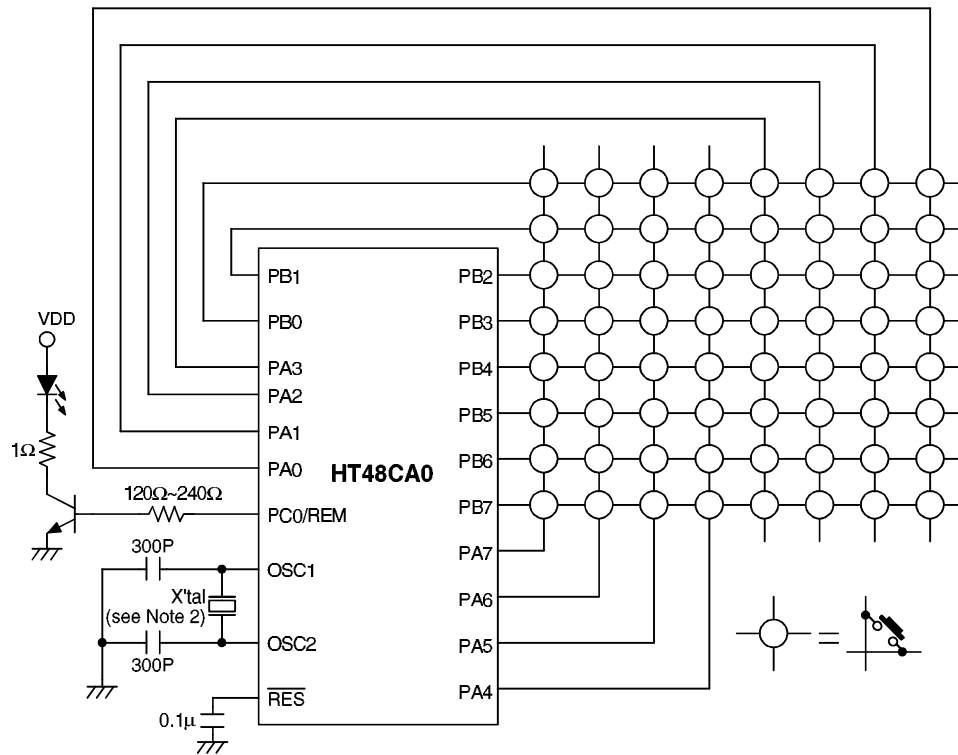
Notes: 1. It is recommended that a 0.1μF decopling capacitor is placed between VSS and VDD.

2. If the X'tal has a value above 1MHz the capacitors are not required.

SYSTEM ARCHITECTURE

Execution Flow

The system clock for the HT48CA0 is derived from a crystal/ceramic resonator oscillator. The system clock is internally divided into four non-overlapping clocks. One instruction cycle consists of four system clock cycles.

Instruction fetching and execution are pipelined in such a way that a fetch takes one instruction cycle while decoding and execution takes the next instruction cycle. However, the pipelining scheme causes each instruction to effectively execute in one cycle. If an instruction changes the program counter, two cycles are required to complete the instruction.

Program Counter - PC

The 10-bit program counter (PC) controls the sequence in which the instructions stored in program ROM are executed and its contents specify a maximum of 1024 addresses.

After accessing a program memory word to fetch an instruction code, the contents of the program counter are incremented by one. The program counter then points to the memory word containing the next instruction code.

When executing a jump instruction, conditional skip execution, loading PCL register, subroutine call, initial reset or return from subroutine, the PC manipulates the program transfer by loading the address corresponding to each instruction.

The conditional skip is activated by instruction. Once the condition is met, the next instruction, fetched during the current instruction execution, is discarded and a dummy cycle replaces it to get the proper instruction. Otherwise proceed with the next instruction.

The lower byte of the program counter (PCL) is a readable and writeable register (06H). Moving data into the PCL performs a short jump. The destination will be within 256 locations.

Once the control transfer takes place, the execution suffers from having an additional dummy cycle.

Program Memory - ROM

The program memory is used to store the program instructions which are to be executed. It also contains data and table and is organized with 1024×14 bits, addressed by the program counter and table pointer.

Certain locations in the program memory are reserved for special usage:

- Location 000H
  This area is reserved for the initialization program. After chip reset, the program always begins execution at location 000H.
- Table location
  Any location in the ROM space can be used as look-up tables. The instructions TABRDC
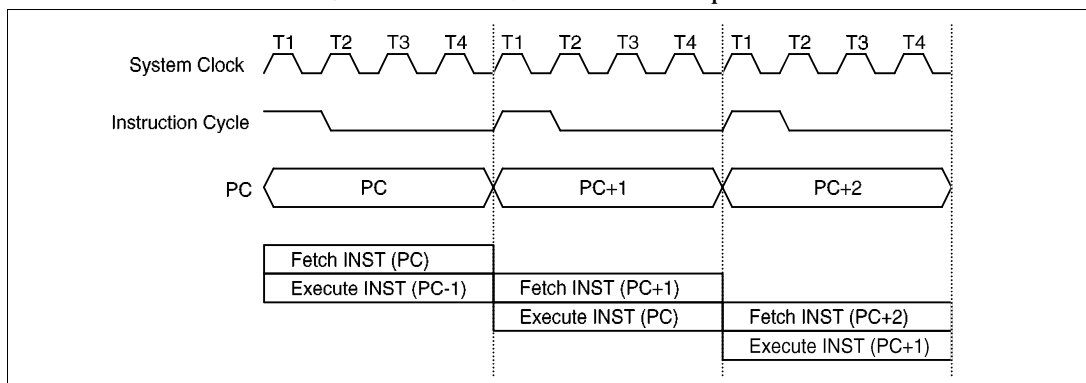
Execution Flow

[m] (the current page, 1 page=256 words) and TABRDL [m] (the last page) transfer the contents of the lower-order byte to the specified data memory, and the higher-order byte to TBLH (08H). Only the destination of the lower-order byte in the table is well-defined, the other bits of the table word are transfered to the lower portion of TBLH, the remaining 2 bits are read as "0". The Table Higher-order byte register (TBLH) is read only. The table pointer (TBLP) is a read/write register (07H), which indicates the table location. Before accessing the table, the location must be placed in TBLP. The TBLH is read only and cannot be restored. All table related instructions need 2 cycles to complete the operation. These areas may function as normal program memory depending upon the user's requirements.
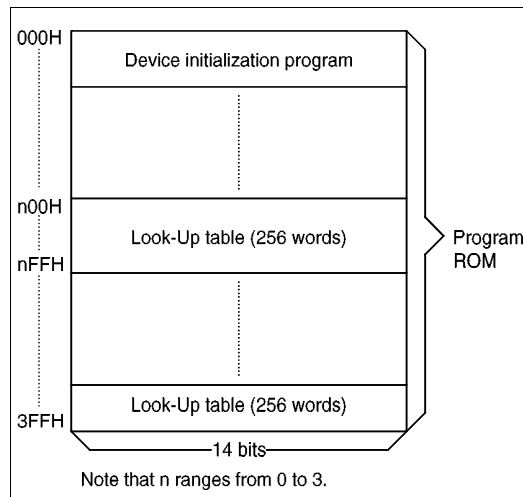
Stack Register - STACK

This is a special part of memory which is used to save the contents of the program counter (PC) only. The stack is organized into one level and is neither part of the data nor program space, and is neither readable nor writeable. The activated level is indexed by the stack pointer (SP) and is neither readable nor writeable. At a subroutine call the contents of the program counter are pushed onto the stack. At end of a subroutine signalled by a return instruction (RET), the program counter is restored to its previous value from the stack.

Program Memory

After a chip reset, the SP will point to the top of the stack.

If the stack is full and a "CALL" is subsequently executed, stack overflow occurs and the first entry will be lost (only the most recent one return address are stored).

Data Memory - RAM

The data memory is designed with 42×8 bits. The data memory is divided into two functional groups: special function registers and general purpose data memory (32×8). Most of them are read/write, but some are read only.

Mode	Program Counter									
	*9	*8	*7	*6	*5	*4	*3	*2	*1	*0
Initial reset	0	0	0	0	0	0	0	0	0	0
Skip	PC+2									
Loading PCL	*9	*8	@7	@6	@5	@4	@3	@2	@1	@0
Jump, call branch	#9	#8	#7	#6	#5	#4	#3	#2	#1	#0
Return from subroutine	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0

Program Counter

Notes:

*9~*0: Bits of Program Counter   S9~S0: Bits of Stack Register
#9~#0: Bits of Instruction Code   @7~@0: Bits of PCL

The special function registers include the Indirect Addressing register (00H), the Memory Pointer register (MP;01H), the Accumulator (ACC;05H) the Program Counter Lower-order byte register (PCL;06H), the Table Pointer (TBLP;07H), the Table Higher-order byte register (TBLH;08H), the Status register (STATUS;0AH) and the I/O registers (PA;12H, PB;14H, PC;16H). The remaining space before the 20H is reserved for future expanded usage and reading these locations will return the result 00H. The general purpose data memory, addressed from 20H to 3FH, is used for data and control information under instruction command.

All data memory areas can handle arithmetic, logic, increment, decrement and rotate operations directly. Except for some dedicated bits, each bit in the data memory can be set and reset by the SET [m].i and CLR [m].i instructions, respectively. They are also indirectly accessable through Memory pointer register (MP;01H).

Indirect Addressing Register

Location 00H is an indirect addressing register that is not physically implemented. Any read/write operation of [00H] accesses data memory pointed to by MP (01H). Reading location 00H itself indirectly will return the result 00H. Writing indirectly results in no operation.

The memory pointer register MP (01H) is a 6-bit register. The bit 7~6 of MP is undefined and reading will return the result "1". Any writing operation to MP will only transfer the lower 6-bit data to MP.
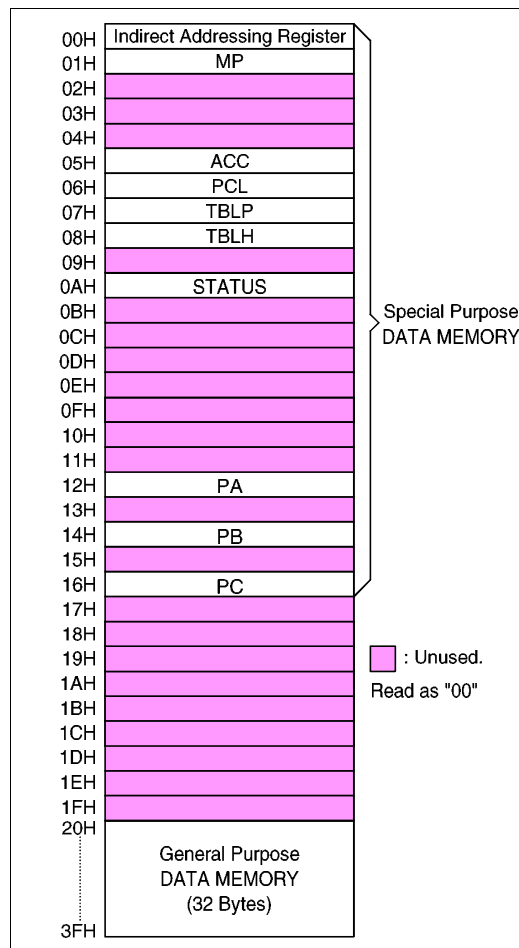
RAM Mapping

Instruction(s)	Table Location									
	*9	*8	*7	*6	*5	*4	*3	*2	*1	*0
TABRDC [m]	P9	P8	@7	@6	@5	@4	@3	@2	@1	@0
TABRDL [m]	1	1	@7	@6	@5	@4	@3	@2	@1	@0

Table Location

Notes:

*9~*0: Bits of table location   P9~P8: Bits of current Program Counter
@7~@0: Bits of table pointer

Accumulator

The accumulator closely relates to ALU operations. It is also mapped to location 05H of the data memory and is the one which can operate with immediate data. The data movement between two data memory must get through the accumulator.

Arithmetic and Logic Unit - ALU

This circuit performs 8-bit arithmetic and logic operation. The ALU provides the following functions:

- Arithmetic operations (ADD, ADC, SUB, SBC, DAA)
- Logic operations (AND, OR, XOR, CPL)
- Rotation (RL, RR, RLC, RRC)
- Increment & Decrement (INC, DEC)
- Branch decision (SZ, SNZ, SIZ, SDZ ....)

The ALU not only saves the results of a data operation but can also change the status register.

Status Register - STATUS

This 8-bit register (0AH) contains the zero flag (Z), carry flag (C), auxiliary carry flag (AC), overflow flag (OV), power down flag (PD) and watch dog time-out flag (TO). It also records the status information and controls the operation sequence.

With the exception of the TO and PD flags, bits in the status register can be altered by instructions like any other register. Any data written into the status register will not change the TO or PD flags. In addition it should be noted that operations related to the status register may give different results from those intended. The TO and PD flags can only be changed by the Watch Dog Timer overflow, chip power-up, clearing the Watch Dog Timer and executing the HALT instruction.

The Z, OV, AC and C flags generally reflect the status of the latest operations.

In addition, on executing the subroutine call, the status register will not be pushed onto the stack automatically. If the contents of status are important and the subroutine can corrupt the status register, the programmer must take precautions to save it properly.

Labels	Bits	Function
C	0	C is set if the operation results in a carry during an addition operation or if a borrow does not take place during a subtraction operation; otherwise C is cleared. Also it is affected by a rotate through carry instruction.
AC	1	AC is set if the operation results in a carry out of the low nibbles in addition or no borrow from the high nibble into the low nibble in subtraction; otherwise AC is cleared.
Z	2	Z is set if the result of an arithmetic or logic operation is zero; otherwise Z is cleared.
OV	3	OV is set if the operation results in a carry into the highest-order bit but not a carry out of the highest-order bit, or vice versa; otherwise OV is cleared.
PD	4	PD is cleared when either a system power-up or executint the CLR WDT instruction. PD is set by executing the HALT instruction.
TO	5	TO is cleared by a system power-up or executing the CLR WDT or HALT instruction. TO is set by a WDT time-out.
—	6	Undefined. Read as "0".
—	7	Undefined. Read as "0".

STATUS Register

Oscillator Configuration

There are 2 oscillator circuits in the HT48CA0.

Both of them are designed for system clocks; the RC oscillator and the Crystal oscillator, which are determined by mask options. No matter what oscillator type is selected, the signal provides the system clock. The HALT mode stops the system oscillator and resists the external signal to conserve power.

If an RC oscillator is used, an external resistor between OSC1 and VSS in needed and the resistance must range from $51K\Omega$ to $1M\Omega$. The system clock, divided by 4, is available on OSC2, which can be used to synchronize external logic. The RC oscillator provides the most cost effective solution. However, the frequency of the oscillation may vary with VDD, temperature and the chip itself due to process variations. It is, therefore, not suitable for timing sensitive operations where accurate oscillator frequency is desired.

If the Crystal oscillator is used, a crystal across OSC1 and OSC2 is needed to provide the feedback and phase shift needed for oscillator, no other external components are needed. Instead of a crystal, the resonator can also be connected between OSC1 and OSC2 to get a frequency reference, but two external capacitors in OSC1 and OSC2 are required.

Watch Dog Timer - WDT

The clock source of the WDT is implemented by
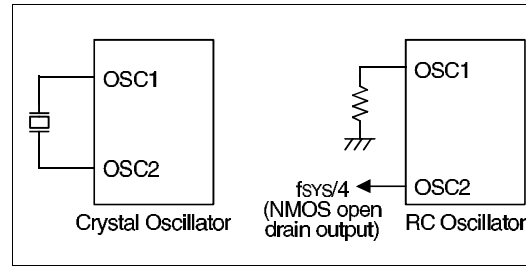
System Oscillator

instruction clock (system clock divided by 4). The clock source is processed by a frequency divider and a prescaller to yield various time out periods.

$$\text{WDT time out period} = \frac{\text{Clock Source}}{2^n}$$

Where n= 8~11 selected by mask option.

This timer is designed to prevent a software malfunction or sequence jumping to an unknown location with unpredictable results. The Watch Dog Timer can be disabled by a mask option. If the Watch Dog Timer is disabled, all the executions related to the WDT result in no operation and the WDT will lose its protecting purpose. In this situation the logic can only be restarted by external logic.

The overflow of WDT under normal operation will initialize "chip reset" and set the status bit TO. To clear the contents of WDT prescaler, 3 methods are adopted; external reset (a low level to $\overline{\text{RES}}$), software instruction(s), or a HALT

Watch Dog Timer

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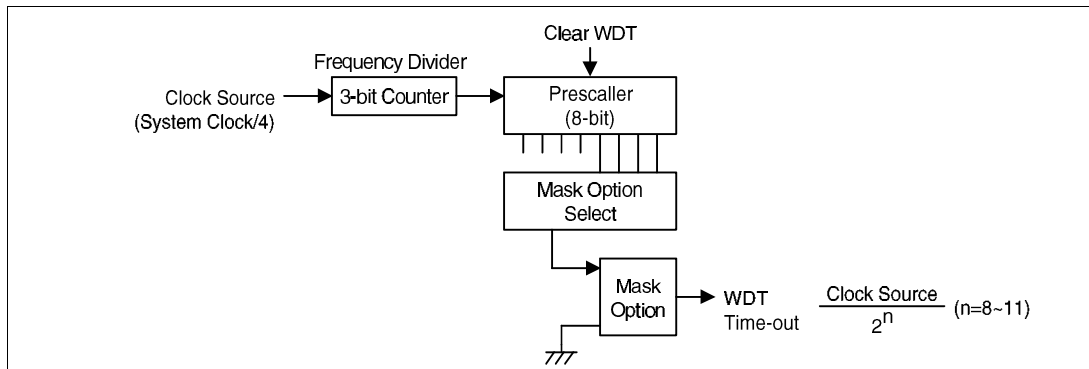
instruction. The software instruction(s) include CLR WDT and the other set — CLR WDT1 and CLR WDT2. Of these two types of instruction, only one can be active depending on the mask option — "CLR WDT times selection option". If the "CLR WDT" is selected (ie. CLRWDT times equal one), any execution of the CLR WDT instruction will clear the WDT. In case "CLR WDT1" and "CLR WDT2" are chosen (ie. CLRWDT times equal two), these two instructions must be executed to clear the WDT; otherwise, the WDT may reset the chip because of the time-out.

Power Down Operation - HALT

The HALT mode is initialized by the HALT instruction and results in the following...

- The system oscillator will turn off and the WDT stop.
- The contents of the on-chip RAM and registers remain unchanged.
- WDT prescaler will be cleared.
- All I/O ports maintain their original status.
- The PD flag is set and the TO flag is cleared.

The system can leave the HALT mode by means of an external reset or an external falling edge signal on port B. An external reset causes a device initialization. Examining the TO and PD flags, the reason for chip reset can be determined. The PD flag is cleared when system power-up or execute the CLR WDT instruction and is set when the HALT instruction is executed. The TO flag is set if the WDT time-out occurs, and causes a wake-up that only resets the PC (Program Counter) and SP, the others keep their original status.

The port B wake-up can be considered as a continuation of normal execution. Each bit in port B can be independently selected to wake up the device by the mask option. Awakening from an I/O port stimulus, the program will resume execution of the next instruction.

Once a wake-up event(s) occurs, it takes 1024 t_{SYS} (system clock period) to resume normal operation. In other words, a dummy cycle period will be inserted after the wake-up.

To minimize power consumption, all I/O pins should be carefully managed before entering the HALT status.

Reset

There are 3 ways in which a reset can occur:

- $\overline{RES}$ reset during normal operation
- $\overline{RES}$ reset during HALT
- WDT time-out reset during normal operation

Some registers remain unchanged during reset conditions. Most registers are reset to the "initial condition" when the reset conditions are met. By examining the PD flag and TO flag, the program can distinguish between different "chip resets".

TO	PD	RESET Conditions
0	0	$\overline{RES}$ reset during power-up
u	u	$\overline{RES}$ reset during normal operation
0	1	$\overline{RES}$ wake-up HALT
1	u	WDT time-out during normal operation

Note: "u" means that "unchange".

To guarantee that the system oscillator has started and stabilized, the SST (System Start-up Timer) provides an extra-delay to delay 1024 system clock pulses when system power up or system awakes from the HALT state.

When the system power-up occurs, the SST delay is added during the reset period. But when the reset comes from the $\overline{RES}$ pin, the SST delay is disabled. Any wake-up from HALT will enable the SST delay.
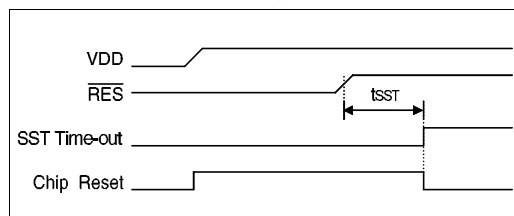
Reset Timing Chart

Reset Circuit
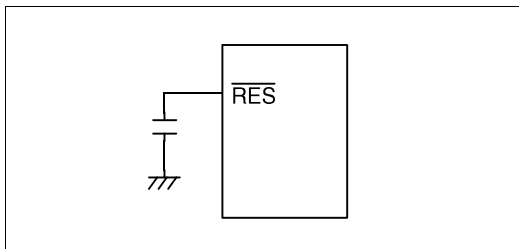
Reset Configuration

The chip reset status of the functional units are shown below.

PC	000H
WDT Prescaler	Clear
Input/output Ports	Input mode
SP	Point to the top of stack
Carrier Output	Low level
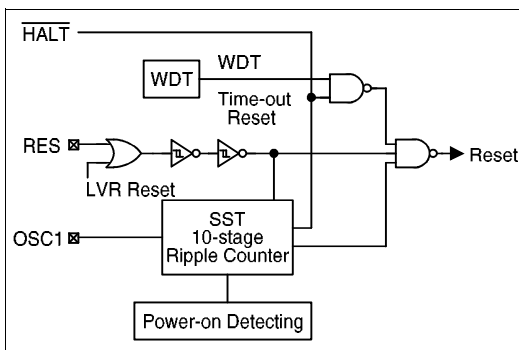
The state of the registers is summarized in the following table:

Register	Reset (power on)	WDT time-out (normal operation)	$\overline{RES}$ reset (normal operation)	$\overline{RES}$ reset (HALT)
PC (Program Counter)	000H	000H	000H	000H
MP	-xxx xxxx	-uuu uuuu	-uuu uuuu	-uuu uuuu
ACC	xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu
TBLP	xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu
TBLH	--xx xxxx	--uu uuuu	--uu uuuu	--uu uuuu
STATUS	--00 xxxx	--1u uuuu	--uu uuuu	--01 uuuu
PA	1111 1111	1111 1111	1111 1111	1111 1111
PB	1111 1111	1111 1111	1111 1111	1111 1111
PC	---- ---1	---- ---1	---- ---1	---- ---1

Note: "u" means that "unchange".
      "x" means that "unknown".

Low Voltage Reset — LVR

The HT48CA0 provides low voltage reset circuit in order to monitor the supply voltage of the device. If the supply voltage of the device is within the range 0.9V~2.2V, such as exchanging battery, the LVR will reset the device internal automatically.

The LVR includes the following specifications:

- The low voltage (0.9V~2.2V) must keep the state to exceed 1 ms. If the low voltage state does not exceed 1 ms, the LVR will ignore it and do not perform the reset function.
- The LVR uses the "OR" function with the external $\overline{RES}$ signal to perform chip reset.
- During HALT mode, if the LVR occurs, the device will be wake-up and the PD flage will be set as "1", same as the external $\overline{RES}$ does.

Because the operating voltage (V_{DD}) is 2.2V~3.6V and the LVR operating voltage (V_{LVR}) is 0.9V~2.2V, therefore one margin voltage about 0.1V is needed for chip proper operation. The relationship between V_{DD} and V_{LVR} is shown below.
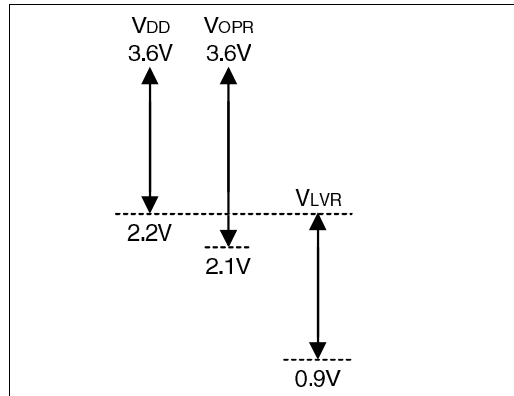
Note: V_{OPR} is the voltage range for chip proper operation at 4MHz system clock.

Carrier

The HT48CA0 provides a carrier output which shares the pin with PC0. It can be selected to be a carrier output (REM) or level output pin (PC0) by mask option. If the carrier output option is selected, setting PC0="0" to enable carrier output and setting PC0="1" to disable it at low level output.
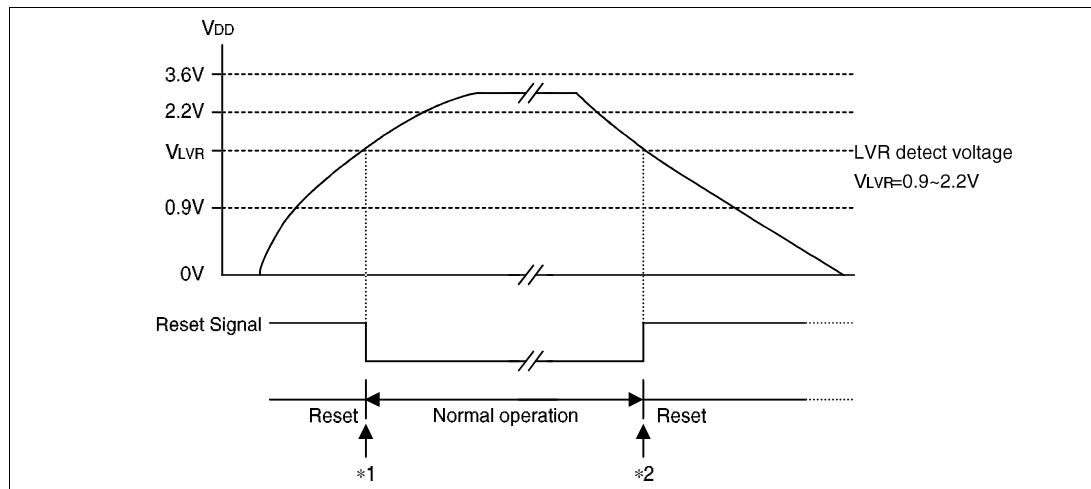
Low Voltage Reset

*1: To gurantee the system oscillator has stabilized, the SST provides an extra-delay to delay 1024 system clock pulses before entering the normal operation.

*2: Because the low voltage must keep its state to exceed 1 ms, therefore 1 ms delay is needy to enter reset mode.

The clock source of the carrier is implemented by instruction clock (system clock divided by 4) and processed by a frequency divider to yield various carry frequency.

$$\text{Carry Frequency} = \frac{\text{Clock Source}}{m \times 2^n}$$

where m=2 or 3 and n=0~3, both of them selected by mask option. If m=2, the duty cycle of the carrier output is 1/2 duty. If m=3, the duty cycle of the carrier output can be 1/2 duty or 1/3 duty also determined by mask option (with the exception of n=0).

Detail selection of the carrier duty is shown below:

$m \times 2^n$	Duty Cycle
2, 4, 8, 16	1/2
3	1/3
6, 12, 24	1/2 or 1/3

Input/Output Ports

There are an 8-bit bi-directional input/output port, a 6-bit input with 2-bit I/O port and a one-bit output port in the HT48CA0, labeled PA, PB and PC which are mapped to [12H], [14H], [16H] of the RAM, respectively. Each bit of PA can be selected to be NMOS output or schmitt trigger with pull-high resistor by software instruction. PB0~PB1 have the same structure with PA, while PB2~PB7 can only be used for input operation (schmitt trigger with pull-high resistors). PC is only one-bit output port shares the pin with carrier output. If the level option is selected, the PC is CMOS output.

Both PA and PB for the input operation, these ports are non-latched, that is, the inputs should be ready at the T2 rising edge of the instruction "MOV A, [m]" (m=12H or 14H). For PA, PB0~PB1 and PC output operation, all data are latched and remain unchanged until the output latch is rewritten.

When the PA and PB0~PB1 is used for input operation, it should be noted that, before reading data from pads should write "1" to the related bits to disable the NMOS device. That is firstly executing the instruction "SET [m].i" (i=0~7 for PA, i=0~1 for PB) to disable related NMOS device, and then "MOV A, [m]" to get stable data.
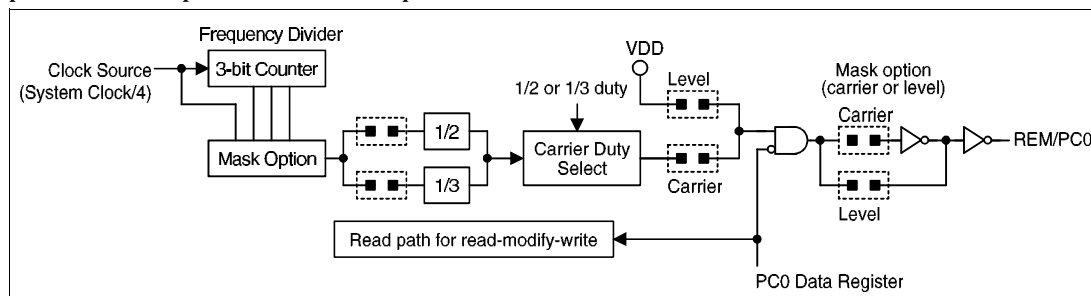
Carrier/Level Output
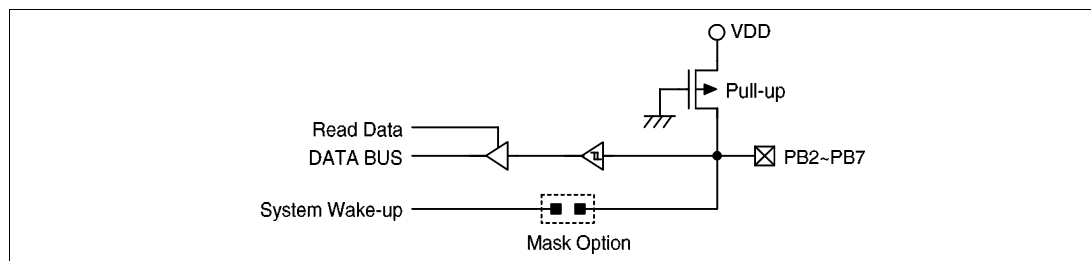
PB Input Lines

After chip reset, PA and PB stay at the high level input line while PC stay at high level output, if the level option is selected.

Each bit of PA, PB0~PB1 and PC output latches can be set or cleared by the "SET [m].i" and "CLR [m].i" (m=12H, 14H or 16H) instructions respectively.

Some instructions first input data and then follow the output operations. For example, "SET [m].i", "CLR [m]", "CPL [m]", "CPLA [m]"

read the entire port states into the CPU, execute the defined operations (bit-operation), and then write the results back to the latches or to the accumulator.

Each line of PB has the capability to wake-up the device by mask option. The highest seven bits of PC are not physically implemented, on reading them a "0" is returned and writing results in a no-operation.
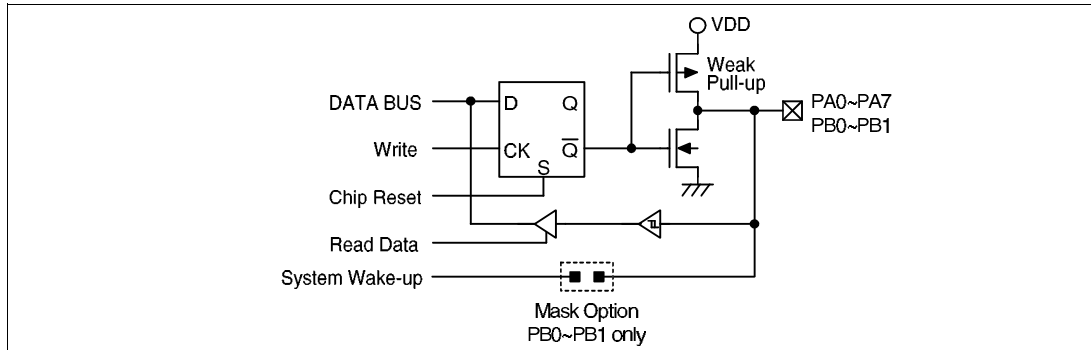
PA, PB Input/Output Lines

Mask Option

The following shows 8 kinds of mask option in the HT48CA0. All the mask options must be defined to ensure proper system function.

No.	Mask Option
1	WDT time-out period selection. Time-out period= $\dfrac{\text{Clock Source}}{2^n}$ where n=8~11.
2	WDT enable/disable selection. This option is to decide the WDT timer to be enable or disable.
3	CLRWDT times selection. This option defines how to clear the WDT by instruction. "One time" means that the CLR WDT instruction can clear the WDT. "Two times" means only if both of the CLR WDT1 and CLR WDT2 instructions have been executed, the WDT can be cleared.
4	Wake-up selection. This option defines the activity of the wake-up function. External input pins (PB only) all have the capability to wake-up the chip from a HALT.
5	Carrier/level output selection. This option defines the activity of PC0 to be carrier output or level output.
6	Carry frequency selection. Carry frequency= $\dfrac{\text{Clock Source}}{(2 \text{ or } 3) \times 2^n}$ where n=0~3.
7	Carrier duty selection. There are two types of selection: 1/2 duty or 1/3 duty. If carrier frequency= Clock Source / (2, 4, 8 or 16), the duty cycle will be 1/2 duty. If carrier frequency= Clock Source / 3, the duty cycle will be 1/3 duty. If carrier frequency= Clock Source / (6, 12 or 24), the duty cycle can be 1/2 duty or 1/3 duty.
8	OSC type selection. This option is to decide if an RC or Crystal oscillator is shosen as system clock. If the Crystal oscillator is selected, the XST (Crystal Start-up Timer) default is activated, otherwise the XST is disabled.

INSTRUCTION SET

Instruction Set Summary

Mnemonic	Description	Instruction Cycle	Flag Affected
Arithmetic			
ADD A,[m]	Add data memory to ACC	1	Z,C,AC,OV
ADDM A,[m]	Add ACC to data memory	$1^{(1)}$	Z,C,AC,OV
ADD A,x	Add immediate data to ACC	1	Z,C,AC,OV
ADC A,[m]	Add data memory to ACC with carry	1	Z,C,AC,OV
ADCM A,[m]	Add ACC to register with carry	$1^{(1)}$	Z,C,AC,OV
SUB A,x	Subtract immediate data from ACC	1	Z,C,AC,OV
SUB A,[m]	Subtract data memory from ACC	1	Z,C,AC,OV
SUBM A,[m]	Subtract data memory from ACC with result in data memory	$1^{(1)}$	Z,C,AC,OV
SBC A,[m]	Subtract data memory from ACC with carry	1	Z,C,AC,OV
SBCM A,[m]	Subtract data memory from ACC with carry with result in data memory	$1^{(1)}$	Z,C,AC,OV
DAA [m]	Decimal adjust ACC for addition with result in data memory	$1^{(1)}$	C
Logic Operation			
AND A,[m]	AND data memory to ACC	1	Z
OR A,[m]	OR data memory to ACC	1	Z
XOR A,[m]	Exclusive-OR data memory to ACC	1	Z
ANDM A,[m]	AND ACC to data memory	$1^{(1)}$	Z
ORM A,[m]	OR ACC to data memory	$1^{(1)}$	Z
XORM A,[m]	Exclusive-OR ACC to data memory	$1^{(1)}$	Z
AND A,x	AND immediate data to ACC	1	Z
OR A,x	OR immediate data to ACC	1	Z
XOR A,x	Exclusive-OR immediate data to ACC	1	Z
CPL [m]	Complement data memory	$1^{(1)}$	Z
CPLA [m]	Complement data memory with result in ACC	1	Z
Increment & Decrement			
INCA [m]	Increment data memory with result in ACC	1	Z
INC [m]	Increment data memory	$1^{(1)}$	Z
DECA [m]	Decrement data memory with result in ACC	1	Z
DEC [m]	Decrement data memory	$1^{(1)}$	Z

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Mnemonic	Description	Instruction Cycle	Flag Affected
Rotate			
RRA [m]	Rotate data memory right with result in ACC	1	
RR [m]	Rotate data memory right	1$^{(1)}$	None
RRCA [m]	Rotate data memory right through carry with result in ACC	1	None
			C
RRC [m]	Rotate data memory right through carry	1$^{(1)}$	C
RLA [m]	Rotate data memory left with result in ACC	1	None
RL [m]	Rotate data memory left	1$^{(1)}$	None
RLCA [m]	Rotate data memory left through carry with result in ACC	1	C
			C
RLC [m]	Rotate data memory left through carry	1$^{(1)}$	
Data Move			
MOV A,[m]	Move data memory to ACC	1	None
MOV [m],A	Move ACC to data memory	1$^{(1)}$	None
MOV A,x	Move immediate data to ACC	1	None
Bit Operation			
CLR [m].i	Clear bit of data memory	1$^{(1)}$	None
SET [m].i	Set bit of data memory	1$^{(1)}$	None
Branch			
JMP addr	Jump unconditionally	2	None
SZ [m]	Skip if data memory is zero	1$^{(2)}$	None
SZA [m]	Skip if data memory is zero with data movement to ACC	1$^{(2)}$	None
SZ [m].i	Skip if bit i of data memory is zero	1$^{(2)}$	None
SNZ [m].i	Skip if bit i of data memory is not zero	1$^{(2)}$	None
SIZ [m]	Skip if increment data memory is zero	1$^{(3)}$	None
SDZ [m]	Skip if decrement data memory is zero	1$^{(3)}$	None
SIZA [m]	Skip if increment data memory is zero with result in ACC	1$^{(2)}$	None
SDZA [m]	Skip if decrement data memory is zero with result in ACC	1$^{(2)}$	None
CALL addr	Subroutine call	2	None
RET	Return from subroutine	2	None
RET A,x	Return from subroutine and load immediate data to ACC	2	None

Mnemonic	Description	Instruction Cycle	Flag Affected
Table Read			
TABRDC [m]	Read ROM code (current page) to data memory and TBLH	$2^{(1)}$	None
TABRDL [m]	Read ROM code (last page) to data memory and TBLH	$2^{(1)}$	None
Miscellaneous			
NOP	No operation	1	None
CLR [m]	Clear data memory	$1^{(1)}$	None
SET [m]	Set data memory	$1^{(1)}$	None
CLR WDT	Clear Watchdog timer	1	TO,PD
CLR WDT1	Pre-clear Watchdog timer	1	$TO^{(4)},PD^{(4)}$
CLR WDT2	Pre-clear Watchdog timer	1	$TO^{(4)},PD^{(4)}$
SWAP [m]	Swap nibbles of data memory	$1^{(1)}$	None
SWAPA [m]	Swap nibbles of data memory with result in ACC	1	None
HALT	Enter power down mode	1	TO,PD

Notes: x = 8 bits immediate data
m = 7 bits data memory address
A = accumulator
i = 0...7 number of bits
addr = 11 bits program memory address
√=Flag(s) is affected
–=Flag(s) is not affected
(1): If a loading to the PCL register occurs, the execution cycle of instructions will be delayed one more cycle (4 system clocks).
(2): If a skipping next instruction occurs, the execution cycle of instructions will be delayed one more cycle (4 system clocks). Otherwise the original instruction cycle(s) is unchanged.
(3): (1) and (2)
(4): The flags may be affected by execution status. If the watchdog timer is cleared by executing the CLR WDT1 or CLR WDT2 instruction, the TO is set and the PD is cleared. Otherwise the TO and PD flags remain unchanged.

Instruction Definition

ADC A,[m] Add data memory and carry to accumulator

Description The contents of the specified data memory, accumulator and the carry flag are added simultaneously, leaving the result in the accumulator.

Operation ACC ← ACC+[m]+C

Affected flag(s)

TC2	TC1	TO	PD	OV	Z	AC	C
–	–	–	–	√	√	√	√

ADCM A,[m] Add accumulator and carry to data memory

Description The contents of the specified data memory, accumulator and the carry flag are added simultaneously, leaving the result in the specified data memory.

Operation [m] ← ACC+[m]+C

Affected flag(s)

TC2	TC1	TO	PD	OV	Z	AC	C
–	–	–	–	√	√	√	√

ADD A,[m] Add data memory to accumulator

Description The contents of the specified data memory and the accumulator are added. The result is stored in the accumulator.

Operation ACC ← ACC+[m]

Affected flag(s)

TC2	TC1	TO	PD	OV	Z	AC	C
–	–	–	–	√	√	√	√

ADD A,x Add immediate data to accumulator

Description The contents of the accumulator and the specified data are added, leaving the result in the accumulator.

Operation ACC ← ACC+x

Affected flag(s)

TC2	TC1	TO	PD	OV	Z	AC	C
–	–	–	–	√	√	√	√

ADDM A,[m]   Add accumulator to data memory

Description   The contents of the specified data memory and the accumulator are added.
                   The result is stored in the data memory.

Operation   [m] ← ACC+[m]

Affected flag(s)

TC2	TC1	TO	PD	OV	Z	AC	C
–	–	–	–	√	√	√	√

AND A,[m]   Logical AND accumulator with data memory

Description   Data in the accumulator and the specified data memory performs a bitwise
                   logical_AND operation. The result is stored in the accumulator.

Operation   ACC ← ACC "AND" [m]

Affected flag(s)

TC2	TC1	TO	PD	OV	Z	AC	C
–	–	–	–	–	√	–	–

AND A,x   Logical AND immediate data to accmulator

Description   Data in the accumulator and the specified data performs a bitwise logi-
                   cal_AND operation. The result is stored in the accumulator.

Operation   ACC ← ACC "AND" x

Affected flag(s)

TC2	TC1	TO	PD	OV	Z	AC	C
–	–	–	–	–	√	–	–

ANDM A,[m]   Logical AND data memory with accumulator

Description   Data in the specified data memory and the accumulator performs a bitwise
                   logical_AND operation. The result is stored in the data memory.

Operation   [m] ← ACC "AND" [m]

Affected flag(s)

TC2	TC1	TO	PD	OV	Z	AC	C
–	–	–	–	–	√	–	–

CALL addr   Subroutine call

Description   The instruction unconditionally calls a subroutine located at the indicated address. The program counter increments once to obtain the address of the next instruction, and pushes this onto the stack. The indicated address is then loaded. Program execution continues with the instruction at this address.

Operation   Stack ← PC+1
PC ← addr

Affected flag(s)

TC2	TC1	TO	PD	OV	Z	AC	C
–	–	–	–	–	–	–	–

CLR [m]   Clear data memory

Description   The contents of the specified data memory are cleared to zero.

Operation   [m] ← 00H

Affected flag(s)

TC2	TC1	TO	PD	OV	Z	AC	C
–	–	–	–	–	–	–	–

CLR [m].i   Clear bit of data memory

Description   The bit i of the specified data memory is cleared to zero.

Operation   [m].i ← 0

Affected flag(s)

TC2	TC1	TO	PD	OV	Z	AC	C
–	–	–	–	–	–	–	–

CLR WDT   Clear watch dog timer

Description   The WDT and the WDT Prescaler are cleared (re-counting from zero). The power down bit (PD) and time-out bit (TO) are cleared.

Operation   WDT & WDT Prescaler ← 00H
PD & TO ← 0

Affected flag(s)

TC2	TC1	TO	PD	OV	Z	AC	C
–	–	0	0	–	–	–	–

CLR WDT1　　　　Preclear watch dog timer

Description　　　　The PD, TO flags, WDT and the WDT Prescaler are cleared (re-counting from zero), if the other preclear WDT instruction had been executed. Only execution of this instruction without the other preclear instruction just sets the indicating flag which implies this instruction was executed and the PD and TO flags remain unchanged.

Operation　　　　WDT & WDT Prescaler ← 00H*
　　　　　　　　　PD & TO ← 0*

Affected flag(s)

TC2	TC1	TO	PD	OV	Z	AC	C
–	–	0*	0*	–	–	–	–

CLR WDT2　　　　Preclear watch dog timer

Description　　　　The PD, TO flags, WDT and the WDT Prescaler are cleared (re-counting from zero), if the other preclear WDT instruction had been executed. Only execution of this instruction without the other preclear instruction, sets the indicating flag which implies this instruction was executed and the PD and TO flags remain unchanged.

Operation　　　　WDT & WDT Prescaler ← 00H*
　　　　　　　　　PD & TO ← 0*

Affected flag(s)

TC2	TC1	TO	PD	OV	Z	AC	C
–	–	0*	0*	–	–	–	–

CPL [m]　　　　Complement data memory

Description　　　　Each bit of the specified data memory is logically complemented (1's complement). Bits which previously contain a one are changed to zero and vice-versa.

Operation　　　　$[m] \leftarrow [\overline{m}]$

Affected flag(s)

TC2	TC1	TO	PD	OV	Z	AC	C
–	–	–	–	–	√	–	–

CPLA [m]   Complement data memory-place result in accumulator

Description   Each bit of the specified data memory is logically complemented (1's complement). Bits which previously contained a one are changed to zero and vice-versa. The complemented result is stored in the accumulator and the contents of the data memory remains unchanged.

Operation   ACC ← [$\overline{m}$]

Affected flag(s)

TC2	TC1	TO	PD	OV	Z	AC	C
–	–	–	–	–	√	–	–

DAA [m]   Decimal-Adjust accumulator for addition

Description   The accumulator value is adjusted to the BCD(Binary Code Decimal) code. The accumulator is divided into two nibbles. Each nibble is adjusted to the BCD code and an internal carry (AC1) will be done if the low nibble of the accumulator is greater than 9. The BCD adjustment is done by adding 6 to the original value if the original value is greater than 9 or a carry (AC or C) is set; otherwise the original value remains unchanged. The result is stored in the data memory and only the carry flag (C) may be affected.

Operation   If (ACC.3~ACC.0) >9 or AC=1
then ([m].3~[m].0) ← (ACC.3~ACC.0)+6, AC1=$\overline{AC}$
else ([m].3~[m].0) ← (ACC.3~ACC.0), AC1=0
If (ACC.7~ACC.4)+AC1 >9 or C=1
then ([m].7~[m].4) ← (ACC.7~ACC.4)+6+AC1, C=1
else ([m].7~[m].4) ← (ACC.7~ACC.4)+AC1, C=C

Affected flag(s)

TC2	TC1	TO	PD	OV	Z	AC	C
–	–	–	–	–	–	–	√

DEC [m]   Decrement data memory

Description   Data in the specified data memory is decremented by one.

Operation   [m] ← [m]–1

Affected flag(s)

TC2	TC1	TO	PD	OV	Z	AC	C
–	–	–	–	–	√	–	–

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DECA [m]   Decrement data memory-place result in accumulator

Description   Data in the specified data memory is decremented by one, leaving the result in the accumulator. The contents of the data memory remain unchanged.

Operation $ACC \leftarrow [m]-1$

Affected flag(s)

TC2	TC1	TO	PD	OV	Z	AC	C
–	–	–	–	–	√	–	–

HALT   Enter power down mode

Description   This instruction stops program execution and turn off the system clock. The contents of the RAM and registers are retained. The WDT and prescaler are cleared. The power down bit (PD) is set and the WDT time-out bit (TO) is cleared.

Operation $PC \leftarrow PC+1$
$PD \leftarrow 1$
$TO \leftarrow 0$

Affected flag(s)

TC2	TC1	TO	PD	OV	Z	AC	C
–	–	0	1	–	–	–	–

INC [m]   Increment data memory

Description   Data in the specified data memory is incremented by one.

Operation $[m] \leftarrow [m]+1$

Affected flag(s)

TC2	TC1	TO	PD	OV	Z	AC	C
–	–	–	–	–	√	–	–

INCA [m]   Increment data memory-place result in accumulator

Description   Data in the specified data memory is incremented by one, leaving the result in the accumulator. The contents of the data memory remain unchanged.

Operation $ACC \leftarrow [m]+1$

Affected flag(s)

TC2	TC1	TO	PD	OV	Z	AC	C
–	–	–	–	–	√	–	–

JMP addr   Direct Jump

Description   Bits 0~9 of the program counter are replaced with the directly–specified address unconditionally, and control passed to this destination.

Operation   PC ← addr

Affected flag(s)

TC2	TC1	TO	PD	OV	Z	AC	C
–	–	–	–	–	–	–	–

MOV A,[m]   Move data memory to accumulator

Description   The contents of the specified data memory is copied to the accumulator.

Operation   ACC ← [m]

Affected flag(s)

TC2	TC1	TO	PD	OV	Z	AC	C
–	–	–	–	–	–	–	–

MOV A,x   Move immediate data to accumulator

Description   The 8–bit data specified by the code is loaded into the accumulator.

Operation   ACC ← x

Affected flag(s)

TC2	TC1	TO	PD	OV	Z	AC	C
–	–	–	–	–	–	–	–

MOV [m],A   Move accumulator to data memory

Description   The contents of the accumulator is copied to the specified data memory (one of the data memory).

Operation   [m] ← ACC

Affected flag(s)

TC2	TC1	TO	PD	OV	Z	AC	C
–	–	–	–	–	–	–	–

NOP   No operation

Description   No operation is performed. Execution continues with the next instruction.

Operation   PC ← PC+1

Affected flag(s)

TC2	TC1	TO	PD	OV	Z	AC	C
–	–	–	–	–	–	–	–

OR A,[m]   Logical OR accumulator with data memory

Description   Data in the accumulator and the specified data memory (one of the data memory) performs a bitwise logical_OR operation. The result is stored in the accumulator.

Operation   ACC ← ACC "OR" [m]

Affected flag(s)

TC2	TC1	TO	PD	OV	Z	AC	C
–	–	–	–	–	√	–	–

OR A,x   Logical OR immediate data to accumulator

Description   Data in the accumulator and the specified data performs a bitwise logical_OR operation. The result is stored in the accumulator.

Operation   ACC ← ACC "OR" x

Affected flag(s)

TC2	TC1	TO	PD	OV	Z	AC	C
–	–	–	–	–	√	–	–

ORM A,[m]   Logical OR data memory with accumulator

Description   Data in the data memory (one of the data memory) and the accumulator performs a bitwise logical_OR operation. The result is stored in the data memory.

Operation   [m] ← ACC "OR" [m]

Affected flag(s)

TC2	TC1	TO	PD	OV	Z	AC	C
–	–	–	–	–	√	–	–

RET   Return from subroutine

Description   The program counter is restored from the stack. This is a two cycle instruction.

Operation   PC ← Stack

Affected flag(s)

TC2	TC1	TO	PD	OV	Z	AC	C
–	–	–	–	–	–	–	–

RET A,x   Return and place immediate data in accumulator

Description   The program counter is restored from the stack and the accumulator loaded with the specified 8-bit immediate data.

Operation   PC ← Stack
                   ACC ← x

Affected flag(s)

TC2	TC1	TO	PD	OV	Z	AC	C
–	–	–	–	–	–	–	–

RETI   Return from interrupt

Description   The program counter is restored from the stack, and interrupts enabled by setting the EMI bit. EMI is the enable master(global) interrupt bit (bit 0; register INTC).

Operation   PC ← Stack
                   EMI ← 1

Affected flag(s)

TC2	TC1	TO	PD	OV	Z	AC	C
–	–	–	–	–	–	–	–

RL [m]   Rotate data memory left

Description   The contents of the specified data memory is rotated left one bit with bit 7 rotated into bit 0.

Operation   [m].(i+1) ← [m].i; [m].i:bit i of the data memory (i=0-6)
                   [m].0 ← [m].7

Affected flag(s)

TC2	TC1	TO	PD	OV	Z	AC	C
–	–	–	–	–	–	–	–

RLA [m]   Rotate data memory left-place result in accumulator

Description   Data in the specified data memory is rotated left one bit with bit 7 rotated into bit 0, leaving the rotated result in the accumulator. The contents of the data memory remain unchanged.

Operation   ACC.(i+1) ← [m].i; [m].i:bit i of the data memory (i=0-6)
                    ACC.0 ← [m].7

Affected flag(s)

TC2	TC1	TO	PD	OV	Z	AC	C
–	–	–	–	–	–	–	–

RLC [m]   Rotate data memory left through carry

Description   The contents of the specified data memory and the carry flag are together rotated left one bit. Bit 7 replaces the carry bit; the original carry flag is rotated into the bit 0 position.

Operation   [m].(i+1) ← [m].i; [m].i:bit i of the data memory (i=0-6)
                    [m].0 ← C
                    C ← [m].7

Affected flag(s)

TC2	TC1	TO	PD	OV	Z	AC	C
–	–	–	–	–	–	–	√

RLCA [m]   Rotate left through carry-place result in accumulator

Description   Data in the specified data memory and the carry flag are together rotated left one bit. Bit 7 replaces the carry bit and the original carry flag is rotated into bit 0 position. The rotated result is stored in the accumulator but the contents of the data memory remain unchanged.

Operation   ACC.(i+1) ← [m].i; [m].i:bit i of the data memory (i=0-6)
                    ACC.0 ← C
                    C ← [m].7

Affected flag(s)

TC2	TC1	TO	PD	OV	Z	AC	C
–	–	–	–	–	–	–	√

RR [m]   Rotate data memory right

Description   The contents of the specified data memory are rotated right one bit with bit 0 rotated to bit 7.

Operation $[m].i \leftarrow [m].(i+1)$; $[m].i$:bit i of the data memory (i=0-6)
$[m].7 \leftarrow [m].0$

Affected flag(s)

TC2	TC1	TO	PD	OV	Z	AC	C
–	–	–	–	–	–	–	–

RRA [m]   Rotate right-place result in accumulator

Description   Data in the specified data memory is rotated right one bit with bit 0 rotated into bit 7, leaving the rotated result in the accumulator. The contents of the data memory remain unchanged.

Operation $ACC.(i) \leftarrow [m].(i+1)$; $[m].i$:bit i of the data memory (i=0-6)
$ACC.7 \leftarrow [m].0$

Affected flag(s)

TC2	TC1	TO	PD	OV	Z	AC	C
–	–	–	–	–	–	–	–

RRC [m]   Rotate data memory right through carry

Description   The contents of the specified data memory and the carry flag are together rotated right one bit. Bit 0 replaces the carry bit; the original carry flag is rotated into the bit 7 position.

Operation $[m].i \leftarrow [m].(i+1)$; $[m].i$:bit i of the data memory (i=0-6)
$[m].7 \leftarrow C$
$C \leftarrow [m].0$

Affected flag(s)

TC2	TC1	TO	PD	OV	Z	AC	C
–	–	–	–	–	–	–	√

RRCA [m]   Rotate right through carry-place result in accumulator

Description   Data of the specified data memory and the carry flag are together rotated
                        right one bit. Bit 0 replaces the carry bit and the original carry flag is rotated
                        into the bit 7 position. The rotated result is stored in the accumulator. The
                        contents of the data memory remain unchanged.

Operation $ACC.i \leftarrow [m].(i+1)$; [m].i:bit i of the data memory (i=0-6)
                        $ACC.7 \leftarrow C$
                        $C \leftarrow [m].0$

Affected flag(s)

TC2	TC1	TO	PD	OV	Z	AC	C
–	–	–	–	–	–	–	√

SBC A,[m]   Subtract data memory and carry from accumulator

Description   The contents of the specified data memory and the complement of the carry
                        flag are together subtracted from the accumulator, leaving the result in the
                        accumulator.

Operation $ACC \leftarrow ACC+[\overline{m}]+C$

Affected flag(s)

TC2	TC1	TO	PD	OV	Z	AC	C
–	–	–	–	√	√	√	√

SBCM A,[m]   Subtract data memory and carry from accumulator

Description   The contents of the specified data memory and the complement of the carry
                        flag are together subtracted from the accumulator, leaving the result in the
                        data memory.

Operation $[m] \leftarrow ACC+[\overline{m}]+C$

Affected flag(s)

TC2	TC1	TO	PD	OV	Z	AC	C
–	–	–	–	√	√	√	√

SDZ [m]   Skip if decrement data memory is zero

Description   The contents of the specified data memory are decremented by one. If the result is zero, the next instruction is skipped. If the result is zero, the following instruction, fetched during the current instruction execution, is discarded and a dummy cycle replaced to get the proper instruction. This makes a 2 cycle instruction. Otherwise proceed with the next instruction.

Operation   Skip if ([m]−1)=0, [m] ← ([m]−1)

Affected flag(s)

TC2	TC1	TO	PD	OV	Z	AC	C
–	–	–	–	–	–	–	–

SDZA [m]   Decrement data memory-place result in ACC, skip if zero

Description   The contents of the specified data memory are decremented by one. If the result is zero, the next instruction is skipped. The result is stored in the accumulator but the data memory remains unchanged. If the result is zero ,the following instruction, fetched during the current instruction execution, is discarded and a dummy cycle is replaced to get the proper instruction, that makes a 2 cycle instruction. Otherwise proceed with the next instruction.

Operation   Skip if ([m]−1)=0, ACC ← ([m]−1)

Affected flag(s)

TC2	TC1	TO	PD	OV	Z	AC	C
–	–	–	–	–	–	–	–

SET [m]   Set data memory

Description   Each bit of the specified data memory is set to one.

Operation   [m] ← FFH

Affected flag(s)

TC2	TC1	TO	PD	OV	Z	AC	C
–	–	–	–	–	–	–	–

SET [m].i   Set bit of data memory

Description   Bit i of the specified data memory is set to one.

Operation   [m].i ← 1

Affected flag(s)

TC2	TC1	TO	PD	OV	Z	AC	C
–	–	–	–	–	–	–	–

SIZ [m]   Skip if increment data memory is zero

Description   The contents of the specified data memory is incremented by one. If the result is zero, the following instruction, fetched during the current instruction execution, is discarded and a dummy cycle is replaced to get the proper instruction. This is a 2 cycle instruction. Otherwise proceed with the next instruction.

Operation   Skip if ([m]+1)=0, [m] ← ([m]+1)

Affected flag(s)

TC2	TC1	TO	PD	OV	Z	AC	C
–	–	–	–	–	–	–	–

SIZA [m]   Increment data memory-place result in ACC, skip if zero

Description   The contents of the specified data memory is incremented by one. If the result is zero, the next instruction is skipped and the result stored in the accumulator. The data memory remains unchanged. If the result is zero, the following instruction, fetched during the current instruction execution, is discarded and a dummy cycle replaced to get the proper instruction. This is a 2 cycle instruction. Otherwise proceed with the next instruction.

Operation   Skip if ([m]+1)=0, ACC ← ([m]+1)

Affected flag(s)

TC2	TC1	TO	PD	OV	Z	AC	C
–	–	–	–	–	–	–	–

SNZ [m].i   Skip if bit i of the data memory is not zero

Description   If bit i of the specified data memory is not zero, the next instruction is skipped. If bit i of the data memory is not zero, the following instruction, fetched during the current instruction execution, is discarded and a dummy cycle is replaced to get the proper instruction. This is a 2 cycle instruction. Otherwise proceed with the next instruction.

Operation   Skip if [m].i≠0

Affected flag(s)

TC2	TC1	TO	PD	OV	Z	AC	C
–	–	–	–	–	–	–	–

SUB A,[m]   Subtract data memory from accumulator

Description   The specified data memory is subtracted from the contents of the accumulator, leaving the result in the accumulator.

Operation $ACC \leftarrow ACC+[\overline{m}]+1$

Affected flag(s)

TC2	TC1	TO	PD	OV	Z	AC	C
–	–	–	–	√	√	√	√

SUBM A,[m]   Subtract data memory from accumulator

Description   The specified data memory is subtracted from the contents of the accumulator, leaving the result in the data memory.

Operation $[m] \leftarrow ACC\ [\overline{m}]+1$

Affected flag(s)

TC2	TC1	TO	PD	OV	Z	AC	C
–	–	–	–	√	√	√	√

SUB A,x   Subtract immediate data from accumulator

Description   The immediate data specified by the code is subtracted from the contents of the accumulator, leaving the result in the accumulator.

Operation $ACC \leftarrow ACC+\overline{x}+1$

Affected flag(s)

TC2	TC1	TO	PD	OV	Z	AC	C
–	–	–	–	√	√	√	√

SWAP [m]   Swap nibbles within the data memory

Description   The low-order and high-order nibbles of the specified data memory (one of the data memory) are interchanged.

Operation   [m].3~[m].0 ↔ [m].7~[m].4

Affected flag(s)

TC2	TC1	TO	PD	OV	Z	AC	C
–	–	–	–	–	–	–	–

SWAPA [m]   Swap data memory-place result in accumulator

escription   The low-order and high-order nibbles of the specified data memory are interchanged, writing the result to the accumulator. The contents of the data memory remain unchanged.

Operation   ACC.3~ACC.0 ← [m].7~[m].4
ACC.7~ACC.4 ← [m].3~[m].0

Affected flag(s)

TC2	TC1	TO	PD	OV	Z	AC	C
–	–	–	–	–	–	–	–

SZ [m]   Skip if data memory is zero

Description   If the contents of the specified data memory is zero, the following instruction, fetched during the current instruction execution, is discarded and a dummy cycle is replaced to get the proper instruction. This is a 2 cycle instruction. Otherwise proceed with the next instruction.

Operation   Skip if [m]=0

Affected flag(s)

TC2	TC1	TO	PD	OV	Z	AC	C
–	–	–	–	–	–	–	–

SZA [m]   Move data memory to ACC, skip if zero

Description   The contents of the specified data memory is copied to accumulator. If the contents is zero, the following instruction, fetched during the current instruction execution, is discarded and a dummy cycle is replaced to get the proper instruction. This is a 2 cycle instruction. Otherwise proceed with the next instruction.

Operation   Skip if [m]=0

Affected flag(s)

TC2	TC1	TO	PD	OV	Z	AC	C
–	–	–	–	–	–	–	–

SZ [m].i   Skip if bit i of the data memory is zero

Description   If bit i of the specified data memory is zero, the following instruction, fetched during the current instruction execution, is discarded and a dummy cycle is replaced to get the proper instruction. This is a 2 cycle instruction. Otherwise proceed with the next instruction.

Operation   Skip if [m].i=0

Affected flag(s)

TC2	TC1	TO	PD	OV	Z	AC	C
–	–	–	–	–	–	–	–

TABRDC [m]   Move ROM code (current page) to TBLH & data memory

Description   The low byte of ROM code (current page) addressed by the table pointer (TBLP) is moved to the specified data memory and the high byte transfered to TBLH directly.

Operation   [m] ← ROM code (low byte)
                        TBLH ← ROM code (high byte)

Affected flag(s)

TC2	TC1	TO	PD	OV	Z	AC	C
–	–	–	–	–	–	–	–

TABRDL [m] Move ROM code (last page) to TBLH & data memory

Description The low byte of ROM code (last page) addressed by the table pointer (TBLP) is moved to the data memory and the high byte transfered to TBLH directly.

Operation $[m] \leftarrow$ ROM code (low byte)
$TBLH \leftarrow$ ROM code (high byte)

Affected flag(s)

TC2	TC1	TO	PD	OV	Z	AC	C
–	–	–	–	–	–	–	–

XOR A,[m] Logical XOR accumulator with data memory

Description Data in the accumulator and the indicated data memory performs a bitwise logical Exclusive_OR operation and the result is stored in the accumulator.

Operation $ACC \leftarrow ACC$ "XOR" $[m]$

Affected flag(s)

TC2	TC1	TO	PD	OV	Z	AC	C
–	–	–	–	–	√	–	–

XORM A,[m] Logical XOR data memory with accumulator

Description Data in the indicated data memory and the accumulator perform a bitwise logical Exclusive_OR operation. The result is stored in the data memory. The zero flag is affected.

Operation $[m] \leftarrow ACC$ "XOR" $[m]$

Affected flag(s)

TC2	TC1	TO	PD	OV	Z	AC	C
–	–	–	–	–	√	–	–

XOR A,x Logical XOR immediate data to accumulator

Description Data in the the accumulator and the specified data perform a bitwise logical Exclusive_OR operation. The result is stored in the accumulator. The zero flag is affected.

Operation $ACC \leftarrow ACC$ "XOR" x

Affected flag(s)

TC2	TC1	TO	PD	OV	Z	AC	C
–	–	–	–	–	√	–	–