ADE-203-053F (Z)

HN58V257 Series

32768-word × 8-bit Electrically Erasable and Programmable CMOS ROM

Rev. 6.0
May. 25, 1995

HITACHI

The Hitachi HN58V257 is a electically erasable and programmable ROM organized as 32768-word × 8-bit. It realizes high speed, low power consumption, and a high level of reliability, employing advanced MNOS memory technology and CMOS process and circuitry technology. It also has a 64-byte page programming function to make its erase and write operations faster.

Features

- Single 3 V supply
- On-chip latches: address, data, $\overline{\text{CE}}$, $\overline{\text{OE}}$, $\overline{\text{WE}}$
- Automatic byte write: 15 ms max
- Automatic page write (64 bytes): 15 ms max
- Fast access time: 350 ns max
- Low power dissipation:
  20 mW/MHz typ (active)
  110 µW max (standby)
- $\overline{\text{Data}}$ polling, RDY/$\overline{\text{Busy}}$
- Data protection circuit on power on/off
- Conforms to JEDEC byte-wide standard
- Reliable CMOS with MNOS cell technology
- 10^5 erase/write cycles (in page mode)
- 10 years data retention
- Write protection by $\overline{\text{RES}}$ pin

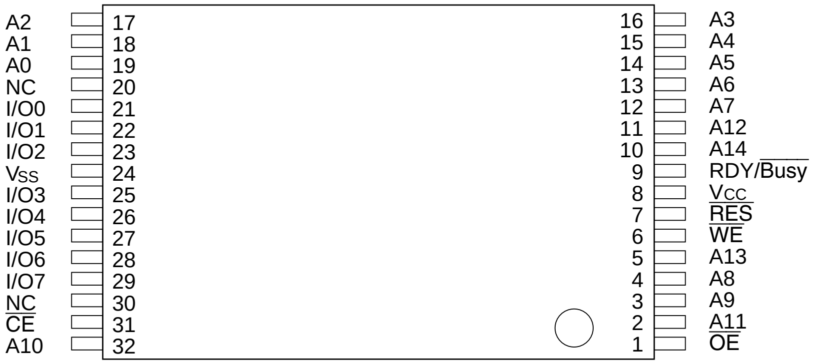
Ordering Information

Type no.	Access time	Package
HN58V257T-35	350 ns	32-pin plastic TSOP (TFP-32DA)

Hitachi
semiconductor

Pin Arrangement

HN58V257T Series

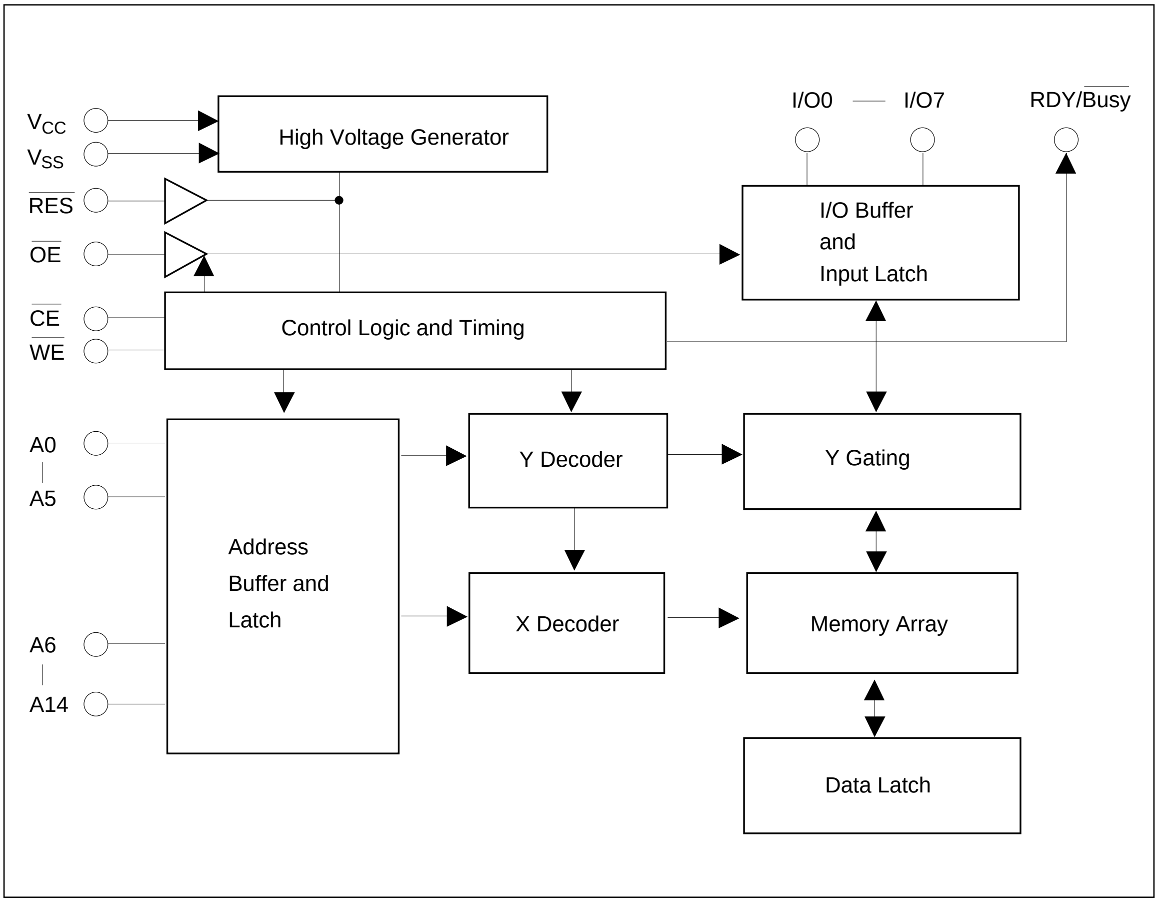


(Top view)

Pin Description

Pin name	**Function**
A0–A14	Address inputs
I/O0–I/O7	Data input/output
$\overline{\text{OE}}$	Output enable
$\overline{\text{CE}}$	Chip enable
$\overline{\text{WE}}$	Write enable
V_{CC}	Power (+3 V)
V_{SS}	Ground
$\overline{\text{RES}}$	Reset
RDY/$\overline{\text{Busy}}$	Ready /$\overline{\text{Busy}}$

Block Diagram



Mode Selection

Pin Mode	$\overline{\text{CE}}$ (31)	$\overline{\text{OE}}$ (1)	$\overline{\text{WE}}$ (6)	RDY/$\overline{\text{Busy}}$ (9)	$\overline{\text{RES}}$ (7)	I/O (21-23, 25-29)
Read	V_{IL}	V_{IL}	V_{IH}	High-Z	V_H*1	Dout
Standby	V_{IH}	×*2	×	High-Z	×	High-Z
Write	V_{IL}	V_{IH}	V_{IL}	High-Z to V_{OL}	V_H	Din
Deselect	V_{IL}	V_{IH}	V_{IH}	High-Z	V_H	High-Z
Write inhibit	×	×	V_{IH}	High-Z	×	—
	×	V_{IL}	×			
$\overline{\text{Data}}$ polling	V_{IL}	V_{IL}	V_{IH}	V_{OL}	V_H	Data out (I/O7)
Program reset	×	×	×	High-Z	V_{IL}	High-Z

Note: 1. Refer to the recommended DC operating condition.
2. × = Don’t care

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage [*1]	V_{CC}	–0.6 to +7.0	V
Input voltage [*1]	Vin	–0.5[*2] to +7.0	V
Operationg temperature range [*3]	Topr	0 to +70	°C
Storage temperature range	Tstg	–55 to +125	°C

Notes: 1. With respect to V_{SS}
2. Vin min = –3.0 V for pulse width ≤ 50 ns
3. Including electrical characteristics and data retention

Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	2.7	3.0	5.5	V
Input voltage	V_{IL}	–0.3	—	0.8	V
	V_{IH}	1.9	—	V_{CC} + 0.3	V
	V_H	V_{CC} – 0.5	—	V_{CC} + 1.0	V
Operating temperature	Topr	0	—	70	°C

DC Characteristics (Ta=0 to +70°C, V_{CC} = 2.7 to 5.5V)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	I_{LI}	—	—	2[*1]	µA	V_{CC} = 5.5 V, Vin = 5.5 V
Output leakage current	I_{LO}	—	—	2	µA	V_{CC} = 5.5 V, Vout = 5.5/0.4 V
V_{CC} current (standby)	I_{CC1}	—	—	20	µA	$\overline{CE}$ = V_{CC}
	I_{CC2}	—	—	1	mA	$\overline{CE}$ = V_{IH}
V_{CC} current (active)	I_{CC3}	—	—	8	mA	Iout = 0 mA, Duty = 100%, Cycle = 1 µs at V_{CC} = 3.6 V
		—	—	20	mA	Iout = 0 mA, Duty = 100%, Cycle = 350 ns at V_{CC} = 3.6 V
Input low voltage	V_{IL}	–0.3[*2]	—	0.8	V	
Input high voltage	V_{IH}	1.9[*3]	—	V_{CC} + 0.3	V	
	V_H	V_{CC}–0.5	—	V_{CC} + 1.0	V	
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2.1 mA
Output high voltage	V_{OH}	$V_{CC} \times 0.8$	—	—	V	I_{OH} = –400 µA

Note: 1. I_{LI} on $\overline{RES}$ = 100 µA max
2. V_{IL} min = –1.0 V for pulse width ≤ 50 ns
3. V_{IH} min = 2.2 V for V_{CC} = 3.6 to 5.5 V.

Capacitance (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test condition
Input capacitance[*1]	Cin	—	—	6	pF	Vin = 0 V
Output capacitance[*1]	Cout	—	—	12	pF	Vout = 0 V

Note: 1. This parameter is periodically sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 2.7 to 5.5V)

Test Conditions

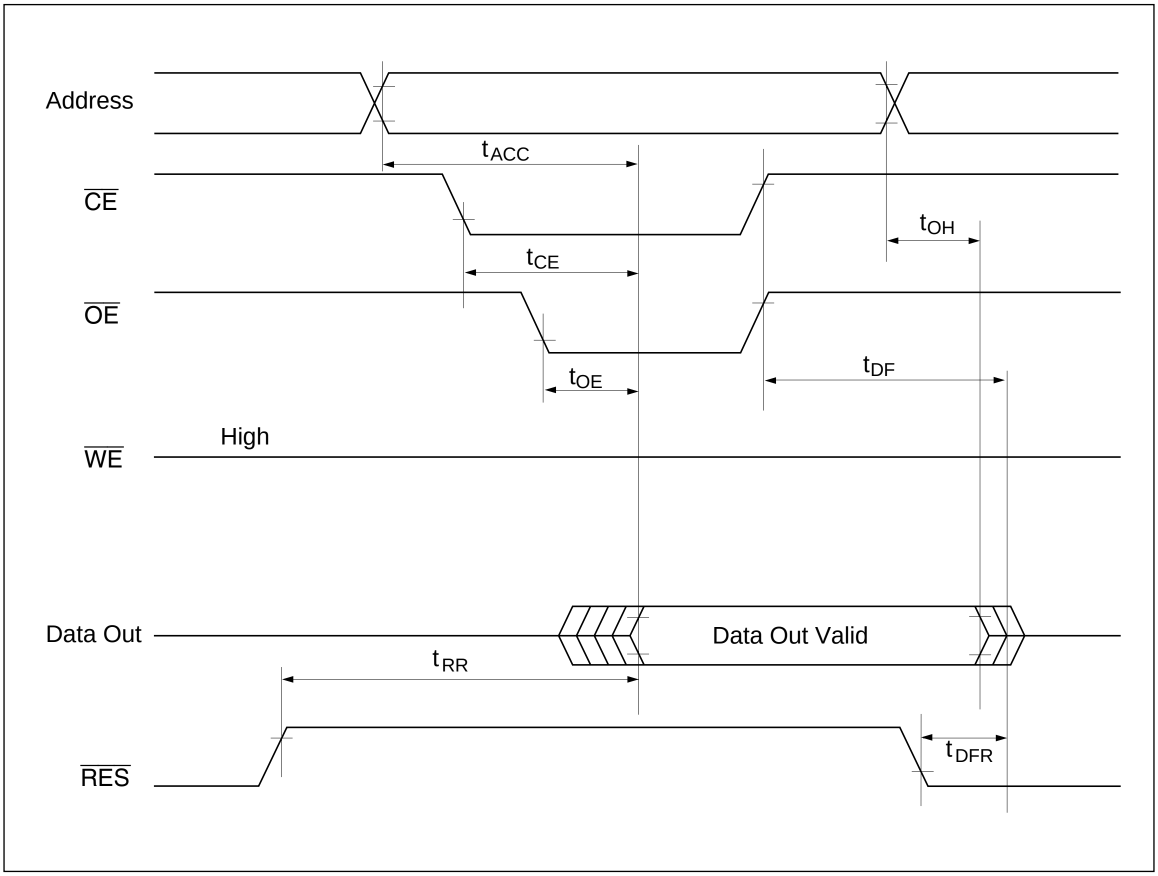
- Input pulse levels : 0.4 V to 2.4 V
  0 V to V_{CC} ($\overline{\text{RES}}$ pin)
- Input rise and fall time : ≤ 20 ns
- Output load : 1TTL Gate +100 pF
- Reference levels for measuring timing : 0.8 V, 1.8 V

Read Cycle

Parameter	Symbol	Min	Max	Unit	Test conditions
Address to output delay	t_{ACC}	—	350	ns	$\overline{\text{CE}} = \overline{\text{OE}} = V_{IL}$, $\overline{\text{WE}} = V_{IH}$
$\overline{\text{CE}}$ to output delay	t_{CE}	—	350	ns	$\overline{\text{OE}} = V_{IL}$, $\overline{\text{WE}} = V_{IH}$
$\overline{\text{OE}}$ to output delay	t_{OE}	10	150	ns	$\overline{\text{CE}} = V_{IL}$, $\overline{\text{WE}} = V_{IH}$
$\overline{\text{OE}}$ ($\overline{\text{CE}}$) high to output float[*1]	t_{DF}	0	90	ns	$\overline{\text{CE}} = V_{IL}$, $\overline{\text{WE}} = V_{IH}$
$\overline{\text{RES}}$ low to output float[*1]	t_{DFR}	0	350	ns	$\overline{\text{CE}} = \overline{\text{OE}} = V_{IL}$, $\overline{\text{WE}} = V_{IH}$
Data output hold	t_{OH}	0	—	ns	$\overline{\text{CE}} = \overline{\text{OE}} = V_{IL}$, $\overline{\text{WE}} = V_{IH}$
$\overline{\text{RES}}$ to output delay	t_{RR}	0	600	ns	$\overline{\text{CE}} = \overline{\text{OE}} = V_{IL}$, $\overline{\text{WE}} = V_{IH}$

Note: 1. t_{DF}, t_{DFR} are defined at which the outputs achieve the open circuit conditions and are no longer driven.

Read Timing Waveform



Write Cycle

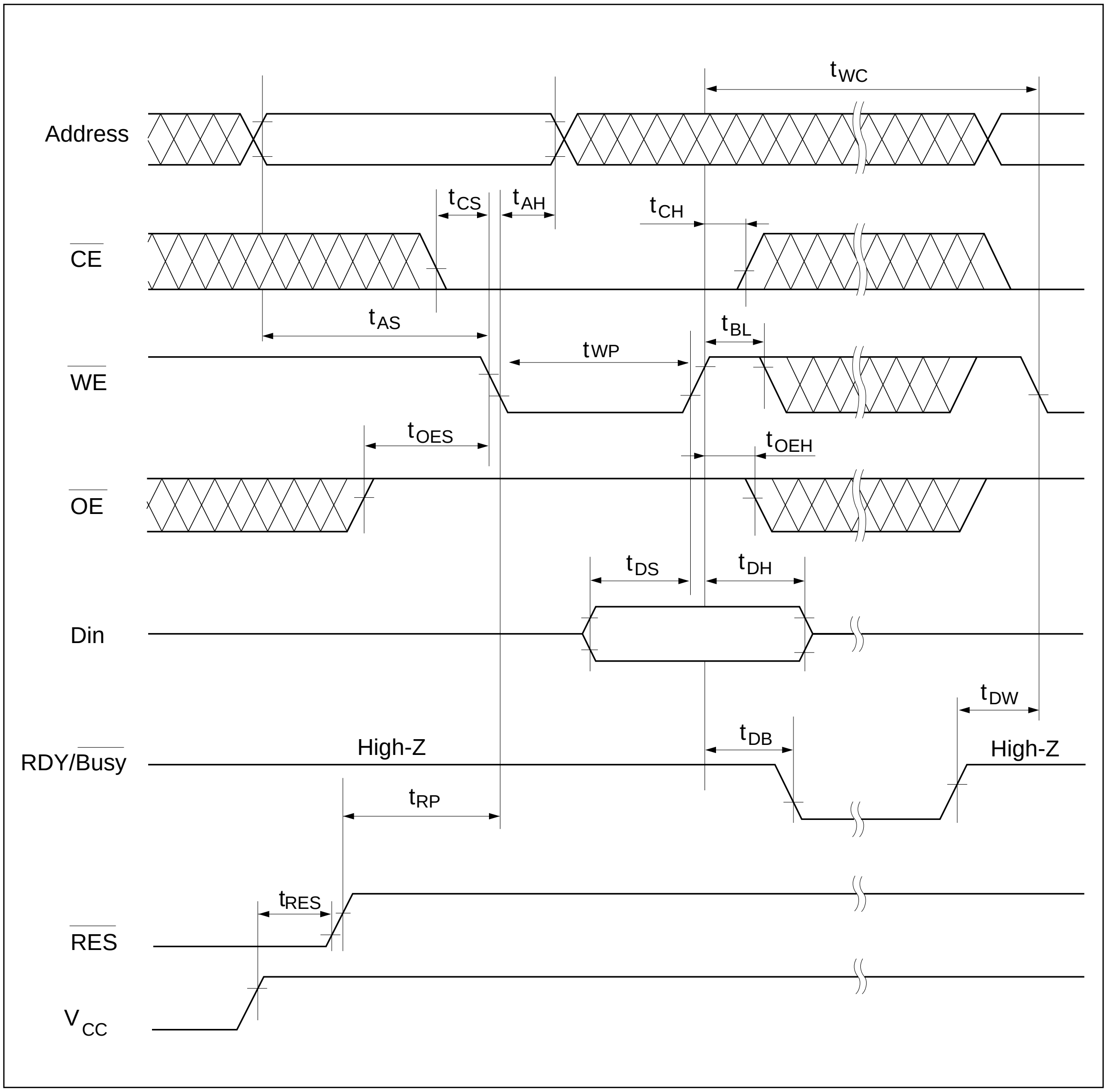
Parameter	Symbol	Min[*1]	Typ	Max	Unit	Test conditions
Address setup time	t_{AS}	0	—	—	ns	
Address hold time	t_{AH}	200	—	—	ns	
$\overline{\text{CE}}$ write setup time ($\overline{\text{WE}}$ controlled)	t_{CS}	0	—	—	ns	
$\overline{\text{CE}}$ hold time ($\overline{\text{WE}}$ controlled)	t_{CH}	0	—	—	ns	
$\overline{\text{WE}}$ to write setup time ($\overline{\text{CE}}$ controlled)	t_{WS}	0	—	—	ns	
$\overline{\text{WE}}$ hold time ($\overline{\text{CE}}$ controlled)	t_{WH}	0	—	—	ns	
$\overline{\text{OE}}$ to write setup time	t_{OES}	0	—	—	ns	
$\overline{\text{OE}}$ hold time	t_{OEH}	0	—	—	ns	
Data setup time	t_{DS}	150	—	—	ns	
Data hold time	t_{DH}	0	—	—	ns	
$\overline{\text{WE}}$ pulse width ($\overline{\text{WE}}$ controlled)	t_{WP}	250	—	—	ns	
$\overline{\text{CE}}$ pulse width ($\overline{\text{CE}}$ controlled)	t_{CW}	250	—	—	ns	
Data latch time	t_{DL}	300	—	—	ns	
Byte load cycle	t_{BLC}	0.55	—	30	µs	
Byte load window	t_{BL}	100	—	—	µs	
Write cycle time	t_{WC}	—	—	15[*2]	ms	
Time to device busy	t_{DB}	120	—	—	ns	
Write start time	t_{DW}	250[*3]	—	—	ns	
Reset protect time	t_{RP}	100	—	—	µs	
Reset low time	t_{RES}	1	—	—	µs	

Note: 1. Use this device in longer cycle than this value.

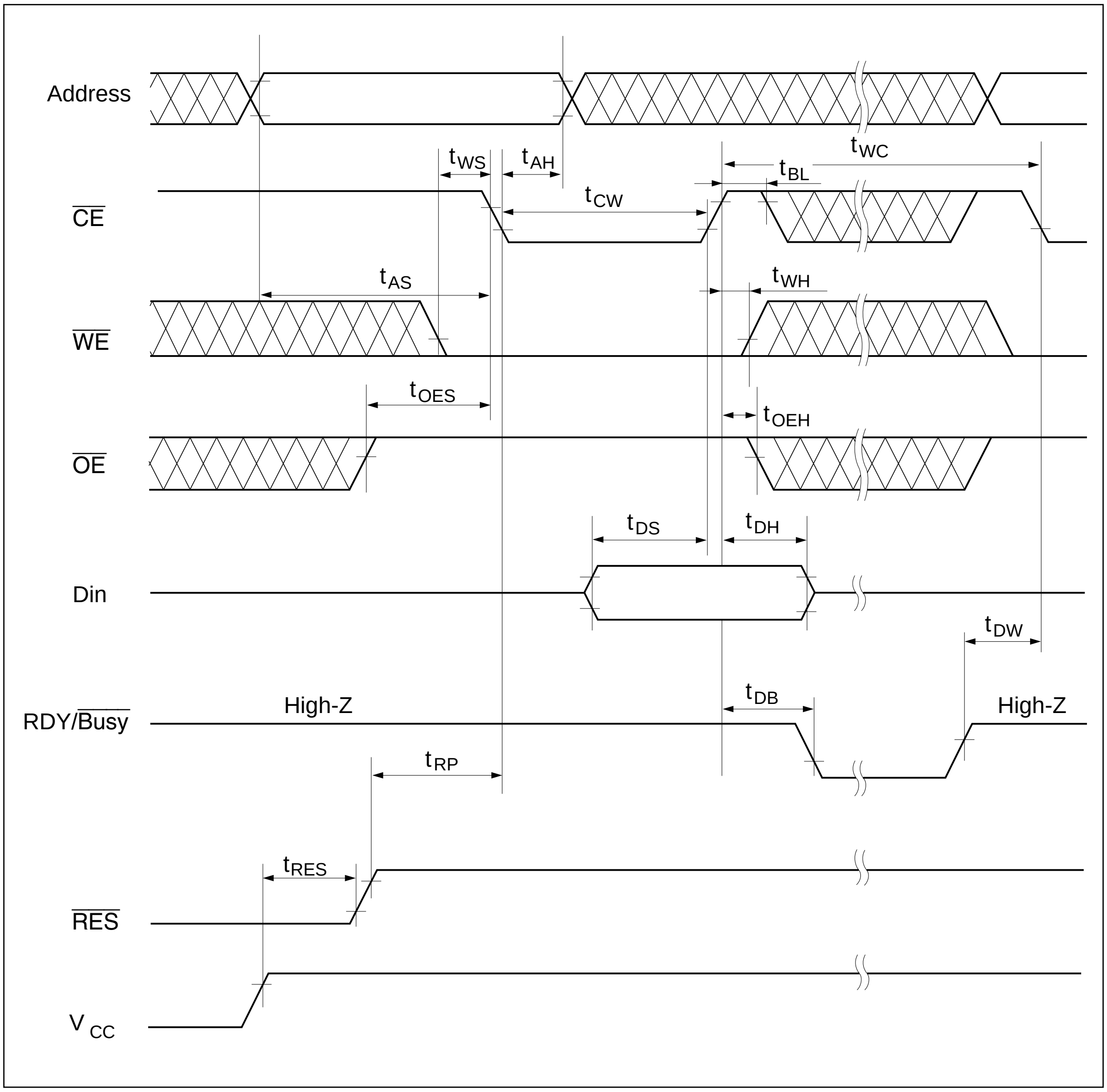
2. t_{WC} must be longer than this value unless polling technique or RDY/$\overline{\text{Busy}}$ are used. This device automatically completes the internal write operation within this value.

3. Next read or write operation can be initiated after t_{DW} if polling technique or RDY/$\overline{\text{Busy}}$ are used.

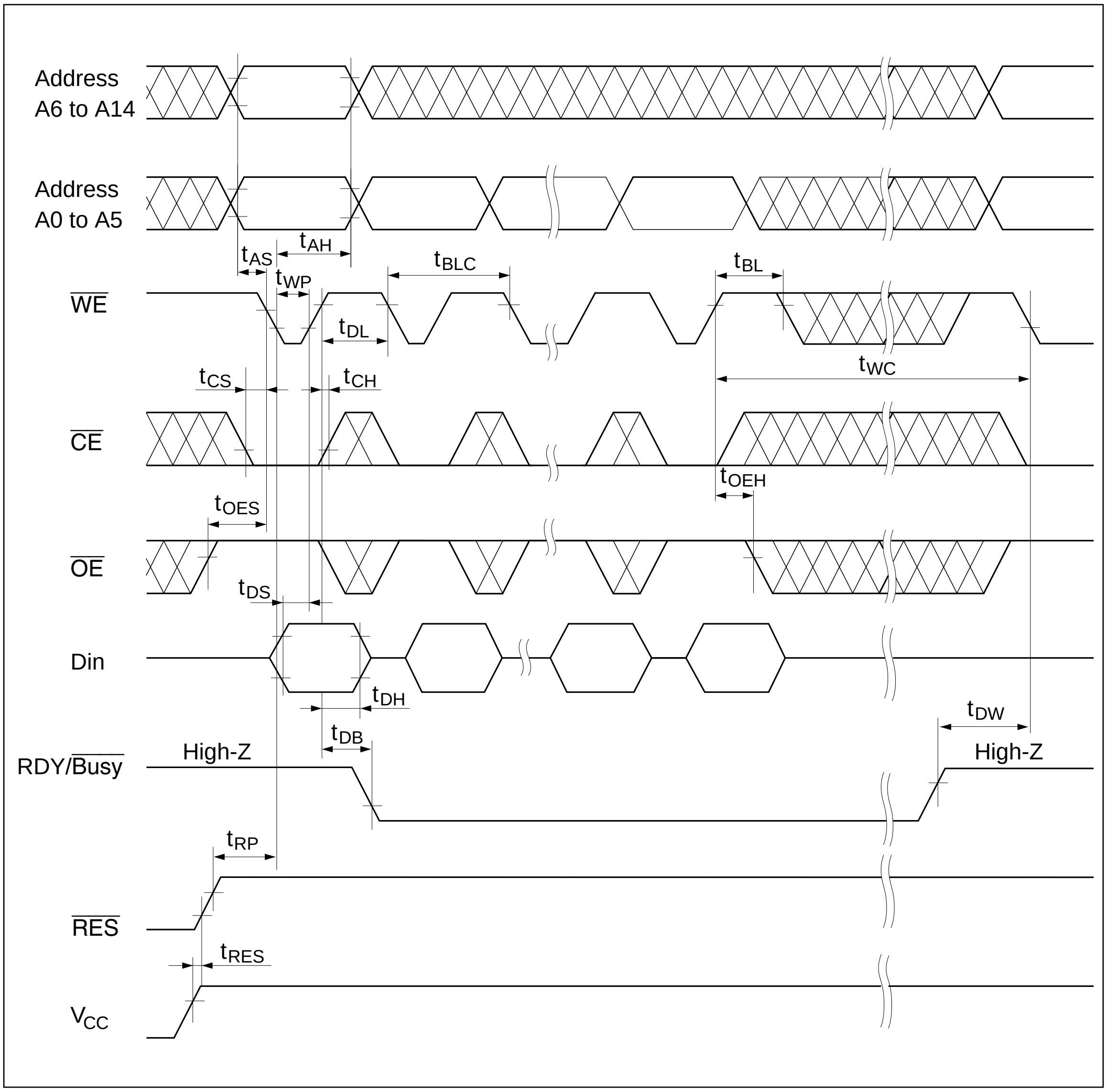
Byte Write Timing Waveform(1) ($\overline{\text{WE}}$ Controlled)



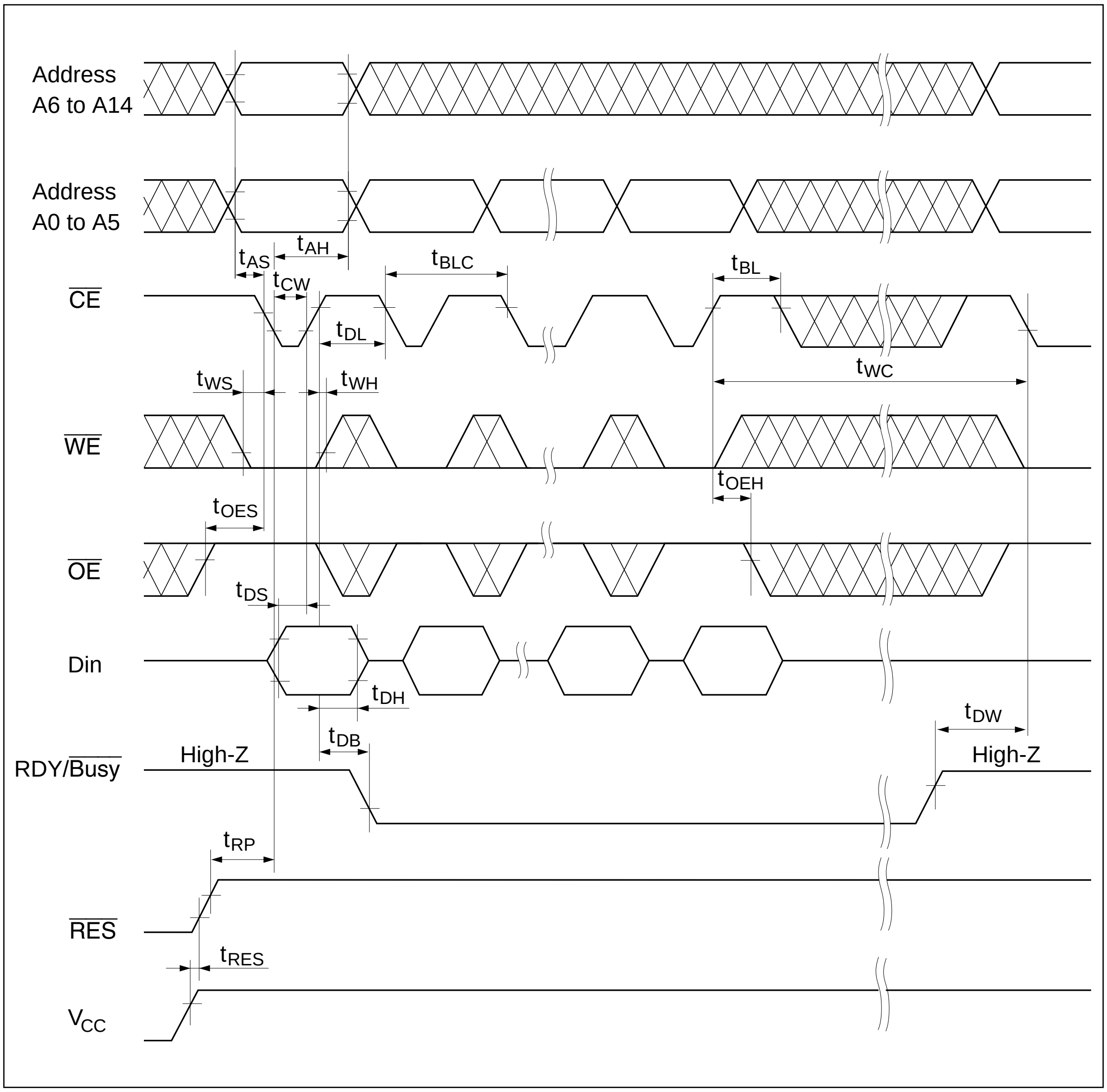
Byte Write Timing Waveform(2) ($\overline{CE}$ Controlled)



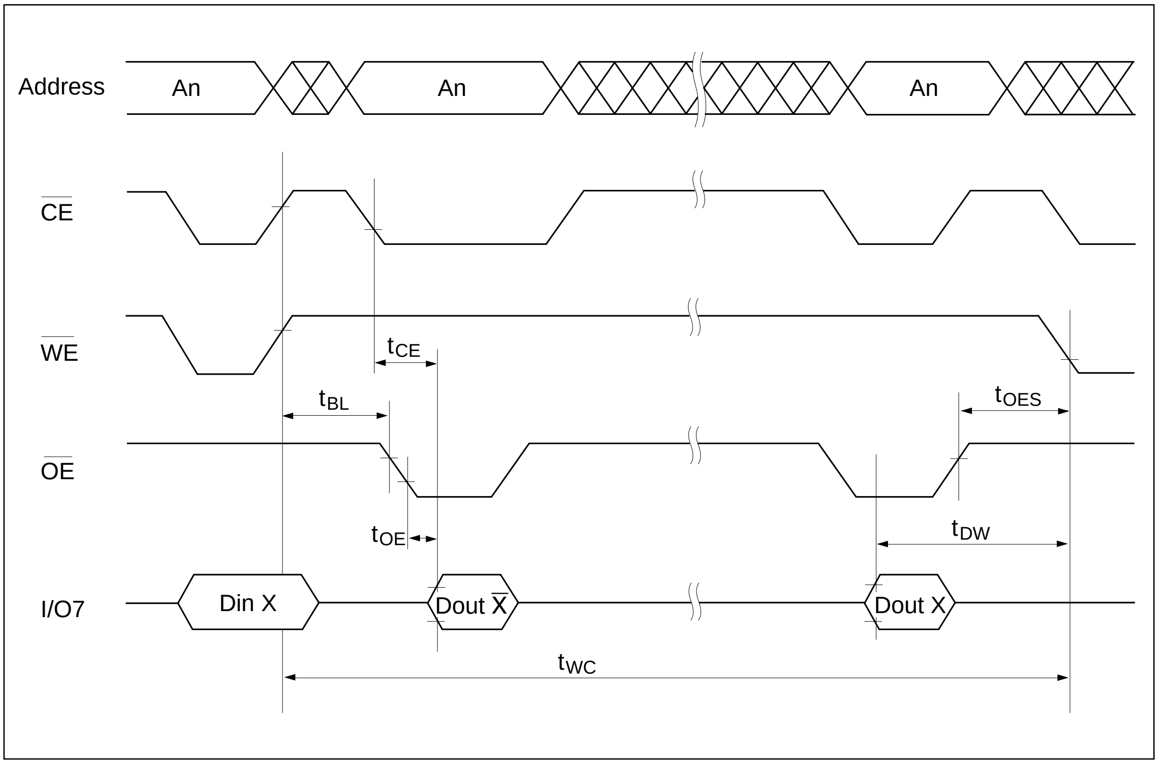
Page Write Timing Waveform(1) ($\overline{\text{WE}}$ Controlled)



Page Write Timing Waveform(2) ($\overline{\text{CE}}$ Controlled)



$\overline{\text{Data}}$ Polling Timing Waveform



Functional Description

Automatic Page Write

Page-mode write feature allows 1 to 64 bytes of data to be written into the EEPROM in a single write cycle. Following the initial byte cycle, an additional 1 to 63 bytes can be written in the same manner. Each additional byte load cycle must be started within 30 µs from the preceding falling edge of $\overline{\text{WE}}$ or $\overline{\text{CE}}$. When $\overline{\text{CE}}$ or $\overline{\text{WE}}$ is high for 100 µs after data input, the EEPROM enters write mode automatically and the input data are written into the EEPROM.

$\overline{\text{Data}}$ Polling

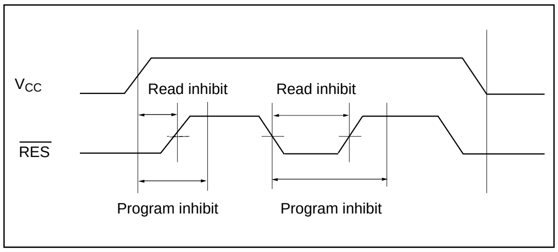
$\overline{\text{Data}}$ polling allows the status of the EEPROM to be determined. If EEPROM is set to read mode during a write cycle, an inversion of the last byte of data to be loaded outputs from I/O7 to indicate that the EEPROM is performing a write operation.

RDY/$\overline{\text{Busy}}$ Signal

RDY/$\overline{\text{Busy}}$ signal also allows the status of the EEPROM to be determined. The RDY/$\overline{\text{Busy}}$ signal has high impedance except in write cycle and is lowered to V_{OL} after the first write signal. At the end of a write cycle, the RDY/$\overline{\text{Busy}}$ signal changes state to high impedance.

$\overline{\text{RES}}$ Signal

When $\overline{\text{RES}}$ is low, the EEPROM cannot be read or programmed. Therefore, data can be protected by keeping $\overline{\text{RES}}$ low when V_{CC} is switched. $\overline{\text{RES}}$ should be high during read and programming because it doesn't provide a latch function.



$\overline{\text{WE}}$, $\overline{\text{CE}}$ Pin Operation

During a write cycle, addresses are latched by the falling edge of $\overline{\text{WE}}$ or $\overline{\text{CE}}$, and data is latched by the rising edge of $\overline{\text{WE}}$ or $\overline{\text{CE}}$.

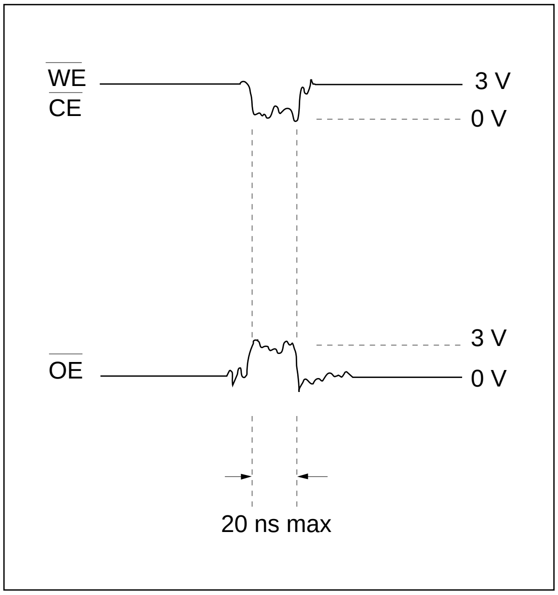
Write/Erase Endurance and Data Retention Time

The endurance is 10^5 cycles in case of the page programming and 10^4 cycles in case of byte programming (1% cumulative failure rate). The data retention time is more than 10 years when a device is page-programmed less than 10^4 cycles.

Data Protection

1.Data Protection against Noise on Control Pins ($\overline{\text{CE}}$, $\overline{\text{OE}}$, $\overline{\text{WE}}$) during Operation

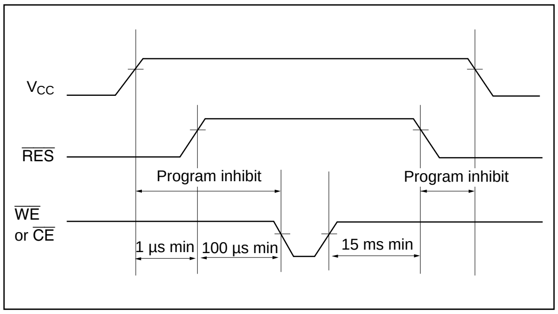
During readout or standby, noise on the control pins may act as a trigger and turn the EEPROM to programming mode by mistake.
To prevent this phenomenon, this device has a noise cancelation function that cuts noise if its width is 20 ns or less in program mode.
Be careful not to allow noise of a width of more than 20 ns on the control pins.



2. Data Protection at V_{CC} On/Off

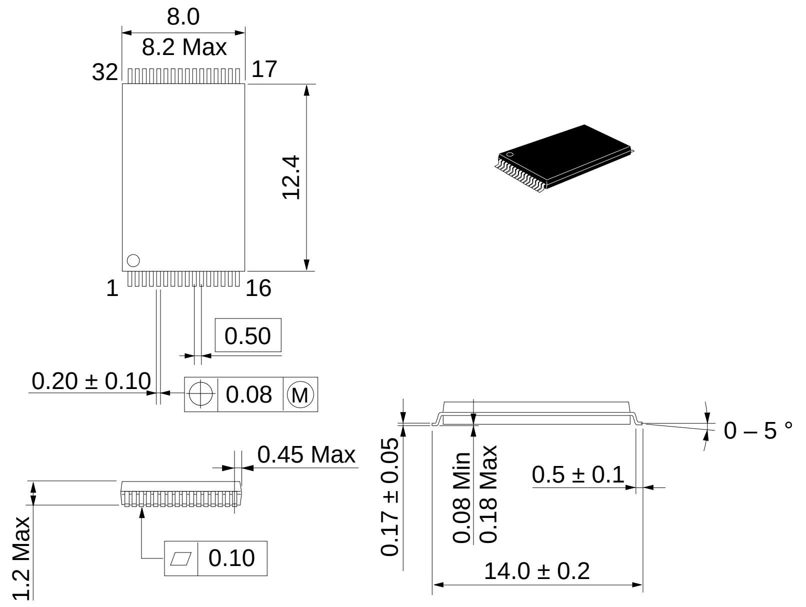
When V_{CC} is turned on or off, noise on the control pins generated by external circuits (CPU, etc) may turn the EEPROM to programming mode by mistake. To prevent this unintentional programming, the EEPROM must be kept in unprogrammable state by using a CPU reset signal to $\overline{\text{RES}}$ pin. $\overline{\text{RES}}$ pin should be kept at V_{SS} level when V_{CC} is turned on or off.

The EEPROM breaks off programming operation when $\overline{\text{RES}}$ becomes low, programming operation doesn't finish correctly in case that $\overline{\text{RES}}$ falls low during programming operation. $\overline{\text{RES}}$ should be kept high for 15 ms after the last data input.



Package Dimensions

HN58V257T Series (TFP-32DA) **Unit : mm**



HN58V256A Series
HN58V257A Series

Preliminary

32768-word x 8-bit Electrically Erasable and Programmable CMOS ROM

HITACHI

Rev. 0.0
Mar. 15, 1995

The Hitachi HN58V256A and HN58V257A are a electrically erasable and programmable EEPROM's organized as 32768-word × 8-bit. Employing advanced MNOS memory technology and CMOS process and circuitry technology. They also have a 64-byte page programming function to make their write operations faster.

Features

- Single 2.7 to 5.5 V supply
- On-chip latches: address, data, $\overline{\text{CE}}$, $\overline{\text{OE}}$, $\overline{\text{WE}}$
- Automatic byte write: 10 ms max
- Automatic page write (64 bytes): 10 ms max
- Fast access time: 120 ns max
- Low power dissipation: 20 mW/MHz, typ (active)
  110 µW max (standby)
- Ready/$\overline{\text{Busy}}$ (♦)[*1]
- $\overline{\text{Data}}$ polling and Toggle bit
- Data protection circuit on power on/off
- Conforms to JEDEC byte-wide standard
- Reliable CMOS with MNOS cell technology
- 10^5 erase/write cycles (in page mode)
- 10 years data retention
- Software data protection
- Write protection by $\overline{\text{RES}}$ pin (♦)[*1]

Notes: 1. All through this datasheet, the mark (♦) indicates the function supported by only the HN58V257A series (32 pin package).

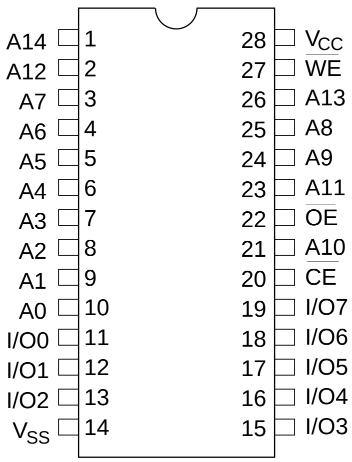
Ordering Information

Type No.	Operating Voltage	Temperature Range	Access Time	Package	Compatible Type No.[*1]
HN58V256AP-12/-15	2.7 to 5.5 V	0 to 70˚C	120/150 ns	600 mil 28-pin plastic DIP(DP-28)	HN58C256P-20
HN58V256AFP-12/-15	2.7 to 5.5V	0 to 70˚C	120/150 ns	400 mil 28-pin plastic SOP (FP-28D)	HN58C256FP-20
HN58V256AFPI-12/-15	2.7 to 5.5 V	–40 to 85˚C			HN58C256FPI-20
HN58V256AT-12/-15	2.7 to 5.5 V	0 to 70˚C	120/150 ns	28-pin plastic TSOP (—)[*2]	
HN58V256AT-12SR /-15SR	2.7 to 5.5 V	–20 to 85˚C			
HN58V257AT-12/-15	2.7 to 5.5 V	0 to 70˚C	120/150 ns	8 × 14 mm 32-pin plastic TSOP (TFP-32DA)	HN58C257T-20 HN58V257T-35
HN58V257AT-12SR /-15SR	2.7 to 5.5 V	–20 to 85˚C			HN58C257T-20SR HN58V257T-35SR

Notes: 1. This type No. can be replaced by the corresponding A–version. (ex. HN58C256P to HN58V256AP)
2. Package type and dimension are under development.

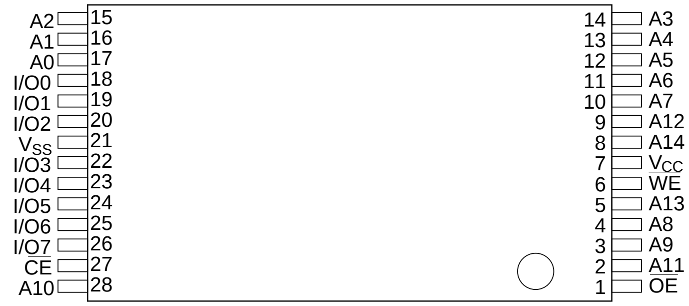
Pin Arrangement

HN58V256AP/AFP Series



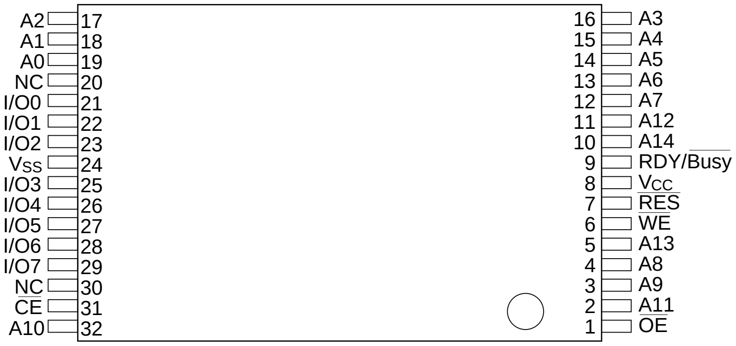
(Top View)

- HN58V256AT Series



(Top View)

- HN58V257AT Series



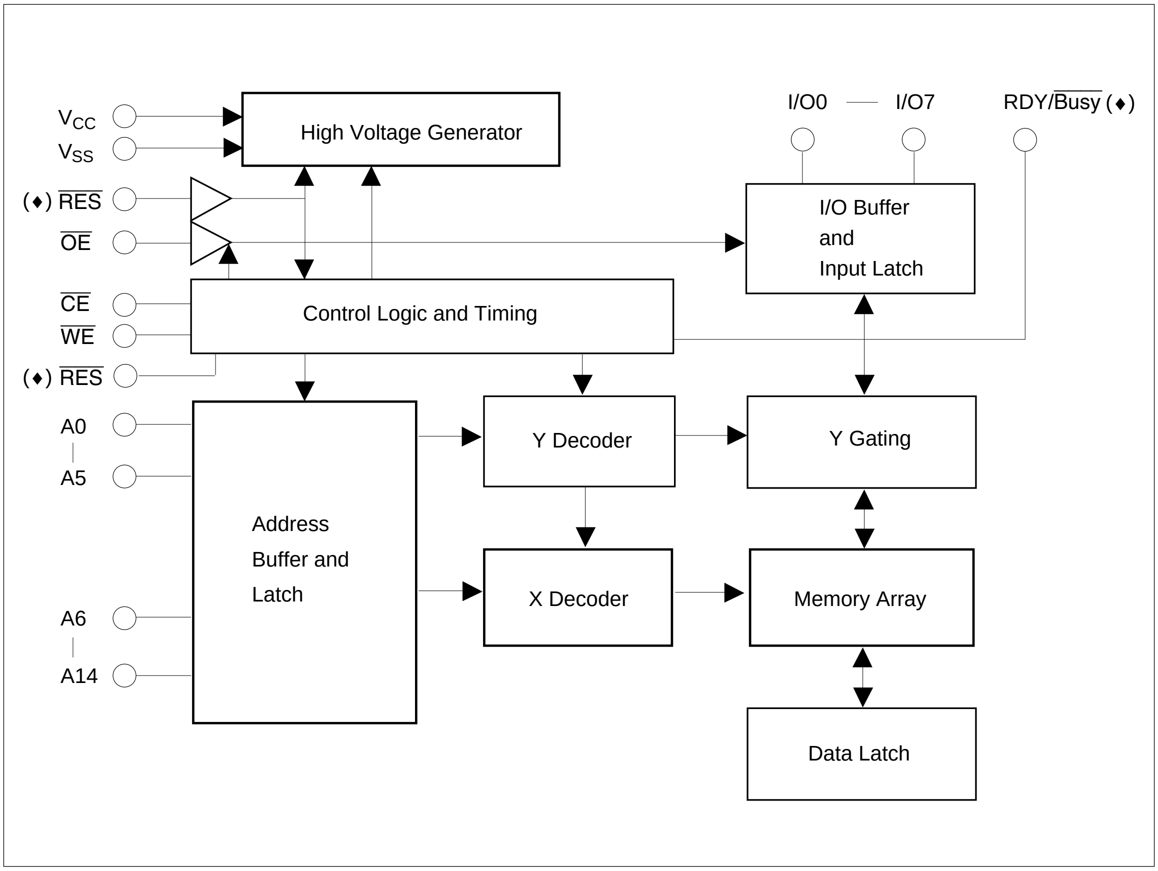
(Top View)

Pin Description

Pin name	Function
A0 to A14	Address
I/O0 to I/O7	Input/output
$\overline{\text{OE}}$	Output enable
$\overline{\text{CE}}$	Chip enable

Pin name	Function
$\overline{\text{WE}}$	Write enable
V_{CC}	Power (+2.7 ~ 5.5 V)
V_{SS}	Ground
RDY/$\overline{\text{Busy}}$ (♦)	Ready busy
$\overline{\text{RES}}$ (♦)	Reset

Block Diagram



Mode Selection

Pin Mode	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	$\overline{\text{RES}}$ (♦)	RDY/$\overline{\text{Busy}}$ (♦)	I/O
Read	V_{IL}	V_{IL}	V_{IH}	V_H*1	High-Z	Dout
Standby	V_{IH}	×*2	×	×	High-Z	High-Z
Write	V_{IL}	V_{IH}	V_{IL}	V_H	High-Z to V_{OL}	Din
Deselect	V_{IL}	V_{IH}	V_{IH}	V_H	High-Z	High-Z
Write Inhibit	×	×	V_{IH}	×	—	—
	×	V_{IL}	×	×	—	—
$\overline{\text{Data}}$ Polling	V_{IL}	V_{IL}	V_{IH}	V_H	V_{OL}	Data out (I/O7)
Program reset	×	×	×	V_{IL}	High-Z	High-Z

Note: 1. Refer to the recommended DC operating condition.
2. × : Don’t care

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Device Group*4
Supply voltage *1	V_{CC}	–0.6 to +7.0	V	A, B, C
Input voltage *1	Vin	–0.5*2 to +7.0	V	A, B, C
Operating temperature range *3	Topr	0 to +70	°C	A
		–20 to 85	˚C	B
		–40 to 85	˚C	C
Storage temperature range	Tstg	–55 to +125	°C	A, B, C

Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Device Group*4
Supply voltage	V_{CC}	2.7	3.0	5.5	V	A, B, C
Input voltage	V_{IL}	–0.3*5	—	0.6	V	A, B, C
	V_{IH}	2.4*6	—	V_{CC} + 0.3*7	V	A, B, C
	V_H(♦)	V_{CC} – 0.5	—	V_{CC} + 1.0	V	A, B, C
Operating temperature	Topr	0	—	70	°C	A
		–20	—	85	˚C	B
		–40	—	85	˚C	C

Notes:
1. With respect to V_{SS}.
2. Vin min : –3.0 V for pulse width ≤ 50 ns.
3. Including electrical characteristics and data retention.
4. Group A includes HN58V256AP/AFP, HN58V257AT and HN58V256AT.
   Group B includes HN58V256AT-SR and HN58V257AT-SR.
   Group C includes HN58V256AFPI.
5. V_{IL} min: –1.0 V for pulse width ≤ 50 ns.
6. V_{IH} min for V_{CC} = 3.6 to 5.5 V is 3.0 V.
7. V_{IH} max: V_{CC} + 1.0 V for pulse width ≤ 50 ns.

DC Characteristics

Supply voltage range (V_{CC}), temperature range (Topr) and input voltage (V_{IH}/V_{IL}/V_H) are referred to the table of Recommended DC Operating Conditions.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	I_{LI}	—	—	2*1	µA	V_{CC} = 5.5 V, Vin = 5.5 V
Output leakage current	I_{LO}	—	—	2	µA	V_{CC} = 5.5 V, Vout = 5.5/0.4 V
VCC current (standby)	I_{CC1}	—	—	20	µA	$\overline{CE}$ = V_{CC}
	I_{CC2}	—	—	1	mA	$\overline{CE}$ = V_{IH}
VCC current (active)	I_{CC3}	—	—	8	mA	Iout = 0 mA, Duty = 100%, Cycle = 1 µs at V_{CC} = 3.6 V
		—	—	12	mA	Iout = 0 mA, Duty = 100%, Cycle = 1 µs at V_{CC} = 5.5 V
		—	—	20	mA	Iout = 0 mA, Duty = 100%, Cycle = 120 ns at V_{CC} = 3.6 V
		—	—	30	mA	Iout = 0 mA, Duty = 100%, Cycle = 120 ns at V_{CC} = 5.5 V
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2.1 mA
Output high voltage	V_{OH}	$V_{CC} \times 0.8$	—	—	V	I_{OH} = –400 µA

Note: 1. I_{LI} on $\overline{RES}$: 100 µA max (♦)

Capacitance (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test condition
Input capacitance	Cin*1	—	—	6	pF	Vin = 0 V
Output capacitance	Cout*1	—	—	12	pF	Vout = 0 V

Note: 1. This parameter is periodically sampled and not 100% tested.

AC Characteristics

Supply voltage (V_{CC}) and temperature range (Topr) are referred to the table of 'Recommended DC Operating Conditions'.

Test Conditions

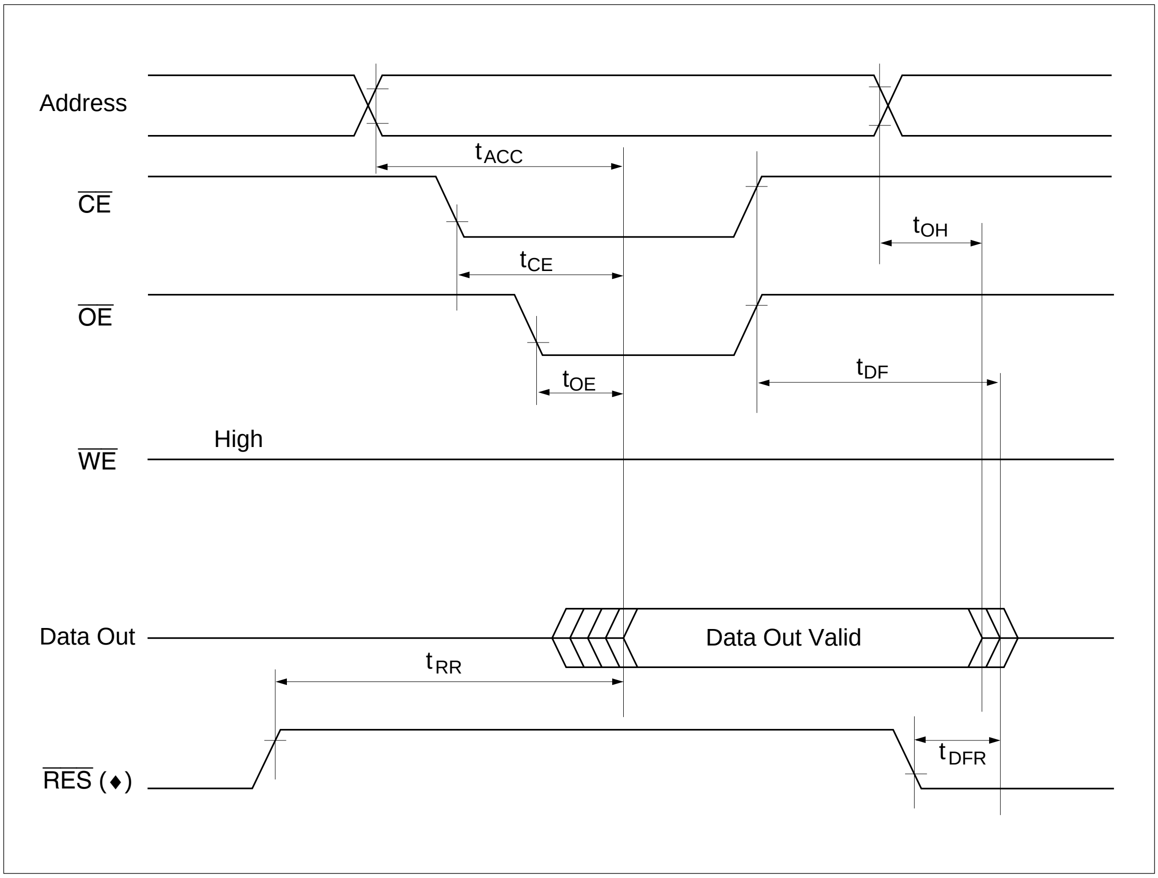
- Input pulse levels : 0 V to 3.0 V
  0 V to V_{CC} ($\overline{RES}$ pin)
- Input rise and fall time : $\leq$ 20 ns
- Input timing reference levels : 0.8, 1.8 V
- Output load : 1TTL Gate +100 pF
- Output reference levels : 1.5 V, 1.5 V

Read Cycle

		-12		-15			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test conditions**
Address to output delay	t_{ACC}	—	120	—	150	ns	$\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$
$\overline{CE}$ to output delay	t_{CE}	—	120	—	150	ns	$\overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$
$\overline{OE}$ to output delay	t_{OE}	10	60	10	60	ns	$\overline{CE} = V_{IL}$, $\overline{WE} = V_{IH}$
Address to output hold	t_{OH}	0	—	0	—	ns	$\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$
$\overline{OE}$ ($\overline{CE}$) high to output float*[1]	t_{DF}	0	40	0	40	ns	$\overline{CE} = V_{IL}$, $\overline{WE} = V_{IH}$
$\overline{RES}$ low to output float*[1](♦)	t_{DFR}	0	350	0	350	ns	$\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$
$\overline{RES}$ to output delay(♦)	t_{RR}	0	600	0	600	ns	$\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$

Note: 1. t_{DF} and t_{DFR} are defined as the time at which the outputs achieve the open circuit conditions and are no longer driven.

Read Timing Waveform



Write Cycle

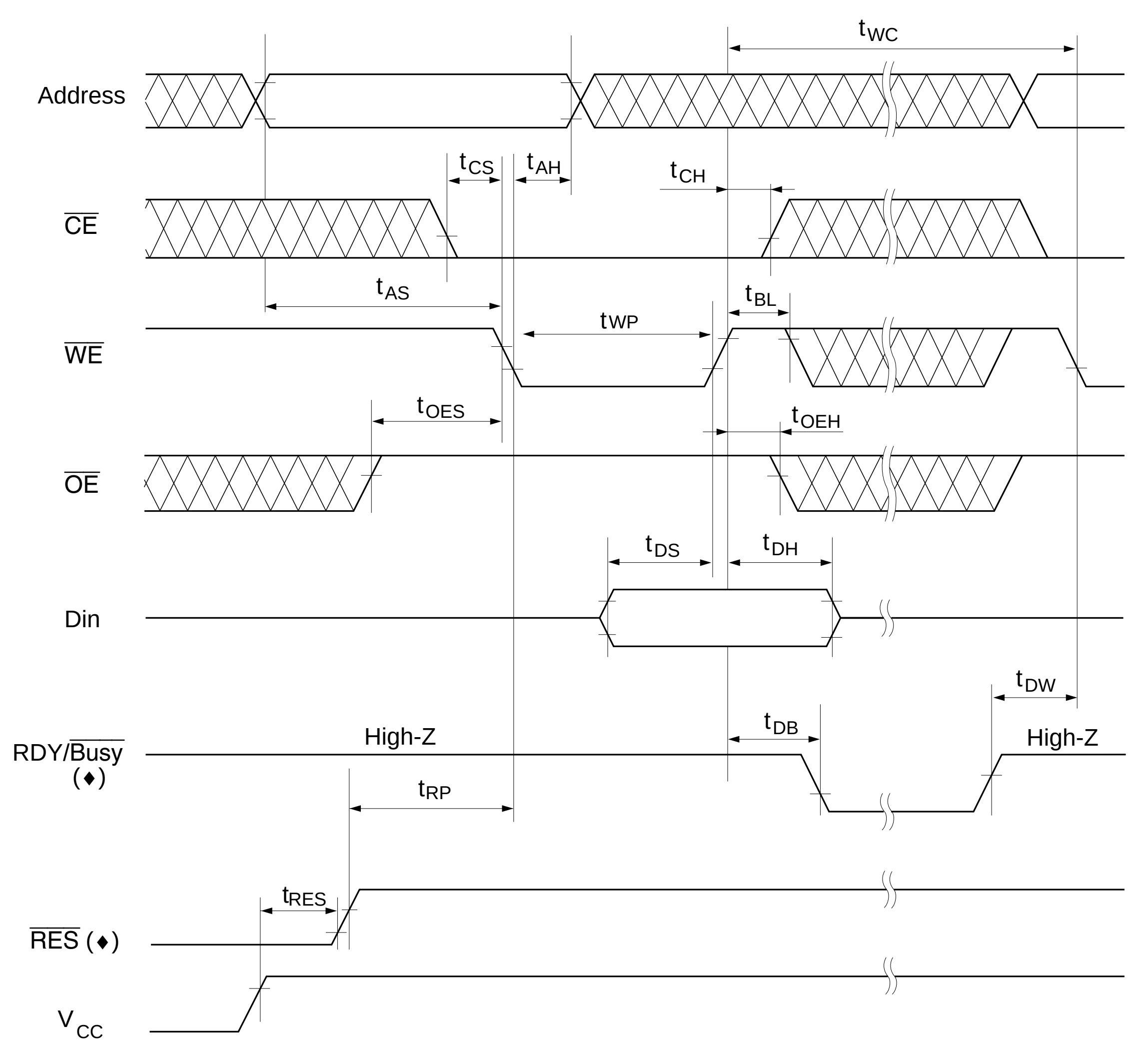
Parameter	Symbol	Min*1	Typ	Max	Unit	Test conditions
Address setup time	t_{AS}	0	—	—	ns	
Address hold time	t_{AH}	50	—	—	ns	
$\overline{\text{CE}}$ to write setup time ($\overline{\text{WE}}$ controlled)	t_{CS}	0	—	—	ns	
$\overline{\text{CE}}$ hold time ($\overline{\text{WE}}$ controlled)	t_{CH}	0	—	—	ns	
$\overline{\text{WE}}$ to write setup time ($\overline{\text{CE}}$ controlled)	t_{WS}	0	—	—	ns	
$\overline{\text{WE}}$ hold time ($\overline{\text{CE}}$ controlled)	t_{WH}	0	—	—	ns	
$\overline{\text{OE}}$ to write setup time	t_{OES}	0	—	—	ns	
$\overline{\text{OE}}$ hold time	t_{OEH}	0	—	—	ns	
Data setup time	t_{DS}	50	—	—	ns	
Data hold time	t_{DH}	0	—	—	ns	
$\overline{\text{WE}}$ pulse width ($\overline{\text{WE}}$ controlled)	t_{WP}	200	—	—	ns	
$\overline{\text{CE}}$ pulse width ($\overline{\text{CE}}$ controlled)	t_{CW}	200	—	—	ns	
Data latch time	t_{DL}	100	—	—	ns	
Byte load cycle	t_{BLC}	0.3	—	30	µs	
Byte load window	t_{BL}	100	—	—	µs	
Write cycle time	t_{WC}	—	—	10*2	ms	
Time to device busy	t_{DB}	120	—	—	ns	
Write start time	t_{DW}	0*3	—	—	ns	
Reset protect time (♦)	t_{RP}	100	—	—	µs	
Reset high time (♦)	t_{RES}	1	—	—	µs	

Note: 1. Use this device in longer cycle than this value.

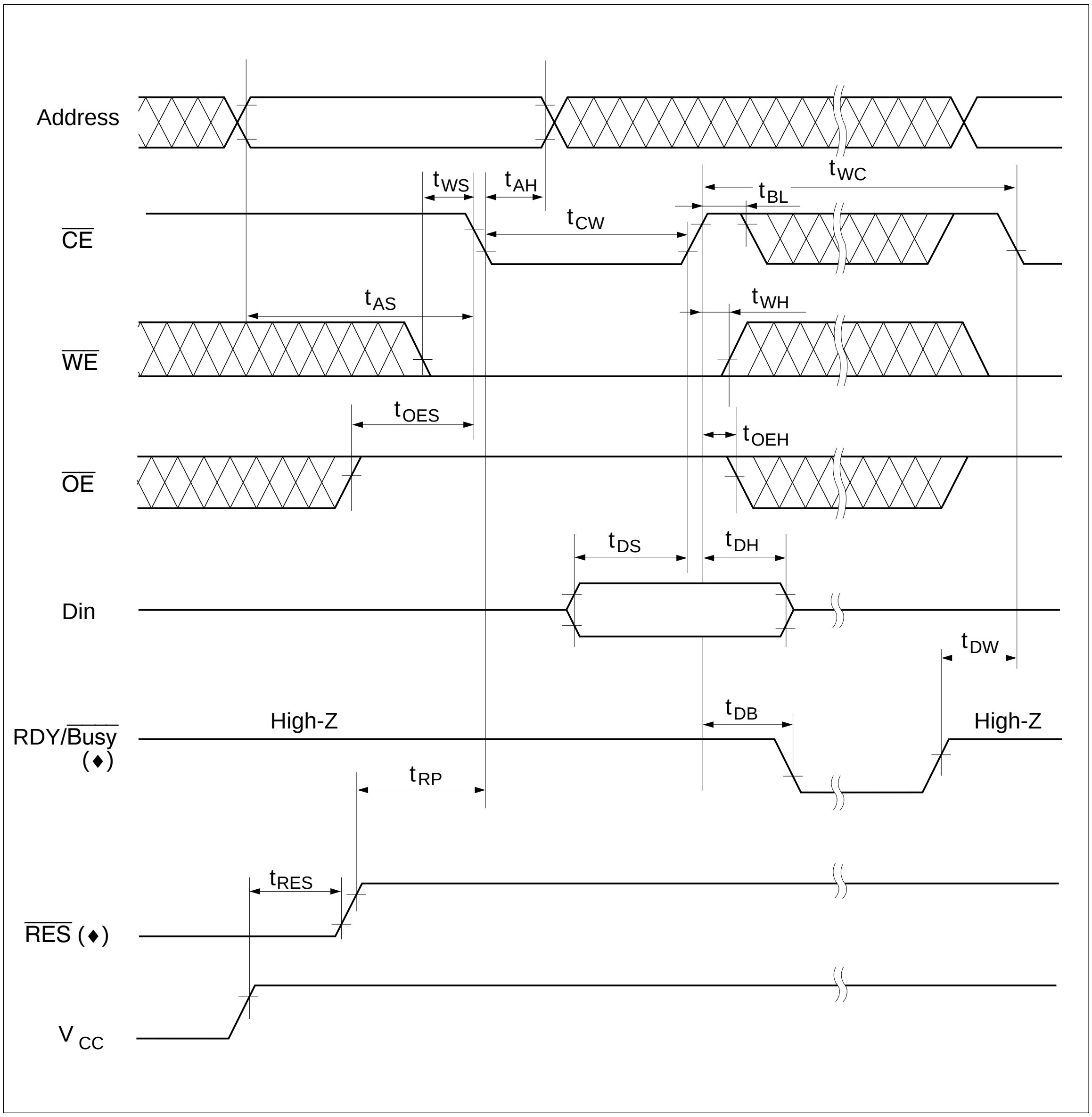
2. t_{WC} must be longer than this value unless polling techniques or RDY/$\overline{\text{Busy}}$ (♦) are used. This device automatically completes the internal write operation within this value.

3. Next read or write operation can be initiated after t_{DW} if polling techniques or RDY/$\overline{\text{Busy}}$ (♦) are used.

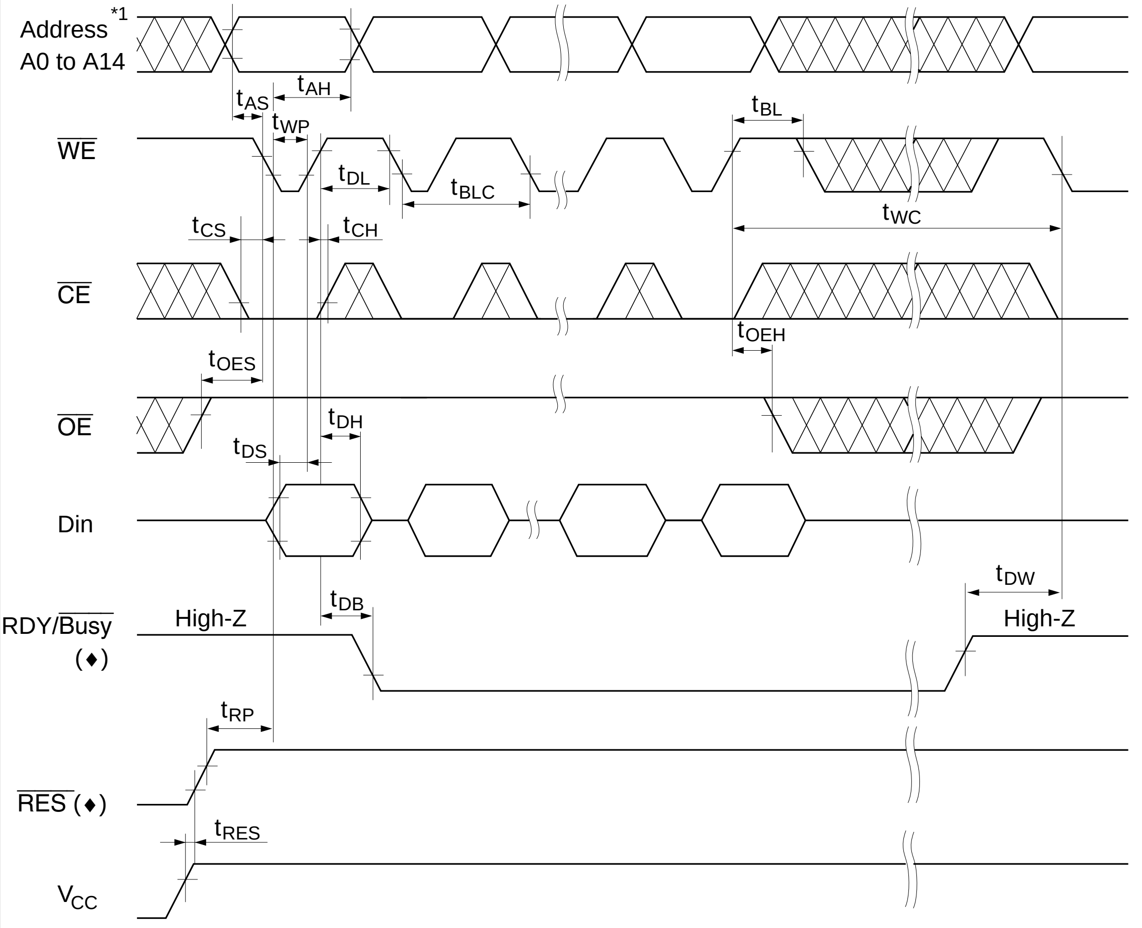
Byte Write Timing Waveform(1) ($\overline{\text{WE}}$ Controlled)



Byte Write Timing Waveform(2) ($\overline{\text{CE}}$ Controlled)

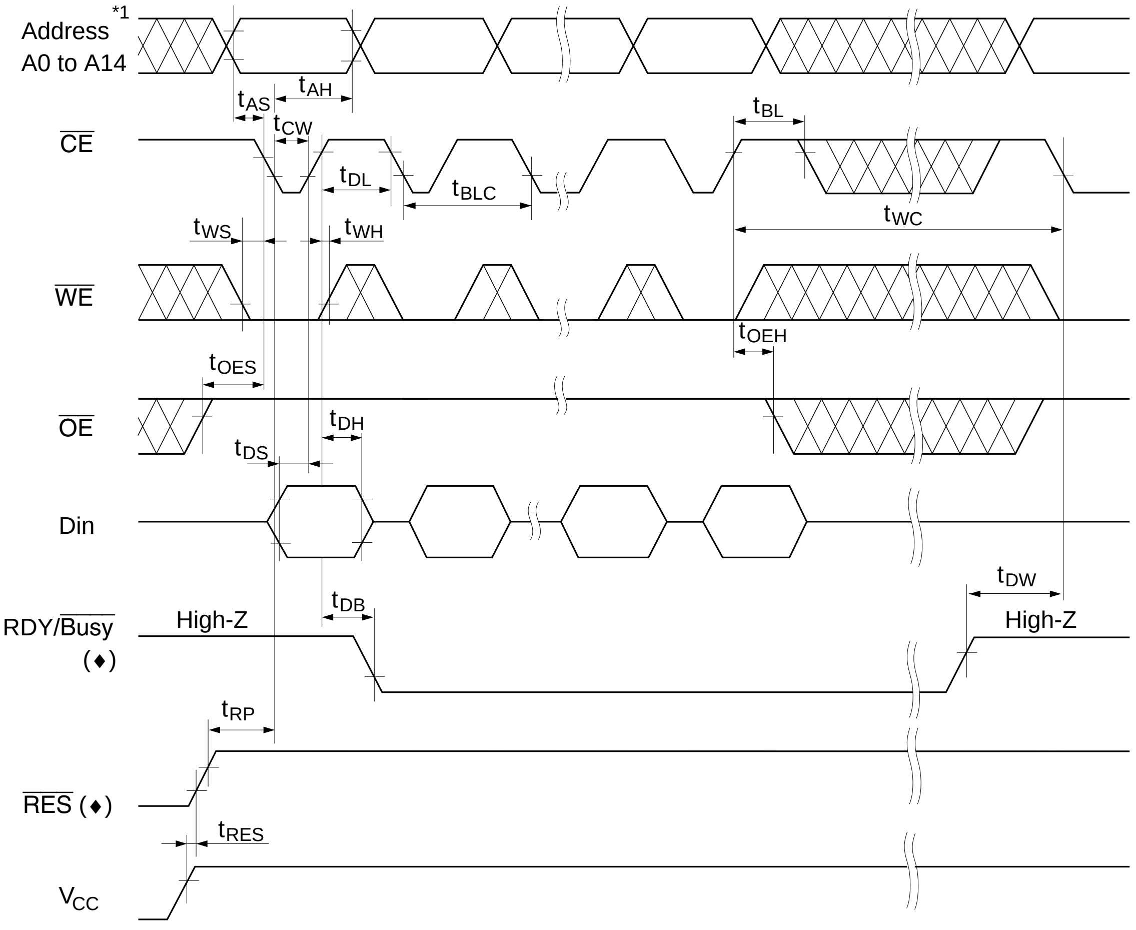


Page Write Timing Waveform(1) ($\overline{\text{WE}}$ Controlled)



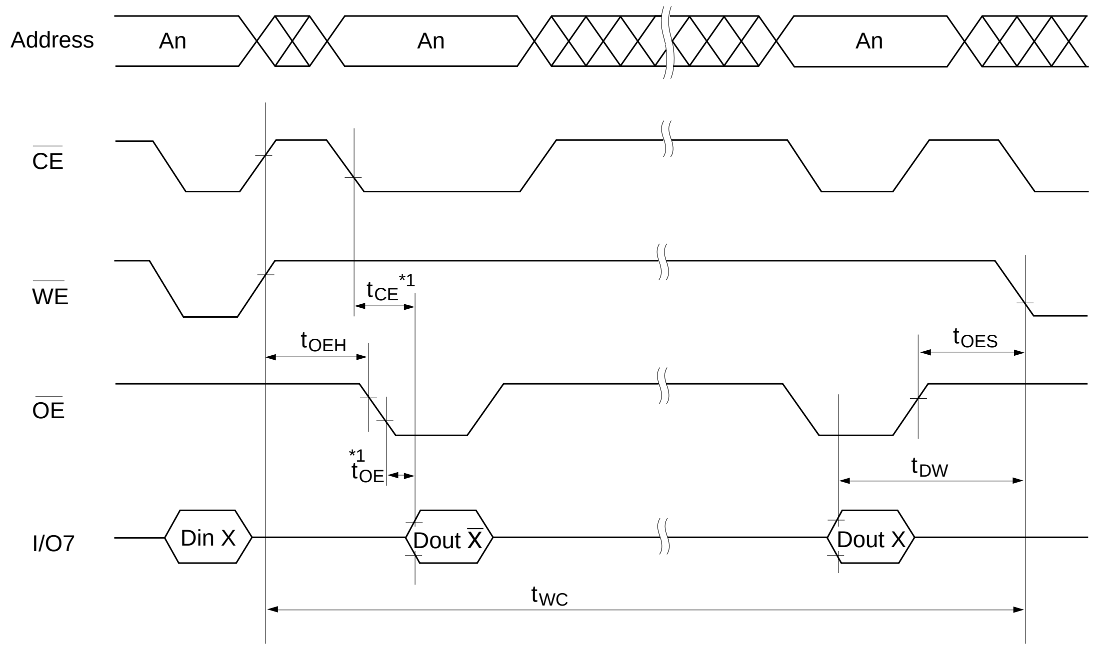
Note: 1. A6 through A14 are page addresses and these address are latched at the first falling edge of $\overline{\text{WE}}$.

Page Write Timing Waveform(2) ($\overline{\text{CE}}$ Controlled)



Note: 1. A6 through A14 are page addresses are these address are latched at the first falling edge of $\overline{\text{CE}}$.

Data Polling Timing Wavefome

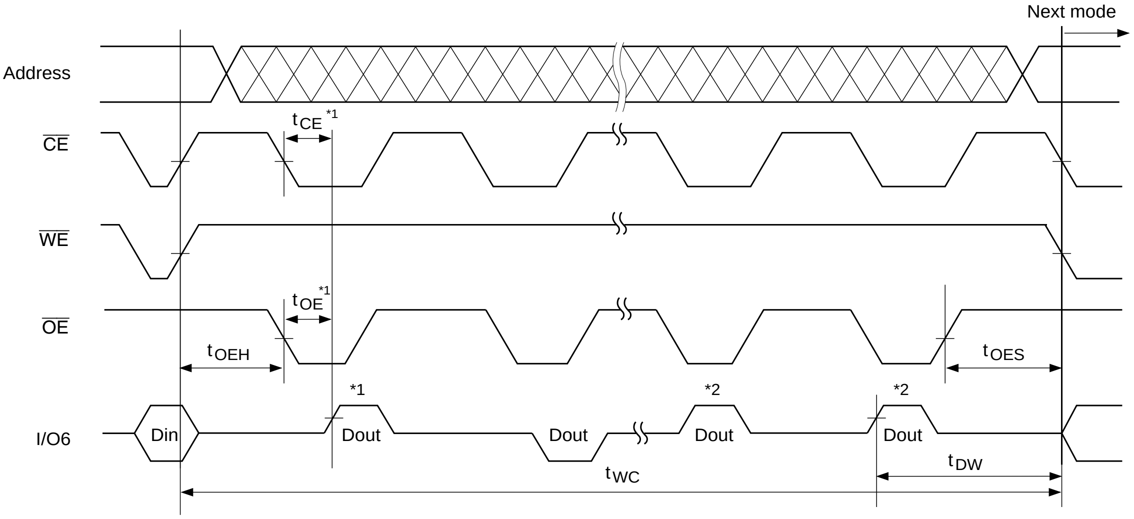


Note: 1. See AC read characteristics.

Toggle bit

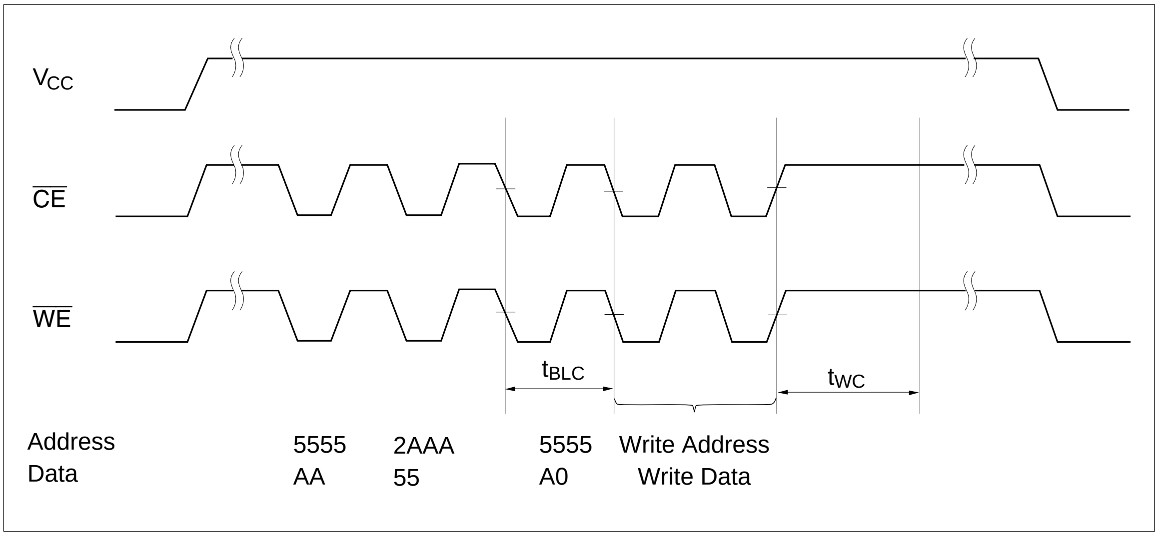
This device provide another function to determine the internal programming cycle. If the EEPROM is set to read mode during the internal programming cycle, I/O6 will charge from "1" to "0" (toggling) for each read. When the internal programming cycle is finished, toggling of I/O6 will stop and the device can be accessible for next read or program.

Toggle bit Wavefome

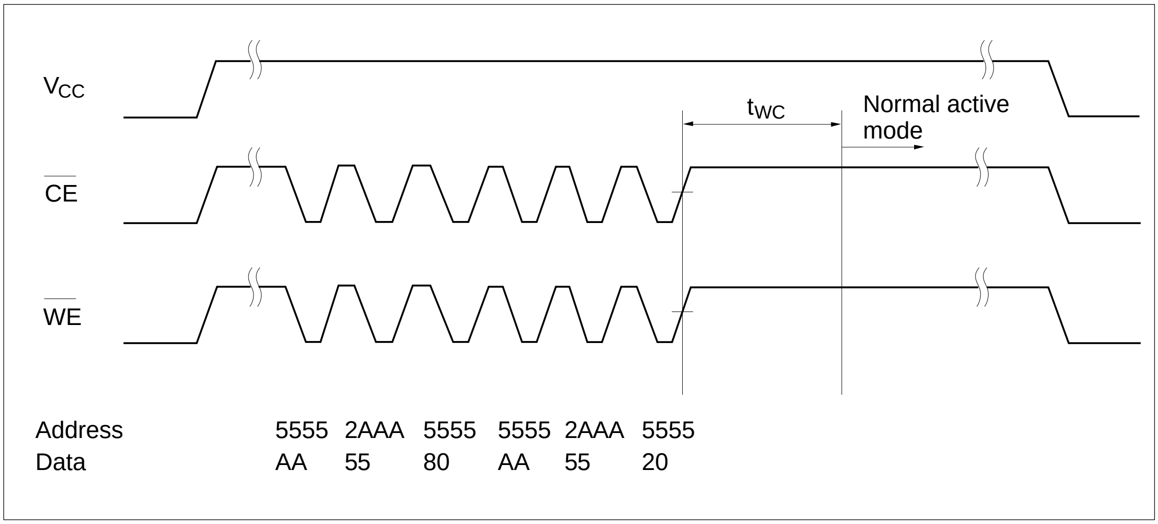


Note: 1. I/O6 beginning state is "1".
2. I/O6 ending state will vary.
3. See AC read characteristics.

Software Data Protection Timing Waveform(1) (in protection mode)



Software Data Protection Timing Waveform(2) (in non-protection mode)



Functional Description

Automatic Page Write

Page-mode write feature allows 1 to 64 bytes of data to be written into the EEPROM in a single write cycle. Following the initial byte cycle, an additional 1 to 63 bytes can be written in the same manner. Each additional byte load cycle must be started within 30 µs from the preceding falling edge of $\overline{\text{WE}}$ or $\overline{\text{CE}}$. When $\overline{\text{CE}}$ or $\overline{\text{WE}}$ is kept high for 100 µs after data input, the EEPROM enters write mode automatically and the input data are written into the EEPROM.

$\overline{\text{Data}}$ Polling

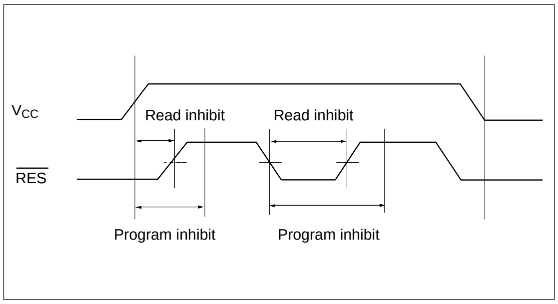
$\overline{\text{Data}}$ polling allows the status of the EEPROM to be determined. If EEPROM is set to read mode during a write cycle, an inversion of the last byte of data to be loaded outputs from I/O7 to indicate that the EEPROM is performing a write operation.

RDY/$\overline{\text{Busy}}$ Signal (♦)

RDY/$\overline{\text{Busy}}$ signal also allows status of the EEPROM to be determined. The RDY/$\overline{\text{Busy}}$ signal has high impedance except in write cycle and is lowered to V_{OL} after the first write signal. At the end of a write cycle, the RDY/$\overline{\text{Busy}}$ signal changes state to high impedance.

$\overline{\text{RES}}$ Signal (♦)

When $\overline{\text{RES}}$ is low, the EEPROM cannot be read or programmed. Therefore, data can be protected by keeping $\overline{\text{RES}}$ low when V_{CC} is switched. $\overline{\text{RES}}$ should be high during read and programming because it doesn't provide a latch function.



$\overline{\text{WE}}$, $\overline{\text{CE}}$ Pin Operation

During a write cycle, addresses are latched by the falling edge of $\overline{\text{WE}}$ or $\overline{\text{CE}}$, and data is latched by the rising edge of $\overline{\text{WE}}$ or $\overline{\text{CE}}$.

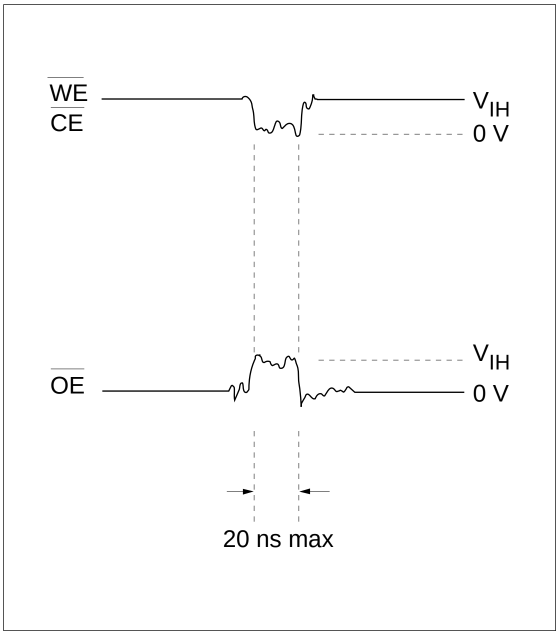
Write/Erase Endurance and Data Retention Time

The endurance is 10^5 cycles in case of the page programming and 10^4 cycles in case of the byte programming (1% cumulative failure rate). The data retention time is more than 10 years when a device is page-programmed less than 10^4 cycles.

Data Protection

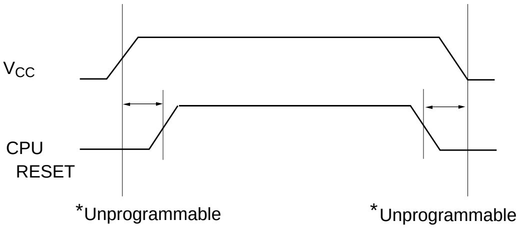
1. Data Protection against Noise on Control Pins ($\overline{\text{CE}}$, $\overline{\text{OE}}$, $\overline{\text{WE}}$) during Operation

During readout or standby, noise on the control pins may act as a trigger and turn the EEPROM to programming mode by mistake.
To prevent this phenomenon, this device has a noise cancelation function that cuts noise if its width is 20 ns or less in programming mode.
Be careful not to allow noise of a width of more than 20 ns on the control pins.



2. Data protection at V_{CC} on/off

When V_{CC} is turned on or off, noise on the control pins generated by external circuits (CPU, etc) may act as a trigger and turn the EEPROM to program mode by mistake. To prevent this unintentional programming, the EEPROM must be kept in an unprogrammable state while the CPU is in an unstable state.



*The EEPROM should be kept in un-programmable state during V_{CC} on/off by using CPU RESET signal.

(1)Protection by $\overline{CE}$, $\overline{OE}$, $\overline{WE}$

To realize the unprogrammable state, the input level of control pins must be held as shown in the table below.

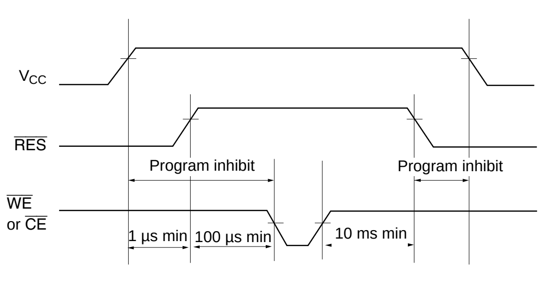
$\overline{CE}$	V_{CC}	×	×
$\overline{OE}$	×	V_{SS}	×
$\overline{WE}$	×	×	V_{CC}

×: Don't care.
V_{CC}: Pull-up to V_{CC} level.
V_{SS}: Pull-down to V_{SS} level.

(2) Protection by $\overline{RES}$ (♦)

The unprogrammable state can be realized by that the CPU's reset signal inputs directly to the EEPROM's $\overline{RES}$ pin. $\overline{RES}$ should be kept V_{SS} level during V_{CC} on/off.

The EEPROM breaks off programming operation when $\overline{RES}$ becomes low, programming operation doesn't finish correctly in case that $\overline{RES}$ falls low during programming operation. $\overline{RES}$ should be kept high for 10 ms after the last data input.



3. Software data protection

To prevent unintentional programming caused by noise generated by external circuits, This device has the software data protection function. In software data protection mode, 3 bytes of data must be input before write data as follows. And these bytes can switch the non-protection mode to the protection mode.

Address	Data	
5555	AA	
↓	↓	
2AAA	55	
↓	↓	
5555	A0	
↓	↓	
Write address	Write data	} Normal data input

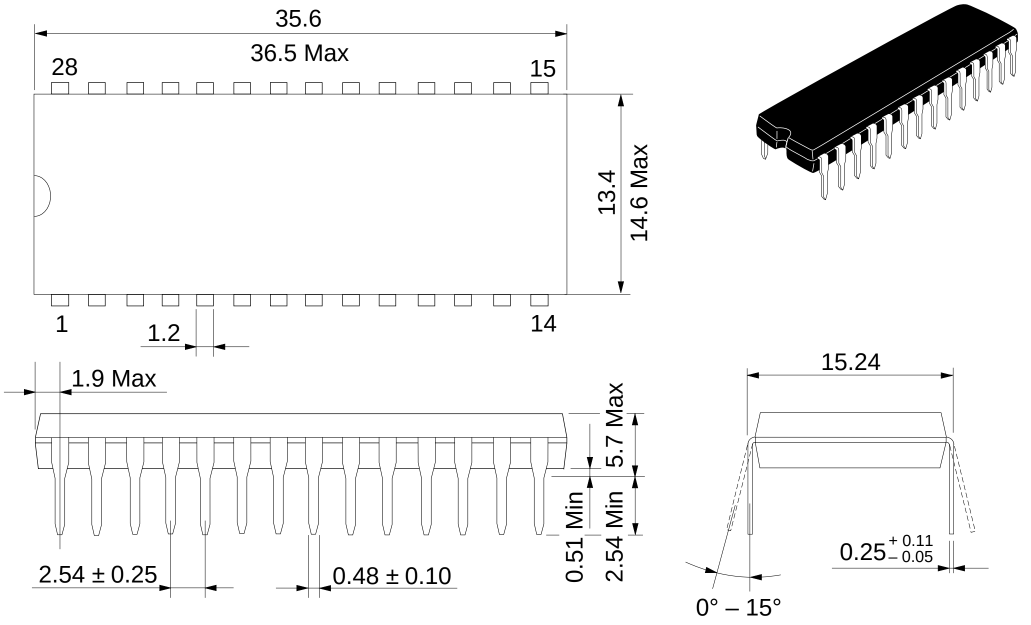
Software data protection mode can be canceled by inputting the following 6 bytes. After that, this device turns to the non-protection mode and can write data normally. But when the data is input in the canceling cycle, the data cannot be written.

Address	Data
5555	AA
↓	↓
2AAA	55
↓	↓
5555	80
↓	↓
5555	AA
↓	↓
2AAA	55
↓	↓
5555	20

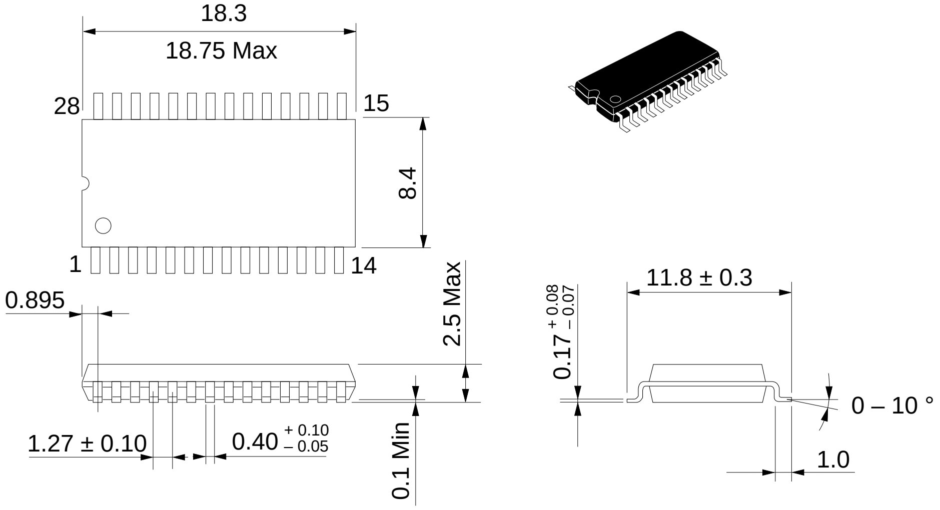
The software data protection is not enabled at the shipment.

Package Dimensions

HN58V256AP Series (DP-28) **Unit : mm**

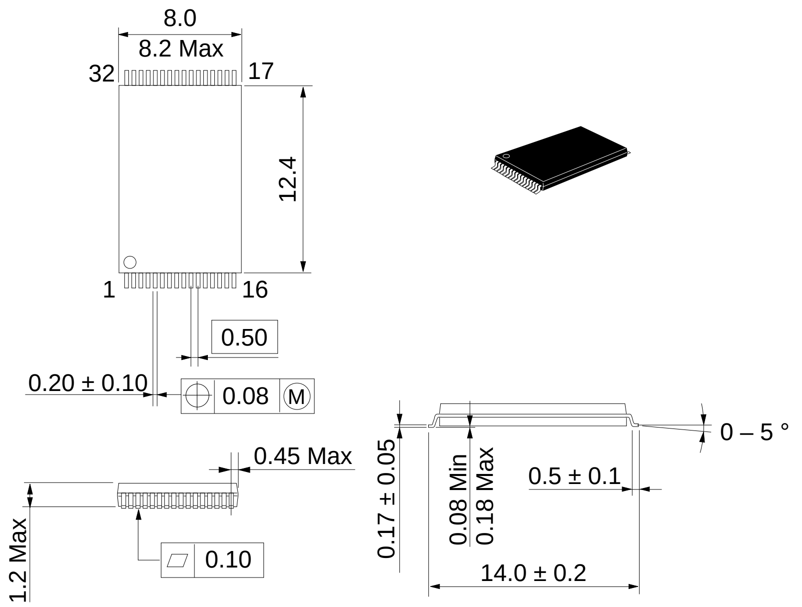


HN58V256AFP Series (FP-28D) **Unit : mm**



Package Dimensions

HN58V257AT Series (TFP-32DA) **Unit : mm**



HN58V256AT Series (—) **Unit : mm**

(To be determined)