HN58C256A, HN58C257A Series

32768-word × 8-bit Electrically Erasable and Programmable CMOS ROM

HITACHI

ADE-203-410(Z)
Preliminary
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Description

The Hitachi HN58C256A and HN58C257A are a electrically erasable and programmable EEPROM's organized as 32768-word × 8-bit. Employing advanced MNOS memory technology and CMOS process and circuitry technology. They also have a 64-byte page programming function to make their write operations faster.

Features

- Single 5 V supply
- On-chip latches: address, data, $\overline{CE}$, $\overline{OE}$, $\overline{WE}$
- Automatic byte write: 10 ms max
- Automatic page write (64 bytes): 10 ms max
- Fast access time: 85/100 ns max
- Low power dissipation: 20 mW/MHz, typ (active)
  110 µW max (standby)
- Ready/$\overline{Busy}$ (♦)[*1]
- $\overline{Data}$ polling and Toggle bit
- Data protection circuit on power on/off
- Conforms to JEDEC byte-wide standard
- Reliable CMOS with MNOS cell technology
- 10^5 erase/write cycles (in page mode)
- 10 years data retention
- Software data protection
- Write protection by $\overline{RES}$ pin (♦)[*1]

Notes: 1. All through this datasheet, the mark (♦) indicates the function supported by only the HN58C257A series (32 pin package).

Note: The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

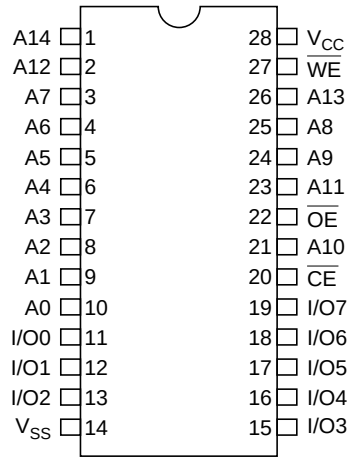
Ordering Information

Type No.	Compatible Type No.*1	Operating Voltage	Temperature Range	Access Time	Package
HN58C256AP-85 HN58C256AP-10	HN58C256P-20	4.5 to 5.5 V	0 to 70°C	85 ns 100 ns	600 mil 28-pin plastic DIP (DP-28)
HN58C256AFP-85 HN58C256AFP-10	HN58C256FP-20	4.5 to 5.5 V	0 to 70°C	85 ns 100 ns	400 mil 28-pin plastic SOP (FP-28D)
HN58C256AT-85 HN58C256AT-10		4.5 to 5.5 V	0 to 70°C	85 ns 100 ns	28-pin plastic TSOP (TFP-28DB)
HN58C257AT-85 HN58C257AT-10	HN58C257T-20	4.5 to 5.5 V	0 to 70°C	85 ns 100 ns	8 × 14 mm 32-pin plastic TSOP (TFP-32DA)

Note: 1. This type No. can be replaced by the corresponding A-version. (ex. HN58C256P to HN58C256AP)

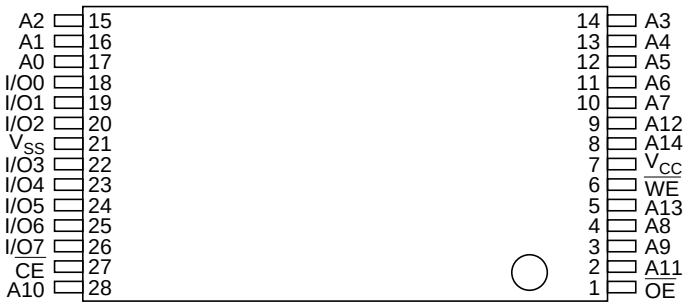
Pin Arrangement

HN58C256AP/AFP Series



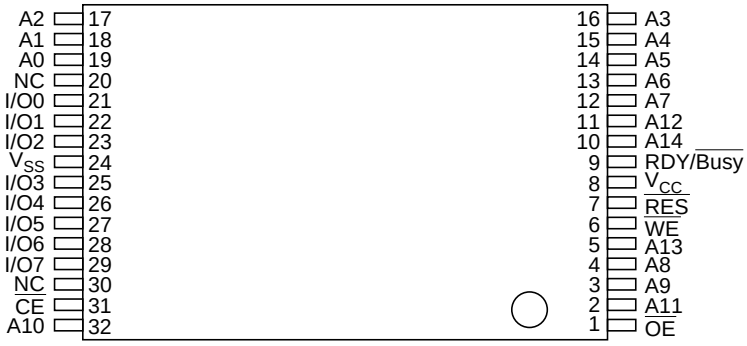
(Top View)

• HN58C256AT Series



(Top View)

• HN58C257AT Series

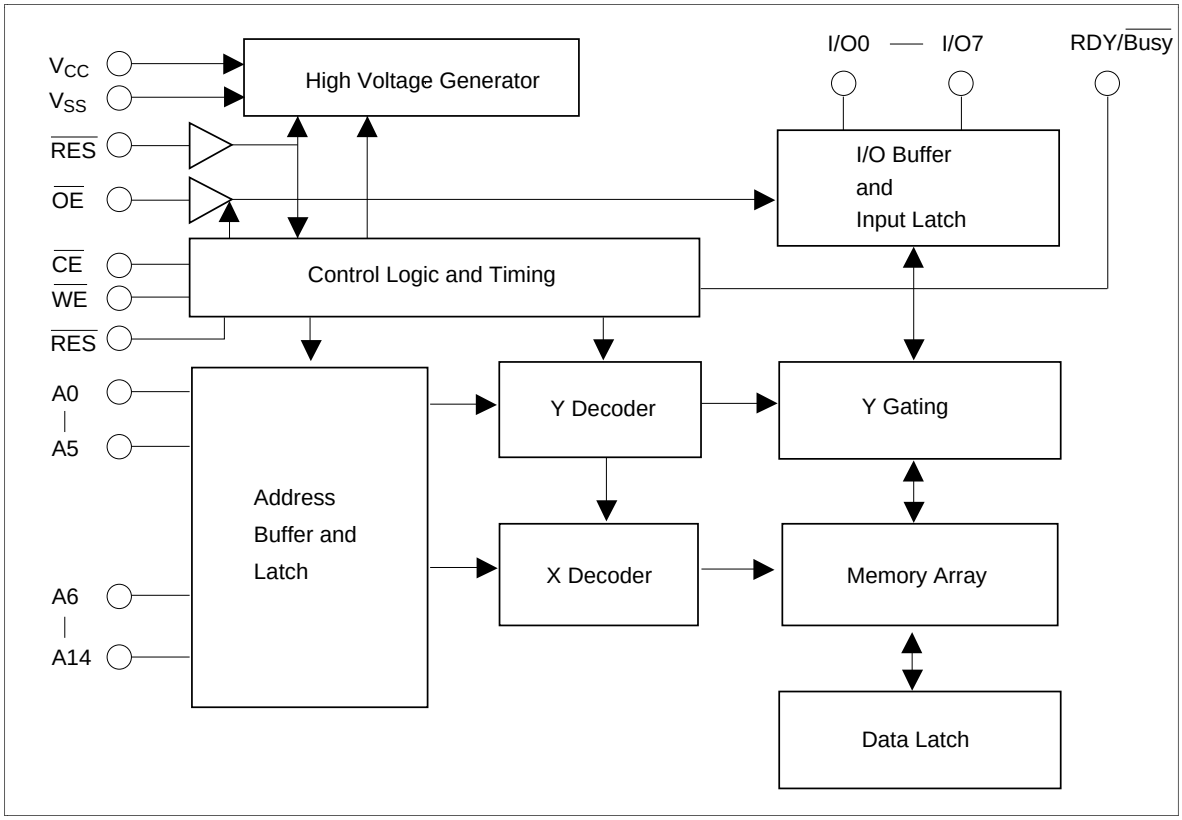


(Top View)

Pin Description

Pin name	Function
A0 to A14	Address
I/O0 to I/O7	Data input/output
$\overline{OE}$	Output enable
$\overline{CE}$	Chip enable
$\overline{WE}$	Write enable
V_{CC}	Power (+5.0 V)
V_{SS}	Ground
RDY/$\overline{Busy}$ (♦)	Ready busy
$\overline{RES}$ (♦)	Reset

Block Diagram



Mode Selection

Pin Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{RES}$ (♦)	RDY/$\overline{Busy}$ (♦)	I/O
Read	V_{IL}	V_{IL}	V_{IH}	V_H [*1]	High-Z	Dout
Standby	V_{IH}	X[*2]	X	X	High-Z	High-Z
Write	V_{IL}	V_{IH}	V_{IL}	V_H	High-Z to V_{OL}	Din
Deselect	V_{IL}	V_{IH}	V_{IH}	V_H	High-Z	High-Z
Write inhibit	X	X	V_{IH}	V_{IH}	—	—
	X	V_{IL}	X	X	—	—
Data polling	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{OL}	Data out (I/O7)
Program reset	X	X	X	V_{IL}	High-Z	High-Z

Notes: 1. Refer to the recommended DC operating condition.
2. X = Don't care

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage[*1]	V_{CC}	–0.6 to +7.0	V
Input voltage[*1]	Vin	–0.5[*2] to +7.0	V
Operationg temperature range[*3]	Topr	0 to +70	°C
Storage temperature range	Tstg	–55 to +125	°C

Notes: 1. With respect to V_{SS}
2. Vin min = –3.0 V for pulse width ≤ 50 ns
3. Including electrical characteristics and data retention

Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IL}	–0.3[*1]	—	0.6	V
	V_{IH}	3.0	—	V_{CC} + 0.3[*2]	V
	V_H (♦)	V_{CC} – 0.5	—	V_{CC} + 1.0	V
Operating temperature	Topr	0	—	70	°C

Notes: 1. V_{IL} min: –1.0 V for pulse width ≤ 50 ns.
2. V_{IH} max: V_{CC} + 1.0 V for pulse width ≤ 50 ns.

DC Characteristics

Supply voltage range (V_{CC}), temperature range (Topr) and input voltage ($V_{IH}/V_{IL}/V_H$) are referred to the table of Recommended DC Operating Conditions.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	I_{LI}	—	—	2*1	µA	V_{CC} = 5.5 V, Vin = 5.5 V
Output leakage current	I_{LO}	—	—	2	µA	V_{CC} = 5.5 V, Vout = 5.5/0.4 V
V_{CC} current (standby)	I_{CC1}	—	—	20	µA	$\overline{CE}$ = V_{CC}
	I_{CC2}	—	—	1	mA	$\overline{CE}$ = V_{IH}
V_{CC} current (active)	I_{CC3}	—	—	12	mA	Iout = 0 mA, Duty = 100%, Cycle = 1 µs at V_{CC} = 5.5 V
		—	—	30	mA	Iout = 0 mA, Duty = 100%, Cycle = 85 ns at V_{CC} = 5.5 V
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2.1 mA
Output high voltage	V_{OH}	V_{CC}×0.8	—	—	V	I_{OH} = –400 µA

Note: 1. I_{LI} on $\overline{RES}$ = 100 µA max (♦)

Capacitance (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance	Cin*1	—	—	6	pF	Vin = 0 V
Output capacitance	Cout*1	—	—	12	pF	Vout = 0 V

Note: 1. This parameter is periodically sampled and not 100% tested.

AC Characteristics

Supply voltage (V_{CC}) and temperature range (Topr) are referred to the table of 'Recommended DC Operating Conditions'.

Test Conditions

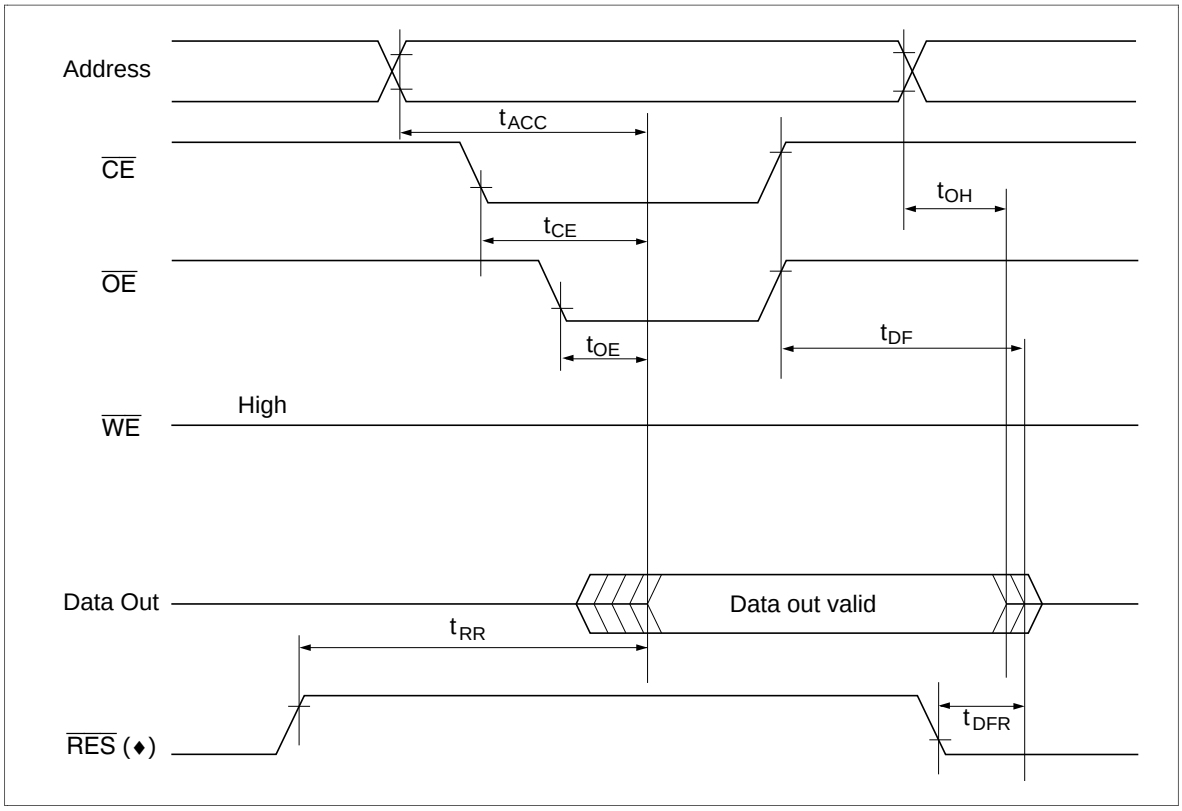
- Input pulse levels: 0 V to 3.0 V
  0V to V_{CC} ($\overline{RES}$ pin)
- Input rise and fall time: ≤ 20 ns
- Input timing reference levels: 0.8, 2.0 V
- Output load: 1TTL Gate +100 pF
- Output reference levels: 1.5 V, 1.5 V

Read Cycle

		HN58C256A, HN58C257A					
		-85		-10			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test conditions**
Address to output delay	t_{ACC}	—	85	—	100	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, WE = V_{IH}
$\overline{CE}$ to output delay	t_{CE}	—	85	—	100	ns	$\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{OE}$ to output delay	t_{OE}	10	40	10	50	ns	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Address to output hold	t_{OH}	0	—	0	—	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{OE}$ ($\overline{CE}$) high to output float[*1]	t_{DF}	0	40	0	40	ns	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{RES}$ low to output float[*1] (♦)	t_{DFR}	0	350	0	350	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{RES}$ to output delay (♦)	t_{RR}	0	450	0	450	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}

Note: 1. t_{DF} and t_{DFR} are defined at which the outputs achieve the open circuit conditions and are no longer driven.

Read Timing Waveform



Write Cycle

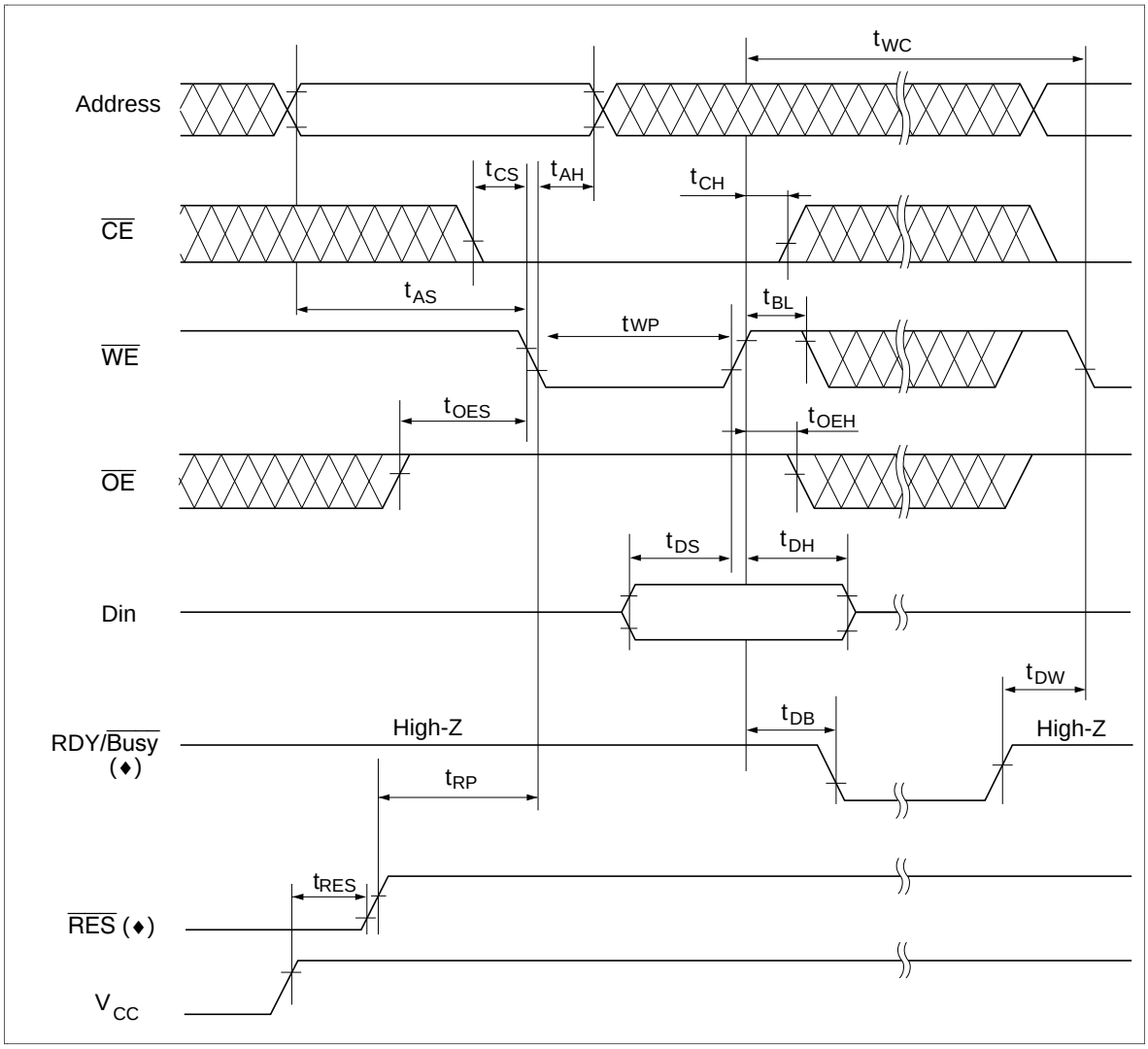
Parameter	Symbol	Min*[1]	Typ	Max	Unit	Test conditions
Address setup time	t_{AS}	0	—	—	ns	
Address hold time	t_{AH}	50	—	—	ns	
$\overline{CE}$ to write setup time ($\overline{WE}$ controlled)	t_{CS}	0	—	—	ns	
$\overline{CE}$ hold time ($\overline{WE}$ controlled)	t_{CH}	0	—	—	ns	
$\overline{WE}$ to write setup time ($\overline{CE}$ controlled)	t_{WS}	0	—	—	ns	
$\overline{WE}$ hold time ($\overline{CE}$ controlled)	t_{WH}	0	—	—	ns	
$\overline{OE}$ to write setup time	t_{OES}	0	—	—	ns	
$\overline{OE}$ hold time	t_{OEH}	0	—	—	ns	
Data setup time	t_{DS}	50	—	—	ns	
Data hold time	t_{DH}	0	—	—	ns	
$\overline{WE}$ pulse width ($\overline{WE}$ controlled)	t_{WP}	100	—	—	ns	
$\overline{CE}$ pulse width ($\overline{CE}$ controlled)	t_{CW}	100	—	—	ns	
Data latch time	t_{DL}	50	—	—	ns	
Byte load cycle	t_{BLC}	0.2	—	30	µs	
Byte load window	t_{BL}	100	—	—	µs	
Write cycle time	t_{WC}	—	—	10*[2]	ms	
Time to device busy	t_{DB}	120	—	—	ns	
Write start time	t_{DW}	0*[3]	—	—	ns	
Reset protect time (♦)	t_{RP}	100	—	—	µs	
Reset high time (♦)	t_{RES}	1	—	—	µs	

Notes: 1. Use this device in longer cycle than this value.

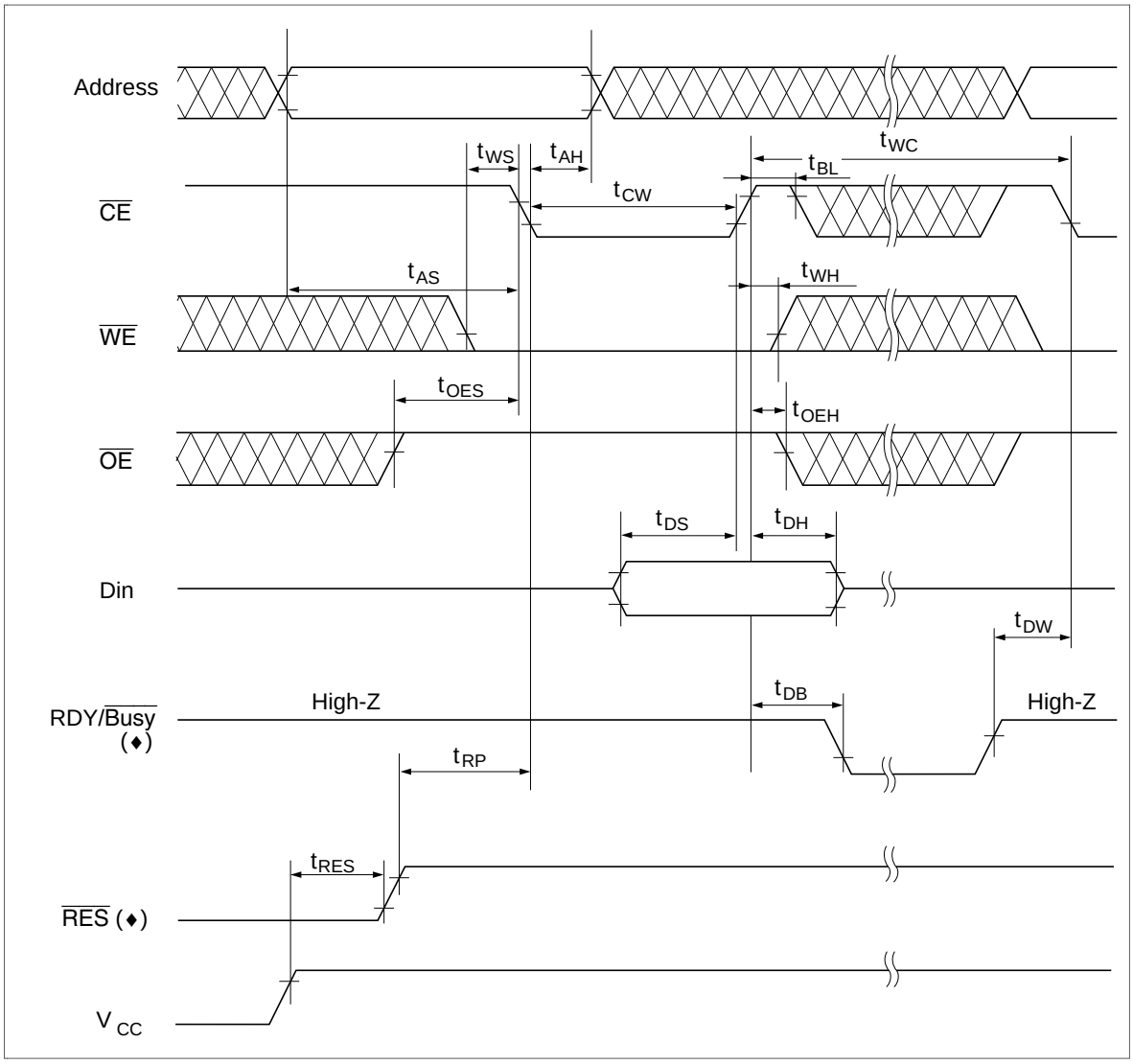
2. t_{WC} must be longer than this value unless polling technique or RDY/$\overline{Busy}$ (♦) are used. This device automatically completes the internal write operation within this value.

3. Next read or write operation can be initiated after t_{DW} if polling technique or RDY/$\overline{Busy}$ (♦) are used.

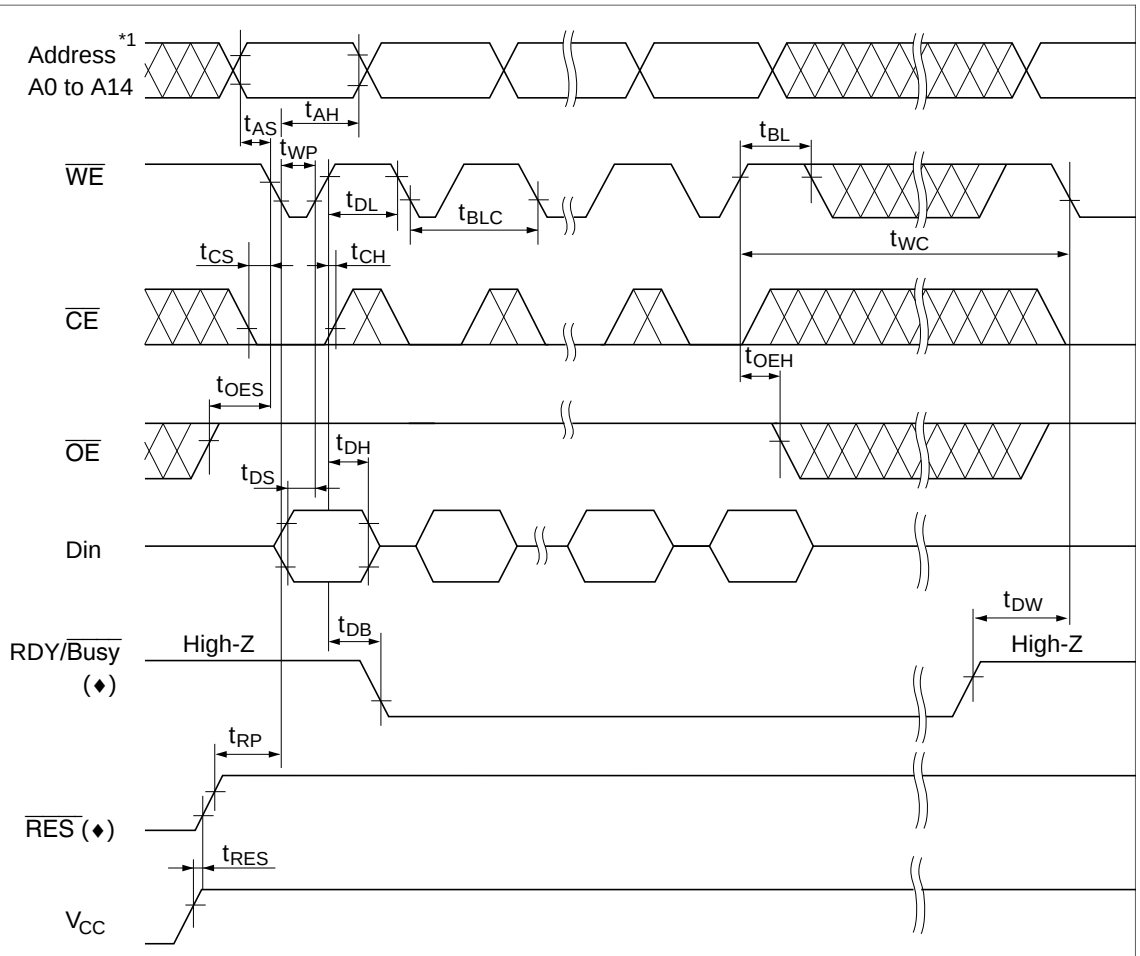
Byte Write Timing Waveform (1) ($\overline{WE}$ Controlled)



Byte Write Timing Waveform (2) ($\overline{CE}$ Controlled)

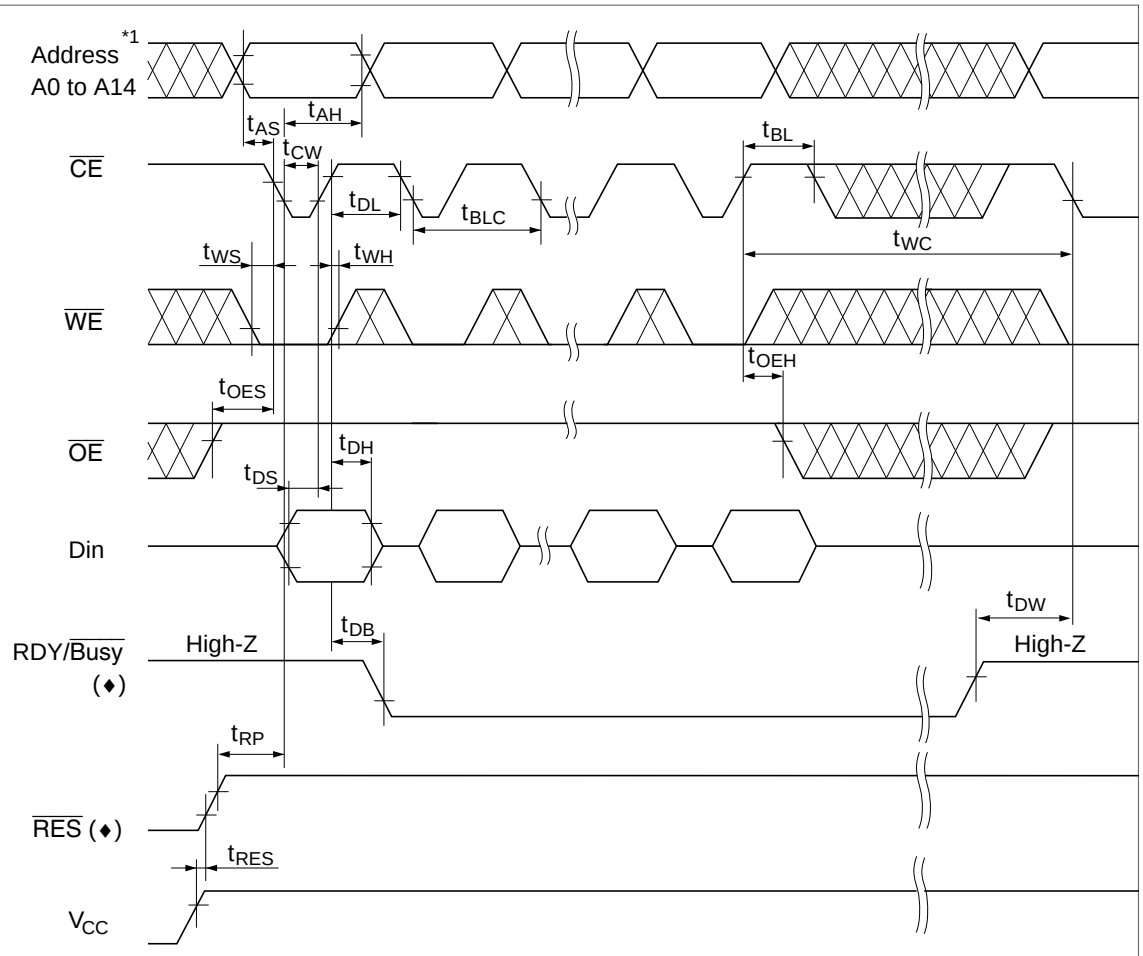


Page Write Timing Waveform (1) ($\overline{WE}$ Controlled)



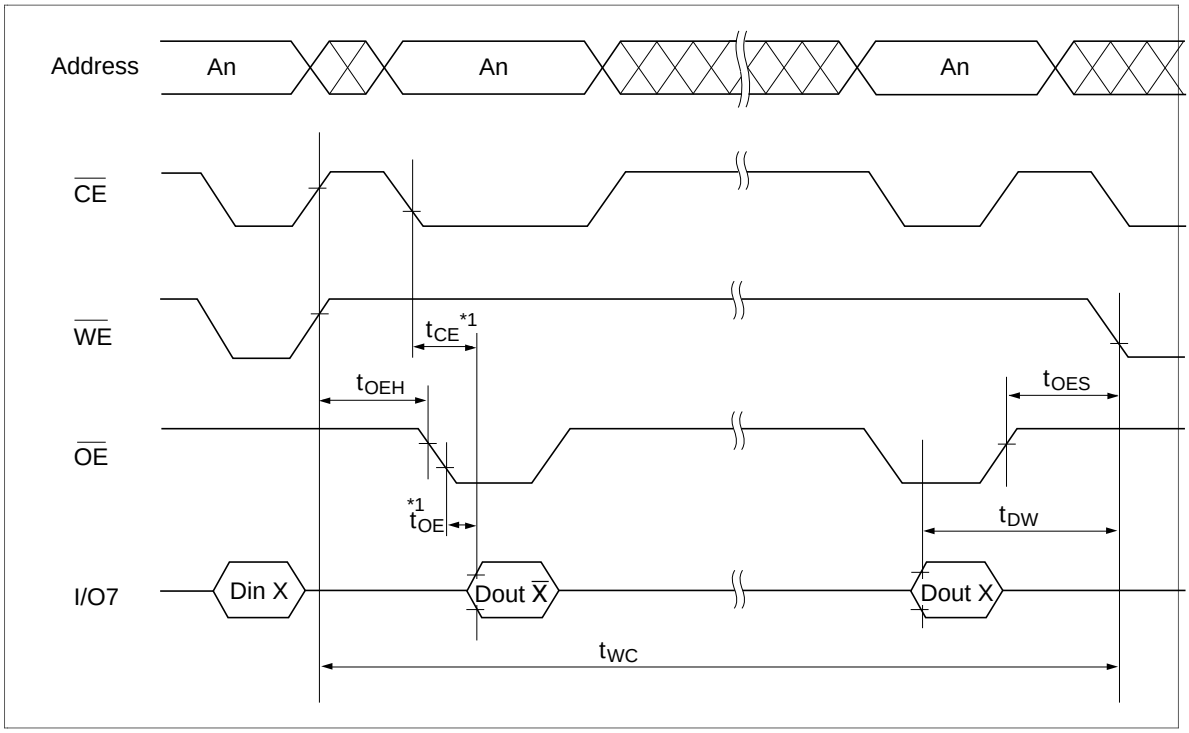
Note: 1. A6 through A14 are page address and these address are latched at the first falling edge of $\overline{WE}$

Page Write Timing Waveform (2) ($\overline{CE}$ Controlled)



Note: 1. A6 through A14 are page address and these address are latched at the first falling edge of $\overline{CE}$

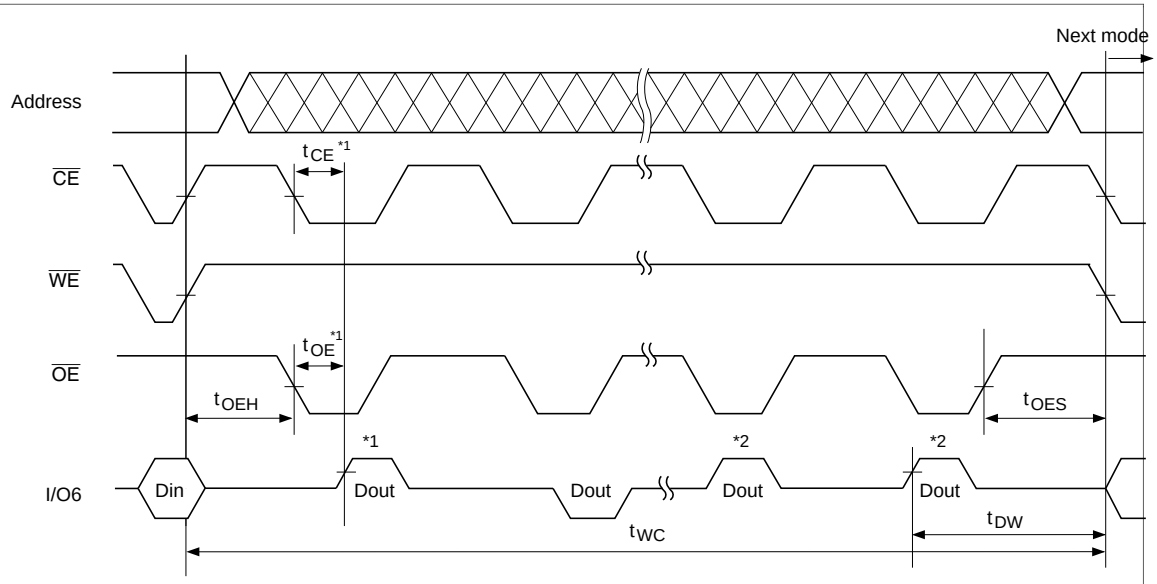
$\overline{\text{Data}}$ Polling Timing Waveform



Toggle bit

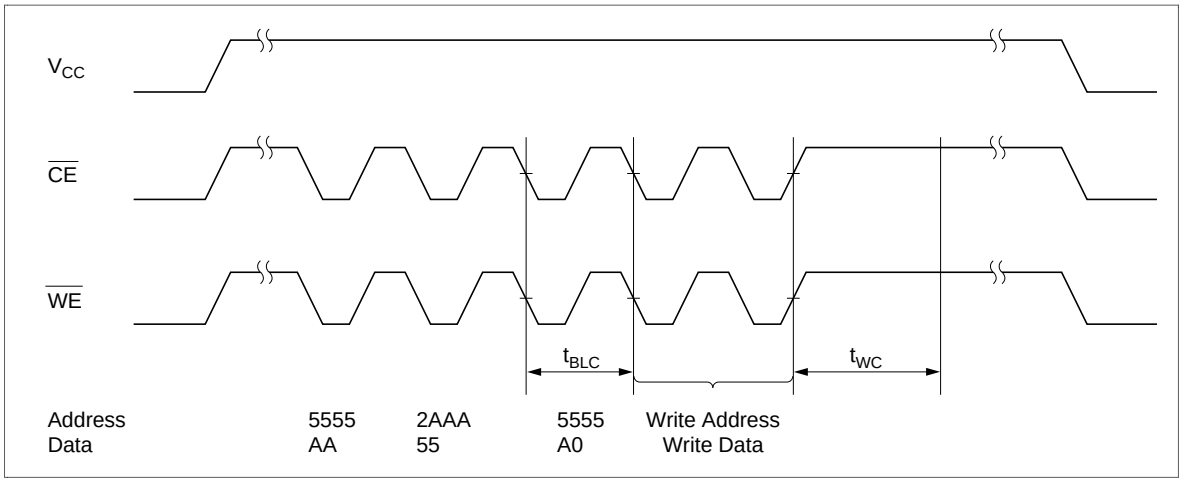
This device provide another function to determine the internal programming cycle. If the EEPROM is set to read mode during the internal programming cycle, I/O6 will charge from „1“ to „0“ (toggling) for each read. when the internal programming cycle is finished, toggling of I/O6 will stop and the device can be accessible for next read or program.

Toggle bit Waveform

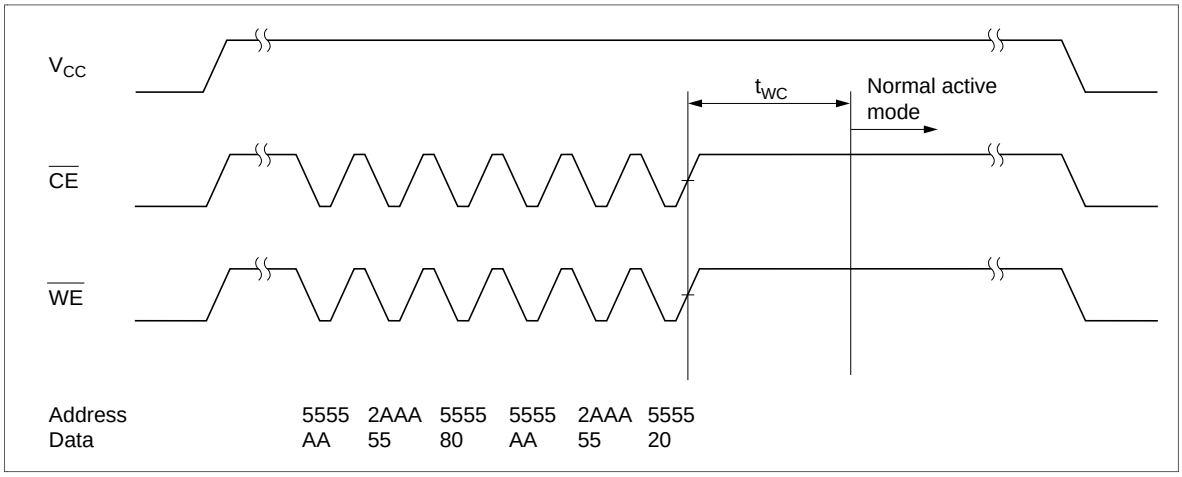


Notes: 1. I/O6 biginning state is "1".
2. I/O7 ending state will vary.
3. See AC read characteristics.

Software Data Protection Timing Waveform (1) (in protection mode)



Software Data Protection Timing Waveform (2) (in non-protection mode)



Functional Description

Automatic Page Write

Page-mode write feature allows 1 to 64 bytes of data to be written into the EEPROM in a single write cycle. Following the initial byte cycle, an additional 1 to 63 bytes can be written in the same manner. Each additional byte load cycle must be started within 30 µs from the preceding falling edge of $\overline{WE}$ or $\overline{CE}$. When $\overline{CE}$ or $\overline{WE}$ is high for 100 µs after data input, the EEPROM enters write mode automatically and the input data are written into the EEPROM.

$\overline{Data}$ Polling

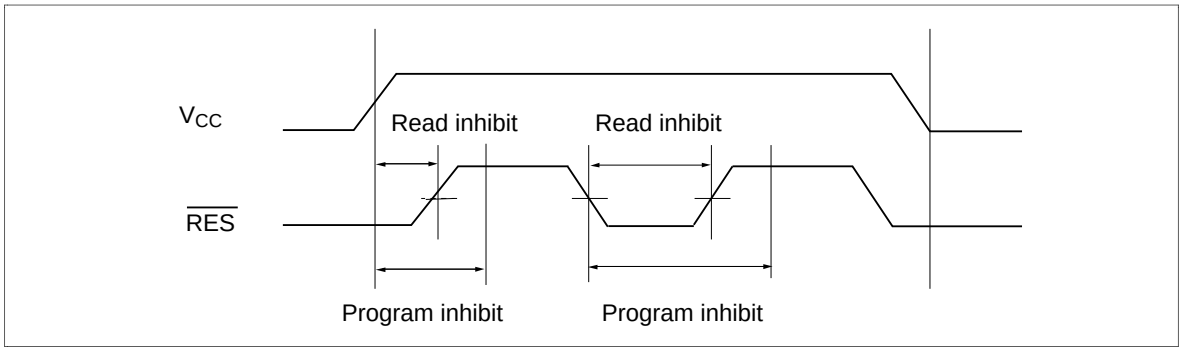
$\overline{Data}$ polling allows the status of the EEPROM to be determined. If EEPROM is set to read mode during a write cycle, an inversion of the last byte of data to be loaded outputs from I/O7 to indicate that the EEPROM is performing a write operation.

RDY/$\overline{Busy}$ Signal (♦)

RDY/$\overline{Busy}$ signal also allows the status of the EEPROM to be determined. The RDY/$\overline{Busy}$ signal has high impedance except in write cycle and is lowered to V_{OL} after the first write signal. At the end of a write cycle, the RDY/$\overline{Busy}$ signal changes state to high impedance.

$\overline{RES}$ Signal (♦)

When $\overline{RES}$ is low, the EEPROM cannot be read or programmed. Therefore, data can be protected by keeping $\overline{RES}$ low when V_{CC} is switched. $\overline{RES}$ should be high during read and programming because it dosen't provide a latch function.



$\overline{WE}$, $\overline{CE}$ Pin Operation

During a write cycle, addresses are latched by the falling edge of $\overline{WE}$ or $\overline{CE}$, and data is latched by the rising edge of $\overline{WE}$ or $\overline{CE}$.

Write/Erase Endurance and Data Retention Time

The endurance is 10^5 cycles in case of the page programming and 10^4 cycles in case of byte programming (1% cumulative failure rate). The data retention time is more than 10 years when a device is page-programmed less than 10^4 cycles.

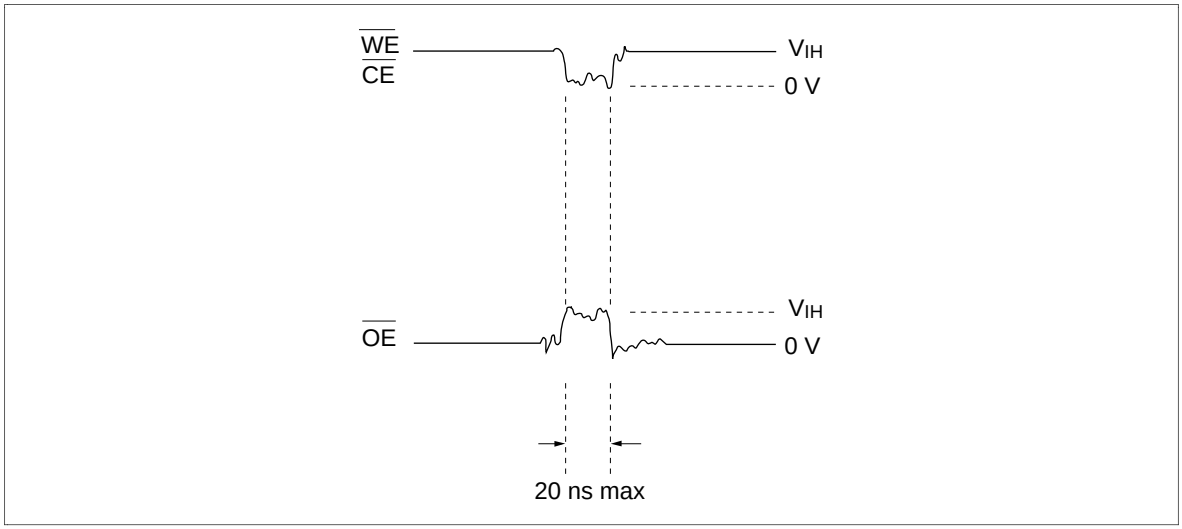
Data Protection

1. Data Protection against Noise on Control Pins ($\overline{CE}$, $\overline{OE}$, $\overline{WE}$) during Operation

During readout or standby, noise on the control pins may act as a trigger and turn the EEPROM to programming mode by mistake.

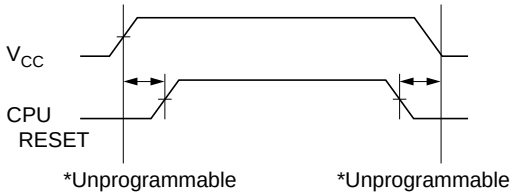
To prevent this phenomenon, this device has a noise cancelation function that cuts noise if its width is 20 ns or less in programming mode.

Be careful not to allow noise of a width of more than 20 ns on the control pins.



2. Data Protection at V_{CC} On/Off

When V_{CC} is turned on or off, noise on the control pins generated by external circuits (CPU, etc) may act as a trigger and turn the EEPROM to program mode by mistake. To prevent this unintentional programming, the EEPROM must be kept in an unprogrammable state while the CPU is in an unstable state.



*The EEPROM shoud be kept in unprogrammable state during V_{CC} on/off using CPU RESET signal.

(1) Protection by $\overline{CE}$, $\overline{OE}$, $\overline{WE}$

To realize the unprogrammable state, the input level of control pins must be held as shown in the table below.

$\overline{CE}$	V_{CC}	×	×
$\overline{OE}$	×	V_{SS}	×
$\overline{WE}$	×	×	V_{CC}

×: Don't care.

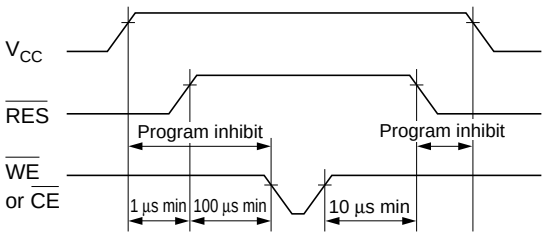
V_{CC}: Pull-up to V_{CC} level.

V_{SS}: Pull-down to V_{SS} level.

(2) Protection by RES (♦)

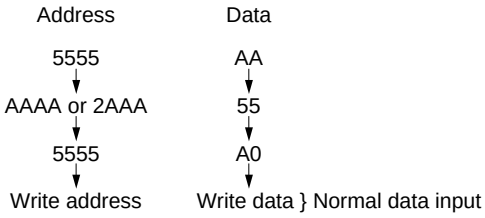
The unprogrammable state can be realized by that the CPU's reset signal inputs directly to the EEPROM's $\overline{RES}$ pin. $\overline{RES}$ should be kept V_{SS} level during V_{CC} on/off.

The EEPROM breaks off programming operation when $\overline{RES}$ becomes low, programming operation doesn't finish correctly in case that $\overline{RES}$ falls low during programming operation. $\overline{RES}$ should be kept high for 10 ms after the last data input.

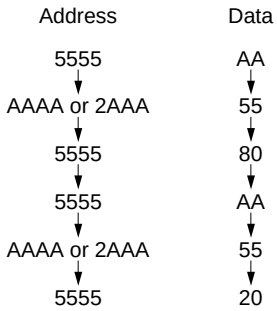


3. Software data protetion

To prevent unintentional programming caused by noise generated by external circuits. This device has the software data protection function. In software data protection mode, 3 bytes of data must be input before write data as follows. And these bytes can switch the non-protection mode to the protection mode.



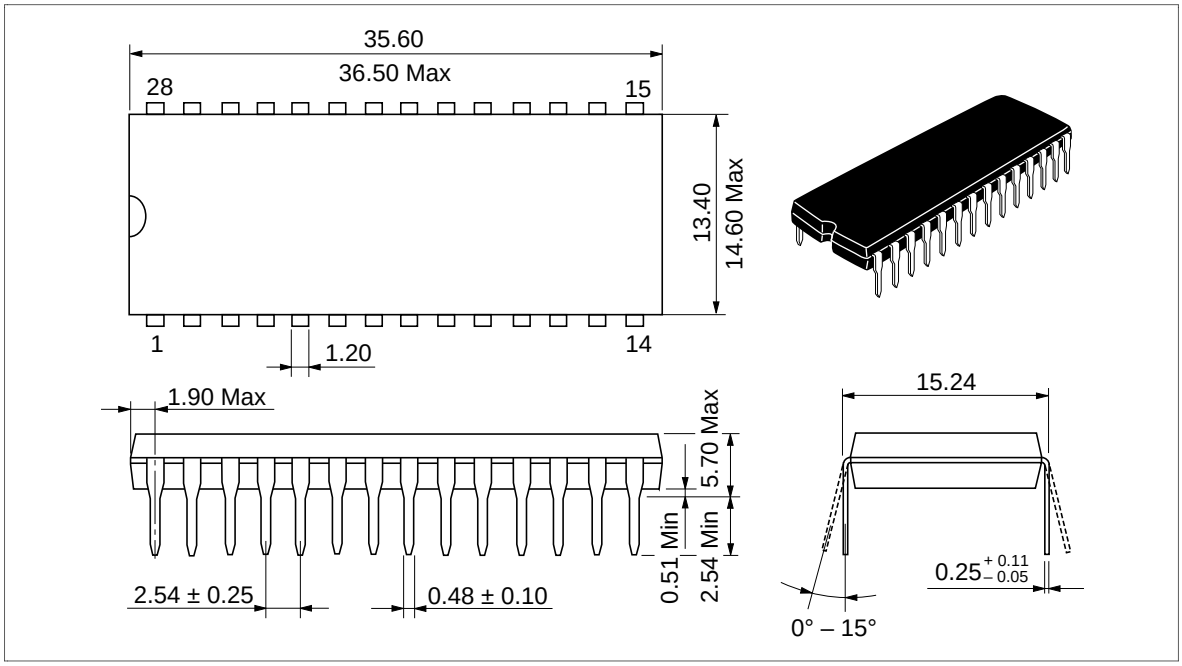
Software data protection mode can be cancelled by inputting the following 6 bytes. After that, this device turns to the non-protection mode and can write data normally. But when the data is input in the cancelling cycle, the data cannot be written.



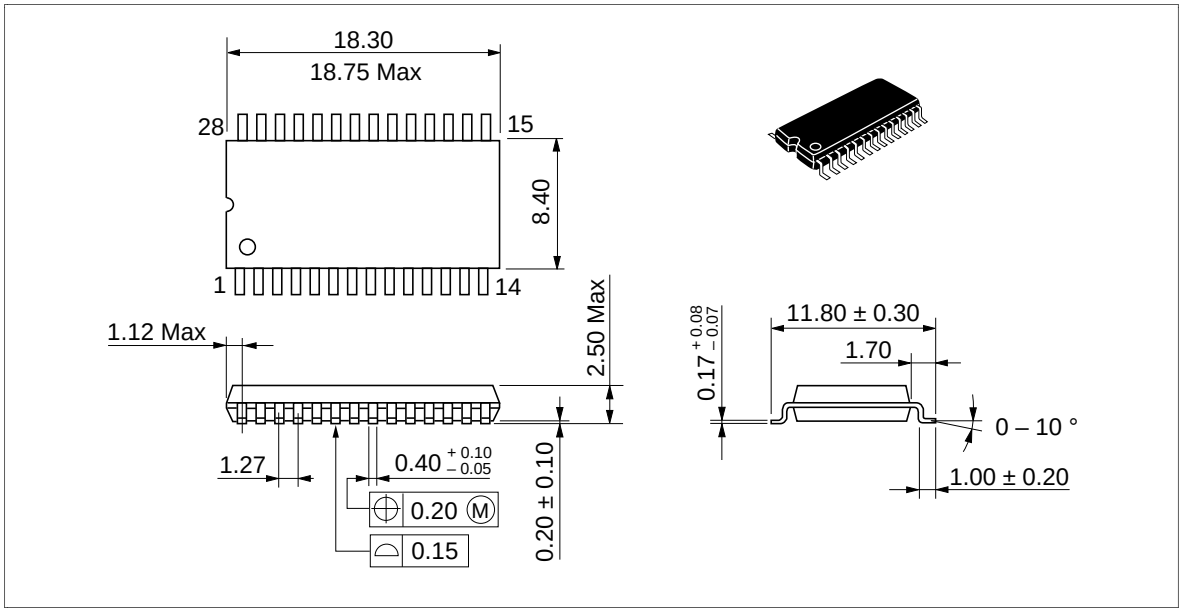
The software data protection is not enabled at the shipment.

Package Dimensions

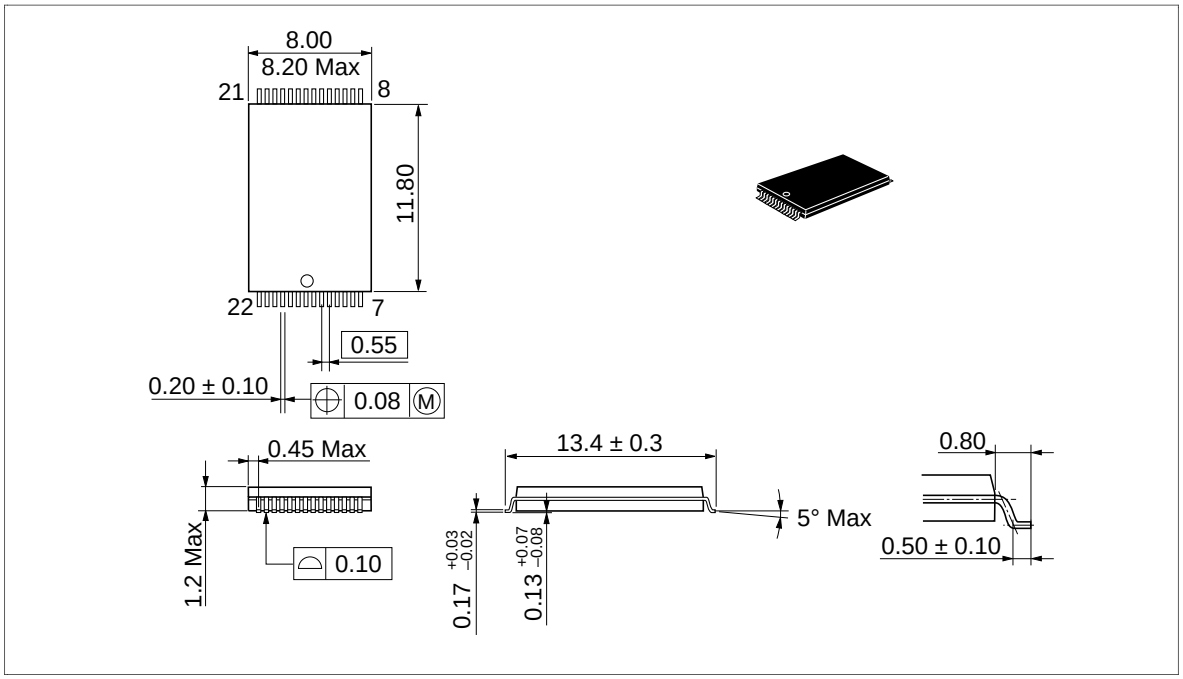
HN58C256AP Series (DP-28) Unit: mm



HN58C256AFP Series (FP-28D) Unit: mm



HN58C256AT Series (TFP-28DB) Unit: mm



HN58C257AT Series (TFP-32DA) Unit: mm