HN27C256HP/HFP Series

32768-word × 8-bit CMOS One Time Electrically Programmable ROM

HITACHI

ADE-203-
Maintenance only
Rev. 0.0
Dec. 1, 1995

Description

The HN27C256HP/HFP is a 32768-word by 8-bit one time electrically programmable ROM. Initially, all bits of the HN27C256HP/HFP are in the „1“ State (Output High). Data is introduced by selectively programming „0“ into the desired bit locations. This device is packaged in a 28-pin plastic package (DIP, SOP). Therefore, this device cannot be re-written.

Features

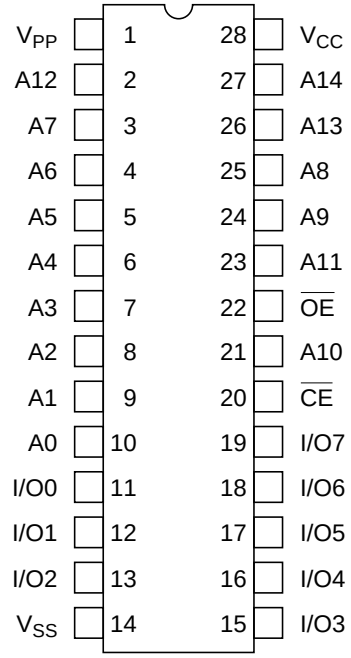
- High speed
  Access time: 85/100 ns (max)
- Low power dissipation
  Active mode: 30 mW (typ) (f = 1 MHz)
- High reliability and fast programming
  Programming voltage: +12.5 V DC
  Fast High-Reliability Programming Algorithm available
- Device identifier mode
  Manufacturer code and device code

Ordering Information

Type No.	Access Time	Package
HN27C256HP-85 HN27C256HP-10	85 ns 100 ns	28-pin plastic DIP (DP-28)
HN27C256HFP-85T HN27C256HFP-10T	85 ns 100 ns	28-pin plastic SOP (FP-28DA)

Note: This device is not available for new application.

Pin Arrangement

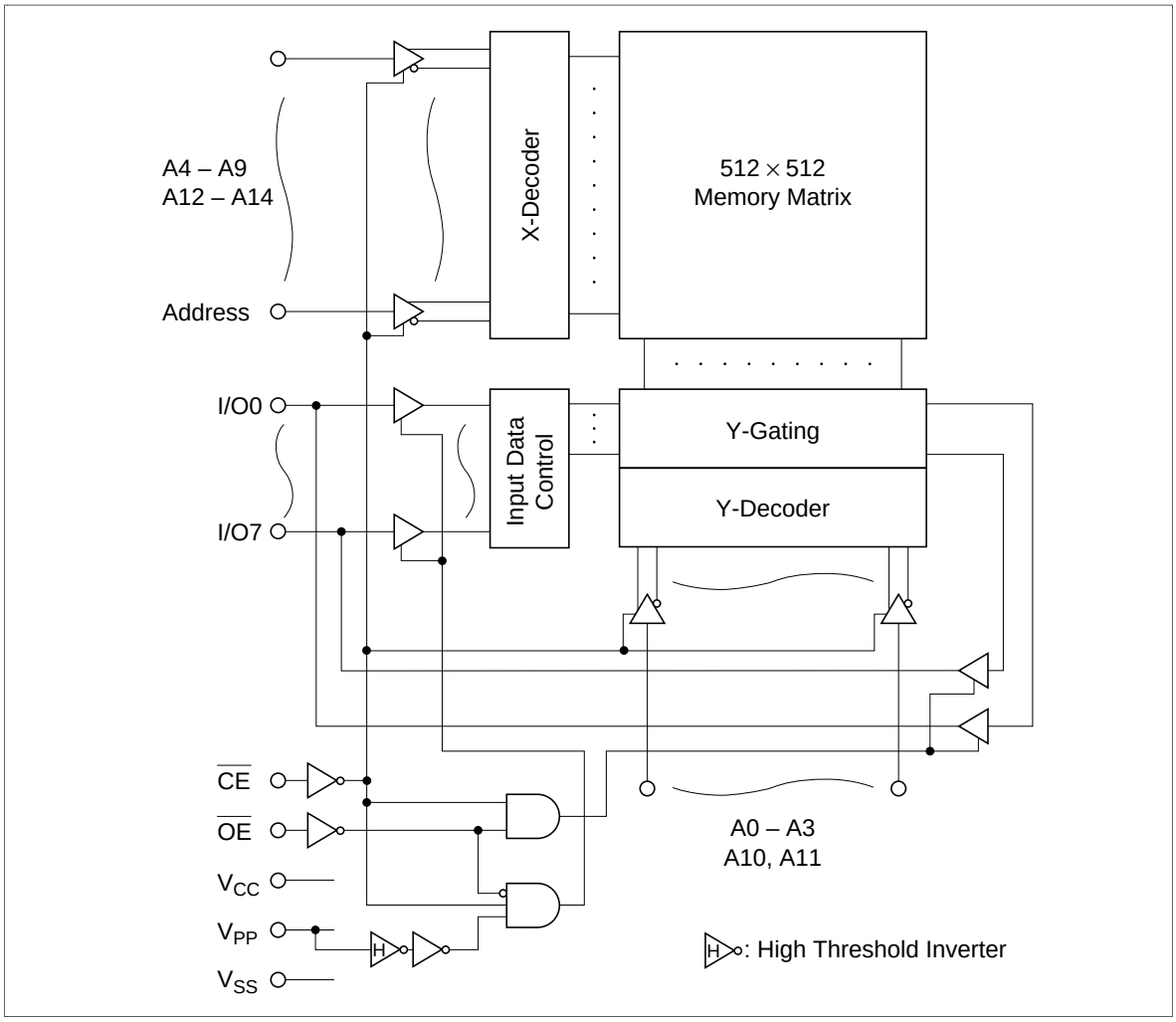


(Top View)

Pin Description

Pin Name	Function
A0 – A14	Address
I/O0 – I/O7	Input/output
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
V_{CC}	Power supply
V_{PP}	Programming power supply
V_{SS}	Ground

Block Diagram



Mode Selection

Mode	$\overline{CE}$ (20)	$\overline{OE}$ (22)	A9 (24)	V_{PP} (1)	V_{CC} (28)	I/O (11 – 13, 15 – 19)
Read	V_{IL}	V_{IL}	X	V_{CC}	V_{CC}	Dout
Output disable	V_{IL}	V_{IH}	X	V_{CC}	V_{CC}	High-Z
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	High-Z
Program	V_{IL}	V_{IH}	X	V_{PP}	V_{CC}	Din
Program verify	V_{IH}	V_{IL}	X	V_{PP}	V_{CC}	Dout
Optional verify	V_{IL}	V_{IL}	X	V_{PP}	V_{CC}	Dout
Program inhibit	V_{IH}	V_{IH}	X	V_{PP}	V_{CC}	High-Z
Identifier	V_{IL}	V_{IL}	V_H *2	V_{CC}	V_{CC}	Code

Notes: 1. x = Don't care.
2. V_H = 12.0 V ± 0.5 V.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
All input and output voltage*1	Vin, Vout	–0.6*2 to +7.0	V
A9 input voltage*1	V_{ID}	–0.6*2 to +13.5	V
V_{PP} voltage*1	V_{PP}	–0.6 to +13.5	V
V_{CC} voltage*1	V_{CC}	–0.6 to +7.0	V
Operating temperature range	Topr	0 to +70	°C
Storage temperature range	Tstg	–55 to +125	°C
Storage temperature range under bias	Tbias	–10 to +80	°C

Notes: 1. Relative to V_{SS}.
2. Vin, Vout, V_{ID} min = –1.0 V for pulse width ≤ 50 ns.

Capacitance (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	Cin	—	4	8	pF	Vin = 0 V
Output capacitance	Cout	—	8	12	pF	Vout = 0 V

Read Operation

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{PP} = V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	—	—	2	µA	Vin = 0 V to V_{CC}
Output leakage current	I_{LO}	—	—	2	µA	Vout = 0 V to V_{CC}
V_{PP} current	I_{PP1}	—	1	100	µA	V_{PP} = 5.5 V
Standby V_{CC} current	I_{SB}	—	—	15	mA	$\overline{CE}$ = V_{IH}
Operating V_{CC} current	I_{CC1}	—	—	30	mA	$\overline{CE}$ = V_{IL}, Iout = 0 mA
	I_{CC2}	—	—	40	mA	f = 11.8 MHz, Iout = 0 mA
	I_{CC3}	—	5	15	mA	f = 1 MHz, Iout = 0 mA
Input low voltage[*3]	V_{IL}	–0.3[*1]	—	0.8	V	
Input high voltage[*3]	V_{IH}	2.2	—	V_{CC} + 1.0[*2]	V	
Output low voltage	V_{OL}	—	—	0.45	V	I_{OL} = 2.1 mA
Output high voltage	V_{OH1}	2.4	—	—	V	I_{OH} = –1.0 mA
	V_{OH2}	V_{CC} – 0.7	—	—	V	I_{OH} = –100 µA

Notes: 1. V_{IL} min = –1.0 V for pulse width ≤ 50 ns.
2. V_{IH} max = V_{CC} + 1.5 V for pulse width ≤ 20 ns.
If V_{IH} is over the specified maximum value, read operation cannot be guaranteed.
3. Only defined for DC function test. V_{IL} max = 0.45 V, V_{IH} min = 2.4 V for AC function test.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{PP} = V_{CC})

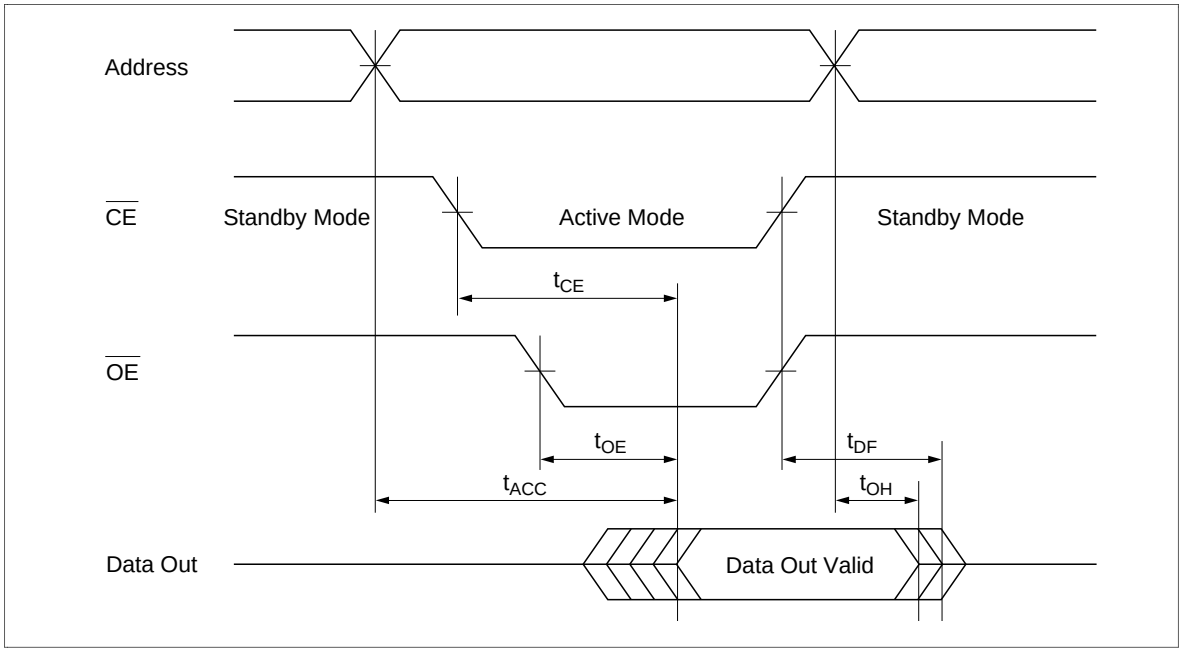
Test Conditions

- Input pulse levels: 0.45 V to 2.4 V
- Input rise and fall time: ≤ 10 ns
- Output load: 1TTL gate + 100 pF
- Reference levels for measuring timing: Inputs; 1.5 V
  Outputs; 1.5 V

		HN27C256HP-85 HN27C256HFP-85T		HN27C256HP-10 HN27C256HFP-10T			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Address to output delay	t_{ACC}	—	85	—	100	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to output delay	t_{CE}	—	85	—	100	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to output delay	t_{OE}	—	45	—	55	ns	$\overline{CE}$ = V_{IL}
$\overline{OE}$ high to output float	t_{DF}	0	30	0	35	ns	$\overline{CE}$ = V_{IL}
Address to output hold	t_{OH}	5	—	5	—	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

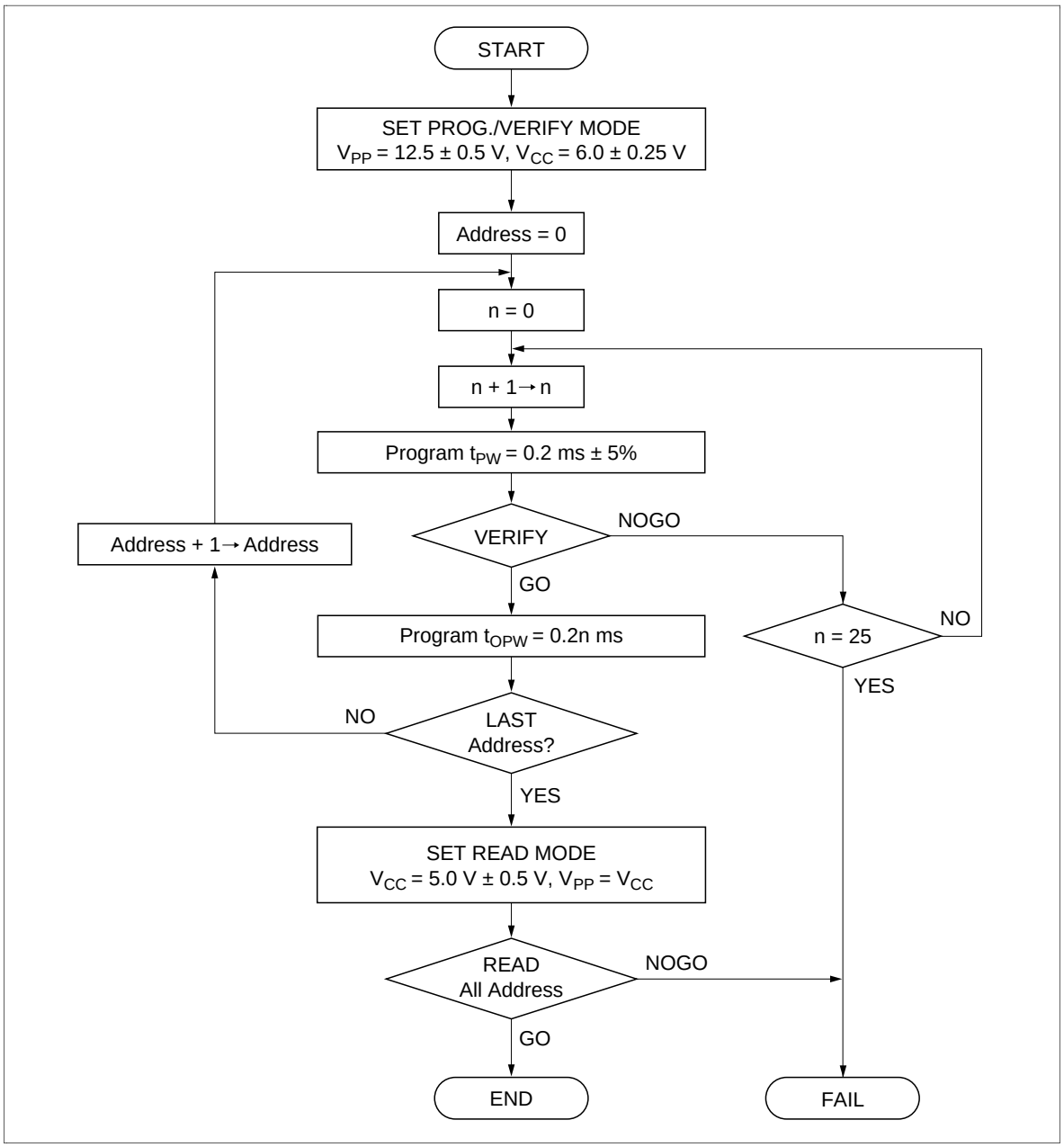
Note: t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

Read Timing Waveform



Fast High-Reliability Programming

This device can be applied the Fast High-Reliability Programming Algorithm shown in following flowchart. This algorithm offers both faster programming time and high reliability data retension. A theoretical programming time (except brank checking and verifying time) is one-tenth of conventional high performance programming algorithm's. Regarding the model and software version of the programmers available this algorithm, please contact programmer maker.



DC Characteristics (Ta = 25°C ± 5°C, V_{CC} = 6 V ± 0.25 V, V_{PP} = 12.5 V ± 0.5 V)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	—	—	2	µA	Vin = 0 V to V_{CC}
V_{PP} supply current	I_{PP}	—	—	30	mA	$\overline{CE}$ = V_{IL}
Operating V_{CC} current	I_{CC}	—	—	30	mA	
Input low level	V_{IL}	–0.1[*5]	—	0.8	V	
Input high level	V_{IH}	2.2	—	V_{CC} + 0.5[*6]	V	
Output low voltage during verify	V_{OL}	—	—	0.45	V	I_{OL} = 2.1 mA
Output high voltage during verify	V_{OH}	2.4	—	—	V	I_{OH} = –400 µA

Notes:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} must not exceed 13.5 V including overshoot.
3. An influence may be had upon device reliability if the device is installed or removed while V_{PP} = 12. 5V.
4. Do not alter V_{PP} either V_{IL} to 12.5 V or 12.5 V or 12.5 V to V_{IL} when $\overline{CE}$ = Low.
5. V_{IL} min = –0.6 V for pulse width ≤ 20 ns.
6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

AC Characteristics (Ta = 25°C ± 5°C, V_{CC} = 6 V ± 0.25 V, V_{PP} = 12.5 V ± 0.5 V)

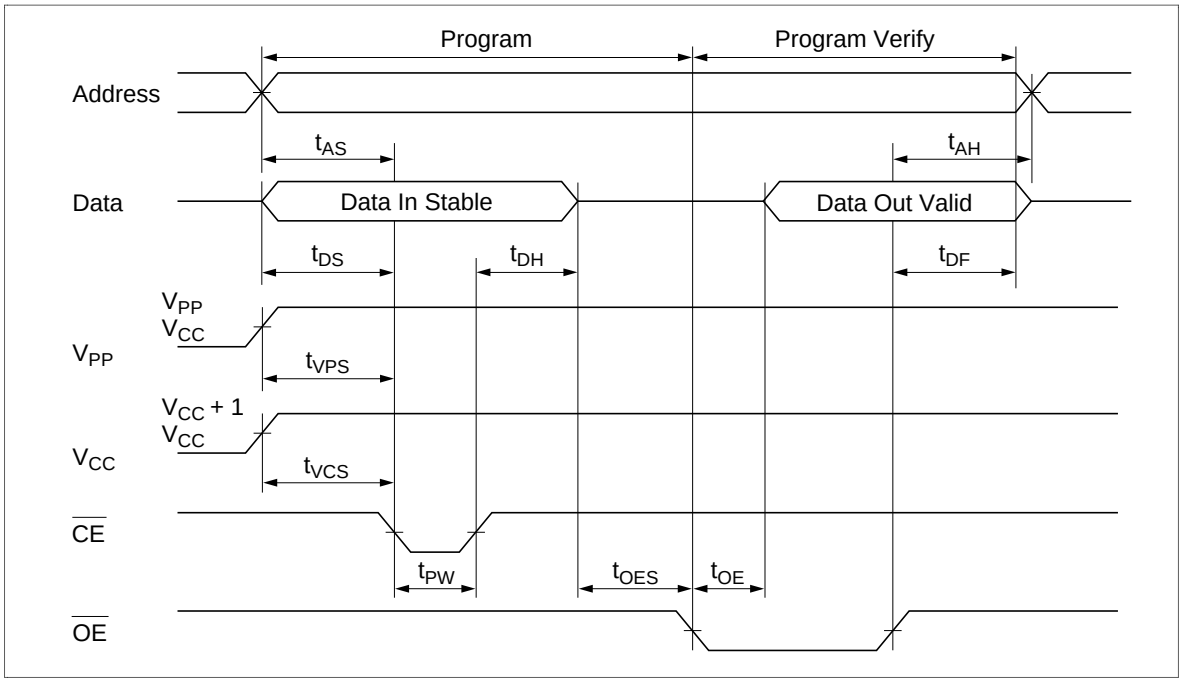
Test Conditions

- Input pulse levels: 0.45 V to 2.4 V
- Input rise and fall time: ≤ 20 ns
- Reference levels for measuring timing: Inputs; 0.8 V and 2.0 V
  Outputs; 0.8 V and 2.0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Address setup time	t_{AS}	2	—	—	µs	
$\overline{OE}$ setup time	t_{OES}	2	—	—	µs	
Data setup time	t_{DS}	2	—	—	µs	
Address hold time	t_{AH}	0	—	—	µs	
Data hold time	t_{DH}	2	—	—	µs	
V_{PP} setup time	t_{VPS}	2	—	—	µs	
V_{CC} setup time	t_{VCS}	2	—	—	µs	
$\overline{CE}$ initial programming pulse width	t_{PW}	0.19	0.20	0.21	ms	
$\overline{CE}$ over programming pulse width	t_{OPW} *1	0.19	—	5.25	ms	
Data valid from $\overline{OE}$	t_{OE}	0	—	150	ns	
$\overline{OE}$ to output float delay	t_{DF} *2	—	—	130	ns	

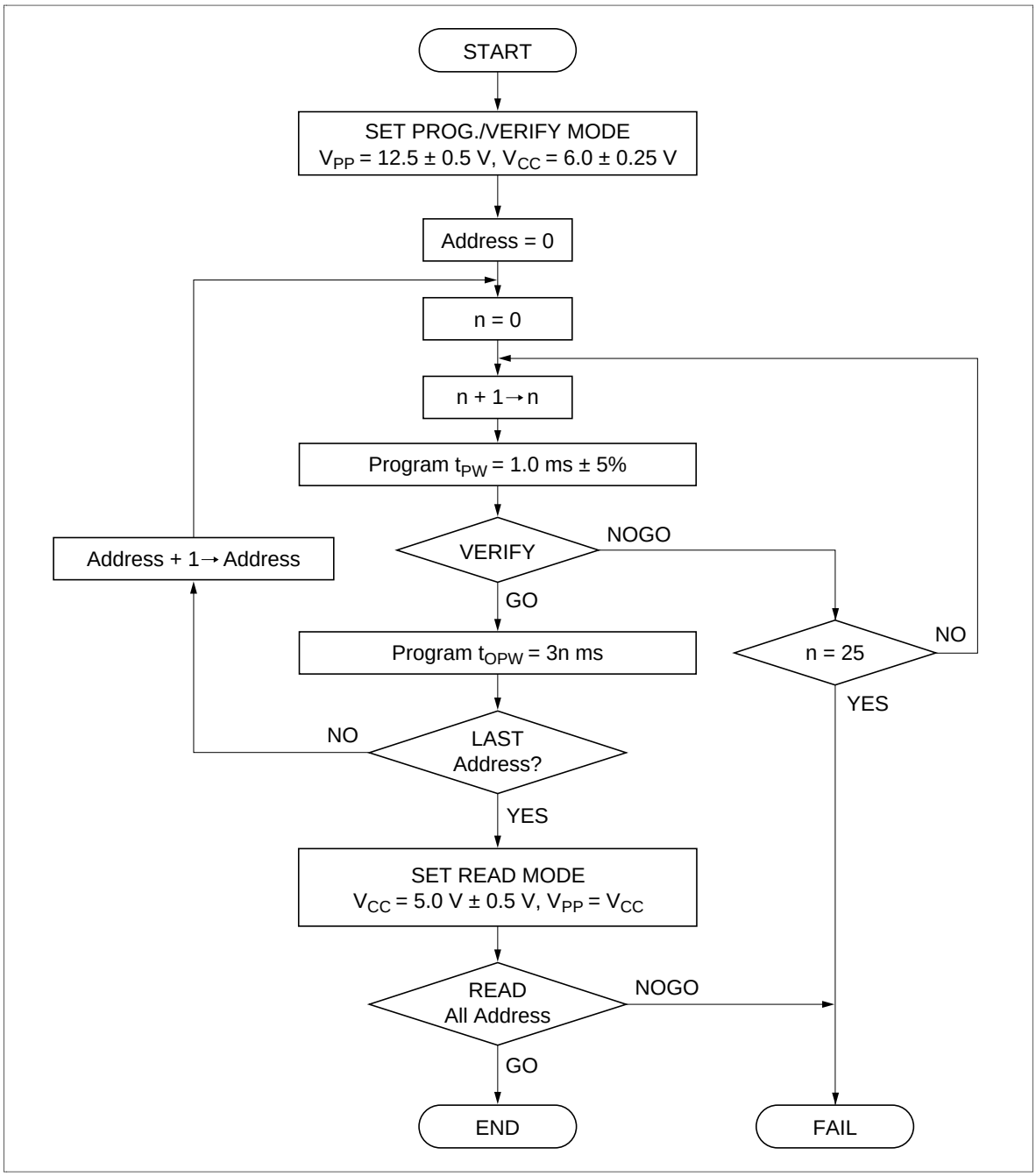
Notes: 1. Refer to the Fast High-Reliability Programming Flowchart for t_{OPW}.
2. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

Fast High-Reliability Programming Timing Waveform



High Performance Programming

This device can be applied the high performance programming algorithm shown in following flowchart. This algorithm is as same as our 256-kbit EPROM series so existing programmers can be used with this device. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.


START
SET PROG./VERIFY MODE
V_{PP} = 12.5 ± 0.5 V, V_{CC} = 6.0 ± 0.25 V
Address = 0
n = 0
n + 1→n
Program t_{PW} = 1.0 ms ± 5%
VERIFY
NOGO
GO
Address + 1→Address
Program t_{OPW} = 3n ms
n = 25
NO
YES
NO
LAST
Address?
YES
SET READ MODE
V_{CC} = 5.0 V ± 0.5 V, V_{PP} = V_{CC}
READ
All Address
NOGO
GO
END
FAIL

DC Characteristics (Ta = 25°C ± 5°C, V_{CC} = 6 V ± 0.25 V, V_{PP} = 12.5 V ± 0.5 V)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	—	—	2	µA	Vin = 0 V to V_{CC}
V_{PP} supply current	I_{PP}	—	—	30	mA	$\overline{CE}$ = V_{IL}
Operating V_{CC} current	I_{CC}	—	—	30	mA	
Input low level	V_{IL}	–0.1[*5]	—	0.8	V	
Input high level	V_{IH}	2.2	—	V_{CC} + 0.5[*6]	V	
Output low voltage during verify	V_{OL}	—	—	0.45	V	I_{OL} = 2.1 mA
Output high voltage during verify	V_{OH}	2.4	—	—	V	I_{OH} = –400 µA

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} must not exceed 13.5 V including overshoot.
3. An influence may be had upon device reliability if the device is installed or removed while V_{PP} = 12. 5V.
4. Do not alter V_{PP} either V_{IL} to 12.5 V or 12.5 V to V_{IL} when $\overline{CE}$ = Low.
5. V_{IL} min = –0.6 V for pulse width ≤ 20 ns.
6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

AC Characteristics (Ta = 25°C ± 5°C, V_{CC} = 6 V ± 0.25 V, V_{PP} = 12.5 V ± 0.5 V)

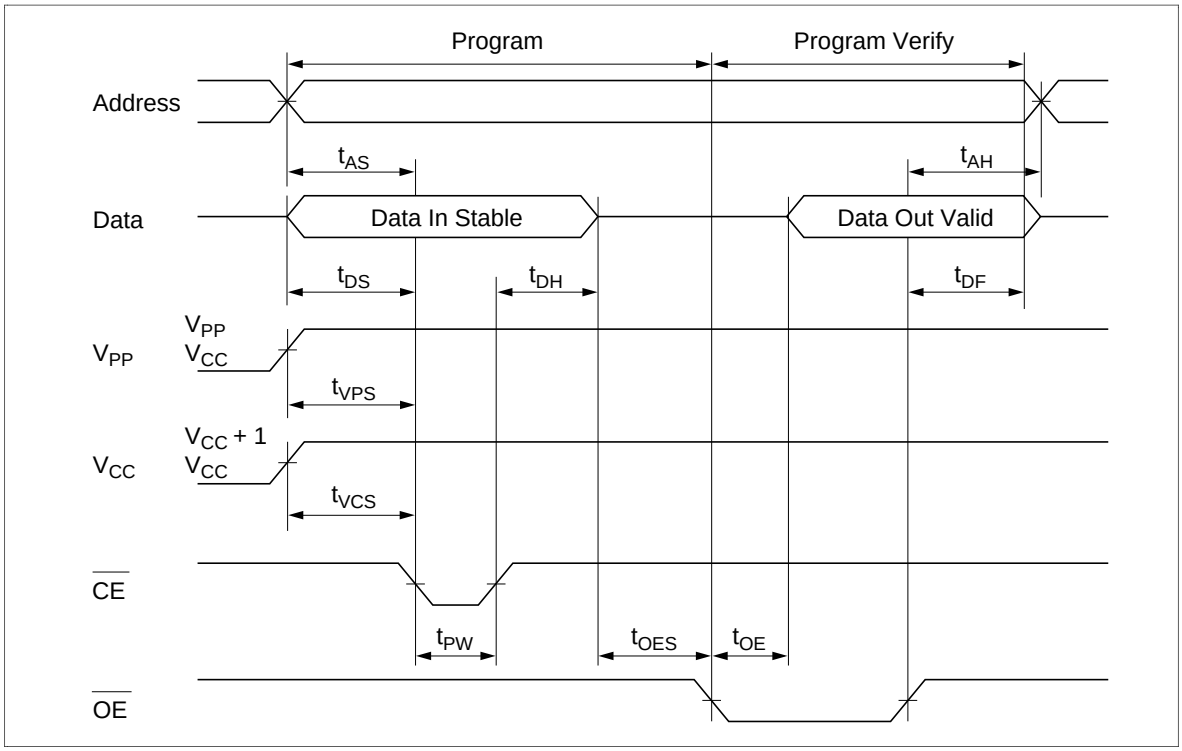
Test Conditions

- Input pulse levels: 0.45 V to 2.4 V
- Input rise and fall time: ≤ 20 ns
- Reference levels for measuring timing: Inputs; 0.8 V and 2.0 V
  Outputs; 0.8 V and 2.0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Address setup time	t_{AS}	2	—	—	µs	
$\overline{OE}$ setup time	t_{OES}	2	—	—	µs	
Data setup time	t_{DS}	2	—	—	µs	
Address hold time	t_{AH}	0	—	—	µs	
Data hold time	t_{DH}	2	—	—	µs	
V_{PP} setup time	t_{VPS}	2	—	—	µs	
V_{CC} setup time	t_{VCS}	2	—	—	µs	
$\overline{CE}$ initial programming pulse width	t_{PW}	0.95	1.0	1.05	ms	
$\overline{CE}$ over programming pulse width	t_{OPW} *1	2.85	—	78.75	ms	
Data valid from $\overline{OE}$	t_{OE}	0	—	150	ns	
$\overline{OE}$ to output float delay	t_{DF} *2	—	—	130	ns	

Notes: 1. Refer to the high performance programming flowchart for t_{OPW}.
2. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

High Performance Programming Timing Waveform



Mode Description

Device Identifier Mode

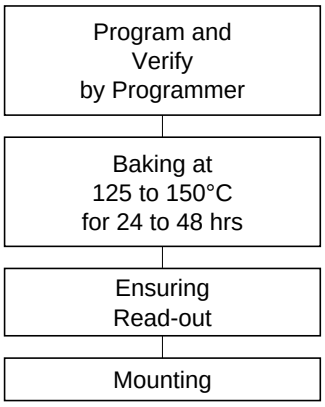
Programming condition of OTPROM is various according to OTPROM manufacturers and device types. It may cause miss operation. To countermeasure it, some OTPROMs provide maker identifier code. Users can write OTPROM by reading out write condition coded before shipped. Some commercial programmers can set write condition by recognizing this code. This function enables effective program. Regarding commercial programmers that can recognize this device's identifier code, please contact programmer maker.

	A0	**I/O7**	**I/O6**	**I/O5**	**I/O4**	**I/O3**	**I/O2**	**I/O1**	**I/O0**	
Identifier	**(10)**	**(19)**	**(18)**	**(17)**	**(16)**	**(15)**	**(13)**	**(12)**	**(11)**	**Hex Data**
Manufacturer code	V_{IL}	0	0	0	0	0	1	1	1	07
Device code	V_{IH}	0	0	1	1	0	0	0	1	31

Notes: 1. A9 = 12.0 V ± 0.5 V.
2. A1 – A8, A10 – A14, $\overline{CE}$, $\overline{OE}$ = V_{IL}.

Recommended Screening Conditions

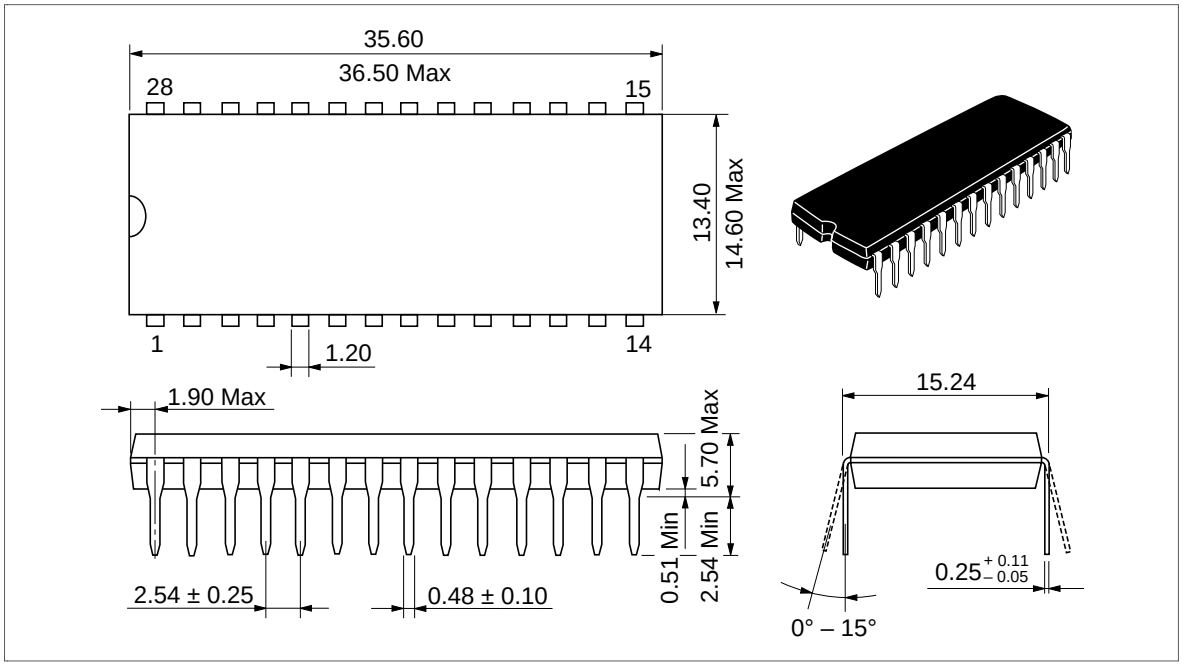
Before mounting, please make the screening (baking without bias) shown in the right.



Recommended
Screening conditions

Package Dimensions

HN27C256HP Series (DP-28) Unit: mm



HN27C256HFP Series (FP-28DA) Unit: mm