

Advanced Information

- 8 388 608 words by 32-bit organization
- Fast access and cycle time
 - 50 ns access time
 - 84 ns cycle time (-50 version)
 - 60 ns access time
 - 104 ns cycle time (-60 version)
- Hyper page mode (EDO) capability
 - 20 ns cycle time (-50 version)
 - 25 ns cycle time (-60 version)
- Single + 5 V (± 10 %) supply
- Low power dissipation
 - max. 5280 mW active (-50 version)
 - max. 4840 mW active (-60 version)
 - CMOS – 88 mW standby
 - TTL – 176 mW standby
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh
 - $\overline{\text{RAS}}$ -only-refresh
 - Hidden-refresh
- 16 decoupling capacitors mounted on substrate
- All inputs, outputs and clocks fully TTL compatible
- 72 pin Single in-Line Memory Module (L-SIM-72-15) with 25.40 mm height
- Utilizes sixteen 4M x 4-DRAMs in SOJ packages
- 2048 refresh cycles / 32 ms
- Optimized for use in byte-write non-parity applications
- Tin-Lead contact pads (S-version)
- Gold contact pads (GS-version)

The HYM 328025S/GS-50/-60 is a 32 MByte DRAM module organized as 8 388 608 words by 32-bit in a 72-pin single-in-line package comprising sixteen HYB 5117405BJ 4M × 4 DRAMs in 300 mil wide SOJ-packages mounted together with sixteen 0.2 µF ceramic decoupling capacitors on a PC board.

Each HYB 5117405BJ is described in the data sheet and is fully electrical tested and processed according to SIEMENS standard quality procedure prior to module assembly. After assembly onto the board, a further set of electrical tests is performed.

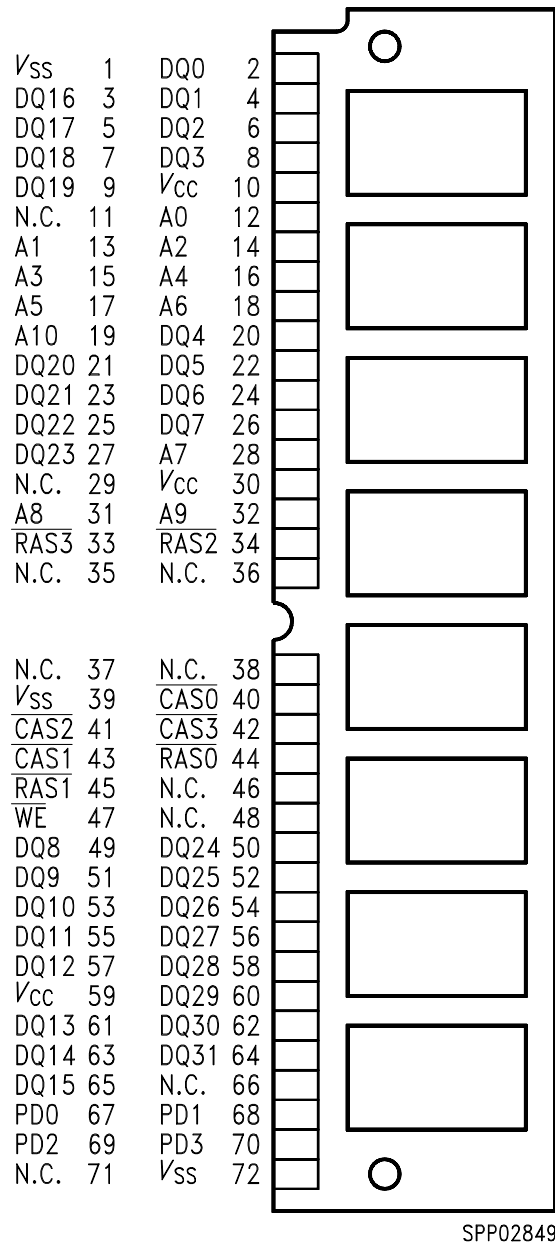
The speed of the module can be detected by the use of four presence detect pins.

The common I/O feature on the HYM 328025S/GS-60/-70 dictates the use of early write cycles.

Ordering Information

Type	Ordering Code	Package	Description
HYM 328025S-50	On request	L-SIM-72-15	EDO-DRAM Module (access time 50 ns)
HYM 328025S-60	On request	L-SIM-72-15	EDO-DRAM Module (access time 60 ns)
HYM 328025GS-50	Q67100-Q2098	L-SIM-72-15	EDO-DRAM Module (access time 50 ns)
HYM 328025GS-60	Q67100-Q2099	L-SIM-72-15	EDO-DRAM Module (access time 60 ns)

Pin Configuration
(top view)

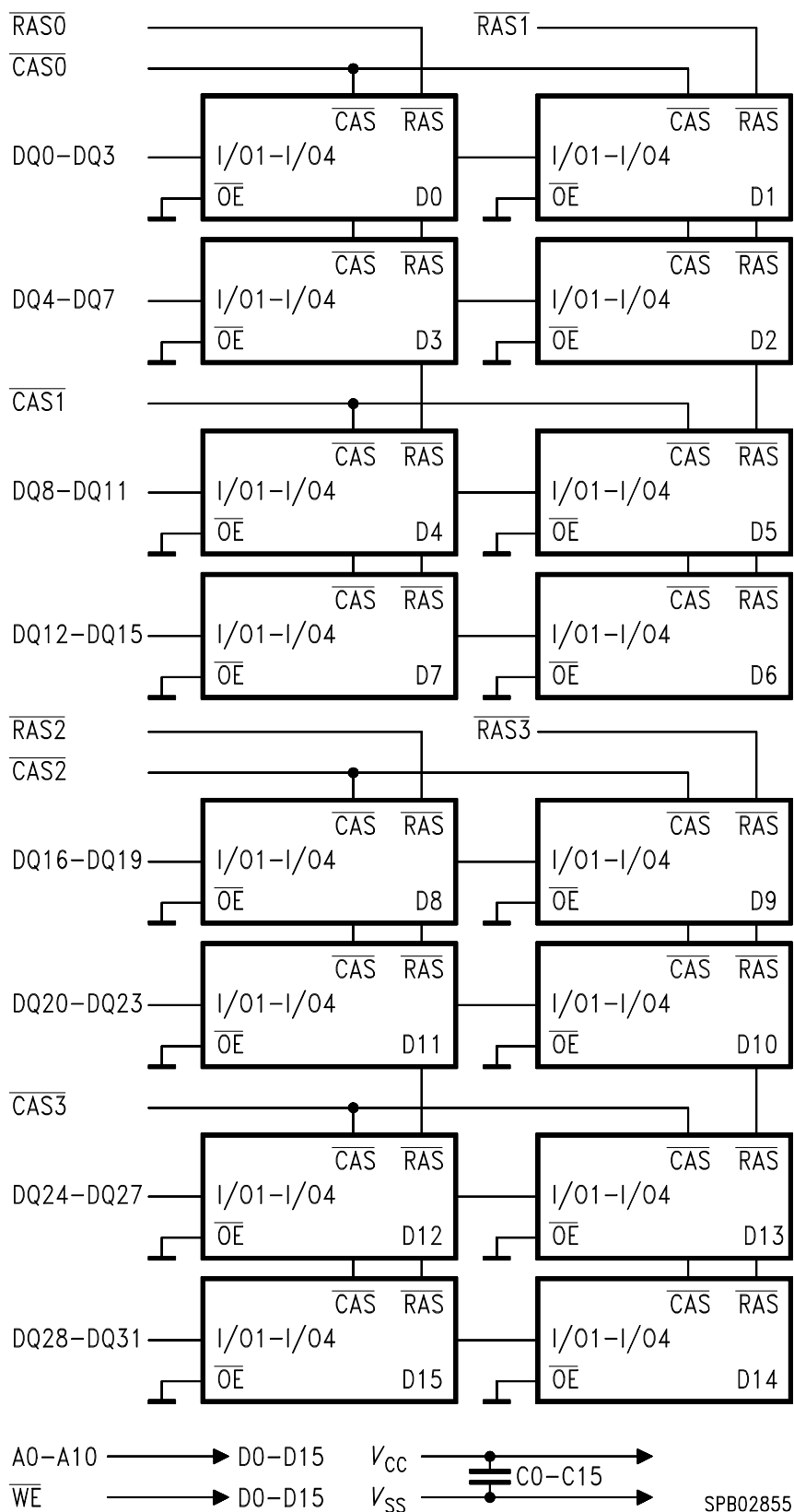


Pin Names

A0-A10	Address Inputs
DQ0-DQ31	Data Input/Output
CAS0 - CAS3	Column Address Strobe
RAS0- RAS3	Row Address Strobe
WE	Read/Write Input
V _{cc}	Power (+ 5 V)
V _{ss}	Ground
PD	Presence Detect Pin
N.C.	No Connection

Presence Detect Pins

	-50	-60
PD0	N.C.	N.C.
PD1	V _{ss}	V _{ss}
PD2	V _{ss}	N.C.
PD3	V _{ss}	N.C.



Block Diagram

Absolute Maximum Ratings

Operation temperature range 0 to + 70 °C
 Storage temperature range – 55 to 125 °C
 Input/output voltage – 0.5 V to min ($V_{CC} + 0.5$, 7.0) V
 Power supply voltage – 1 to + 7 V
 Power dissipation 6.72 W
 Data out current (short circuit) 50 mA

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

$T_A = 0$ to 70 °C, $V_{CC} = 5$ V $\pm$ 10 %

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input high voltage	V_{IH}	2.4	$V_{CC} + 0.5$	V	1)
Input low voltage	V_{IL}	– 0.5	0.8	V	1)
Output high voltage ($I_{OUT} = -5$ mA)	V_{OH}	2.4	–	V	1)
Output low voltage ($I_{OUT} = 4.2$ mA)	V_{OL}	–	0.4	V	1)
Input leakage current (0 V < V_{IN} < 6.5 V, all other pins = 0 V)	$I_{I(L)}$	– 20	20	μA	1)
Output leakage current (DO is disabled, 0 V < V_{OUT} < 5.5 V)	$I_{O(L)}$	– 10	10	μA	1)
Average V_{CC} supply current (RAS, CAS, address cycling, $t_{RC} = t_{RC}$ min) –50 version –60 version	I_{CC1}	– –	960 880	mA mA	2) 3) 4)
Standby V_{CC} supply current (RAS = CAS = V_{IH})	I_{CC2}	–	32	mA	
Average V_{CC} supply current during RAS only refresh cycles (RAS cycling, CAS = V_{IH} , $t_{RC} = t_{RC}$ min) –50 version –60 version	I_{CC3}	– –	960 880	mA mA	2) 4)

DC Characteristics¹⁾ (cont'd)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Average V_{CC} supply current during hyper page mode (EDO) ($\overline{RAS} = V_{IL}$, $\overline{CAS}$, address cycling, $t_{PC} = t_{PC\ min}$) -50 version -60 version	I_{CC4}	— —	560 440	mA mA	2) 3) 4)
Standby V_{CC} supply current ($\overline{RAS} = \overline{CAS} = V_{CC} - 0.2\ V$)	I_{CC5}	—	16	mA	1)
Average V_{CC} supply current during CAS-before-RAS refresh mode ($\overline{RAS}$, $\overline{CAS}$ cycling, $t_{RC} = t_{RC\ min}$) -50 version -60 version	I_{CC6}	— —	960 880	mA mA	2) 4)

Capacitance

$T_A = 0\ \text{to}\ 70\ ^\circ\text{C}$, $V_{CC} = 5\ V \pm 10\ \%$, $f = 1\ \text{MHz}$

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance ($A0$ to $A10$, $\overline{WE}$)	C_{I1}	—	120	pF
Input capacitance ($\overline{RAS0}$ - $\overline{RAS3}$)	C_{I2}	—	45	pF
Input capacitance ($\overline{CAS0}$ - $\overline{CAS3}$)	C_{I3}	—	40	pF
I/O capacitance ($DQ0$ - $DQ31$)	C_{IO}	—	25	pF

AC Characteristics ⁵⁾⁶⁾

$T_A = 0 \text{ to } 70^\circ\text{C}$, $V_{CC} = 5 \text{ V} \pm 10\%$, $t_T = 2 \text{ ns}$

Parameter	Symbol	Limit Values				Unit	Note
		-50		-60			
		min.	max.	min.	max.		

Common Parameters

Random read or write cycle time	t_{RC}	84	—	104	—	ns	
RAS precharge time	t_{RP}	30	—	40	—	ns	
RAS pulse width	t_{RAS}	50	10k	60	10k	ns	
CAS pulse width	t_{CAS}	8	10k	10	10k	ns	
Row address setup time	t_{ASR}	0	—	0	—	ns	
Row address hold time	t_{RAH}	8	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	ns	
Column address hold time	t_{CAH}	8	—	10	—	ns	
RAS to CAS delay time	t_{RCD}	12	37	14	45	ns	
RAS to column address delay time	t_{RAD}	10	25	12	30	ns	
RAS hold time	t_{RSH}	13		15	—	ns	
CAS hold time	t_{CSH}	50		60	—	ns	
CAS to RAS precharge time	t_{CRP}	5	—	5	—	ns	
Transition time (rise and fall)	t_T	1	50	1	50	ns	7
Refresh period	t_{REF}	—	32	—	32	ms	

Read Cycle

Access time from RAS	t_{RAC}	—	50	—	60	ns	8, 9
Access time from CAS	t_{CAC}	—	13	—	15	ns	8, 9
Access time from column address	t_{AA}	—	25	—	30	ns	8,10
Column address to RAS lead time	t_{RAL}	25	—	30	—	ns	
Read command setup time	t_{RCS}	0	—	0	—	ns	
Read command hold time	t_{RCH}	0	—	0	—	ns	11
Read command hold time referenced to RAS	t_{RRH}	0	—	0	—	ns	11
CAS to output in low-Z	t_{CLZ}	0	—	0	—	ns	8
Output buffer turn-off delay	t_{OFF}	0	13	0	15	ns	12

AC Characteristics (cont'd) ⁵⁾⁶⁾

$T_A = 0 \text{ to } 70^\circ\text{C}$, $V_{CC} = 5 \text{ V} \pm 10\%$, $t_T = 2 \text{ ns}$

Parameter	Symbol	Limit Values				Unit	Note
		-50		-60			
		min.	max.	min.	max.		

Early Write Cycle

Write command hold time	t_{WCH}	8	—	10	—	ns	
Write command pulse width	t_{WP}	8	—	10	—	ns	
Write command setup time	t_{WCS}	0	—	0	—	ns	13
Write command to $\overline{\text{RAS}}$ lead time	t_{RWL}	13	—	15	—	ns	
Write command to $\overline{\text{CAS}}$ lead time	t_{CWL}	13	—	15	—	ns	
Data setup time	t_{DS}	0	—	0	—	ns	14
Data hold time	t_{DH}	8	—	10	—	ns	14

Hyper Page Mode (EDO) Cycle

Hyper page mode (EDO) cycle time	t_{HPC}	20	—	25	—	ns	
$\overline{\text{CAS}}$ precharge time	t_{CP}	8	—	10	—	ns	
Access time from $\overline{\text{CAS}}$ precharge	t_{CPA}	—	27	—	32	ns	7
Output data hold time	t_{COH}	5	—	5	—	ns	
$\overline{\text{RAS}}$ pulse width in hyper page mode	t_{RAS}	50	200k	60	200k	ns	
$\overline{\text{CAS}}$ precharge to $\overline{\text{RAS}}$ Delay	t_{RHCP}	27	—	32	—	ns	

$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh Cycle

$\overline{\text{CAS}}$ setup time	t_{CSR}	10	—	10	—	ns	
$\overline{\text{CAS}}$ hold time	t_{CHR}	10	—	10	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	t_{RPC}	5	—	5	—	ns	
Write to $\overline{\text{RAS}}$ precharge time	t_{WRP}	10	—	10	—	ns	
Write hold time referenced to $\overline{\text{RAS}}$	t_{WRH}	10	—	10	—	ns	

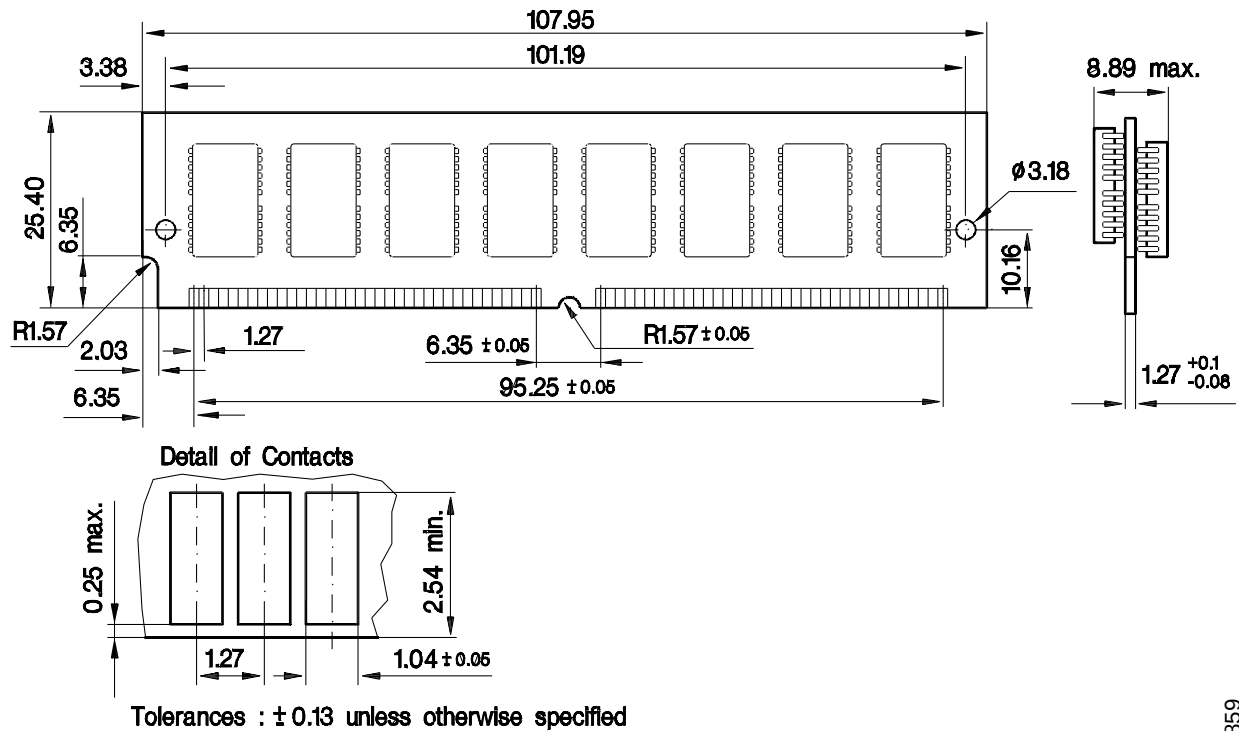
Notes:

- 1) All voltages are referenced to V_{SS} .
- 2) I_{CC1} , I_{CC3} , I_{CC4} and I_{CC6} depend on cycle rate.
- 3) I_{CC1} and I_{CC4} depend on output loading. Specified values are obtained with the output open.
- 4) Address can be changed once or less while $RAS = V_{IL}$. In case of I_{CC4} it can be changed once or less during a hyper page mode (EDO) cycle.
- 5) An initial pause of 200 μs is required after power-up followed by 8 $\overline{RAS}$ cycles of which at least one cycle has to be a refresh cycle, before proper device operation is achieved. In case of using the internal refresh counter, a minimum of 8 $\overline{CAS}$ -before- $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
- 6) AC measurements assume $t_T = 2$ ns.
- 7) $V_{IH (min.)}$ and $V_{IL (max.)}$ are reference levels for measuring timing of input signals. Transition times are also measured between V_{IH} and V_{IL} .
- 8) Measured with the specified current load and 100 pF at $V_{OL} = 0.8$ V and $V_{OH} = 2.0$ V. Access time is determined by the latter of t_{RAC} , t_{CAC} , t_{AA} , t_{CPA} . t_{CAC} is measured from tristate.
- 9) Operation within the $t_{RCD (max.)}$ limit ensures that $t_{RAC (max.)}$ can be met. $t_{RCD (max.)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD (max.)}$ limit, then access time is controlled by t_{CAC} .
- 10) Operation within the $t_{RAD (max.)}$ limit ensures that $t_{RAC (max.)}$ can be met. $t_{RAD (max.)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD (max.)}$ limit, then access time is controlled by t_{AA} .
- 11) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
- 12) $t_{OFF (max.)}$ define the time at which the output achieves the open-circuit conditions and are not referenced to output voltage levels. t_{OFF} is referenced from the rising edge of RAS or CAS , whichever occurs last.
- 13) t_{WCS} is not a restrictive operating parameter. This is included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS (min.)}$, the cycle is an early write cycle and data out pin will remain open-circuit (high impedance) through the entire cycle.
- 14) These parameters are referenced to the $\overline{CAS}$ leading edge.

Package Outlines

L-SIM-72-15

(Single In-line Module)



GLS05859

Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

Dimensions in mm