HIP2030EVAL

August 1994

Isolated MCT/IGBT Gate Driver Evaluation Board

Features

- **3000VDC Isolation**
- **10,000V/μS dv/dt Capability**
- **± Polarity Gate Drive**
- **Standard Opto-Coupler LED Input**
- **Peak Output Current 6.0A**
- **Power CMOS Output Stage**
- **Fast Rise Time . . . . . .200ns at 60,000pF**
- **Ability to Drive MCT or IGBT Modules**
- **Programmable Minimum ON/OFF (Times)**
- **On Board Prototyping Area**
- **120kHz Gate Switching . . . . . C_{LOAD} at 15,000pF**

Applications

- **Resonant Inverters**
- **Motor Controllers**
- **Uninterruptible Power Supplies**
- **Inverters**
- **Converters**
- **Arc Welders**

Ordering Information

PART NUMBER	TEMPERATURE RANGE
HIP2030EVAL	-40°C to +85°C

Description

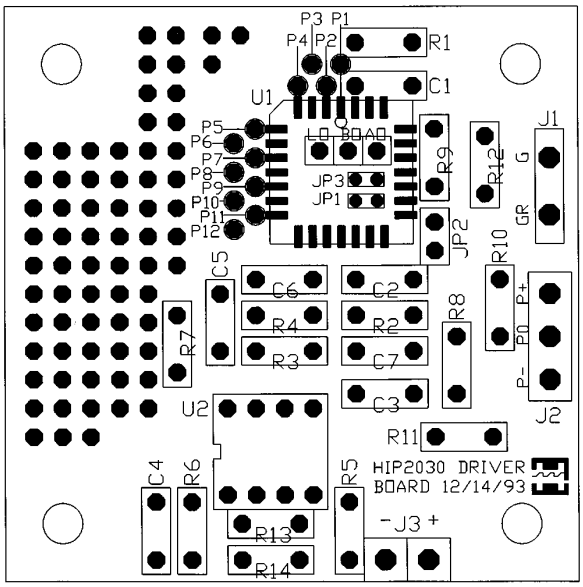
The HIP2030 is a medium voltage integrated circuit (MVIC) capable of driving large capacitive loads at high voltage slew rates (dv/dts). This device is optimized for driving 60nF of MOS gate capacitance at 30V peak to peak in less than 200ns. The half bridge gate driver is ideal for driving MOS Controlled Thyristor (MCT) and IGBT modules.

The architecture of the HIP2030 includes four comparator input channels, a 5V reference, a 12V regulator, and a high side charge pump. The device provides the user with the ability to control minimum low time (MLT) and minimum high time (MHT) at the gate channel output (GO) by varying two external capacitances. In addition, the device contains two uncommitted comparator channels (channels A and B) that can be used as monitors (temperature sensing), indicators (LEDs or opto-couplers), input signal conditioning (both contain Schmitt triggers), or oscillators.

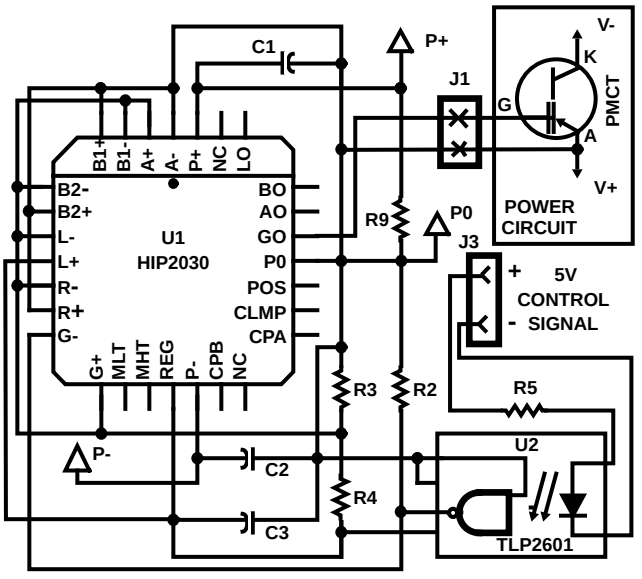
The Harris HIP2030 Evaluation Board (HIP2030EVAL) is a printed circuit board (PCB) developed to help evaluate the performance of the HIP2030 MCT/IGBT Driver IC in power switching circuits. The component layout of the HIP2030EVAL circuit enables the user to conveniently utilize either photo-coupled or fiber-optic receivers. In addition, the PCB layout has provisions for “on board prototyping” and special function components. This facilitates the gate drive circuit design and allows the user to exercise the internal architecture and special functions of the HIP2030.

Board Layout

ASSEMBLY LAYER



Simplified Board Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3918**

HIP2030EVAL Application Information

Initial HIP2030EVAL Configuration

The HIP2030EVAL is populated with the Harris Photo-Coupled Isolated Gate Driver (HPCIGD) components and is configured as a dual polarity gate driver. To operate the driver board, the user must provide a damping resistor, an isolated DC bias voltage between 24V and 30V, and a control signal to the photo-coupler subcircuit. The schematic of the HIP2030EVAL shows the initial jumper and component configurations in the PCB Schematic. For more detailed information please refer to Applications Note AN9408.

DC Input Power

The HIP2030EVAL is configured for a 12V regulated single supply DC bias (SSDCB) operation. The SSDCB bias scheme allows the HIP2030EVAL to operate reliably with a single isolated DC supply and will accept input bias voltages ranging from 24V to 30V. Dropping resistor R9 and an internal clamp V_{CLMP} are used in combination to provide a regulated 12VDC bias voltage for the HIP2030 logic circuitry. The DC voltage input connections, for SSDCB operation, are applied to connector J2 between inputs P+ and P-.

Control Signal

HIP2030EVAL photo-coupler input can be driven with any signal generator that can supply a control signal with a pulse amplitude of 5V peak and provide 25mA of diode current. The input signal connections for the photo-coupled subcircuit, shown in the Simplified Board Diagram, are applied to connector J3 between inputs (+) and (-). The input signal requirements of the HIP2030EVAL are designed to be simple and allows the user to control the driver board with peripherals that contain either discrete logic or linear circuits.

Gate Output (GO)

The HIP2030EVAL is configured as a dual polarity gate driver with the gate return referenced to P0. In this mode of operation, the HIP2030 generates a -12V or a +18V output voltage when the SSDCB voltage equals 30V. The GO output connections, for -12V or +18V operation, are located at connector J1 between inputs G and GR.

Methods of DC Bias

The HIP2030EVAL can be biased in one of three configurations: a single supply (with a dropping resistor), a dual supply, and a single supply with a high side charge pump.

Single supply operation, using a dropping resistor (R9) and V_{CLMP}, uses one high side voltage supply and provides enough charging current to drive large capacitive loads at high frequencies. An example of this bias scheme is shown in the PCB Schematic.

Dual supply biasing (DSB) is configured by removing the droppigng resistor, adding a bias resistor and connecting two isolated power supplies. Follow steps 1 through 6 to use the DSB.

1. Apply voltage source #1 (V1) between P0 and P-.
2. Apply voltage source #2 (V2) between P+ and P0.
3. Install 10Ω resistor R8.
4. Remove dropping resistor R9.
5. Adjust V1 to provide the desired negative gate drive voltage.
6. Adjust V2 to provide the desired positive gate drive voltage.

Adjusting Gate Drive Output Polarity

The driver board is configured for driving a generic power switch and references the gate drive to P0; which is approximately half the voltage that is applied between P+ and P-. The HIP2030EVAL has provided the ability to adjust the gate drive output polarity to accommodate input voltage requirements for various power switches. Configurations for symmetric and asymmetric output polarities are given below.

Symmetric Output Polarity

Open JP2 (configures the middle of the R1/R2 voltage divider for the gate return reference). Add R1 and R2 (select equal values of R1 and R2; typical values are between 1K and 10K).

Asymmetric Output Polarity

Open JP2 (configures the middle of the R1/R2 voltage divider for the gate return reference), select R2 with this equation:

$$R2 = \left[\frac{(VPO)(R1)}{((VP+) - VPO)}\right] \quad \text{(EQ. 1)}$$

Add R1 and R2 (typical values are between 1K and 10K).

Jumper Settings

Jumpers JP1, JP2, and JP3 are initially configured as shorts. Jumpers names and their functions are listed:

JP1 - Connect the internal 12V clamp, located inside the HIP2030, across P0 to P-.

JP2 - Use P0 for the gate return reference.

JP3 - Applies DC bias voltage to charge pump circuitry.

Minimum High and Low Time Functions

The HIP2030 provides two special functions that are unique to driving MCT power devices. These functions are called Minimum High Time (MHT) and Minimum Low Time (MLT). MLT and MHT are used to ensure that input control signals, with gate signals <1µs in duration, turn on and off the MCT devices reliability. The time settings for MHT and MLT are set as a function of MCT “ON” and “OFF” delay times. Both of these time settings can be independently programmed by installing a capacitor between its function pin (MHT and MLT) and pin P0. The value of either capacitor can be approximated by the equation:

$$C = \frac{(100\mu A)(DELAYTIME)}{5V} \quad \text{(EQ. 2)}$$

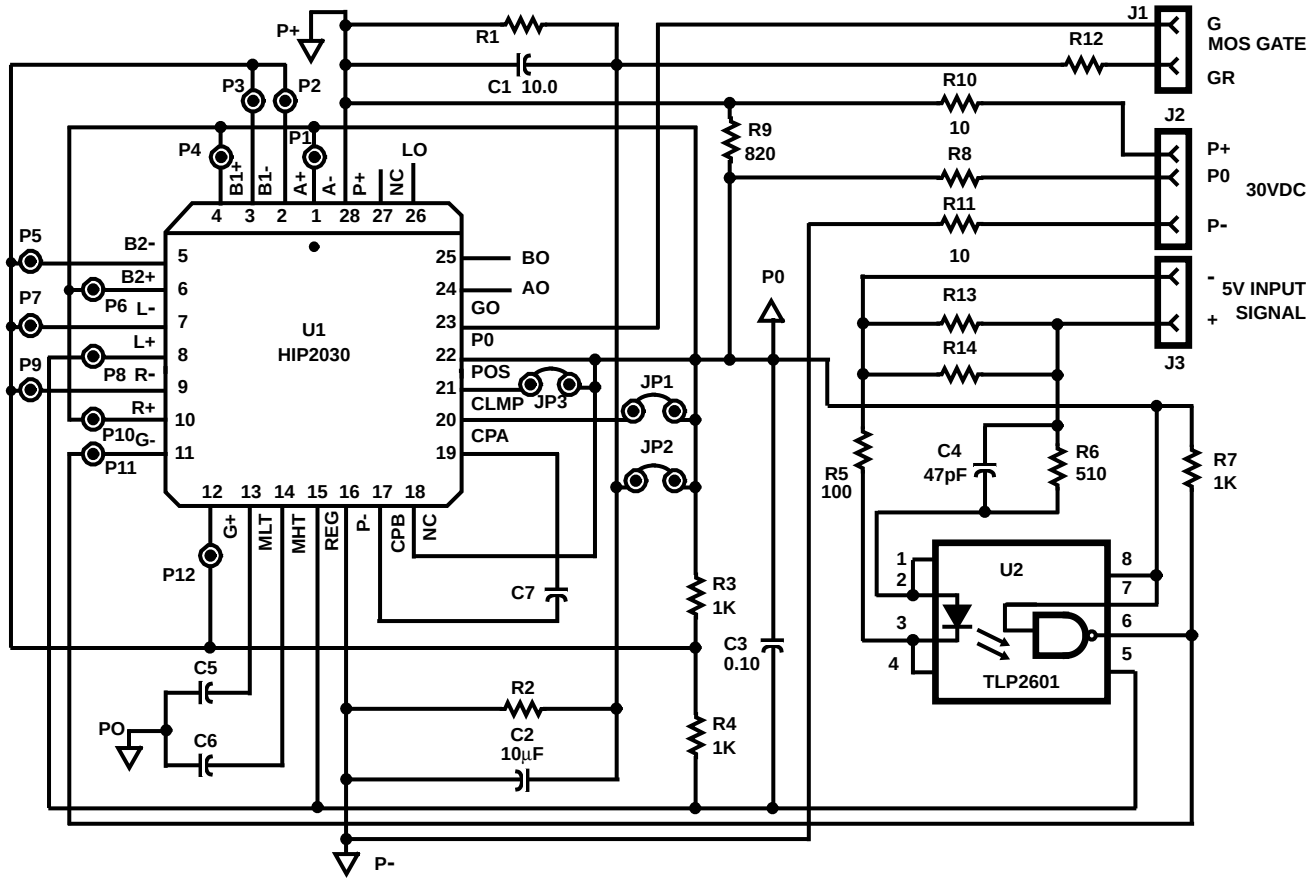
Monitor Channel Outputs

Channel outputs A, B, and L are accessed on the solder side of the HIP2030EVAL and are located above jumpers JP3 and JP4. The locations for AO, BO, LO, J1, and J3 are illustrated in the HIP2030EVAL PCB assembly layer drawing.

On Board Prototyping Suggestions

The HIP2030EVAL PCB furnishes the experimenter with a 1” x 0.6” prototyping area that provides a 62mil solder pad array at 100mil spacing. Pads P1 through P12, located at the inputs of the voltage comparators, are used as access points to the channel inputs and may be jumpered over to the prototype areas. These pads are currently connected to either the middle of the regulated voltage divider (between R3 and R4), P0 (U1-22), REG (U1-15) or control signal (U2-6). These traces are easily cut with the use of an “exacto-knife” and can be disconnected to prototype various circuits.

PCB Schematic



NOTES:

1. Capacitors C5 and C6 are special function components which control MLT and MHT.
2. Asymmetrical gate drive may be obtained by opening J2 and adjusting R1 and R2 for the desired voltage ratio.
3. Insert C7 for charge pump operation.
4. Open J3 to disable the charge pump oscillator.
5. Open J1 to disable the internal 12V regulator.
6. R5 is added for noise rejection at Cdv/dts.
7. The internal 5V regulator (REG) must be operational for MHT and MLT functions to work properly.
8. P1 - P12 are access pads for all comparitor inputs.

TABLE 1. EVALUATION BOARD PARTS LIST

REFERENCE DESIGNATOR	VALUE	TYPE
R1, R2, R8, R12, R13, R14	Unpopulated	1/3W Metal Film (1%)
R3, R4, R7	1K	1/3W Metal Film (1%)
R5	100Ω	1/3W Metal Film (1%)
R6	510Ω	1/3W Metal Film (1%)
R9	820Ω	1/3W Metal Film (1%)
R10, R11	10Ω	1/3W Metal Film (1%)
R12 (Damping Resistor)	Unpopulated	1/3W Metal Film (1%)
R13, R14	Unpopulated	1/3W Metal Film (1%)
C1, C2	10µF	Tantalum at 35V
C3	0.1µF	Ceramic at 35V
C4	47pF	Mica at 50V
C5, C6 (MLT/MHT)	Unpopulated (20pF - 100µF)	Varies Based on Capacitance Size
C7 (Charge Pump)	Unpopulated (0.01µF Typ)	Varies Based on Capacitance Size
U1	HIP2030	28 Pin PLCC
U2	TLP2601	8 Pin Plastic Dip

TABLE 2. LOGIC

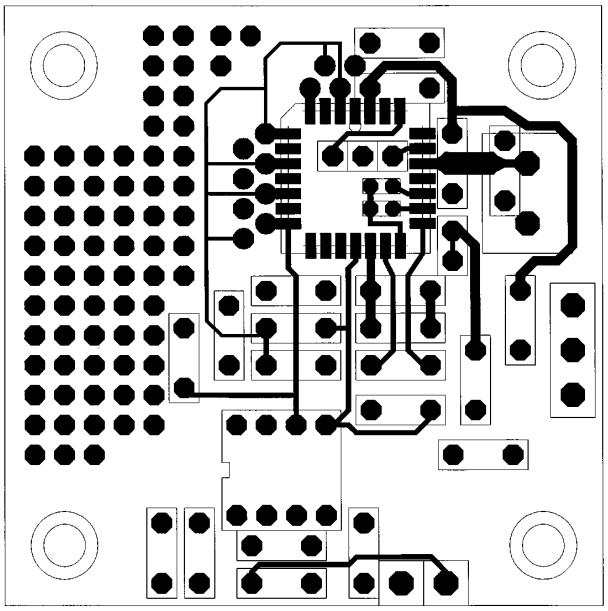
INPUTS			OUTPUTS	
G	L	R	LO	GO
0	0	0	LS	H
0	0	1	H	H
0	1	0	L	H
0	1	1	L	H
1	0	0	LS	U
1	0	1	H	L
1	1	0	L	H
1	1	1	L	H

1 = Input True
0 = Input False

U = Undefined
LS = Last State

Board Layouts

TOP LAYER



BOTTOM LAYER