HARRIS SEMICONDUCTOR

HGTB12N60D1C

April 1995

12A, 600V Current Sensing N-Channel IGBT

Features

- **12A, 600V**
- **$r_{DS(ON)}$ 0.27Ω**
- **Low $V_{CE(SAT)}$ at 25A . . . . 2.5V (Typ)**
- **Ultra-Fast Turn-On . . . . 100ns (Typ)**
- **Polysilicon MOS Gate - Voltage Controlled Turn On/Off**
- **High Current Handling at +100°C. 10A**
- **Current Sensing Pilot**

Description

The HGTB12N60D1C Insulated-Gate Bipolar Transistor is a MOS-gate turn on/off power switching device combining the best advantages of power MOSFETs and bipolar transistors, and current sensing pilots. The result is a device that has the high input impedance of MOSFETs and the low on-state conduction losses similar to bipolar transistors. The device design and gate characteristics of the IGBT are also similar to power MOSFETs. An important difference is the equivalent $r_{DS(ON)}$ drain resistance which is modulated to a low value (ten times lower) when the gate is turned on. The much lower on-state voltage drop also varies only moderately between +25°C and +150°C, offering extended power handling capability.

The IGBT is ideal for many high-voltage switching applications operating at low frequencies and where low conduction losses are essential, such as AC and DC motor controls, power supplies and drivers for solenoids, relays and contactors.

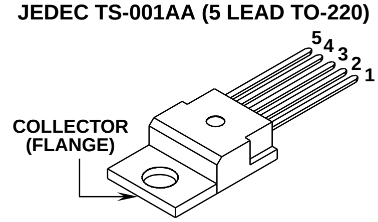
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
HGTB12N60D1C	TS-001AA	12N60D1C

NOTE: When ordering, use the entire part number.

Package

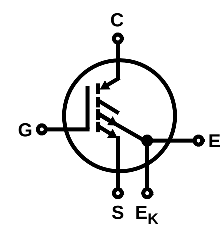
JEDEC TS-001AA (5 LEAD TO-220)



1 - GATE
2 - SENSE
3 - COLLECTOR
4 - (KELVIN) EMITTER
5 - EMITTER

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		HGTB12N60D1C	UNITS
Collector-Emitter Voltage (V_{GE} = 0V)	V_{CES}	600	V
Collector-Gate Voltage (R_{GE} = 1MΩ)	V_{CGR}	600	V
Collector Current Continuous at T_C = +100°C	I_C	12	A
at T_C = +25°C	I_C	18	A
Collector Current Pulsed (Note 1)	I_{CM}	40	A
Gate-Emitter Voltage	V_{GE}	±25	V
Power Dissipation Total at T_C = +25°C	P_D	75	W
Power Dissipation Derating T_C > +25°C		0.6	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.67	°C/W
Maximum Lead Temperature for Soldering (1/8 inch from case for 5s)	T_L	260	°C

NOTE: 1. Repetitive Rating: Pulse width limited by maximum junction temperature. Gate control turn-off not allowed above 50A.

HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS		LIMITS MIN	TYP	MAX	UNITS
OFF CHARACTERISTICS							
Collector-Emitter Breakdown Voltage	BV_{CES}	$I_C = 25\mu A$, $V_{GE} = 0V$		600	-	-	V
Collector Cut-Off Current	I_{CES}	$T_C = +25^oC$, $V_{GE} = 0V$, V_{CE} = Maximum Rating		-	-	250	µA
		$T_C = +150^oC$, $V_{GE} = 0V$, V_{CE} = Maximum Rating x 0.8 (Note 1)		-	-	4	mA
Gate-Emitter Leakage Current	I_{GES}	$V_{GE} = \pm 20V$		-	-	±500	nA
ON CHARACTERISTICS (Note 2)							
Gate Threshold Voltage	$V_{GE(TH)}$	$V_{CE} = V_{GE}$, $I_C = 250\mu A$	$T_C = +25^oC$	2	4	5	V
			$T_C = +150^oC$	-	2.5	-	V
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$V_{GE} = 15V$, $I_C = 10A$, $T_C = +25^oC$		-	2.5	2.7	V
		$V_{GE} = 15V$, $I_C = 10A$, $T_C = +150^oC$		-	2.8	-	V
		$V_{GE} = 10V$, $I_C = 10A$, $T_C = +25^oC$		-	2.9	-	V
DYNAMIC CHARACTERISTICS							
Input Capacitance	C_{IES}	$V_{GE} = 0V$, $V_{CE} = 25V$, f = 1MHz		-	1050	-	pF
Output Capacitance	C_{OES}			-	340	-	pF
Reverse Transfer Capacitance	C_{RES}			-	10	-	pF
SWITCHING CHARACTERISTICS (See Figures 8 and 9) (Note 2)							
Turn-On Delay Time	$t_{D(ON)}$	Resistive Load, $T_J = +125^oC$, $I_C = 10A$, $V_{CE} = 500V$, $V_{GE} = 15V$, $R_{G(ON)} = 50\Omega$, $R_{G(OFF)} = 100\Omega$		-	100	-	ns
Rise Time	t_R			-	100	-	ns
Turn-Off Delay Time	$t_{D(OFF)}$			-	0.4	-	µs
Fall Time	t_F			-	2.5	-	µs
Turn-Off Delay Time	$t_{D(OFF)I}$	Inductive Load, $T_J = +125^oC$, $L = 45\mu H$, $I_C = 10A$, $V_{CE(CLAMP)} = 500V$, $V_{GE} = 15V$, $R_{G(ON)} = 50\Omega$, $R_{G(OFF)} = 100\Omega$		-	0.8	1.2	µs
Fall Time	t_{FI}			-	0.8	1.0	µs
Equivalent Fall Time	$t_{F(EQ)}$			-	0.6	0.8	µs
Turn-Off Switching Losses	W_{OFF}			-	1.6	2.0	mJ
PILOT CHARACTERISTICS (Notes 2, 3 and 4)							
Pilot-Emitter Kelvin Voltage	V_{PEK}	$V_{GE} = 15V_{DC}$, $R_P = 2k\Omega$					
$I_C = 5A$				-	1.25	-	V
$I_C = 10A$				1.4	1.67	1.8	V
$I_C = 20A$				-	2.06	-	V

NOTES:

1. Applies for 3.3^oC per watt maximum thermal resistance, case-to-ambient.
2. Pulse test: Pulse widths ≤ 300µs, duty cycle ≤ 2%.
3. Refer to Figure 10.
4. When not in use connect S to emitter.

Typical Performance Curves

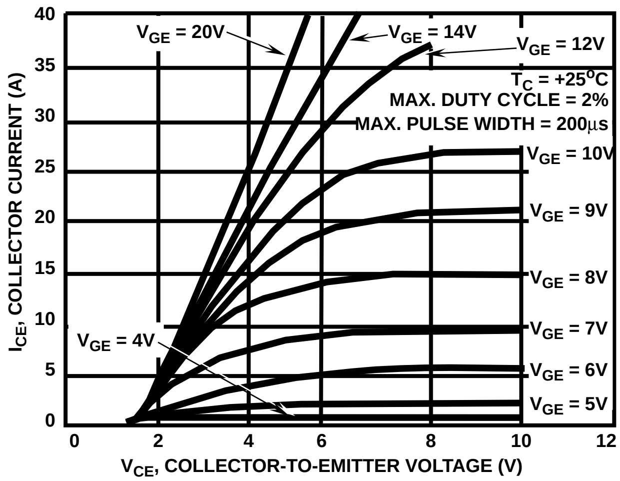


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

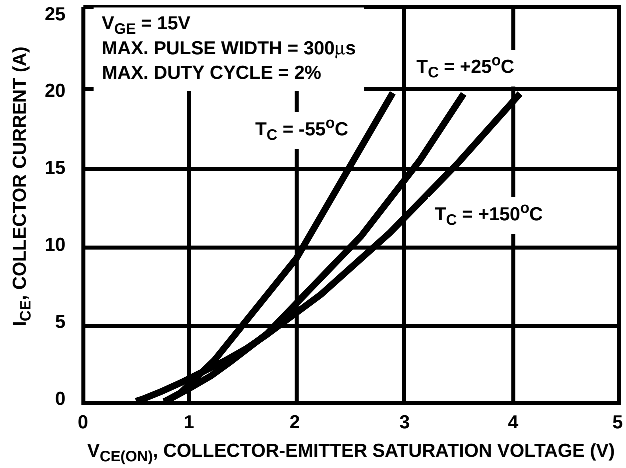


FIGURE 2. TYPICAL COLLECTOR-EMITTER SATURATION VOLTAGE

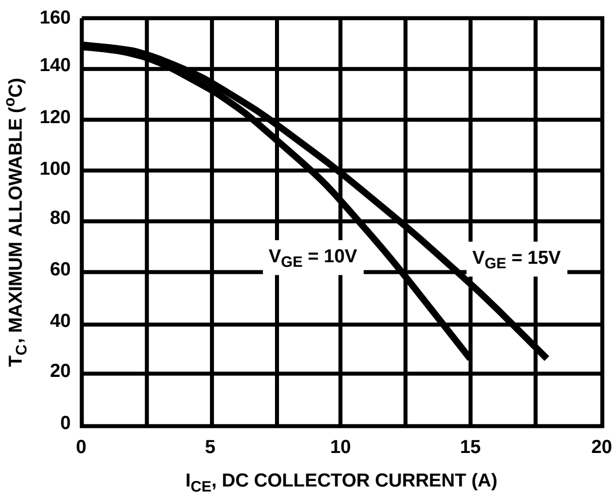
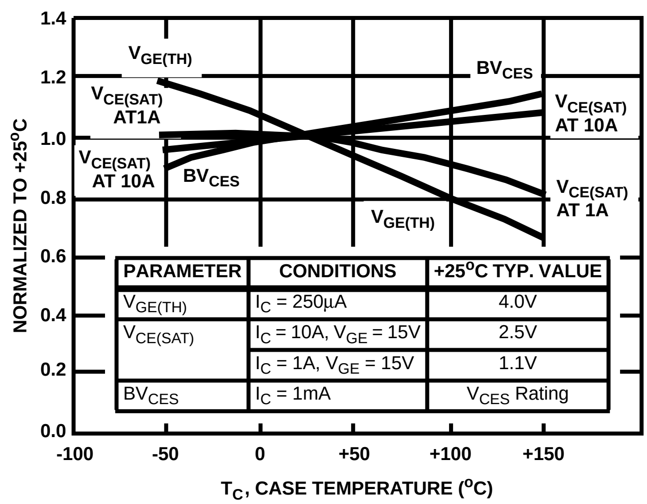


FIGURE 3. MAXIMUM ALLOWABLE CASE TEMPERATURE vs DC COLLECTOR CURRENT



PARAMETER	CONDITIONS	+25°C TYP. VALUE
$V_{GE(TH)}$	I_C = 250µA	4.0V
$V_{CE(SAT)}$	I_C = 10A, V_{GE} = 15V	2.5V
	I_C = 1A, V_{GE} = 15V	1.1V
BV_{CES}	I_C = 1mA	V_{CES} Rating

FIGURE 4. TYPICAL TEMPERATURE DEPENDENCE OF PARAMETERS

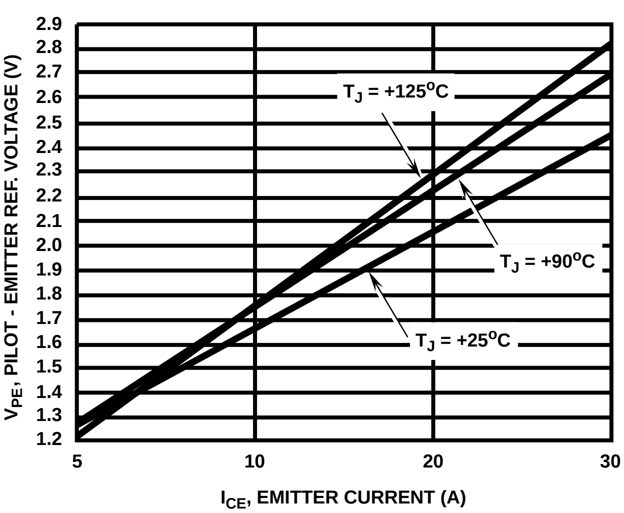


FIGURE 5. TYPICAL EMITTER PILOT CHARACTERISTICS 2kΩ PILOT RESISTOR

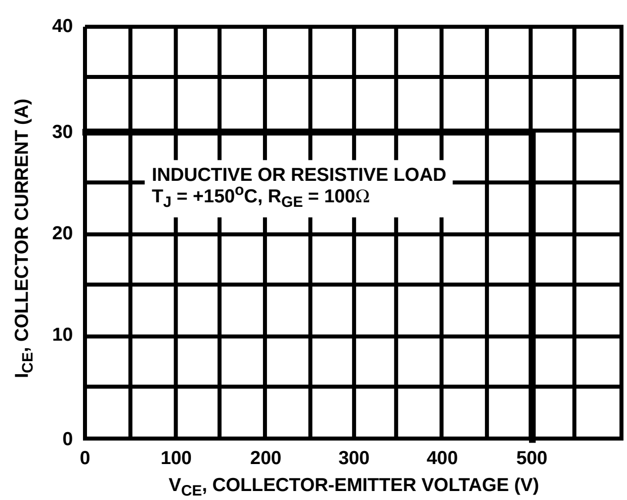


FIGURE 6. TURN-OFF SAFE OPERATING AREA

Typical Performance Curves (Continued)

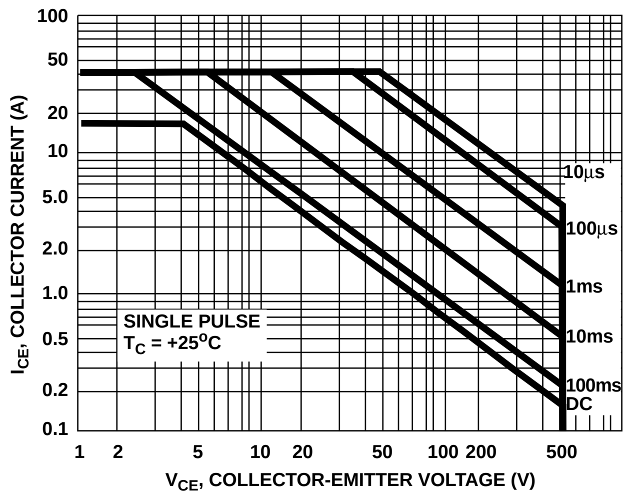


FIGURE 7. TURN-ON SAFE OPERATING AREA

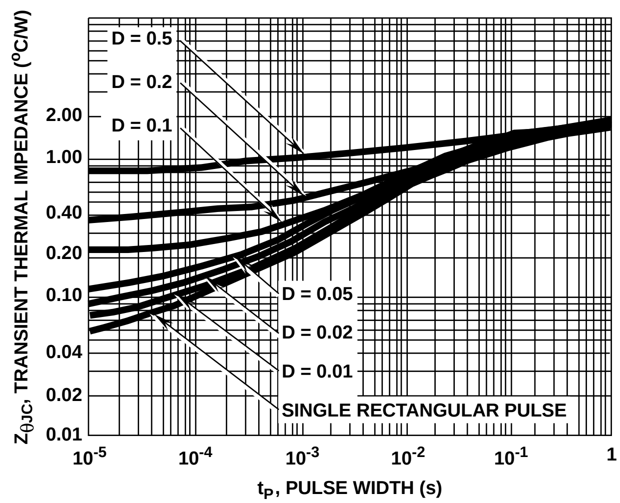
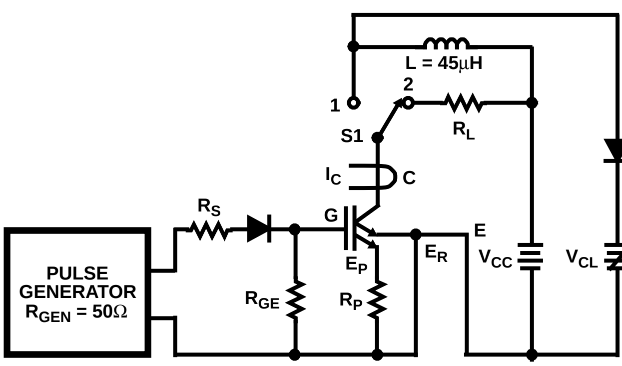


FIGURE 8. MAXIMUM TRANSIENT THERMAL IMPEDANCE

Test Circuits and Waveforms

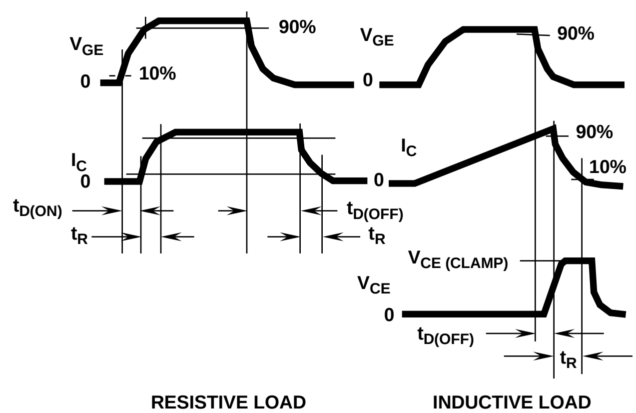


S1 SWITCH POSITION 1 CLAMPED INDUCTIVE LOAD
2 RESISTIVE LOAD

$R_{G(ON)} = \frac{(R_{GEN} + R_S)(R_{GE})}{R_{GEN} + R_S + R_{GE}}$ PULSE WIDTH 60µs V_{CC}

L-$I_{C\ MAXIMUM}$, PULSE WIDTH

FIGURE 9. BASIC SWITCHING TEST CIRCUIT



(WAVEFORMS NOT TO SCALE)

FIGURE 10. SWITCHING WAVEFORMS

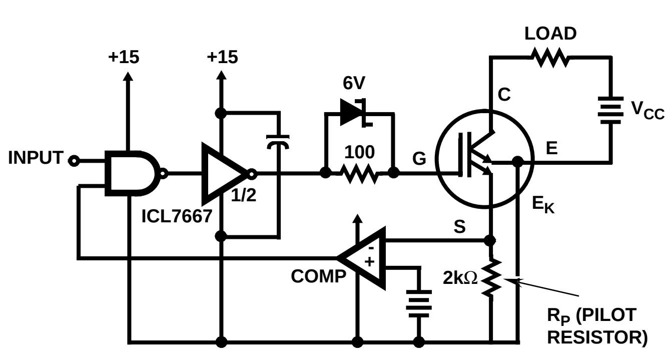


FIGURE 11. TYPICAL CIRCUIT UTILIZING THE EMITTER PILOT FOR OVERCURRENT PROTECTION