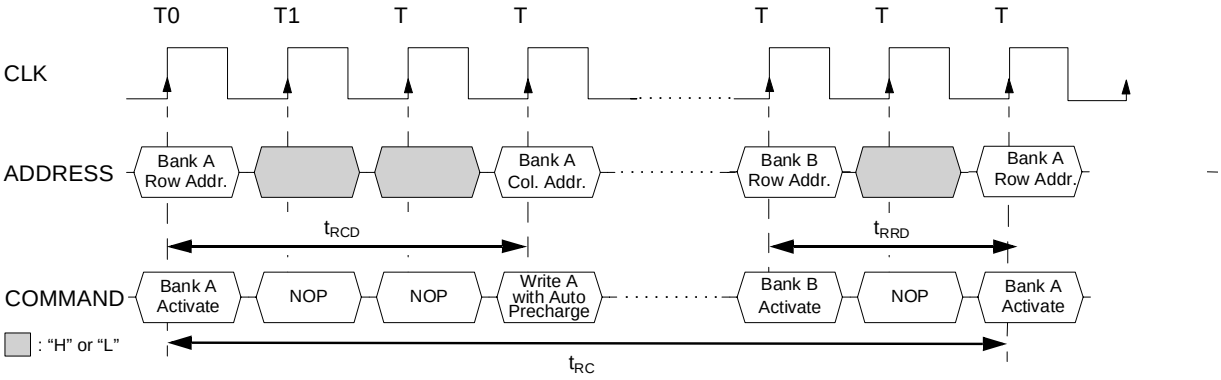
Timing Diagrams

Timing Diagrams (cont'd)

18. Random Row Read (Interleaving Banks) with Precharge
    - 18.1 $\overline{CAS}$ Latency = 2
    - 18.2 $\overline{CAS}$ Latency = 3
19. Random Row Write (Interleaving Banks) with Precharge
    - 19.1 $\overline{CAS}$ Latency = 2
    - 19.2 $\overline{CAS}$ Latency = 3
20. Full Page Read Cycle
    - 20.1 $\overline{CAS}$ Latency = 2
    - 20.2 $\overline{CAS}$ Latency = 3
21. Full Page Write Cycle
    - 21.1 $\overline{CAS}$ Latency = 2
    - 21.2 $\overline{CAS}$ Latency = 3
22. Precharge Termination of a Burst
    - 22.1 $\overline{CAS}$ Latency = 2
    - 22.2 $\overline{CAS}$ Latency = 3

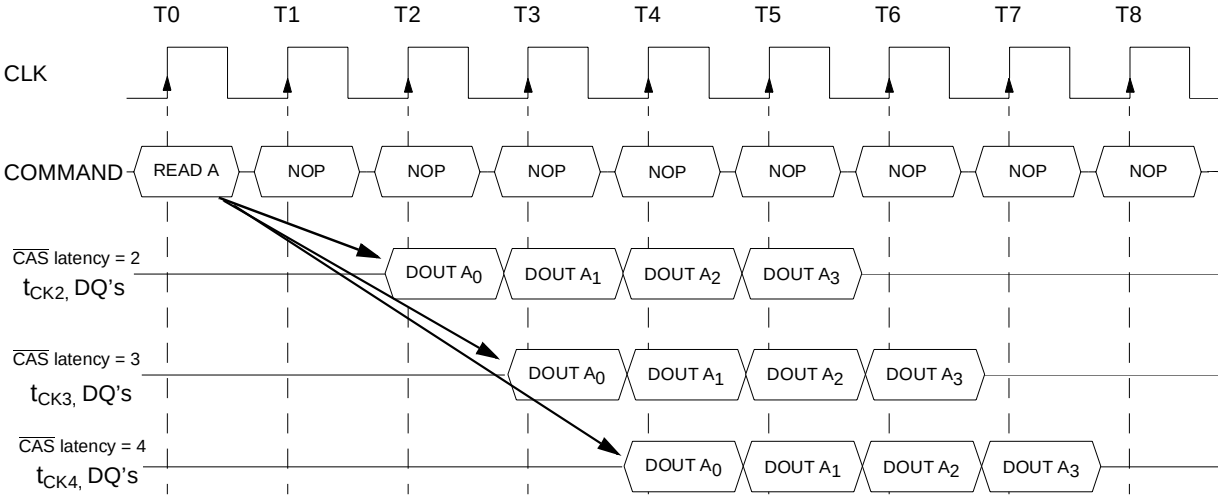
1. Bank Activate Command Cycle

($\overline{\text{CAS}}$ latency = 3)



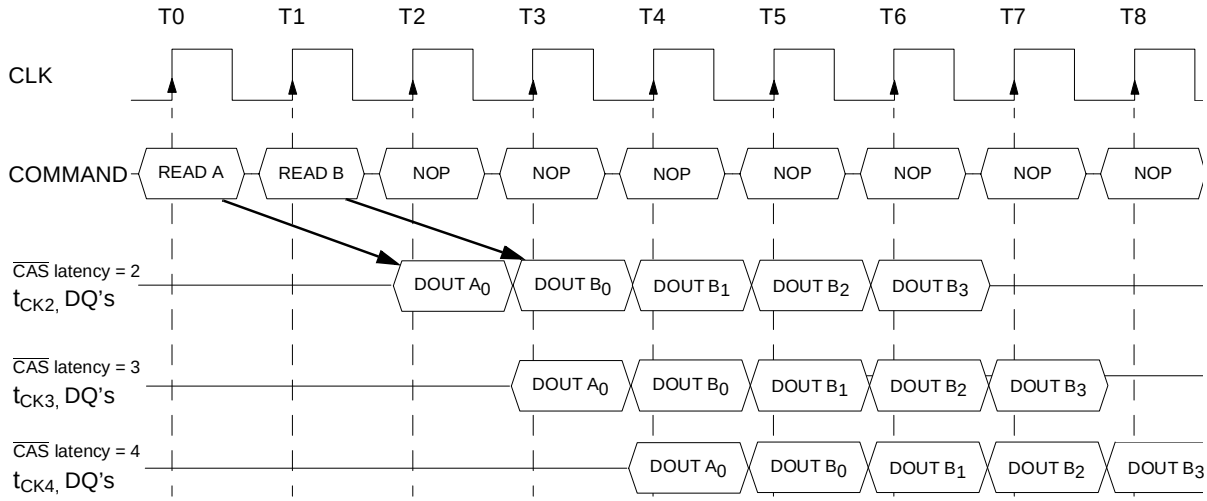
2. Burst Read Operation

(Burst Length = 4, $\overline{\text{CAS}}$ latency = 2, 3, 4)



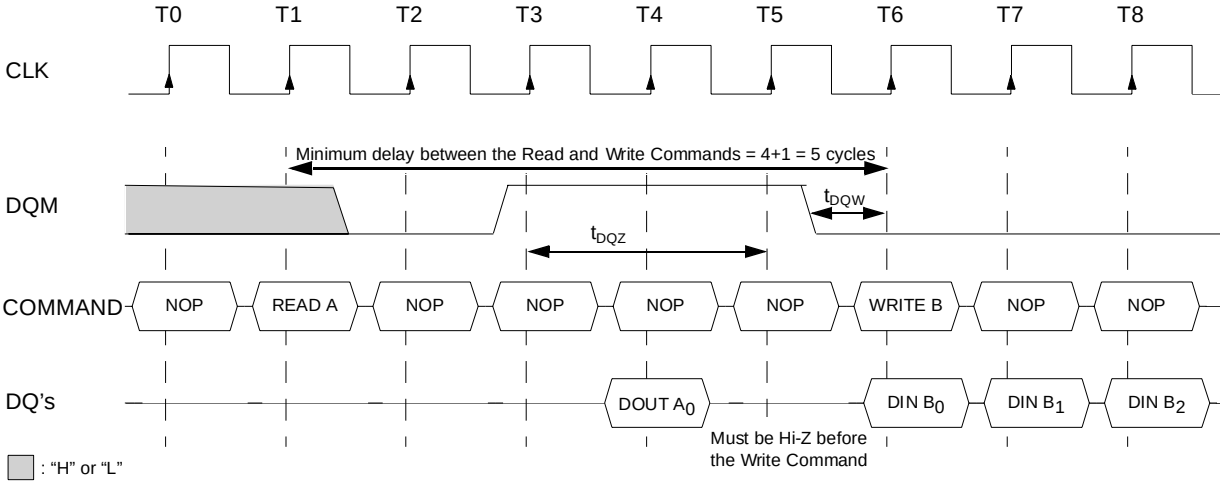
3. Read Interrupted by a Read

(Burst Length = 4, $\overline{CAS}$ latency = 2, 3, 4)



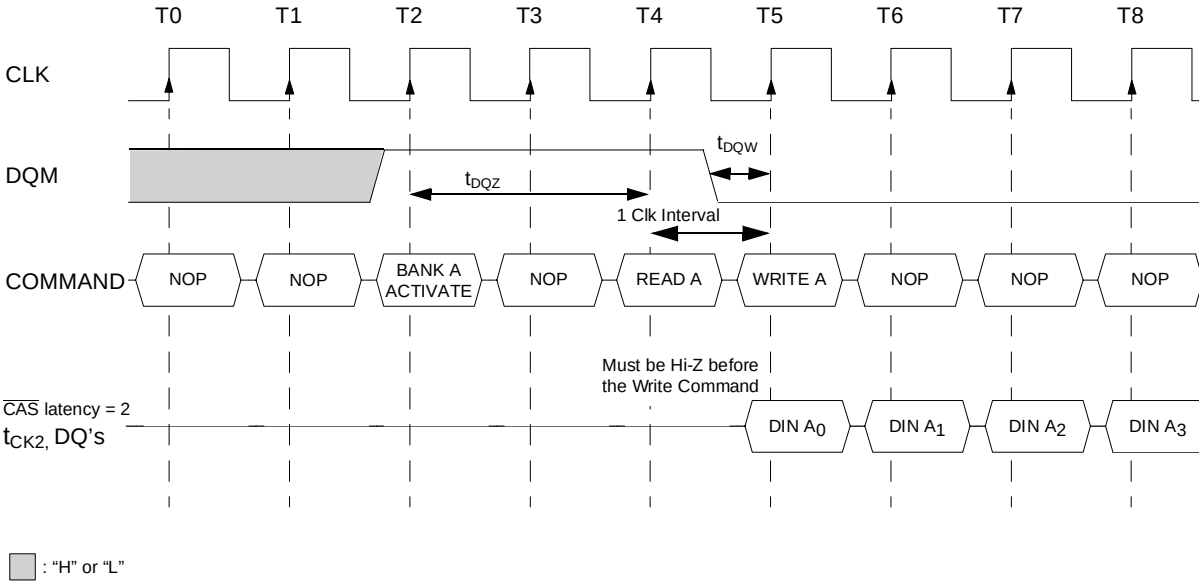
4.1 Read to Write Interval

(Burst Length = 4, $\overline{CAS}$ latency = 3)



4 2. Minimum Read to Write Interval

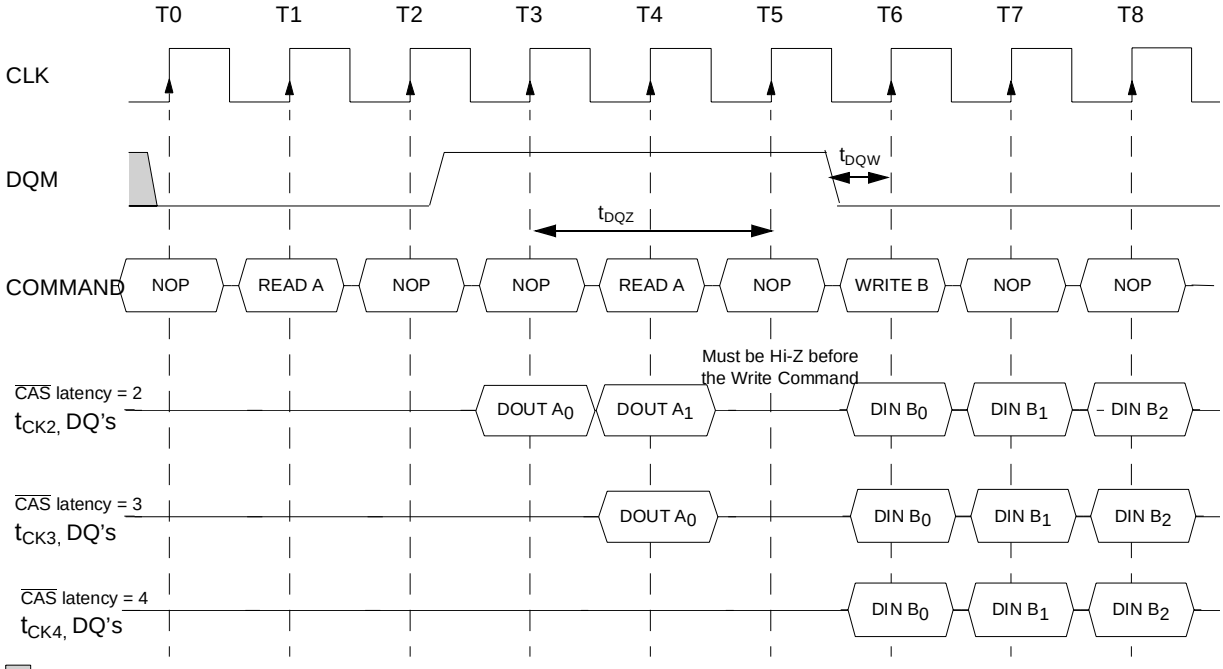
(Burst Length = 4, $\overline{CAS}$ latency = 2)



: "H" or "L"

4. 3. Non-Minimum Read to Write Interval

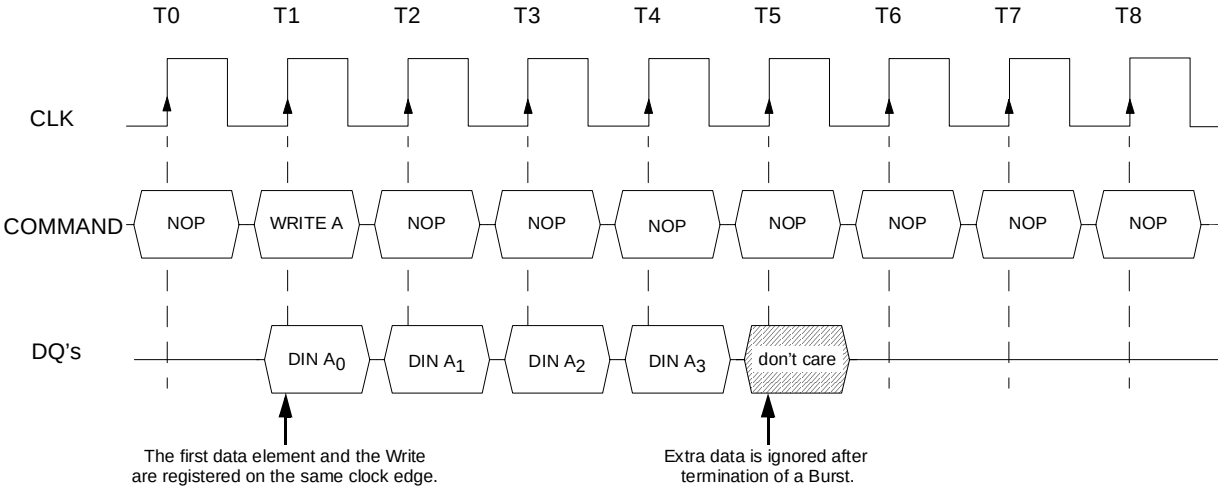
(Burst Length = 4, $\overline{CAS}$ latency = 2, 3, 4



: "H" or "L"

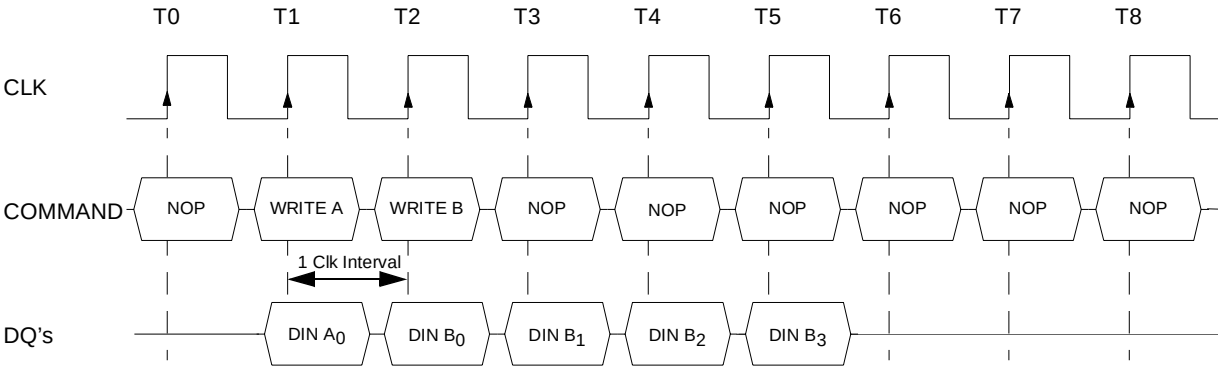
5. Burst Write Operation

(Burst Length = 4, $\overline{\text{CAS}}$ latency = 2, 3, 4)



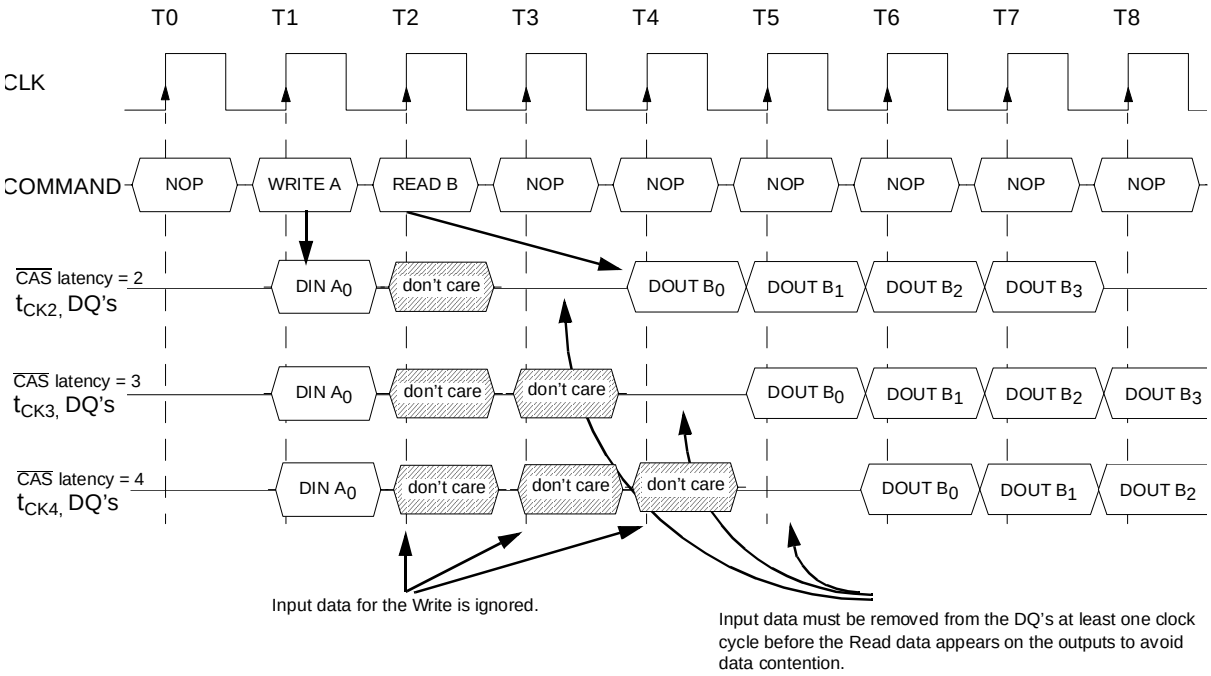
6.1 Write Interrupted by a Write

(Burst Length = 4, $\overline{\text{CAS}}$ latency = 2, 3, 4)



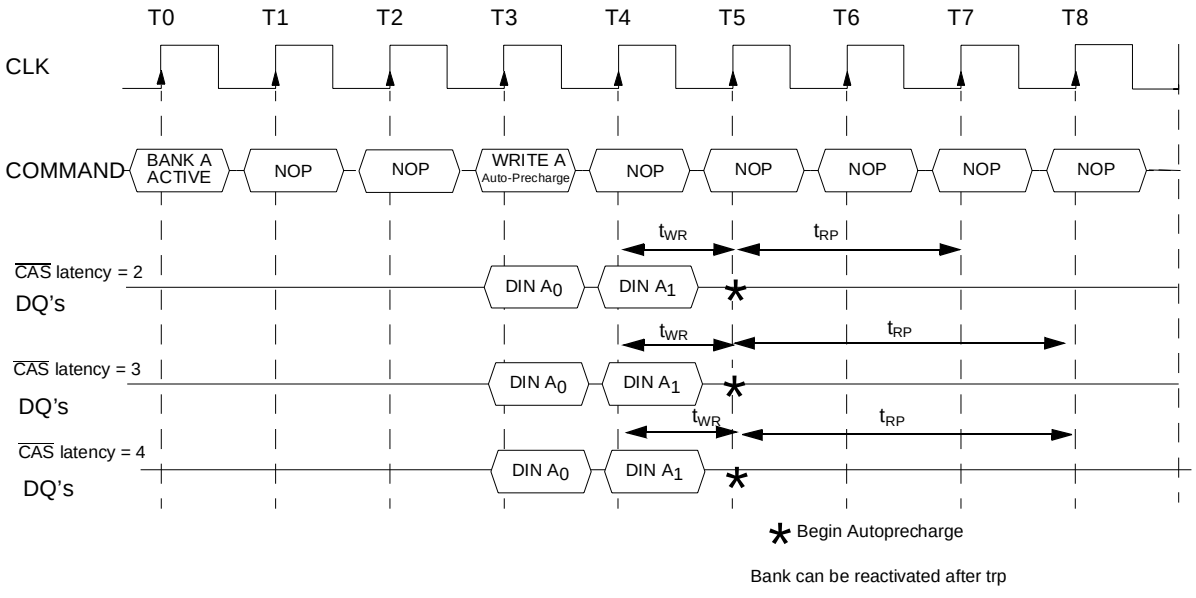
6.2 Write Interrupted by a Read

(Burst Length = 4, $\overline{CAS}$ latency = 2, 3, 4)



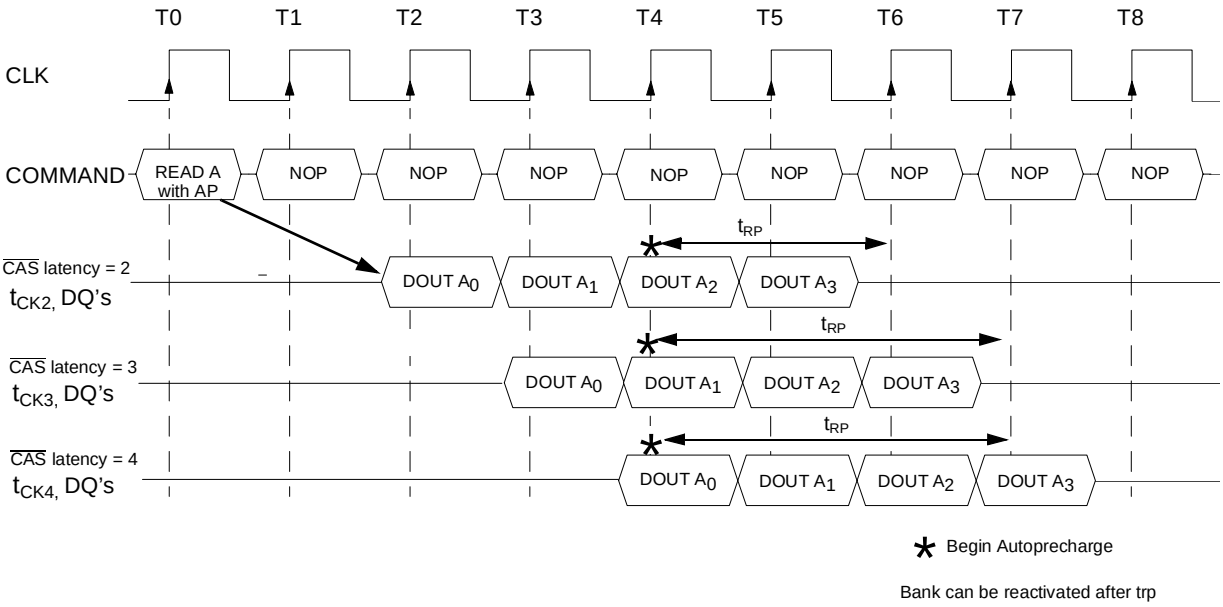
7.1 Burst Write with Auto-Precharge

Burst Length = 2, $\overline{CAS}$ latency = 2, 3, 4)



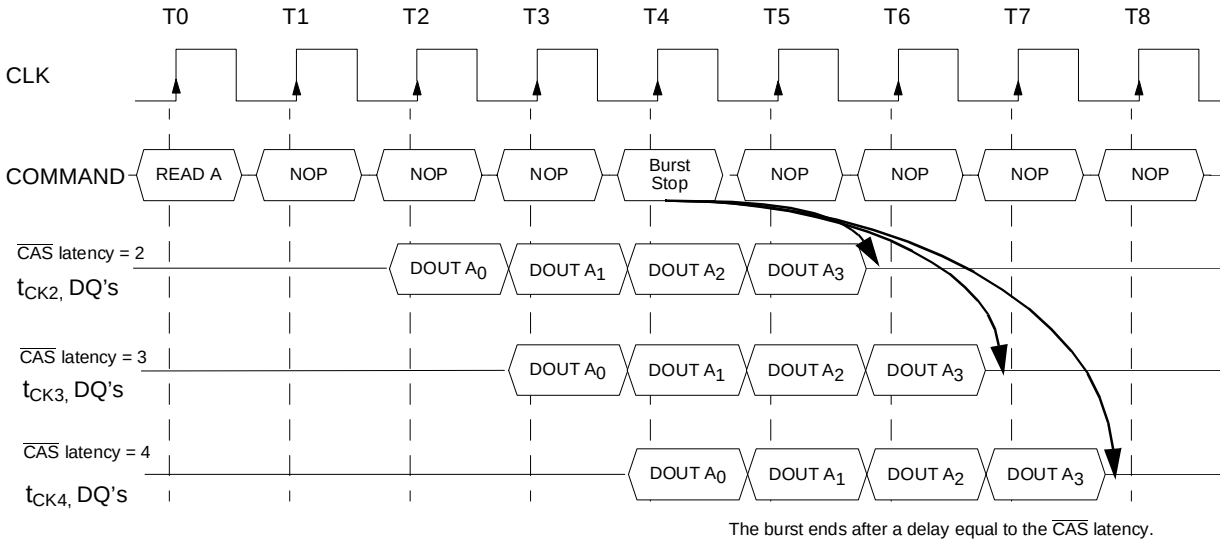
7.2 Burst Read with Auto-Precharge

(Burst Length = 4, $\overline{CAS}$ latency = 1, 2, 3)



8.1 Termination of a Full Page Burst Read Operation

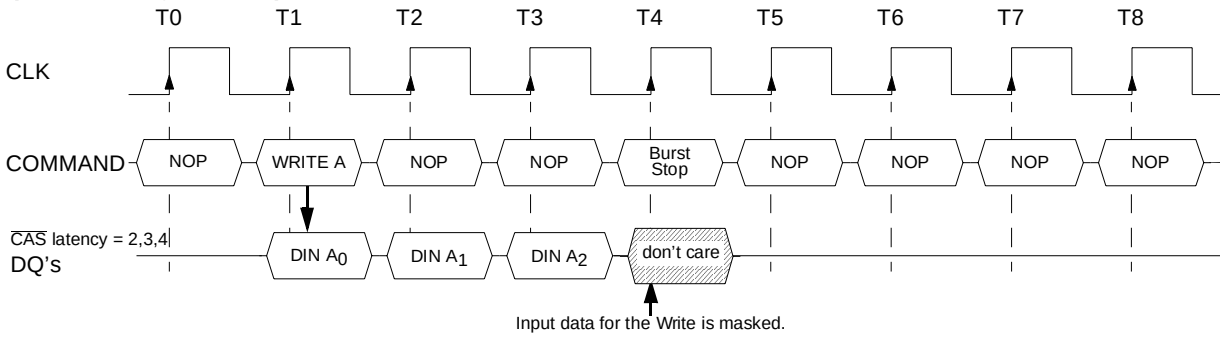
($\overline{\text{CAS}}$ latency = 2, 3, 4)



The burst ends after a delay equal to the $\overline{\text{CAS}}$ latency.

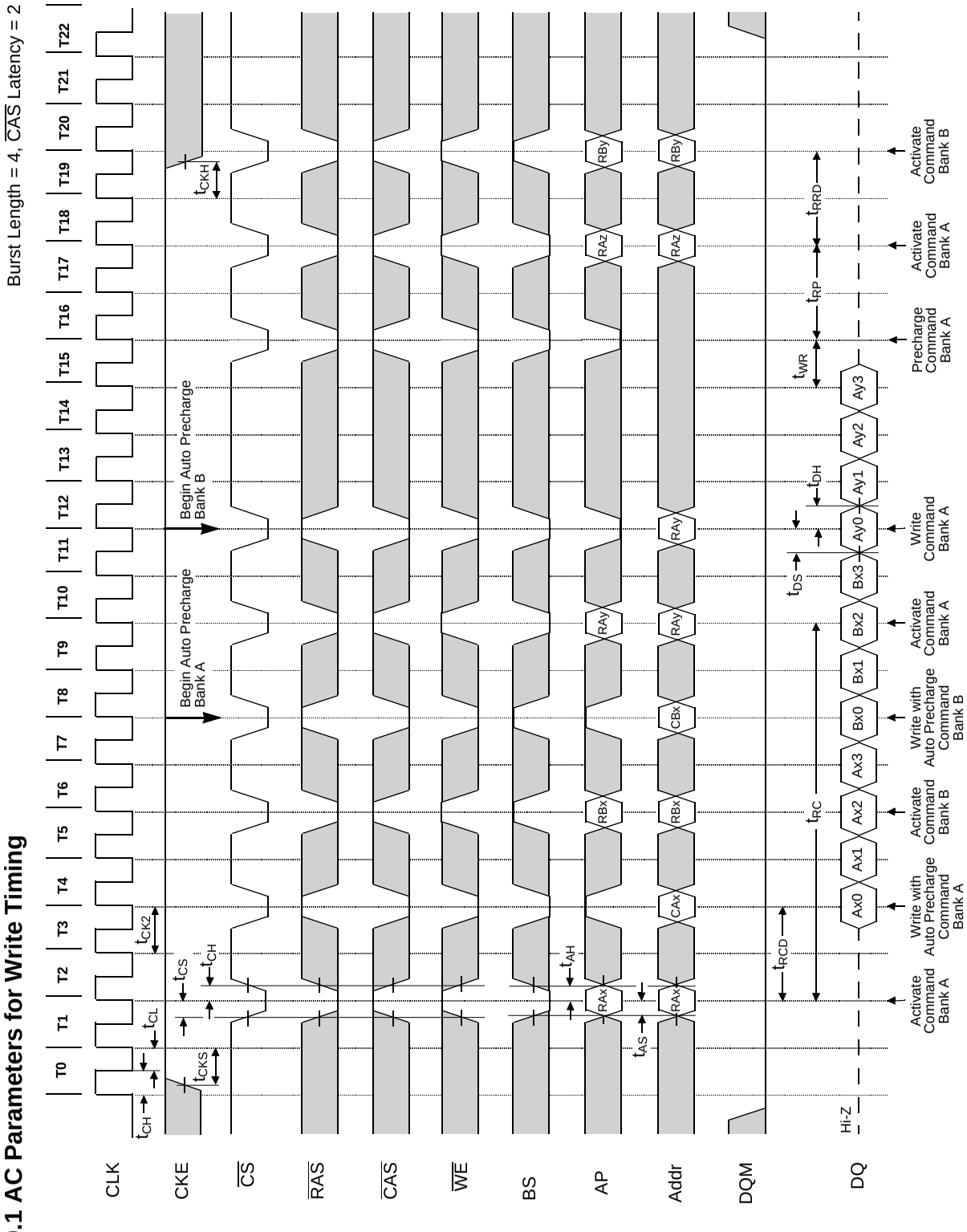
8.2 Termination of a Full Page Burst Write Operation

(CAS Latency = 2, 3, 4)

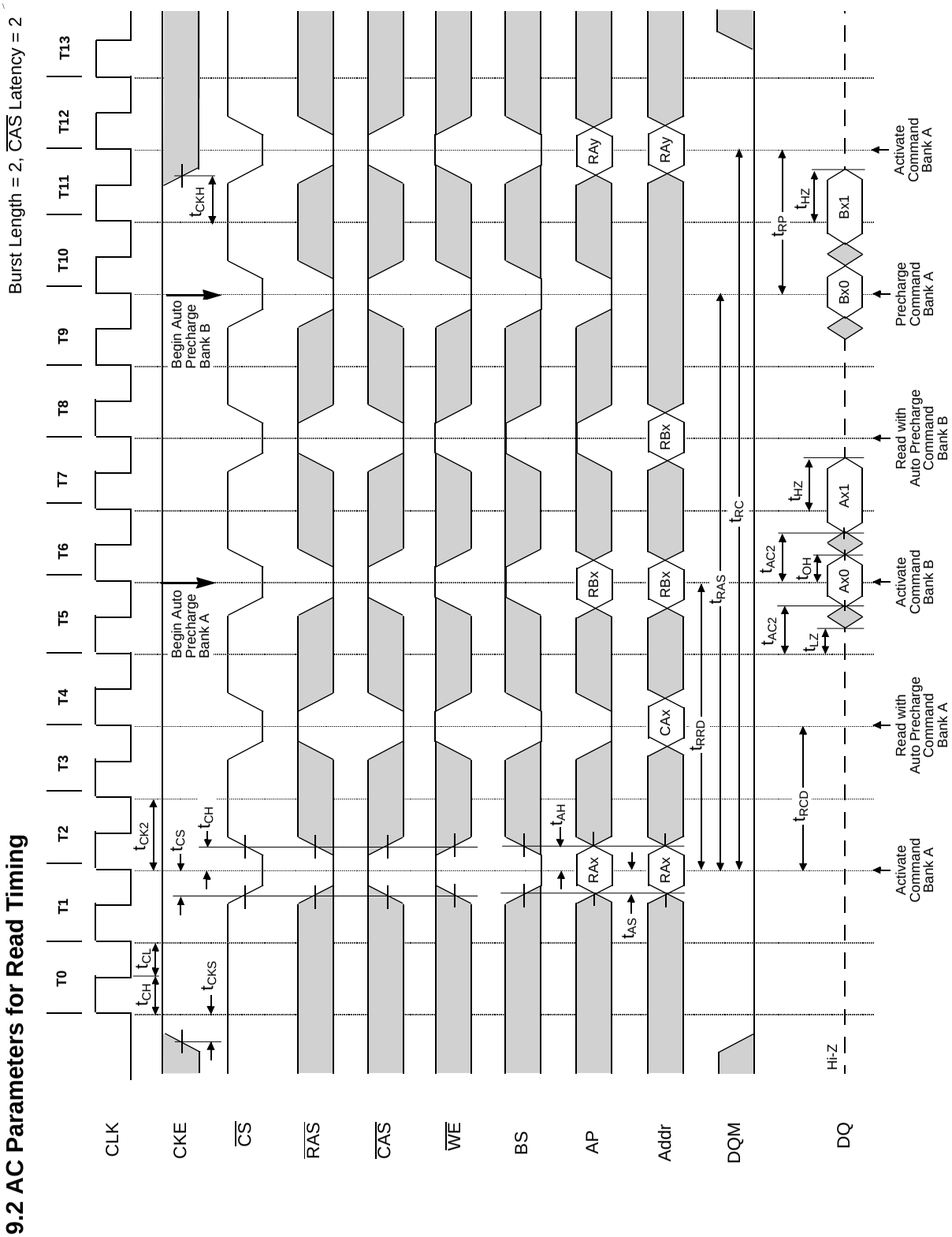


Input data for the Write is masked.

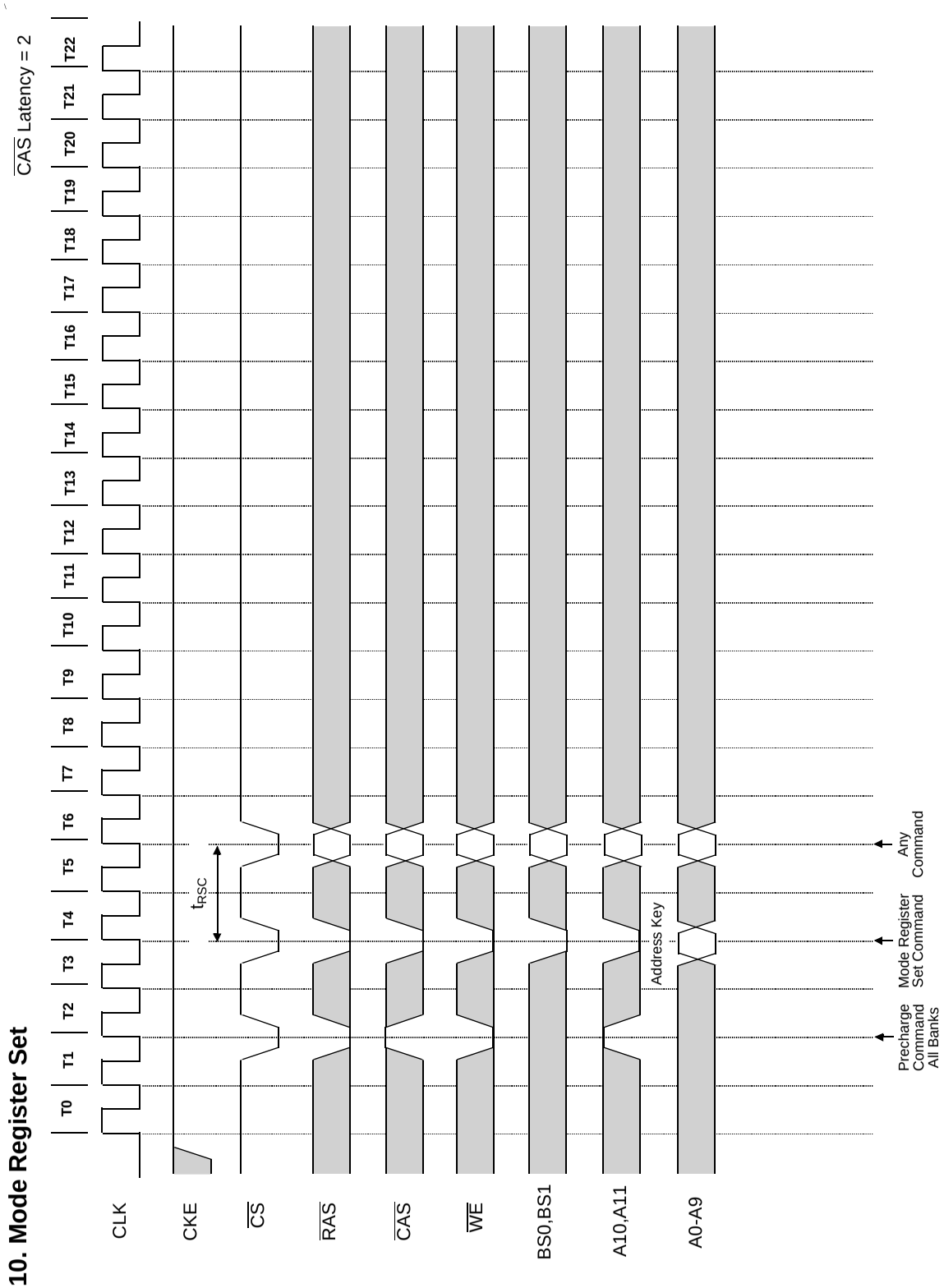
9.1 AC Parameters for Write Timing



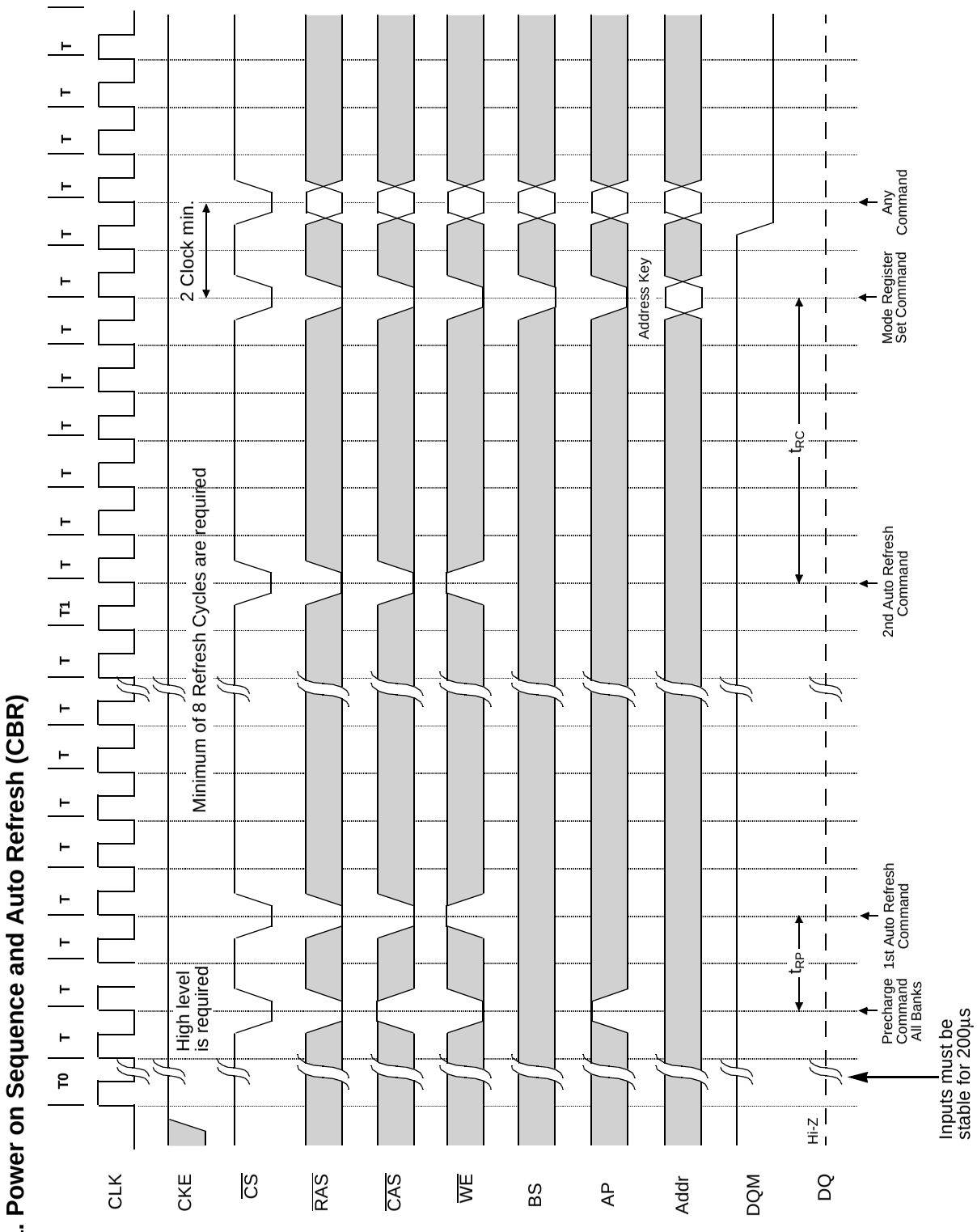
9.2 AC Parameters for Read Timing



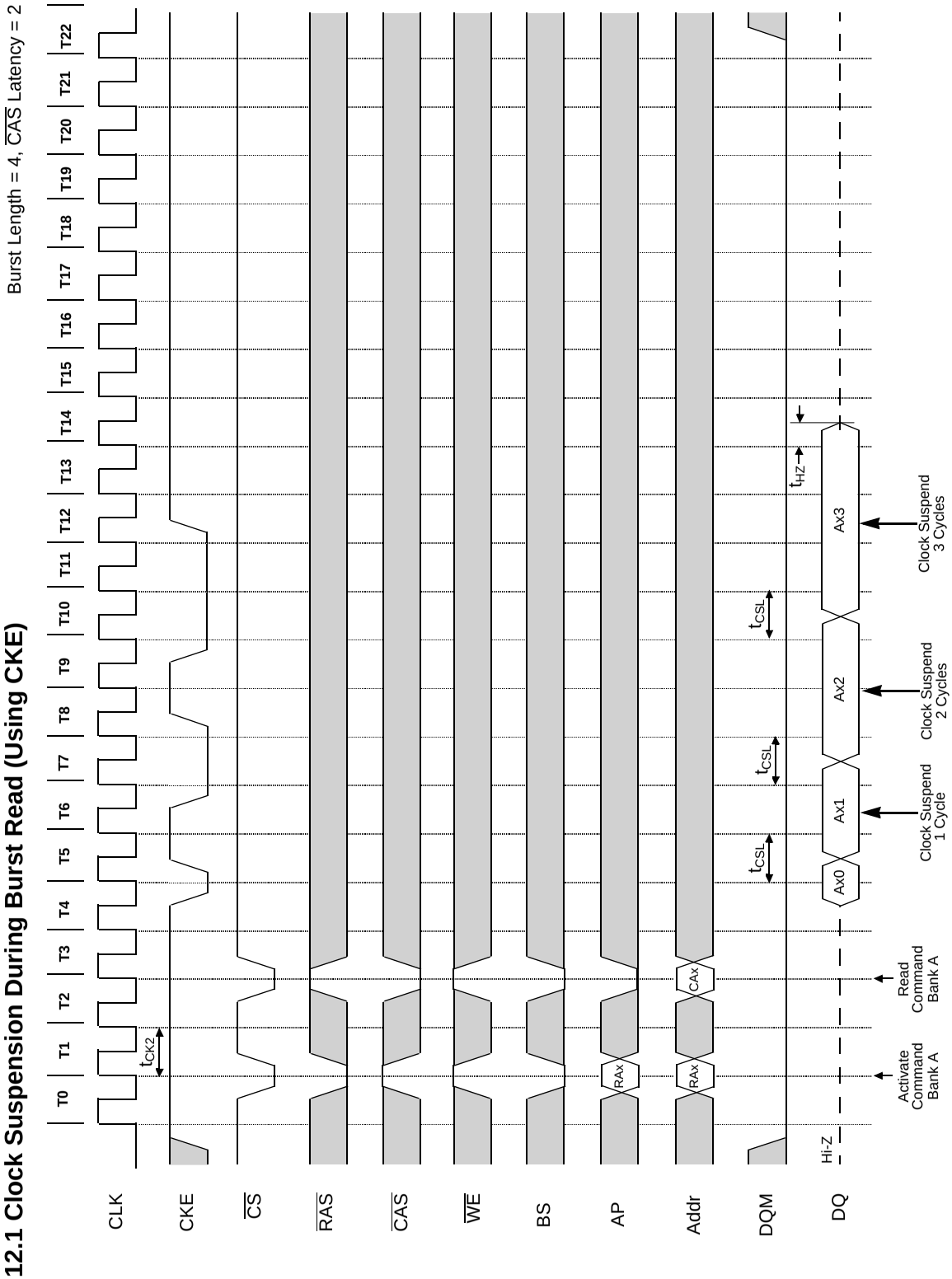
10. Mode Register Set



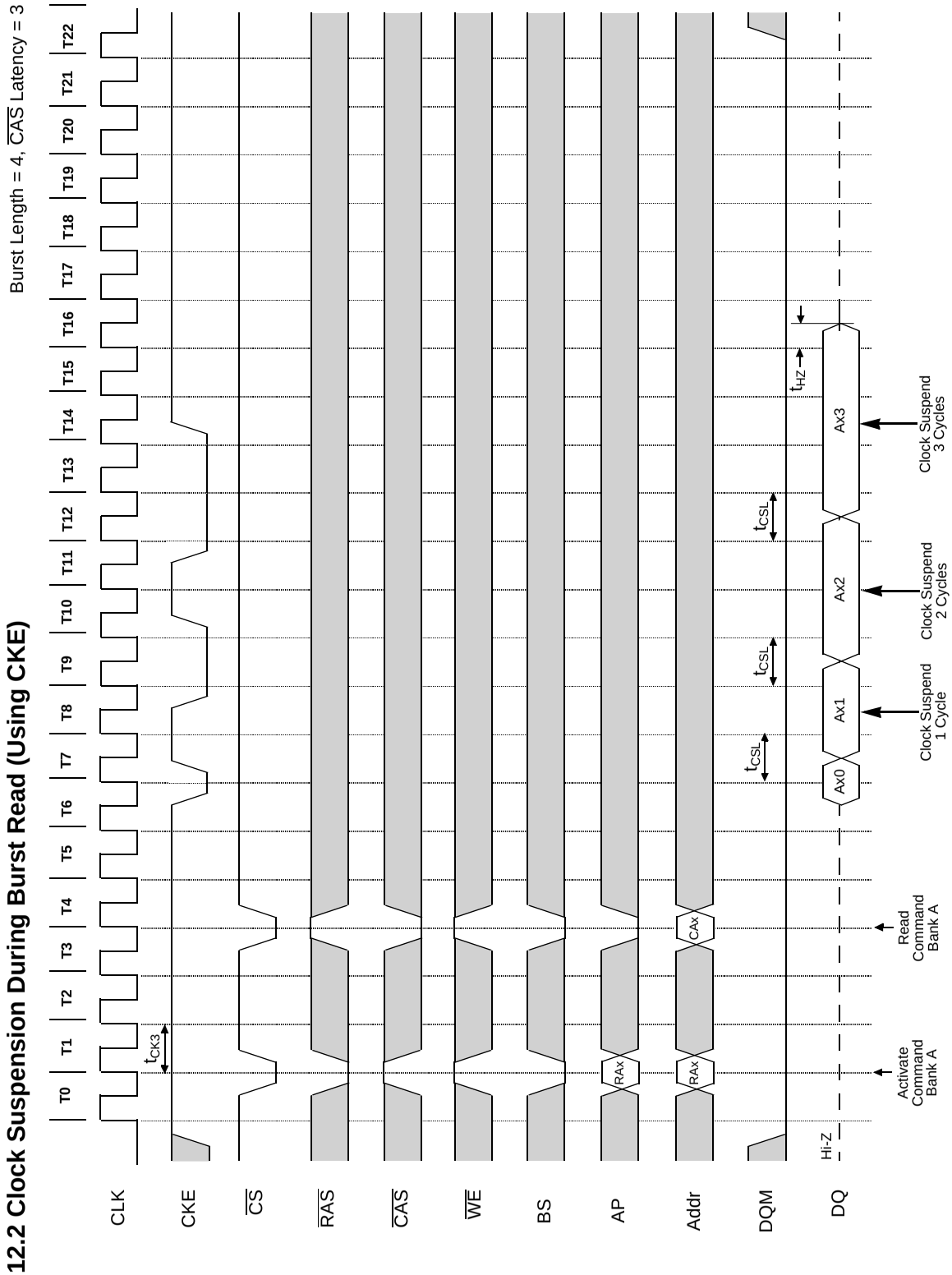
11. Power on Sequence and Auto Refresh (CBR)



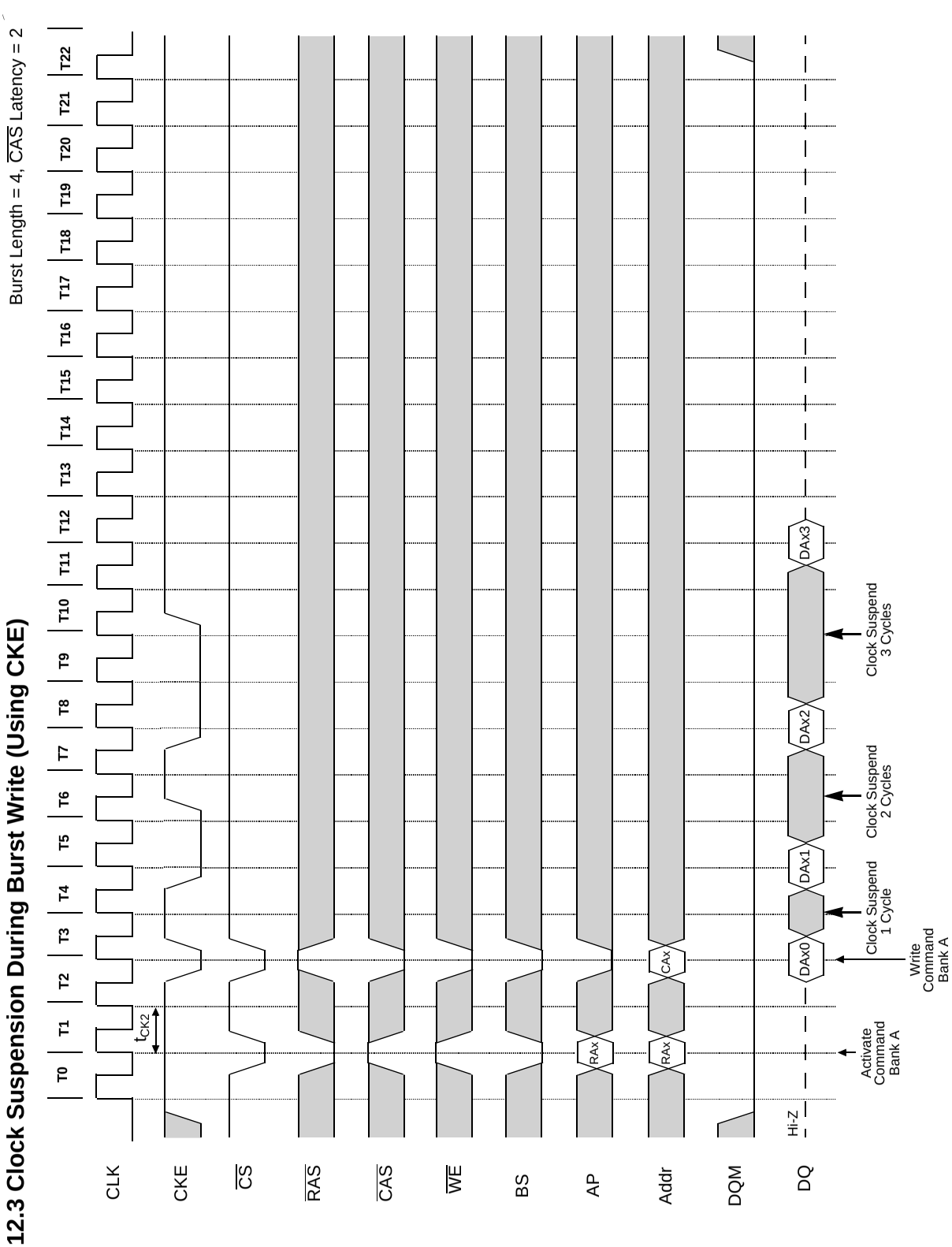
12.1 Clock Suspension During Burst Read (Using CKE)



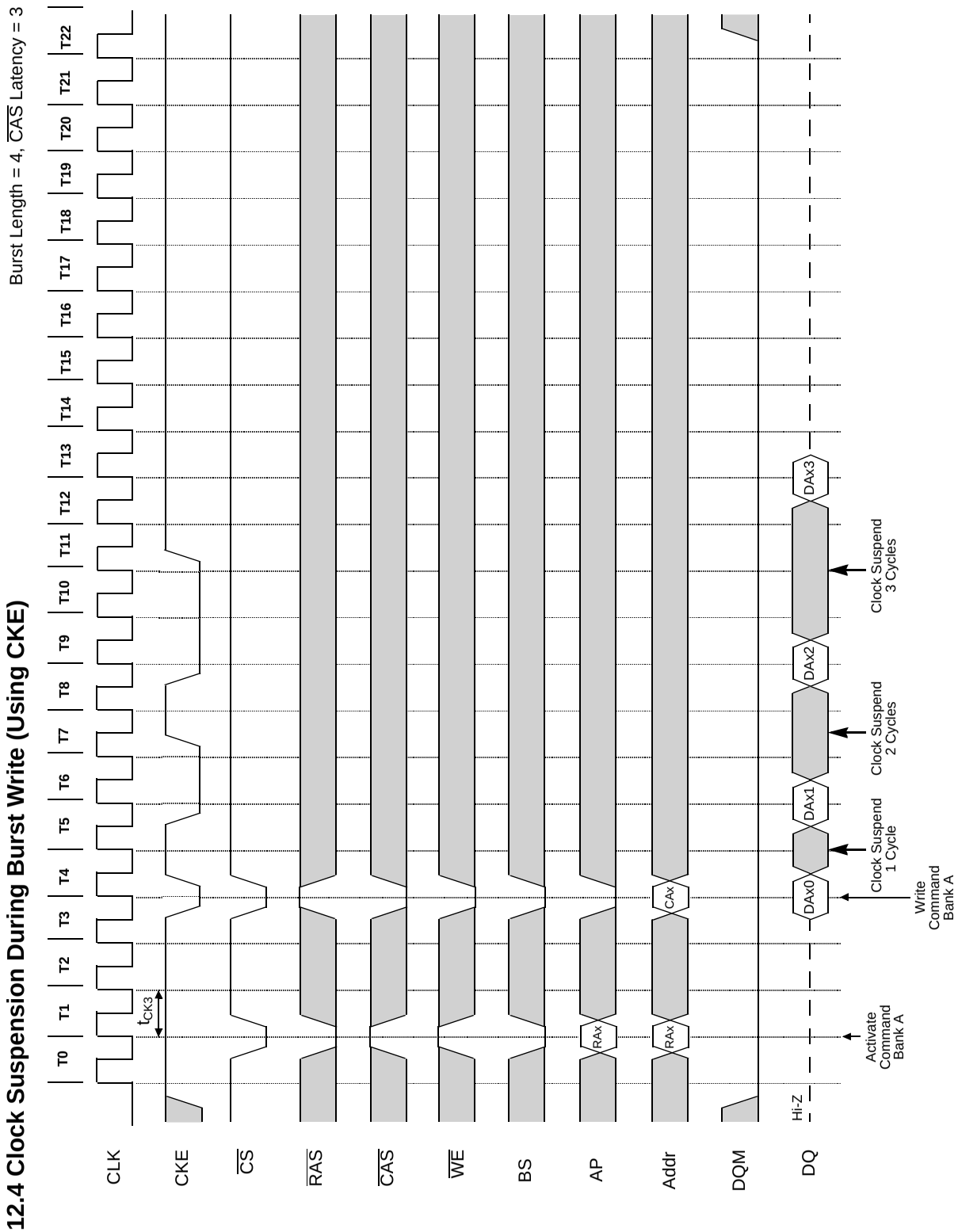
12.2 Clock Suspension During Burst Read (Using CKE)



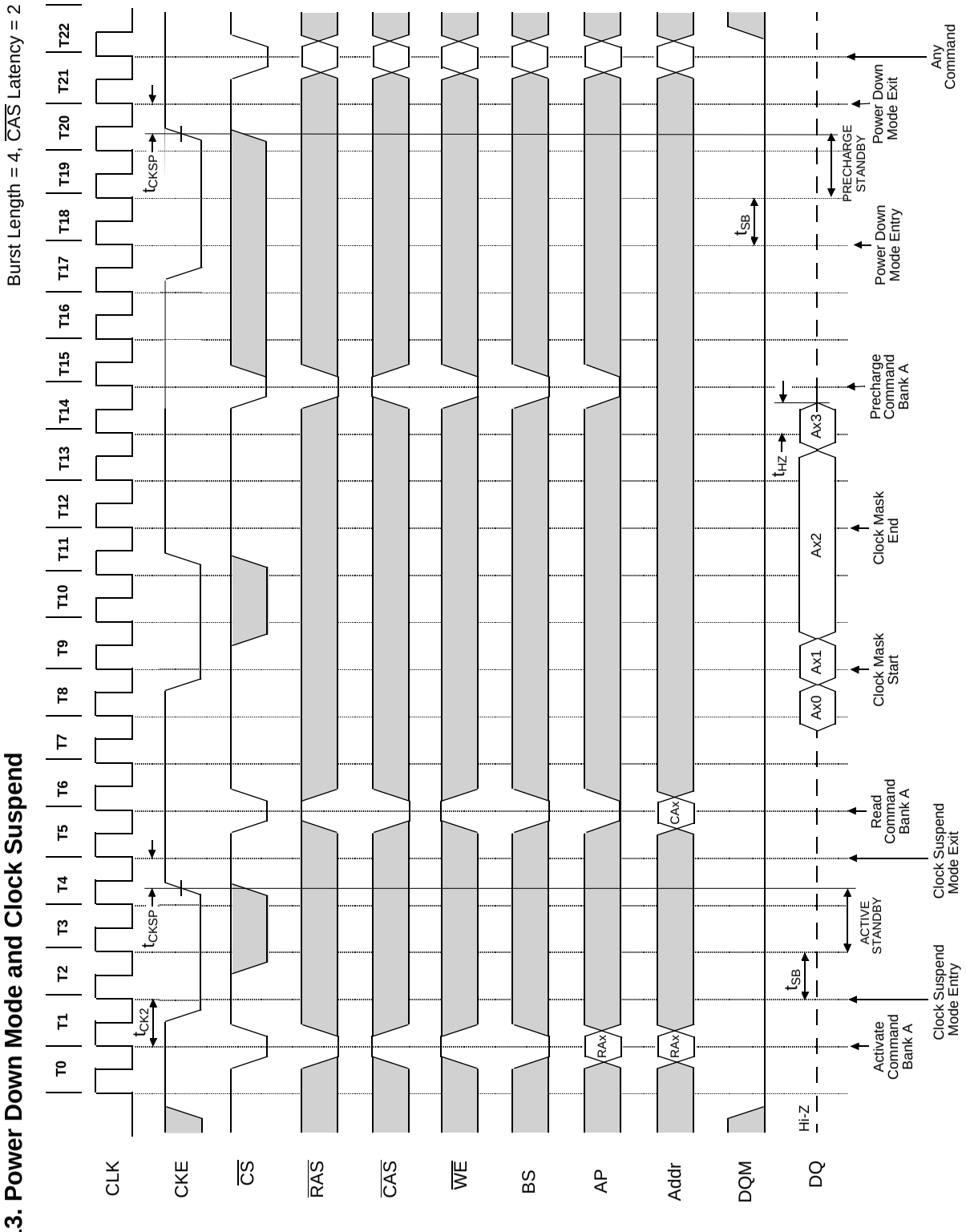
12.3 Clock Suspension During Burst Write (Using CKE)



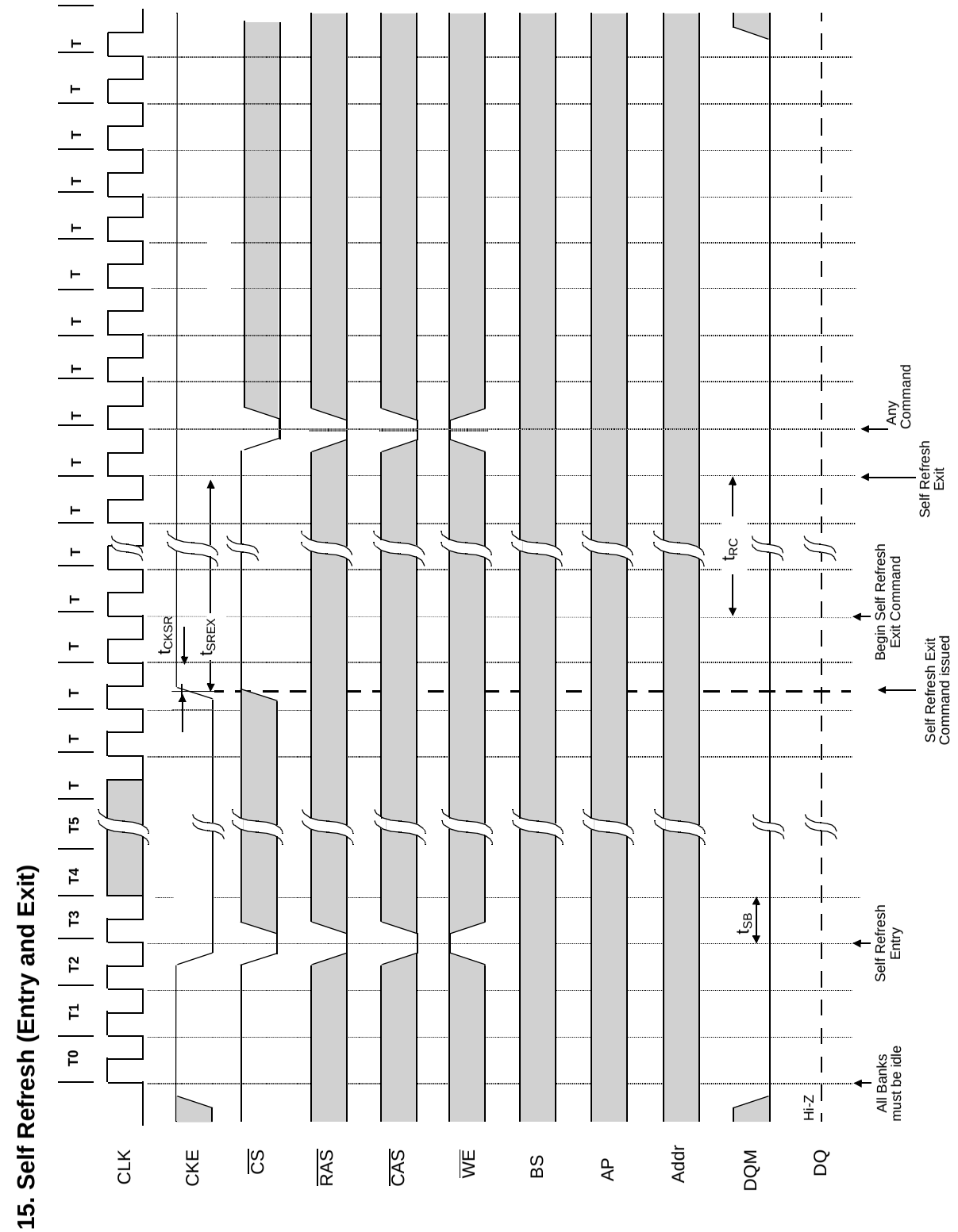
12.4 Clock Suspension During Burst Write (Using CKE)



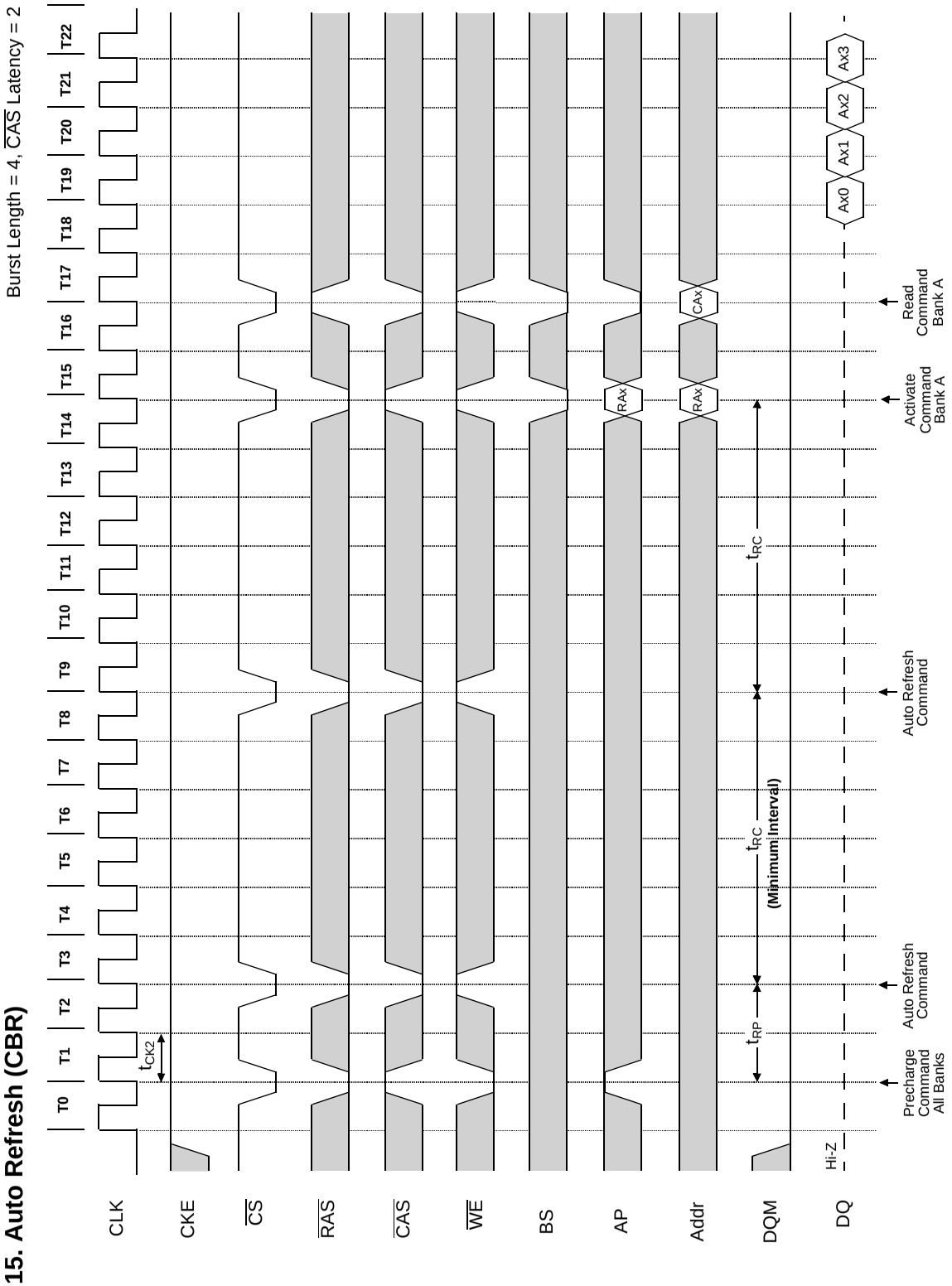
13. Power Down Mode and Clock Suspend



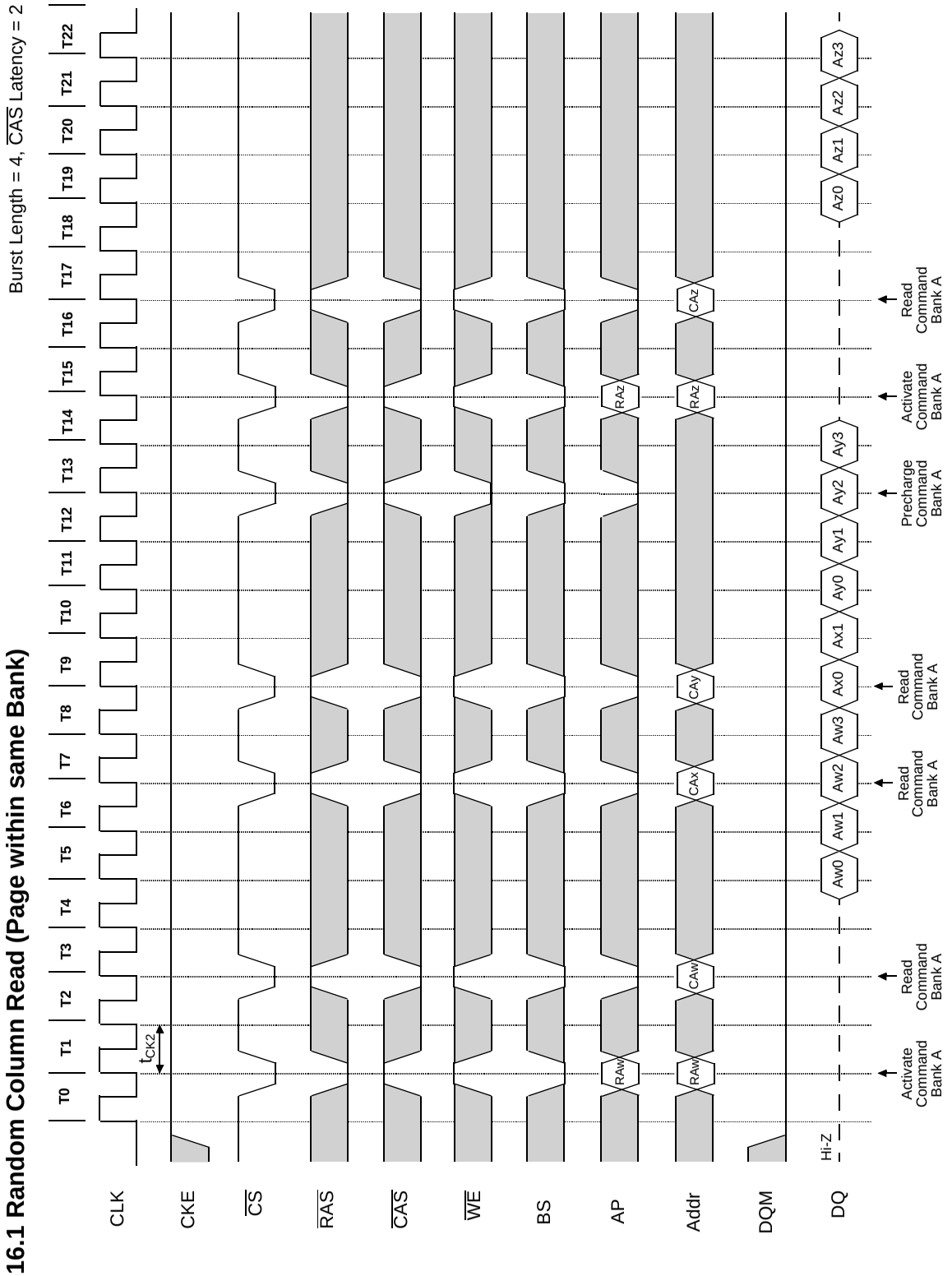
15. Self Refresh (Entry and Exit)



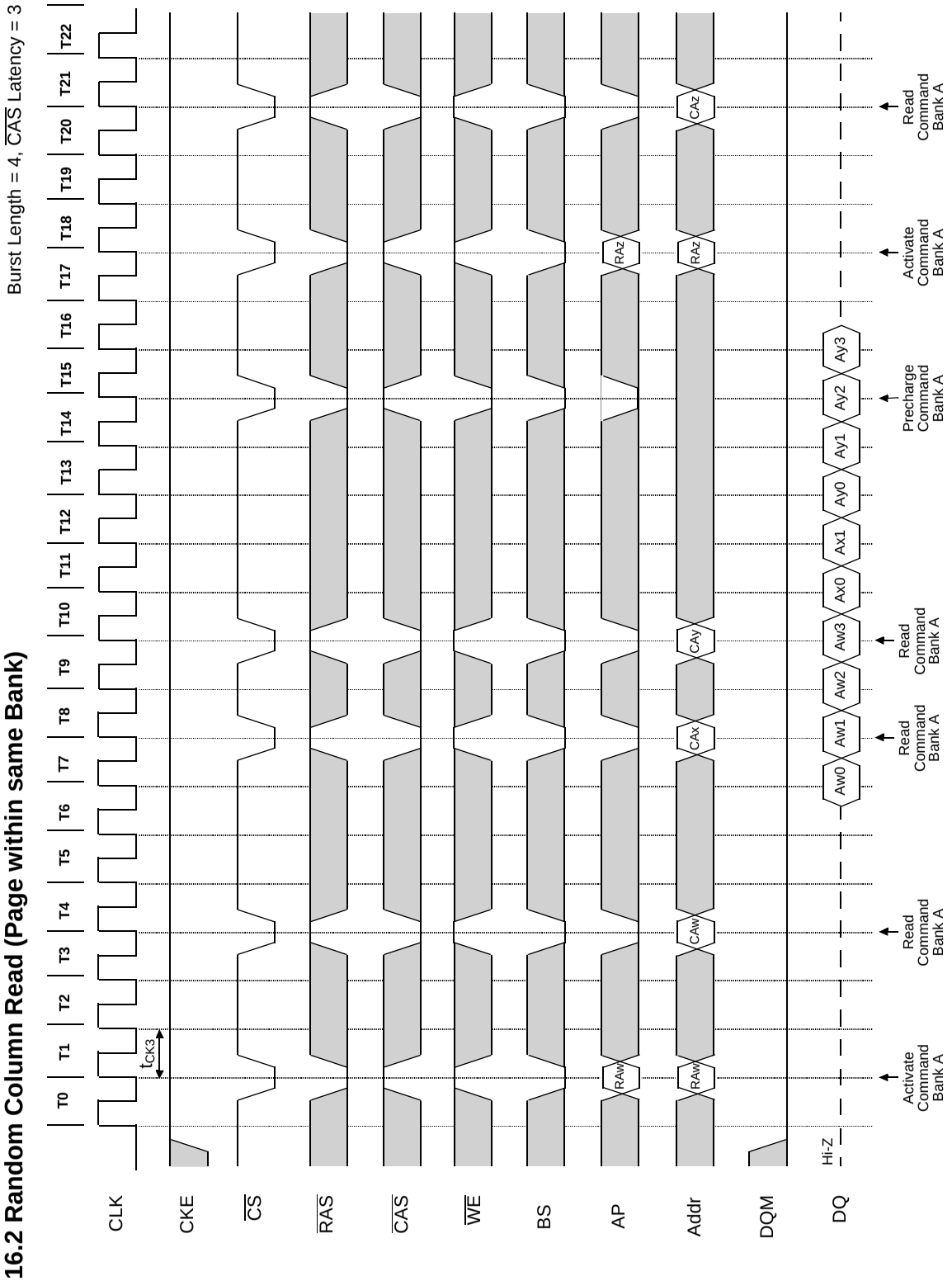
15. Auto Refresh (CBR)



16.1 Random Column Read (Page within same Bank)

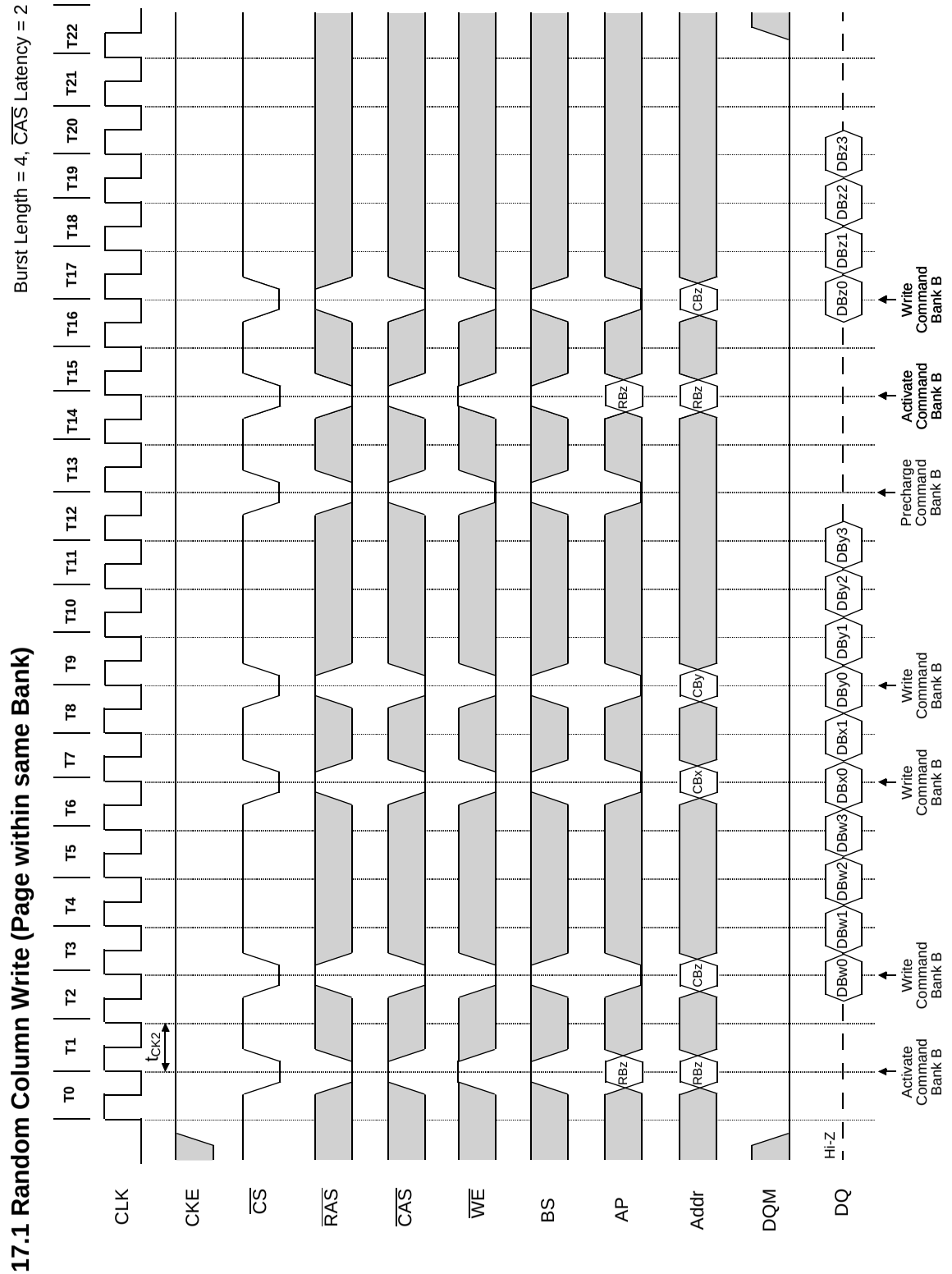


16.2 Random Column Read (Page within same Bank)

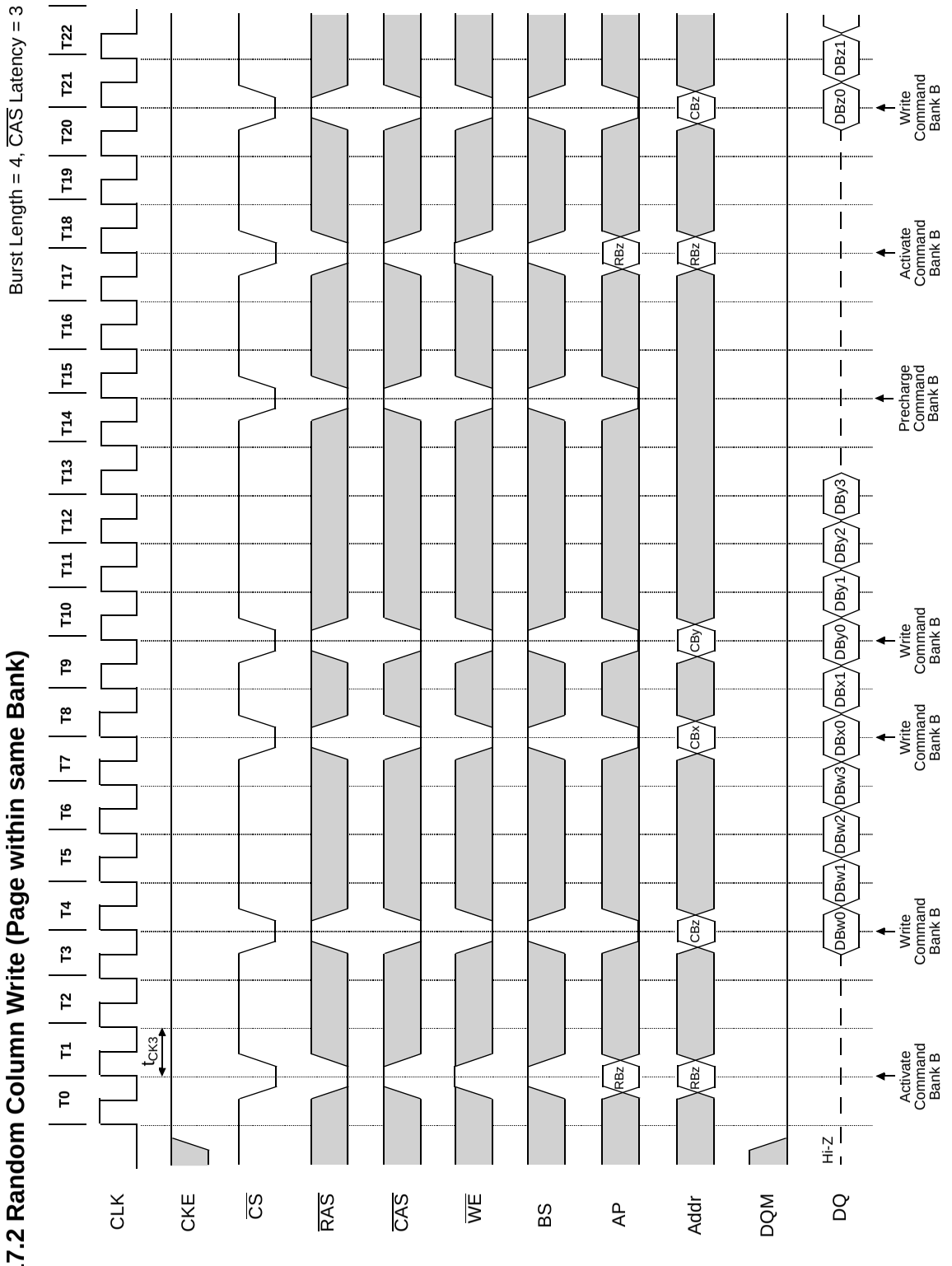


17.1 Random Column Write (Page within same Bank)

Burst Length = 4, $\overline{CAS}$ Latency = 2

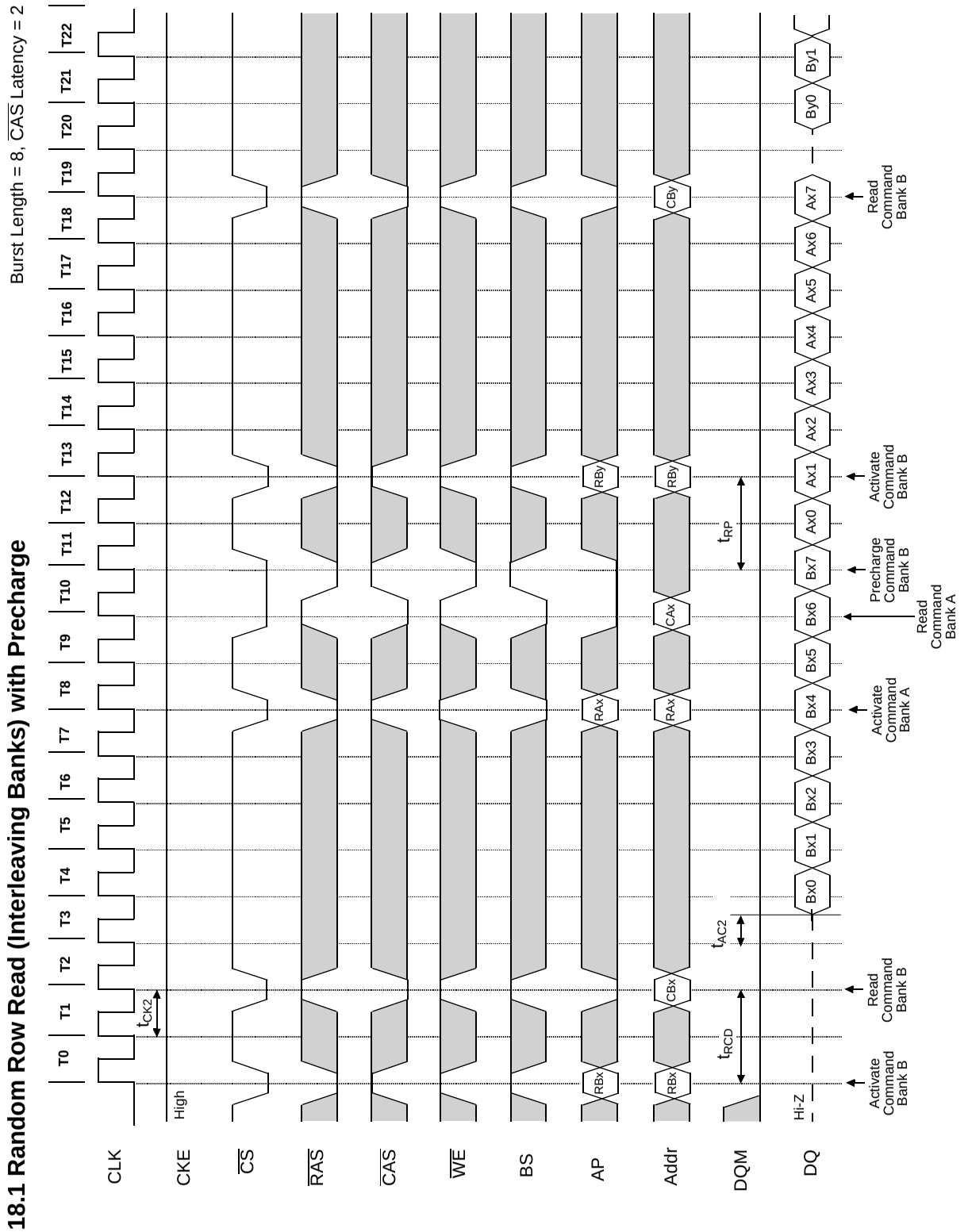


17.2 Random Column Write (Page within same Bank)



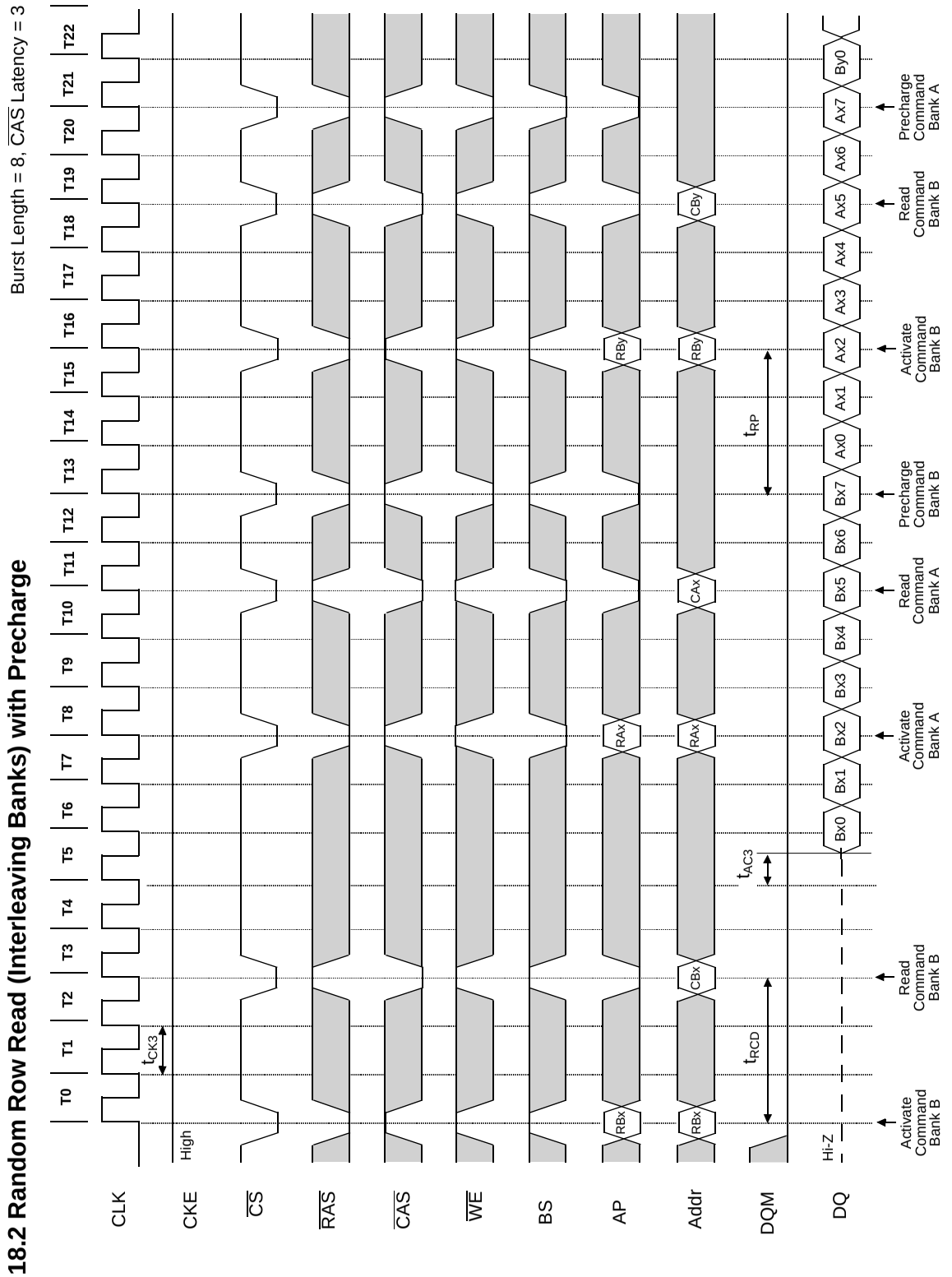
18.1 Random Row Read (Interleaving Banks) with Precharge

Burst Length = 8, $\overline{CAS}$ Latency = 2



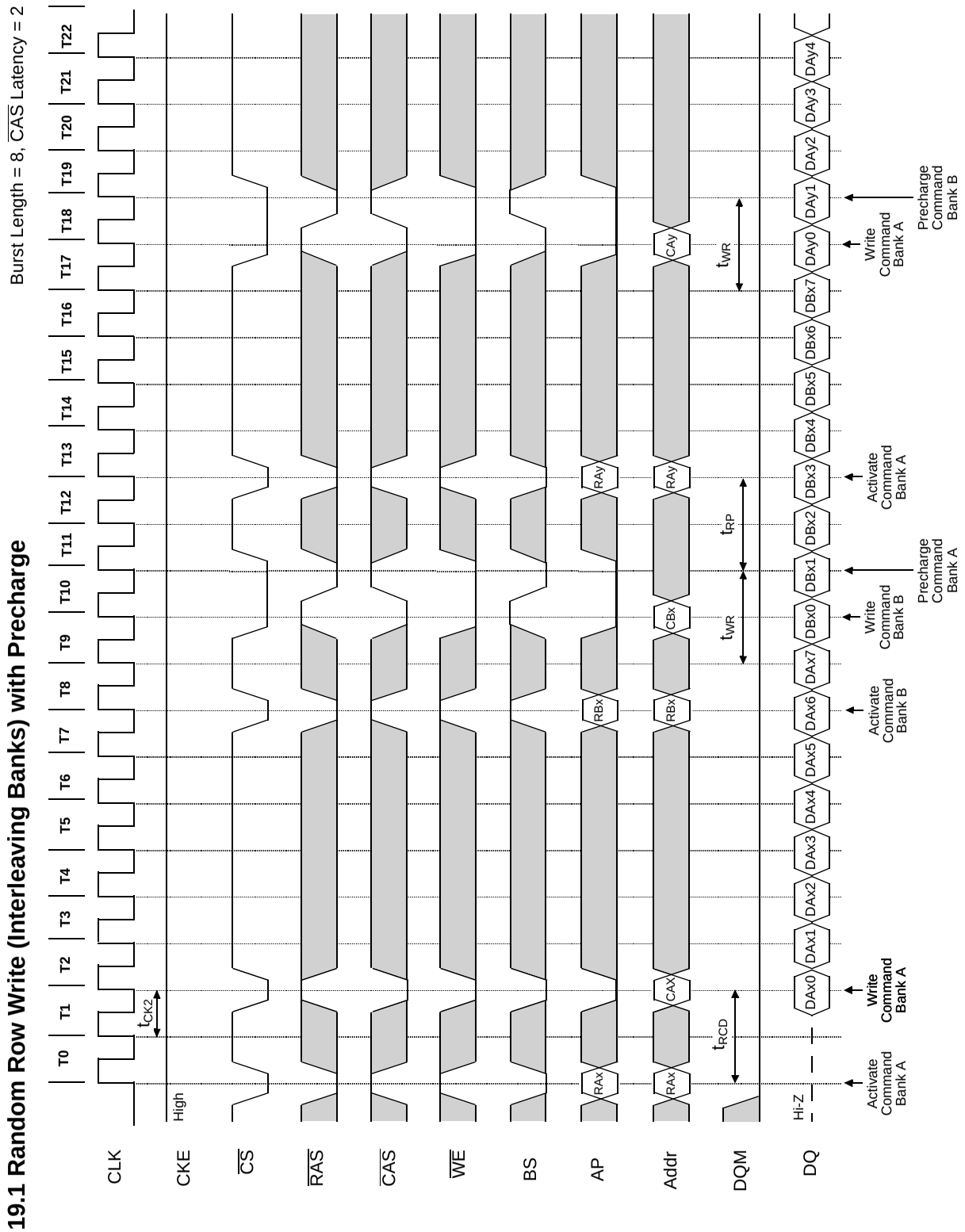
18.2 Random Row Read (Interleaving Banks) with Precharge

Burst Length = 8, $\overline{CAS}$ Latency = 3



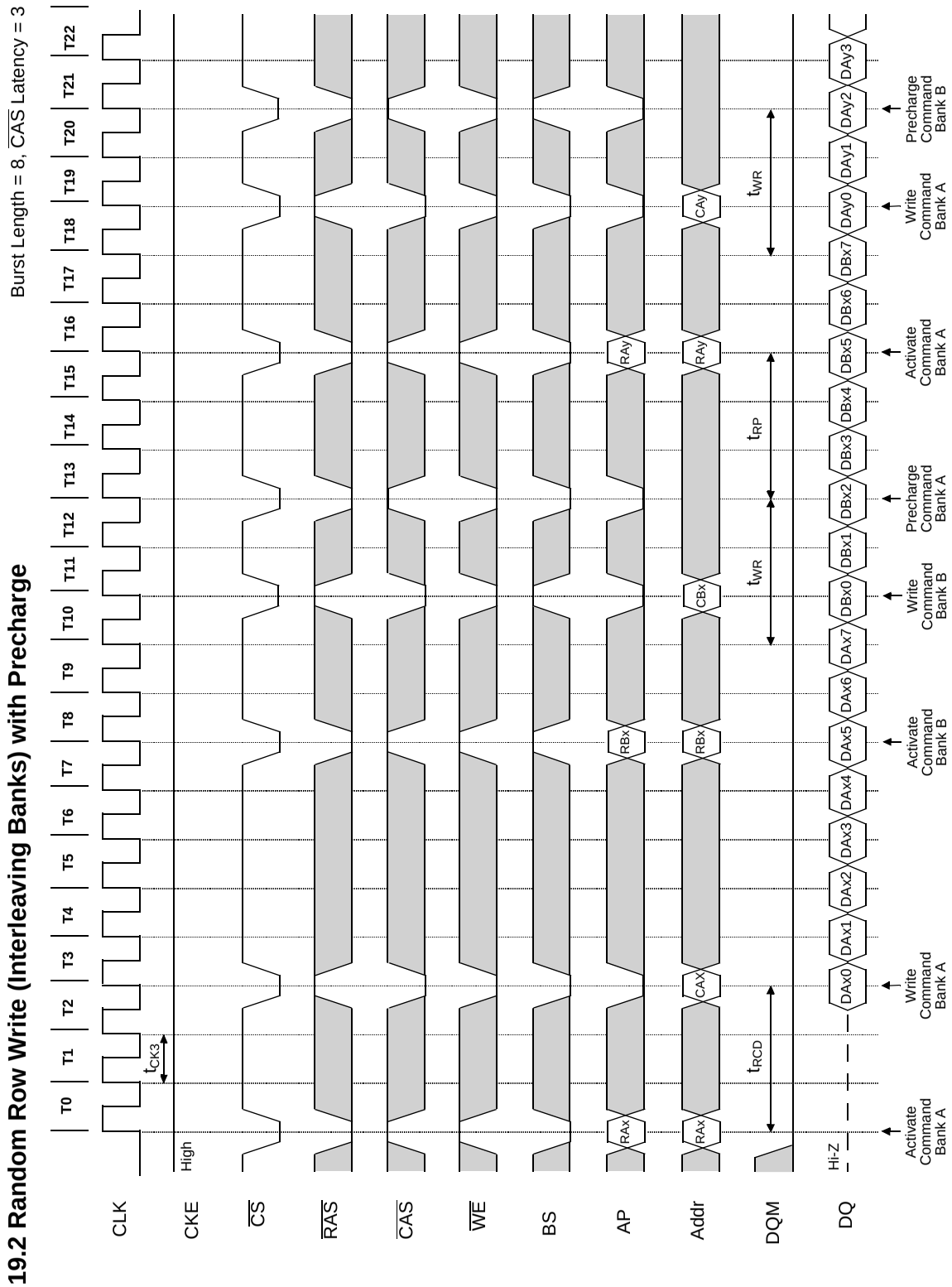
19.1 Random Row Write (Interleaving Banks) with Precharge

Burst Length = 8, $\overline{CAS}$ Latency = 2

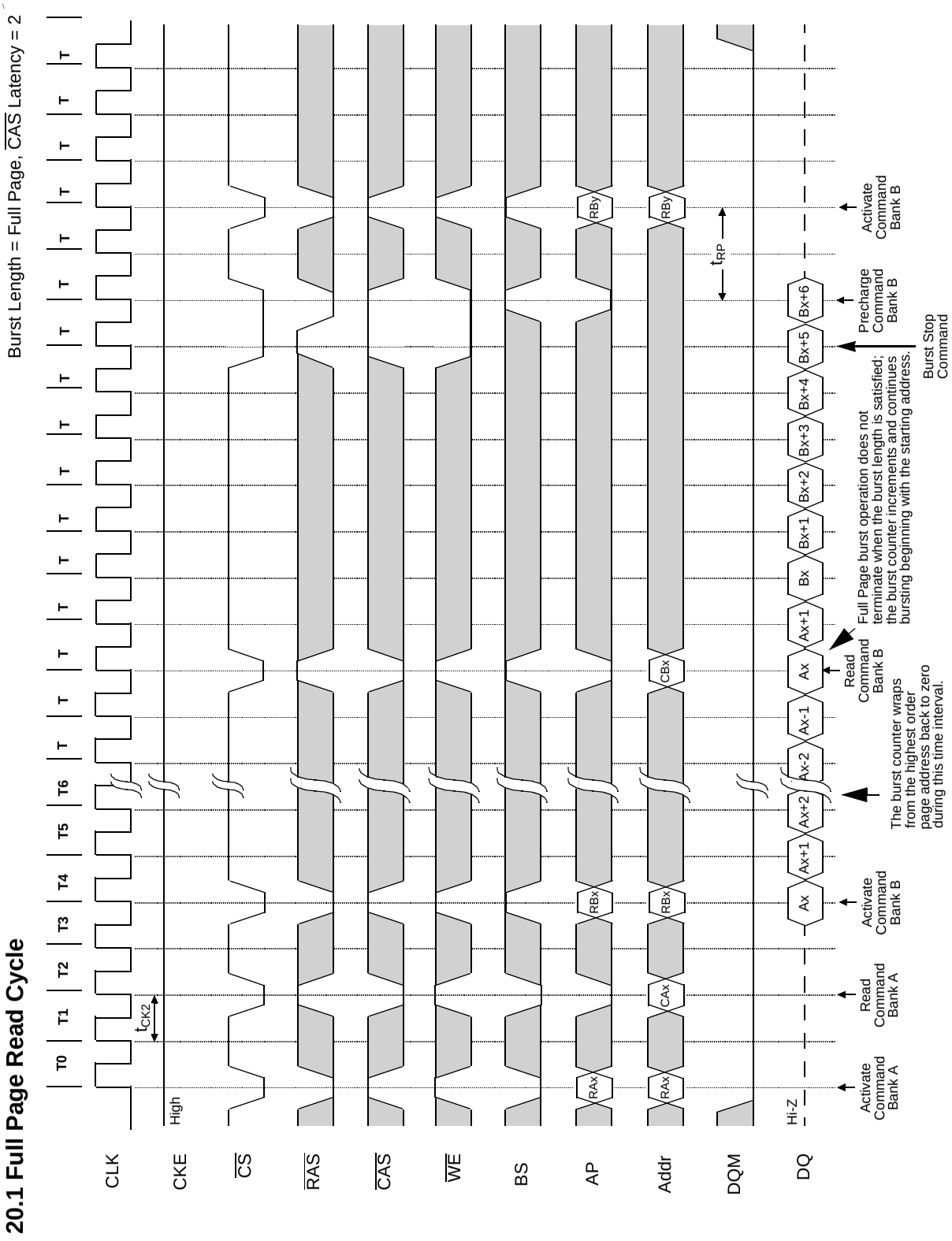


19.2 Random Row Write (Interleaving Banks) with Precharge

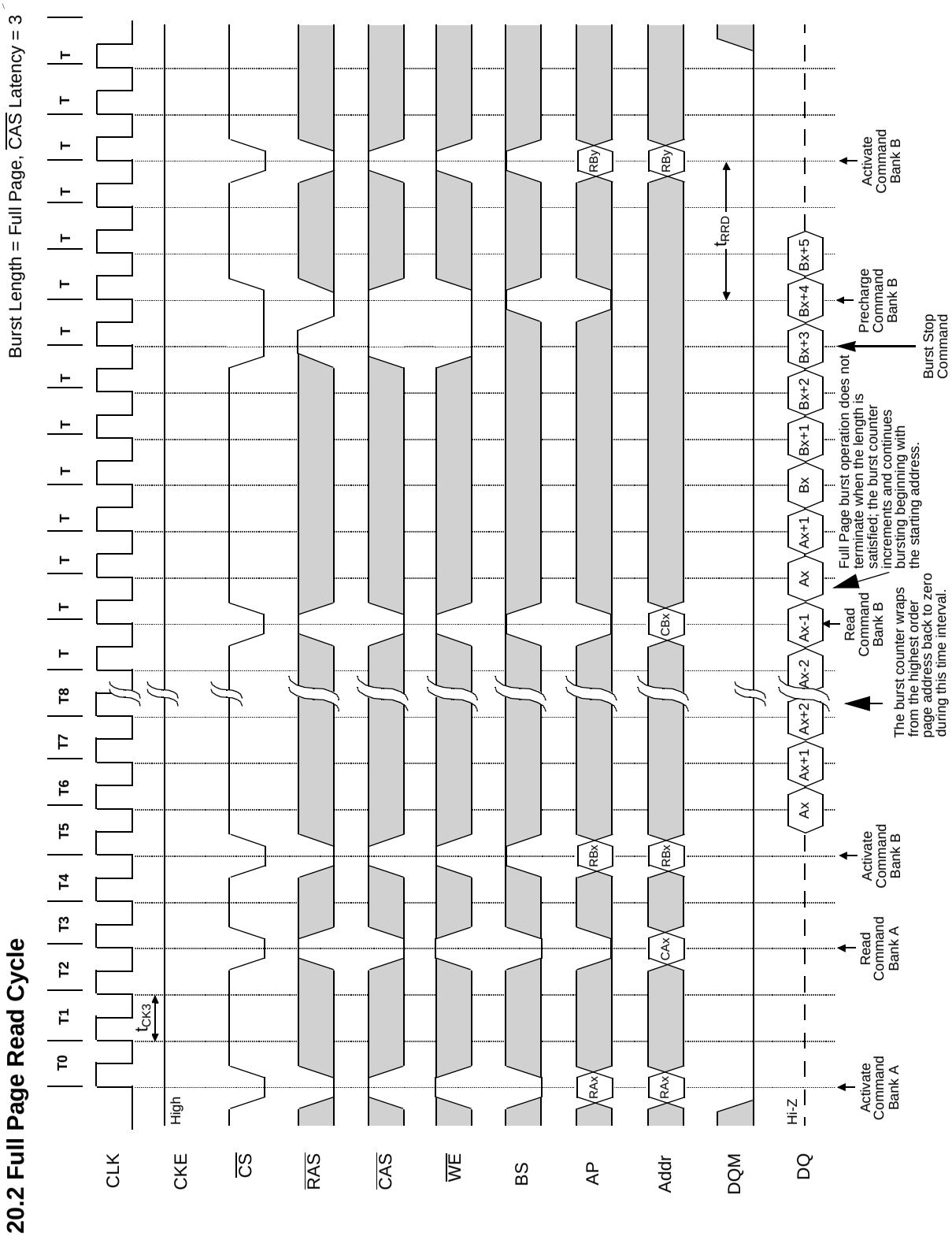
Burst Length = 8, $\overline{CAS}$ Latency = 3



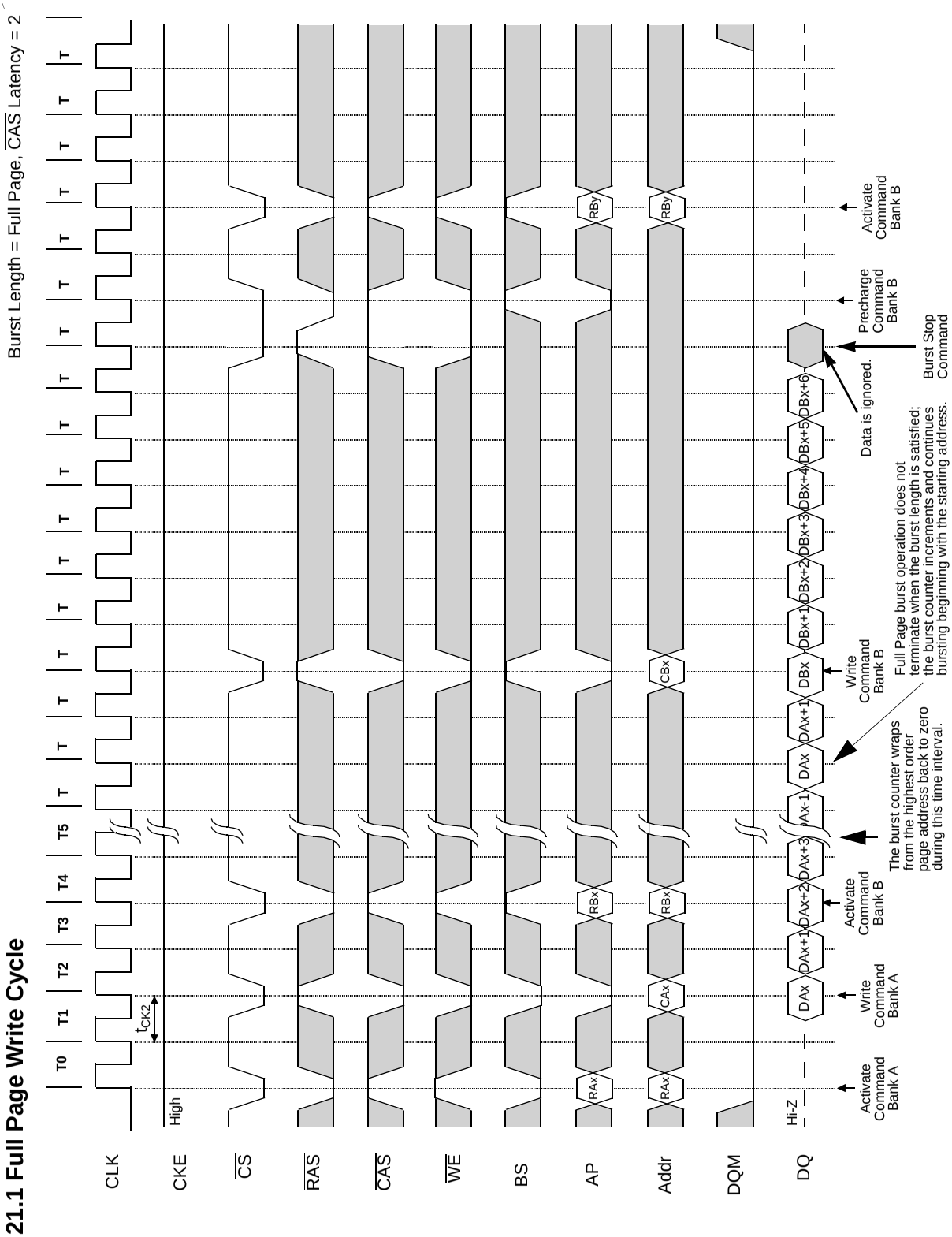
20.1 Full Page Read Cycle



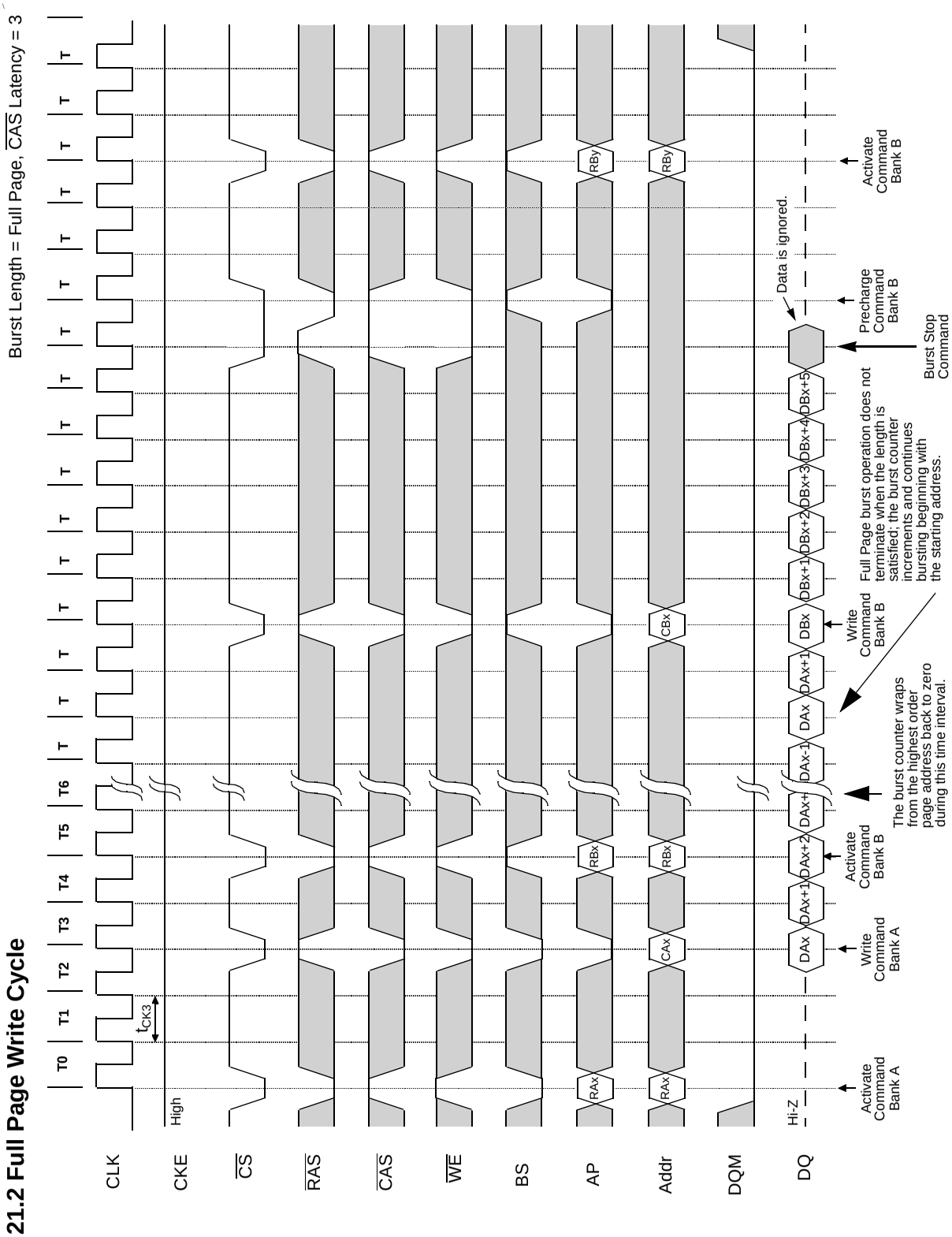
20.2 Full Page Read Cycle



21.1 Full Page Write Cycle



21.2 Full Page Write Cycle



22.1 Precharge Termination of a Burst