

Timing Diagrams

1. Bank Activate Command Cycle
2. Burst Read Operation
3. Read Interrupted by a Read
4. Read to Write Interval
 - 4.1 Read to Write Interval
 - 4.2 Minimum Read to Write Interval
 - 4.3 Non-Minimum Read to Write Interval
5. Burst Write Operation
6. Write and Read Interrupt
 - 6.1 Write Interrupted by a Write
 - 6.2 Write Interrupted by Read
7. Burst Write & Read with Auto-Precharge
 - 7.1 Burst Write with Auto-Precharge
 - 7.2 Burst Read with Auto-Precharge
8. Burst Termination
 - 8.1 Termination of a full Page Burst Write Operation
 - 8.2 Termination of a Full Page Burst Write Operation
9. AC- Parameters
 - 9.1 AC Parameters for a Write Timing
 - 9.2 AC Parameters for a Read Timing
10. Mode Register Set
11. Power on Sequence and Auto Refresh (CBR)
12. Clock Suspension (using CKE)
 12. 1 Clock Suspension During Burst Read $\overline{\text{CAS}}$ Latency = 2
 12. 2 Clock Suspension During Burst Read $\overline{\text{CAS}}$ Latency = 3
 12. 3 Clock Suspension During Burst Write $\overline{\text{CAS}}$ Latency = 2
 12. 4 Clock Suspension During Burst Write $\overline{\text{CAS}}$ Latency = 3
13. Power Down Mode and Clock Suspend
14. Self Refresh (Entry and Exit)
15. Auto Refresh (CBR)
16. Random Column Read (Page within same Bank)
 - 16.1 $\overline{\text{CAS}}$ Latency = 2
 - 16.2 $\overline{\text{CAS}}$ Latency = 3
17. Random Column Write (Page within same Bank)
 - 17.1 $\overline{\text{CAS}}$ Latency = 2
 - 17.2 $\overline{\text{CAS}}$ Latency = 3

Timing Diagrams (cont'd)

18. Random Row Read (Interleaving Banks) with Precharge

18.1 $\overline{\text{CAS}}$ Latency = 218.2 $\overline{\text{CAS}}$ Latency = 3

19. Random Row Write (Interleaving Banks) with Precharge

19.1 $\overline{\text{CAS}}$ Latency = 219.2 $\overline{\text{CAS}}$ Latency = 3

20. Full Page Read Cycle

20.1 $\overline{\text{CAS}}$ Latency = 220.2 $\overline{\text{CAS}}$ Latency = 3

21. Full Page Write Cycle

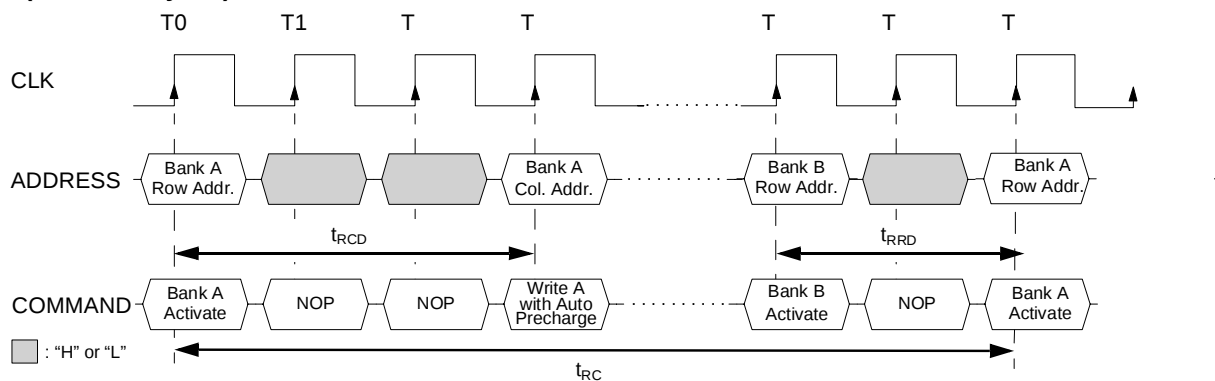
21.1 $\overline{\text{CAS}}$ Latency = 221.2 $\overline{\text{CAS}}$ Latency = 3

22. Precharge Termination of a Burst

22.1 $\overline{\text{CAS}}$ Latency = 222.2 $\overline{\text{CAS}}$ Latency = 3

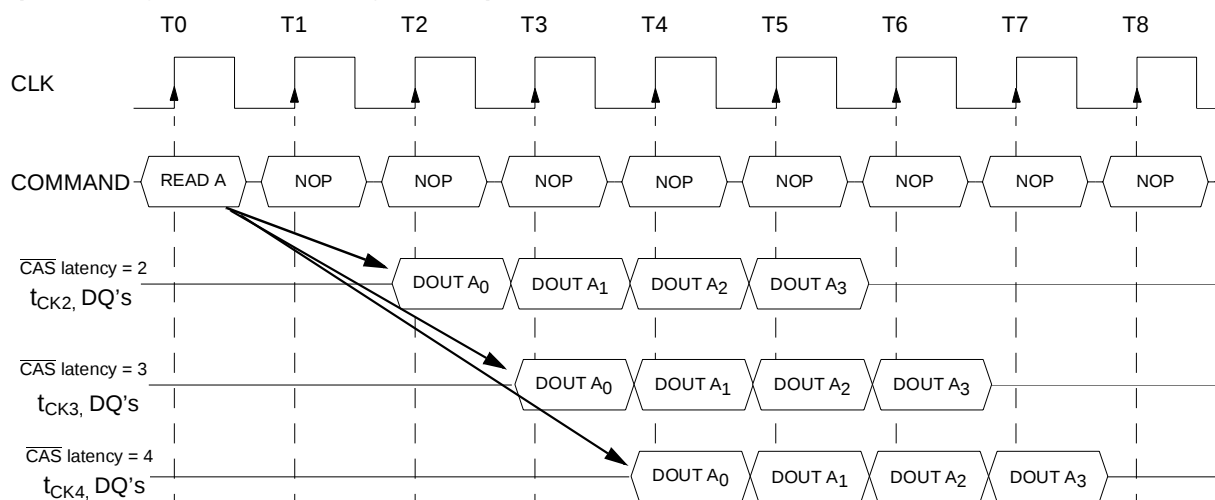
1. Bank Activate Command Cycle

($\overline{\text{CAS}}$ latency = 3)



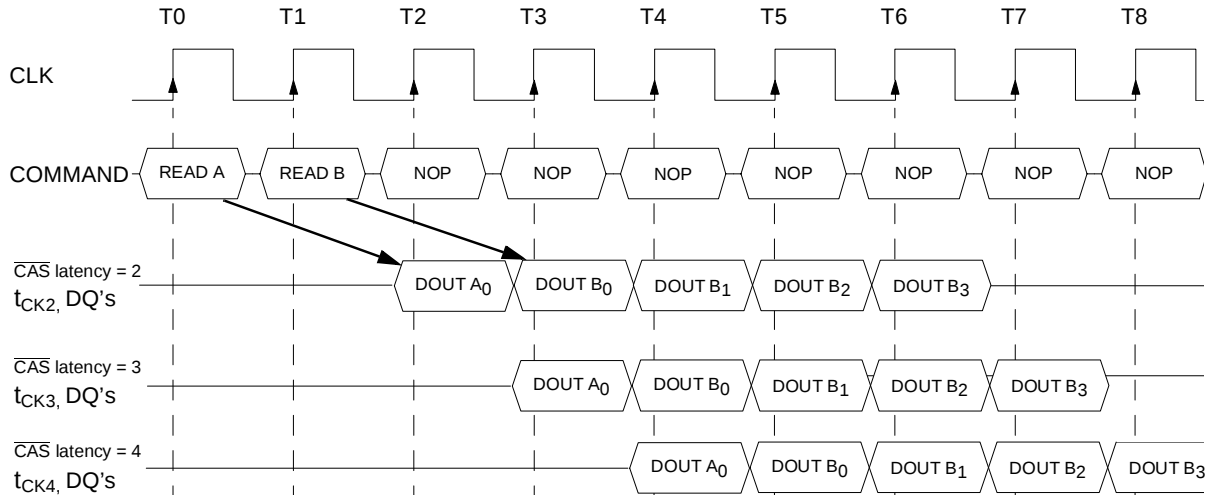
2. Burst Read Operation

(Burst Length = 4, $\overline{\text{CAS}}$ latency = 2, 3, 4)



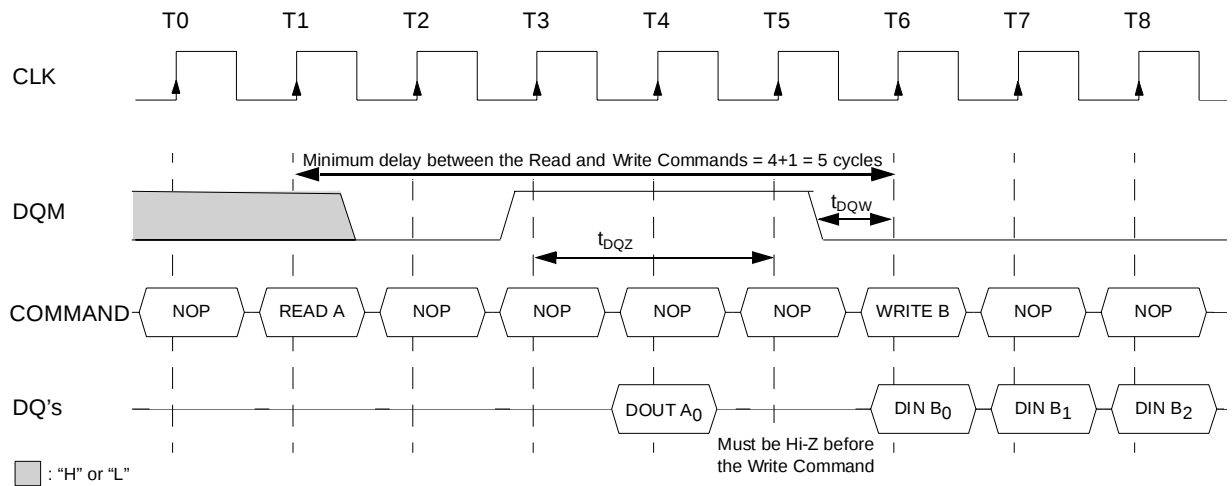
3. Read Interrupted by a Read

(Burst Length = 4, $\overline{\text{CAS}}$ latency = 2, 3, 4)



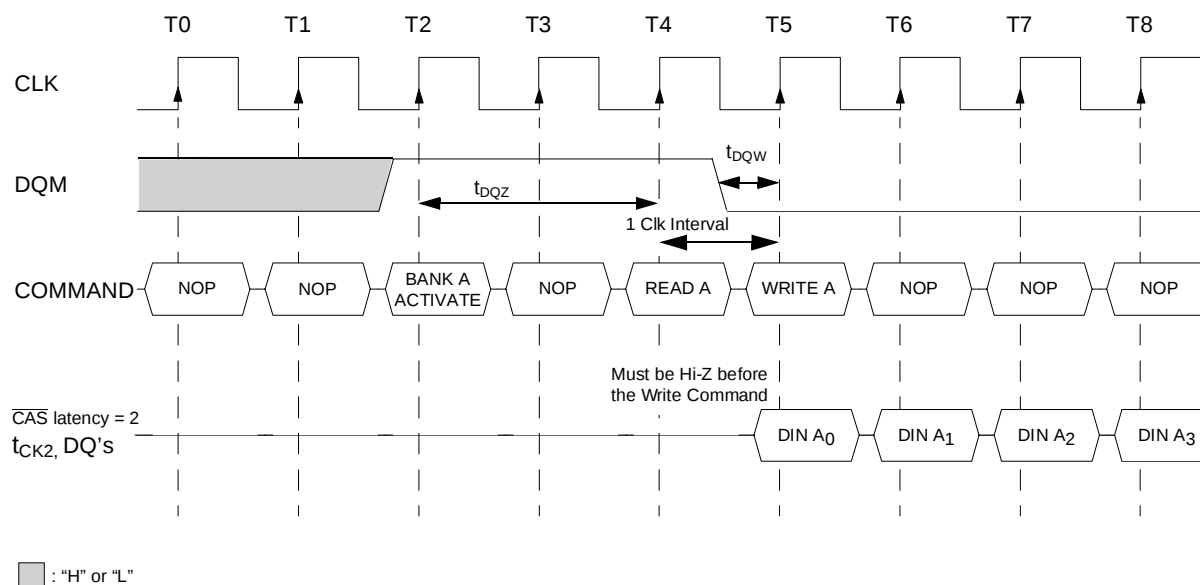
4.1 Read to Write Interval

(Burst Length = 4, $\overline{\text{CAS}}$ latency = 3)



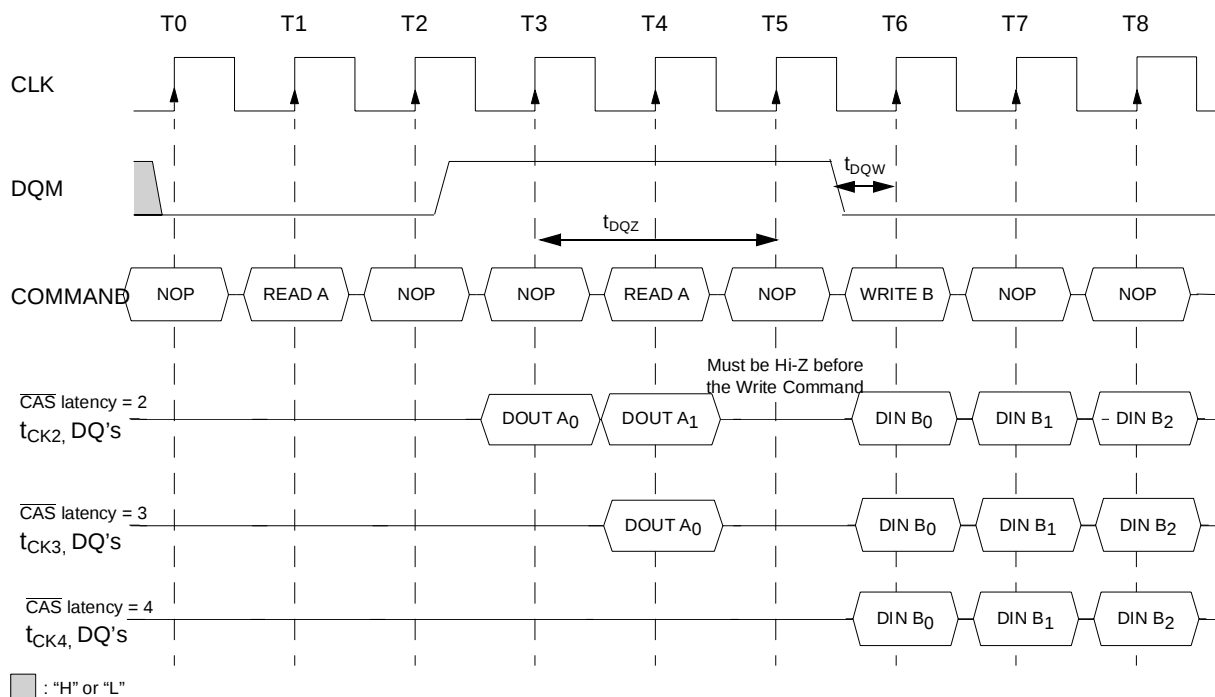
4 2. Minimum Read to Write Interval

(Burst Length = 4, $\overline{\text{CAS}}$ latency = 2)



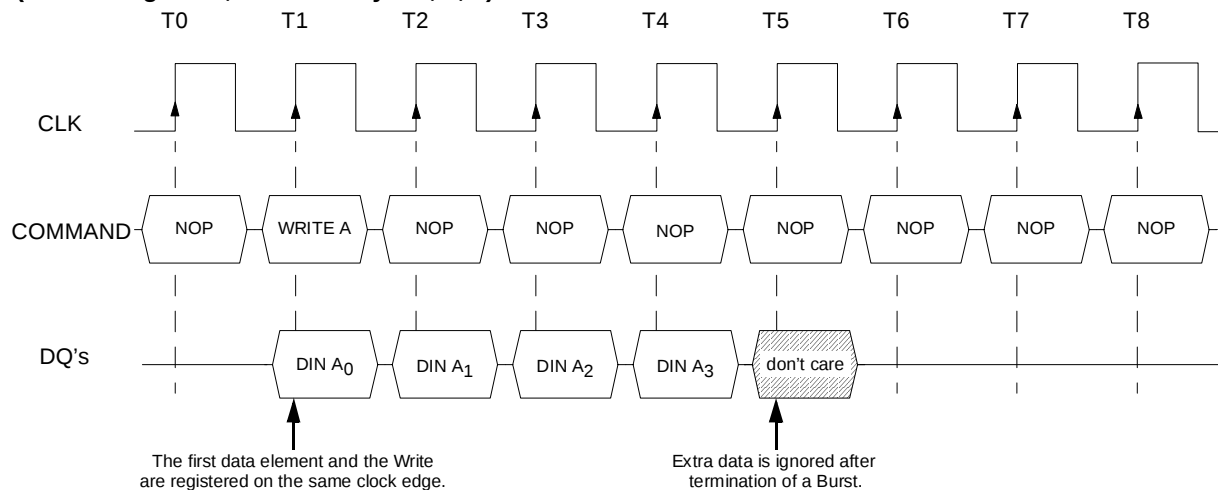
4. 3. Non-Minimum Read to Write Interval

(Burst Length = 4, $\overline{\text{CAS}}$ latency = 2, 3, 4)



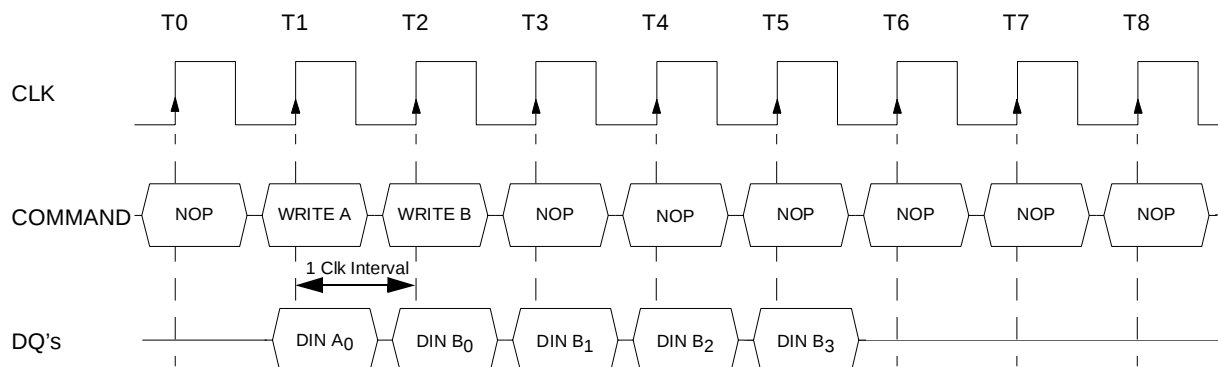
5. Burst Write Operation

(Burst Length = 4, $\overline{\text{CAS}}$ latency = 2, 3, 4)



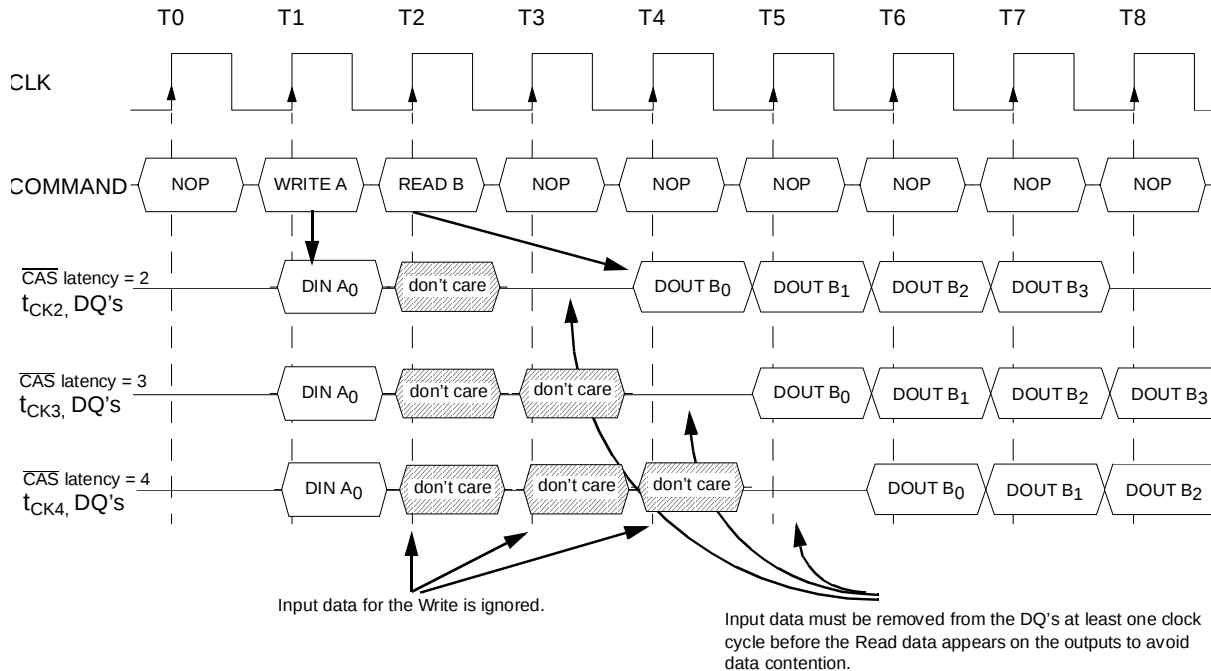
6.1 Write Interrupted by a Write

(Burst Length = 4, $\overline{\text{CAS}}$ latency = 2, 3, 4)



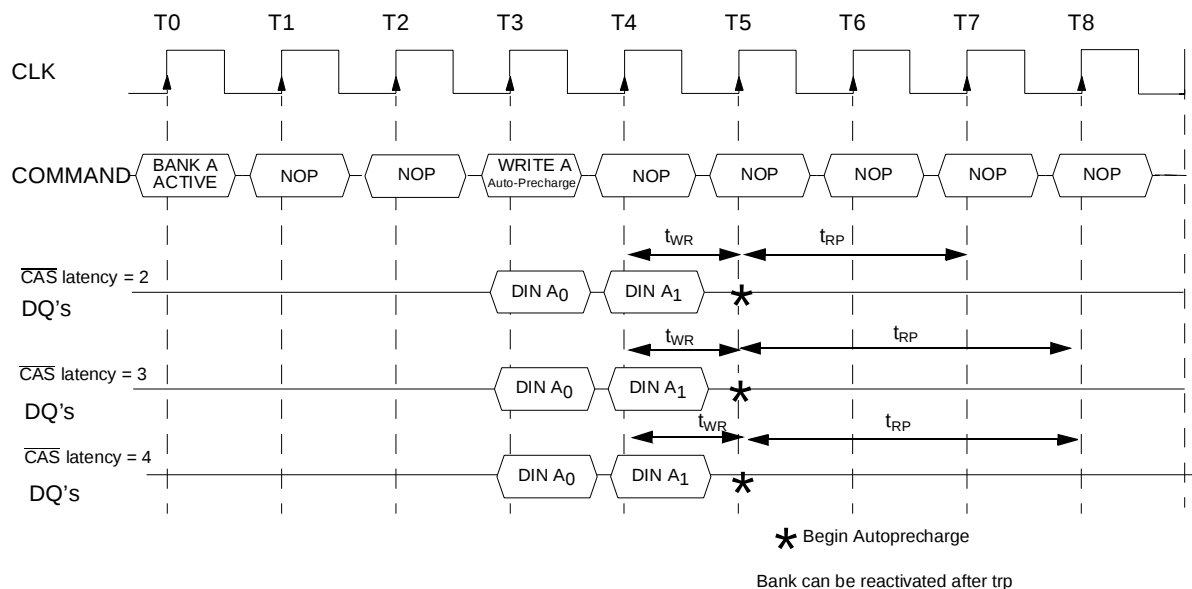
6.2 Write Interrupted by a Read

(Burst Length = 4, $\overline{\text{CAS}}$ latency = 2, 3, 4)



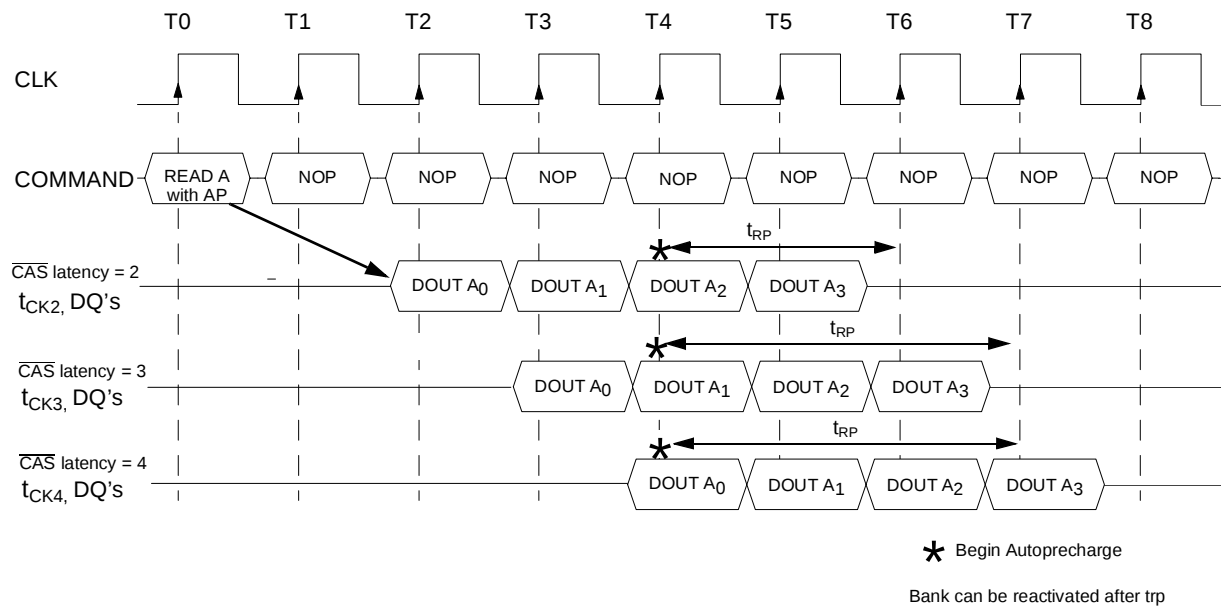
7.1 Burst Write with Auto-Precharge

Burst Length = 2, $\overline{\text{CAS}}$ latency = 2, 3, 4)



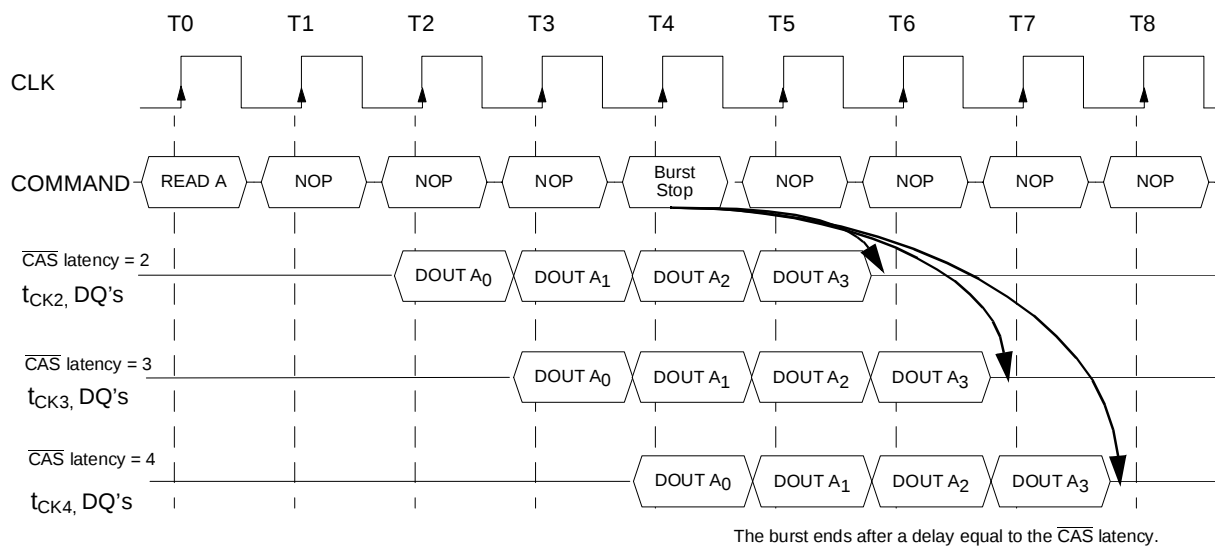
7.2 Burst Read with Auto-Precharge

(Burst Length = 4, $\overline{\text{CAS}}$ latency = 1, 2, 3)



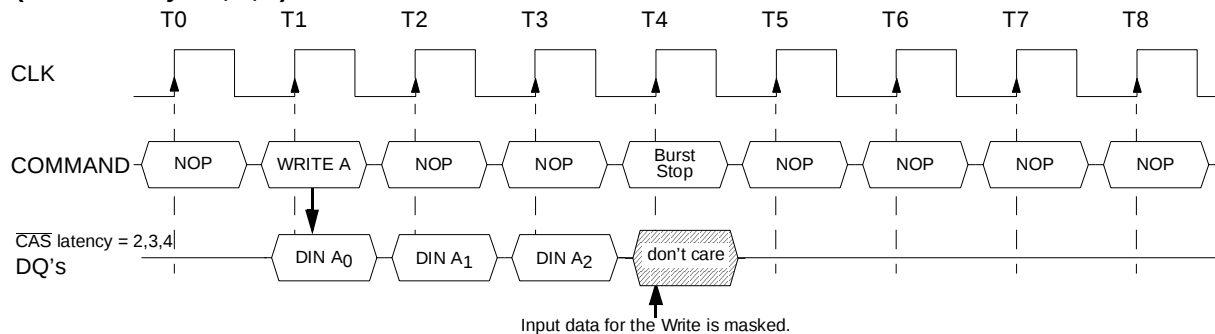
8.1 Termination of a Full Page Burst Read Operation

($\overline{\text{CAS}}$ latency = 2, 3, 4)

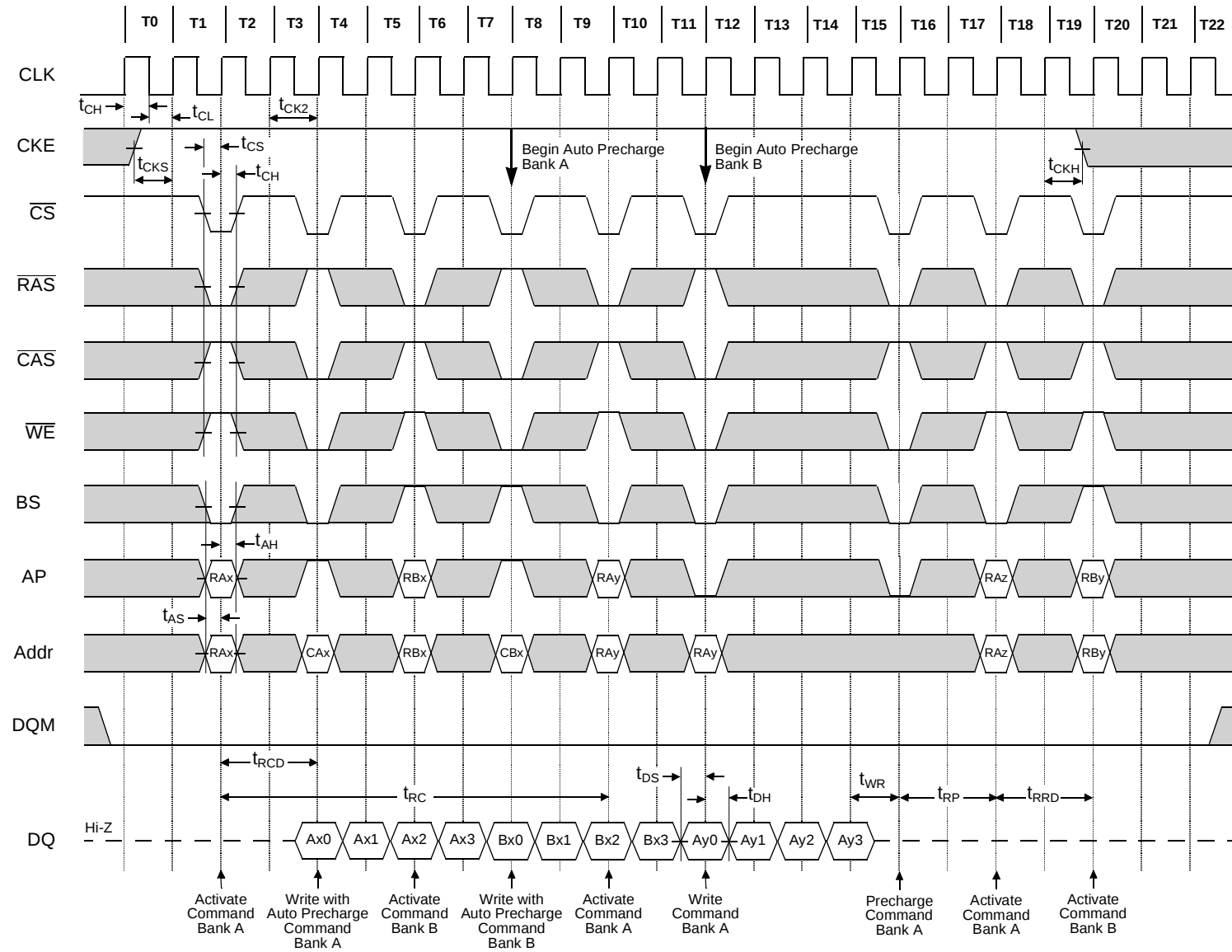


8.2 Termination of a Full Page Burst Write Operation

(CAS Latency = 2, 3, 4)

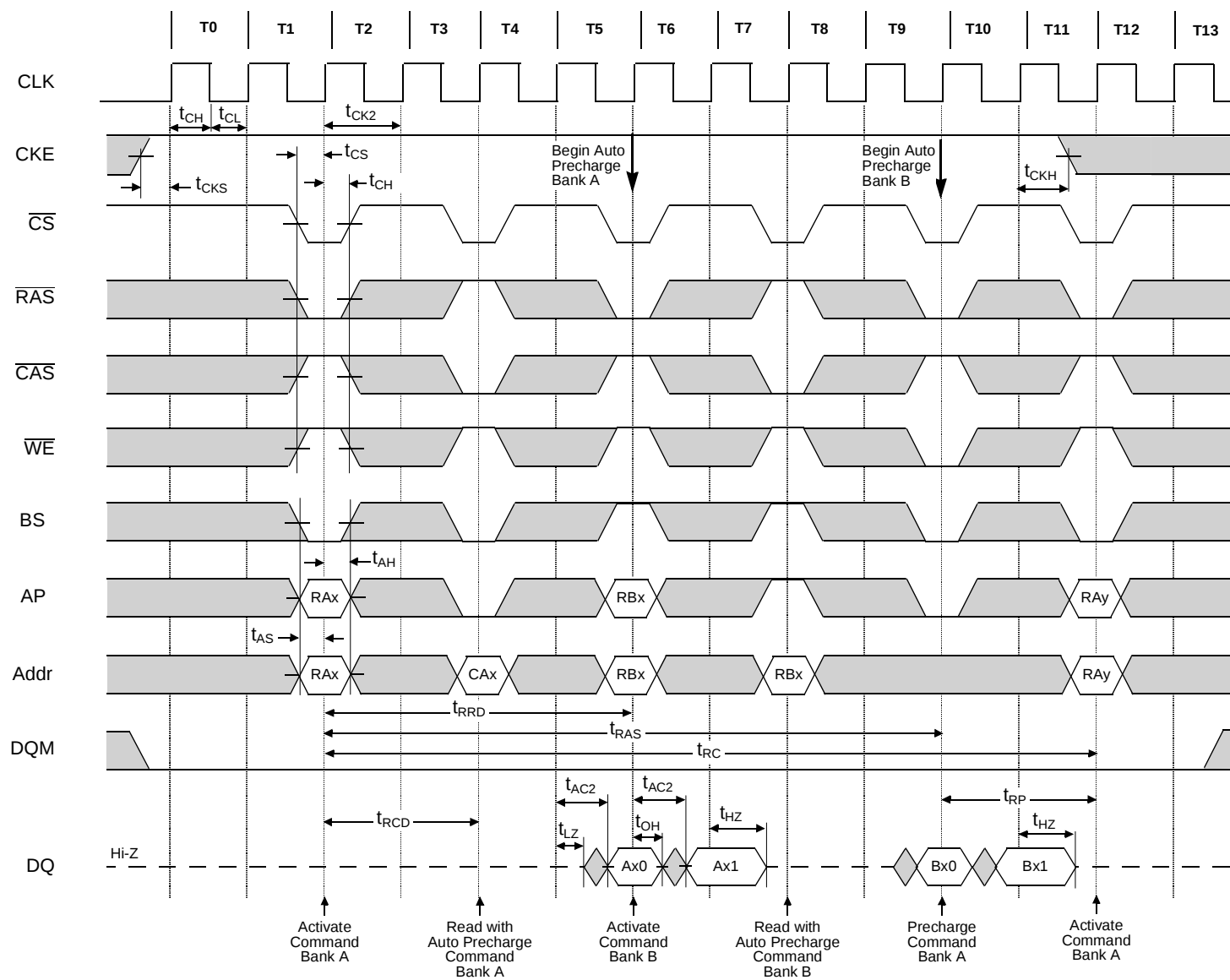


9.1 AC Parameters for Write Timing

Burst Length = 4, $\overline{\text{CAS}}$ Latency = 2

9.2 AC Parameters for Read Timing

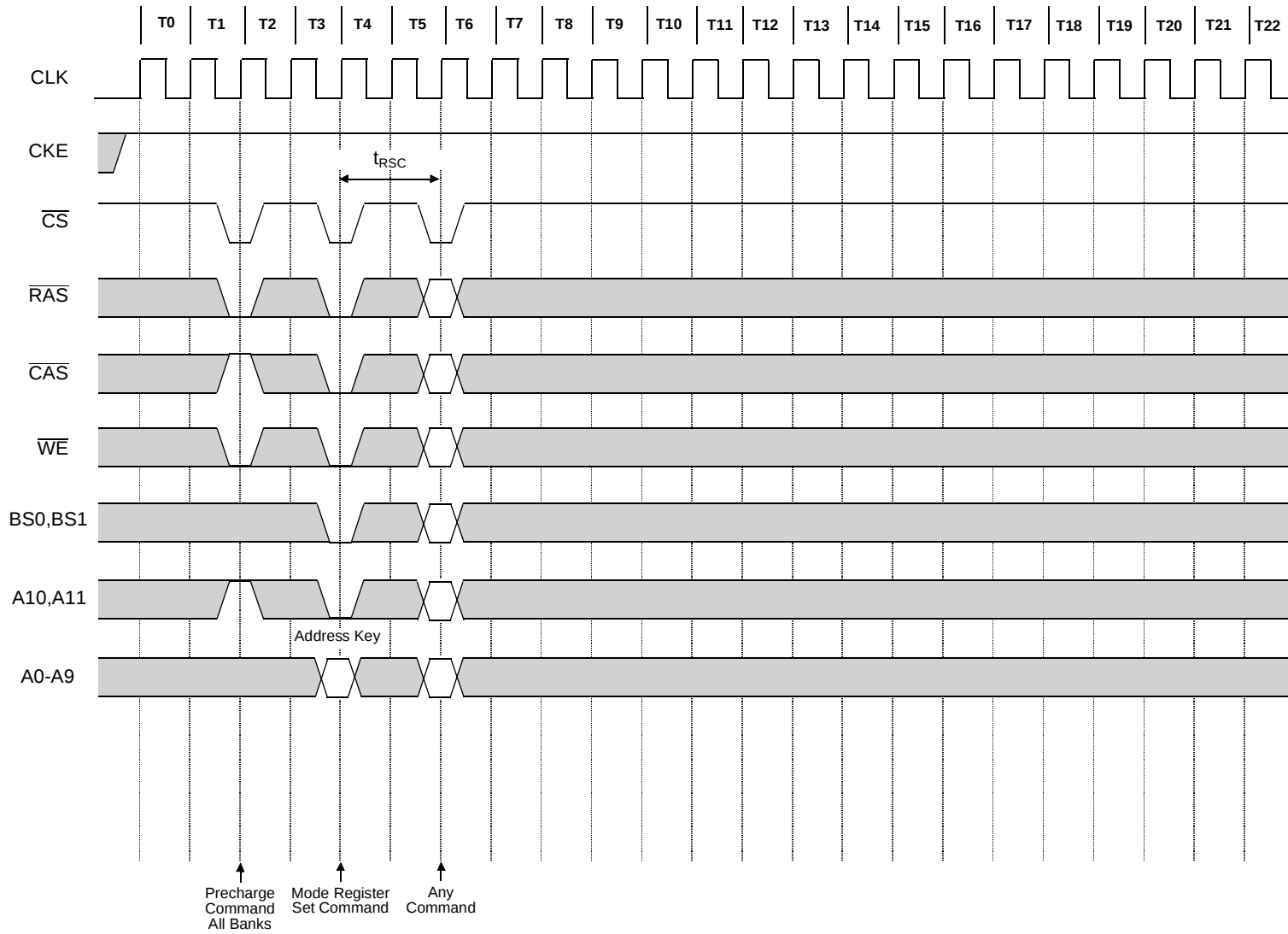
Burst Length = 2, $\overline{\text{CAS}}$ Latency = 2



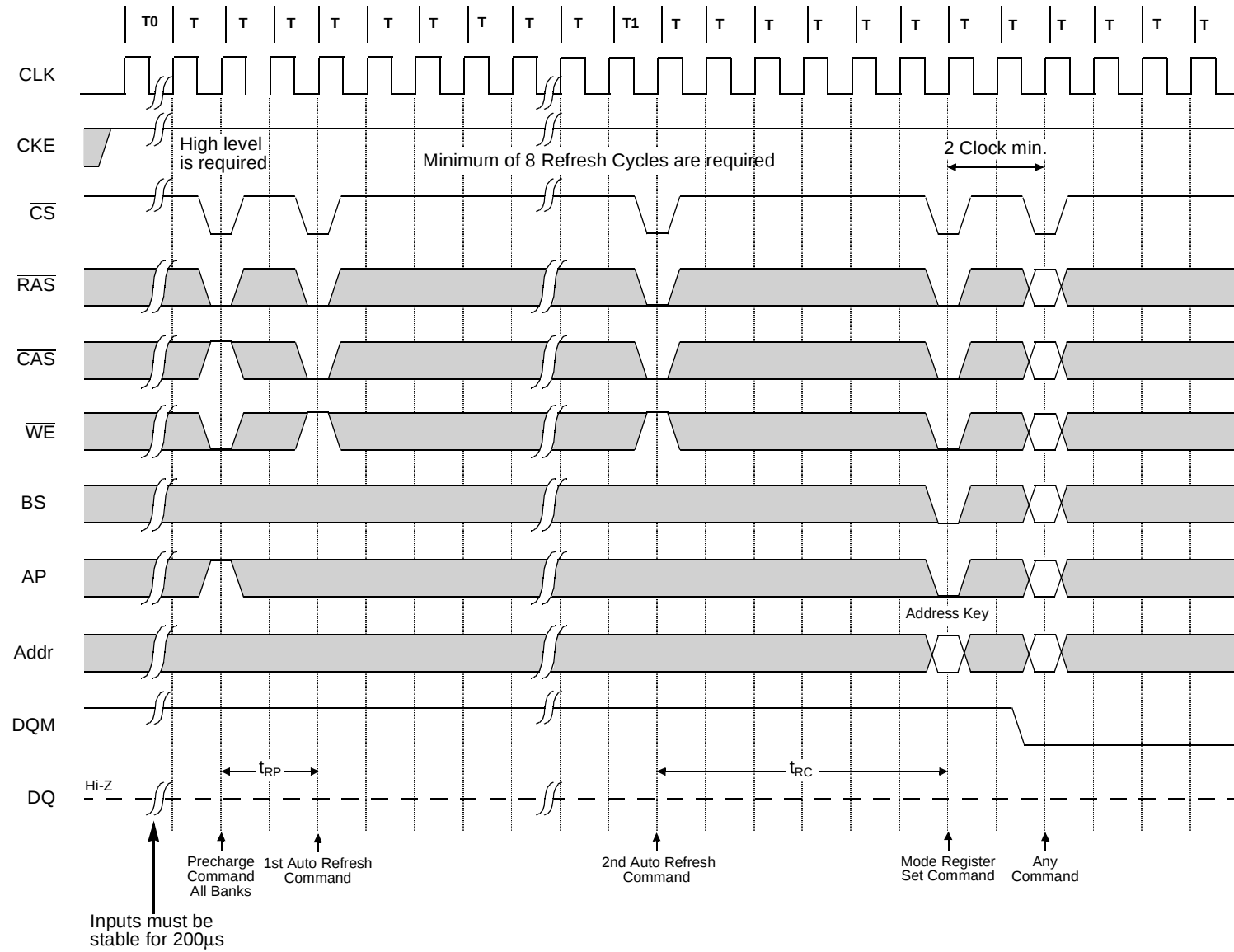
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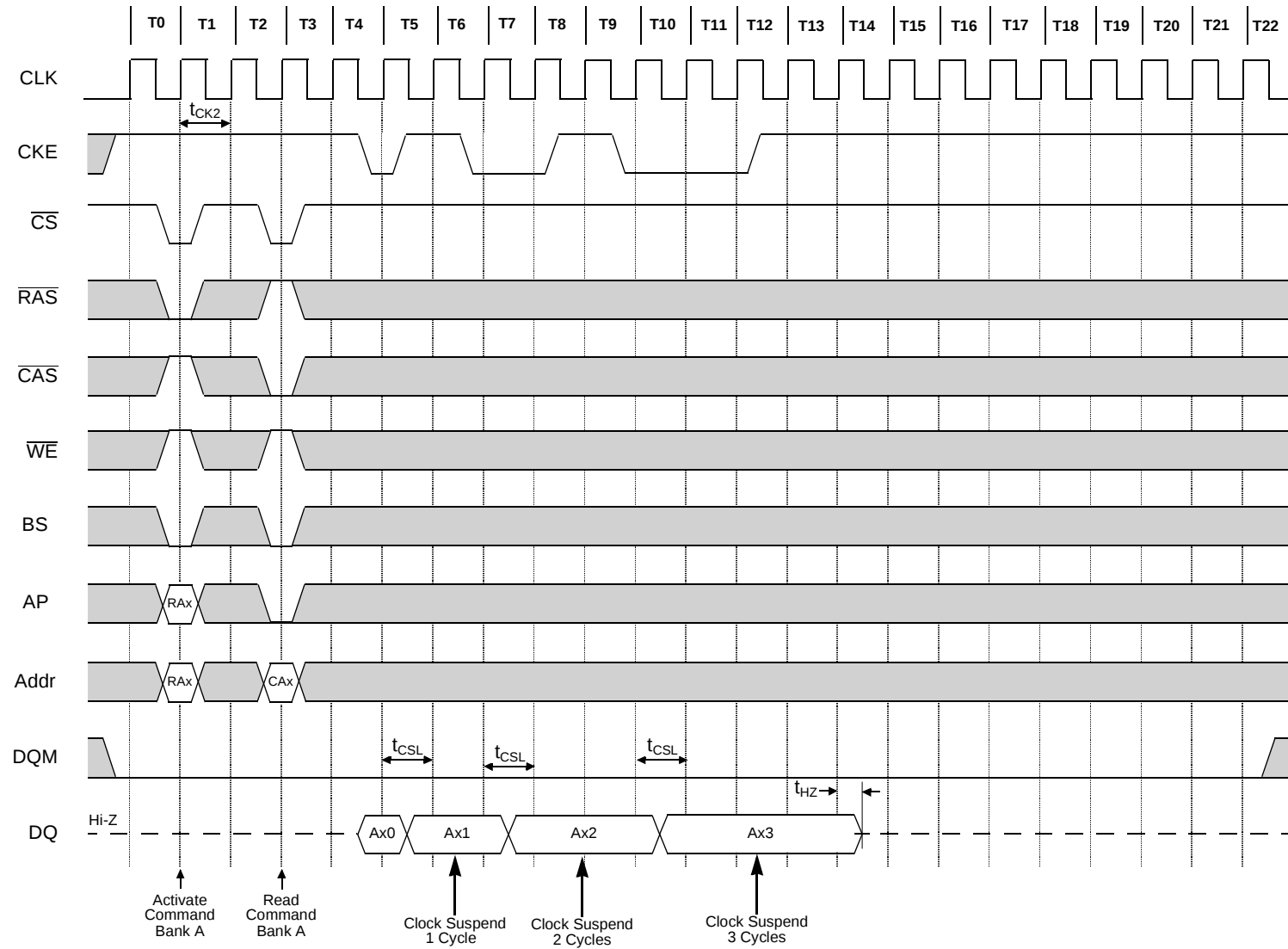
10. Mode Register Set

 $\overline{\text{CAS}}$ Latency = 2

11. Power on Sequence and Auto Refresh (CBR)

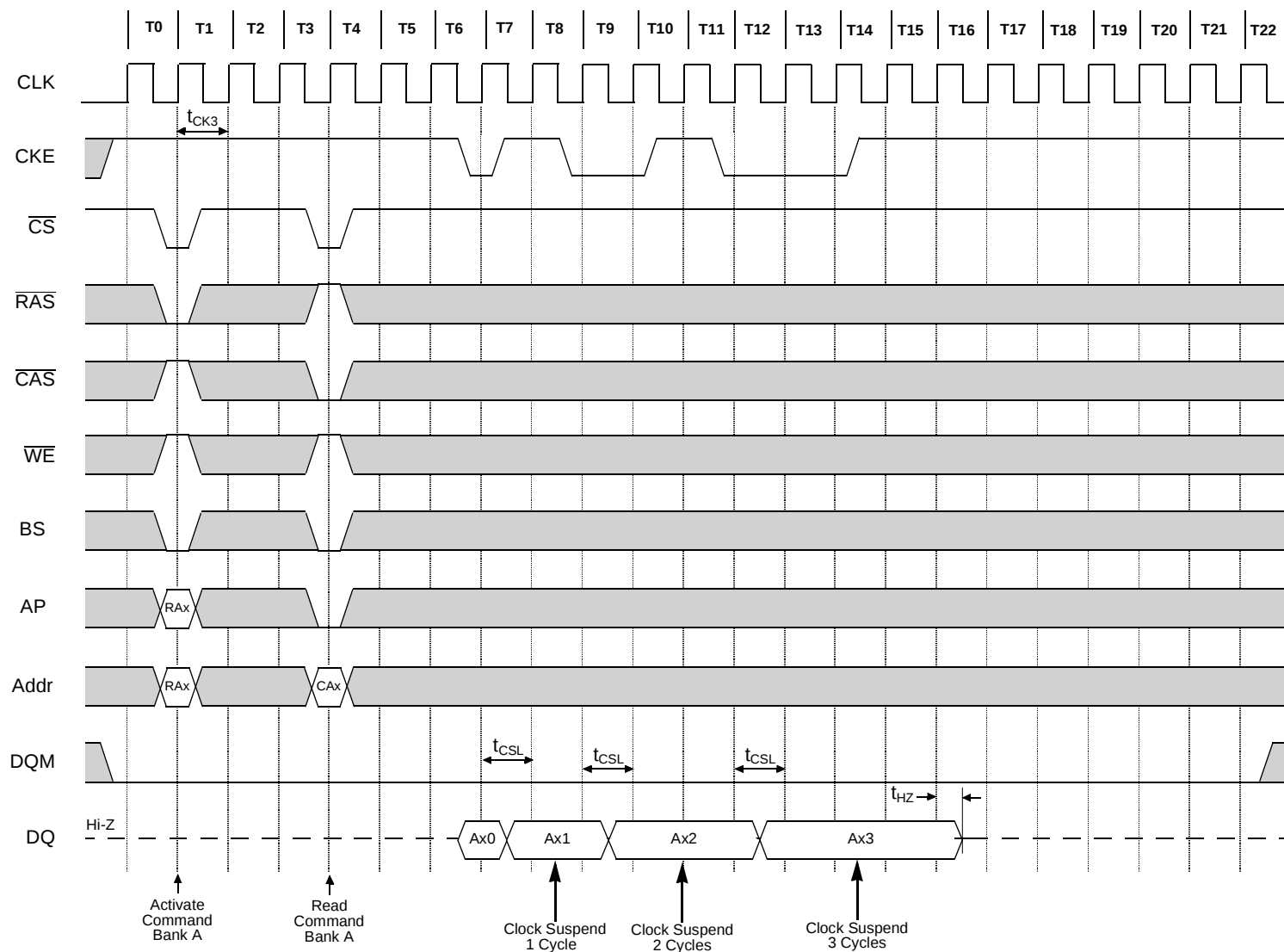


12.1 Clock Suspension During Burst Read (Using CKE)

Burst Length = 4, $\overline{\text{CAS}}$ Latency = 2

12.2 Clock Suspension During Burst Read (Using CKE)

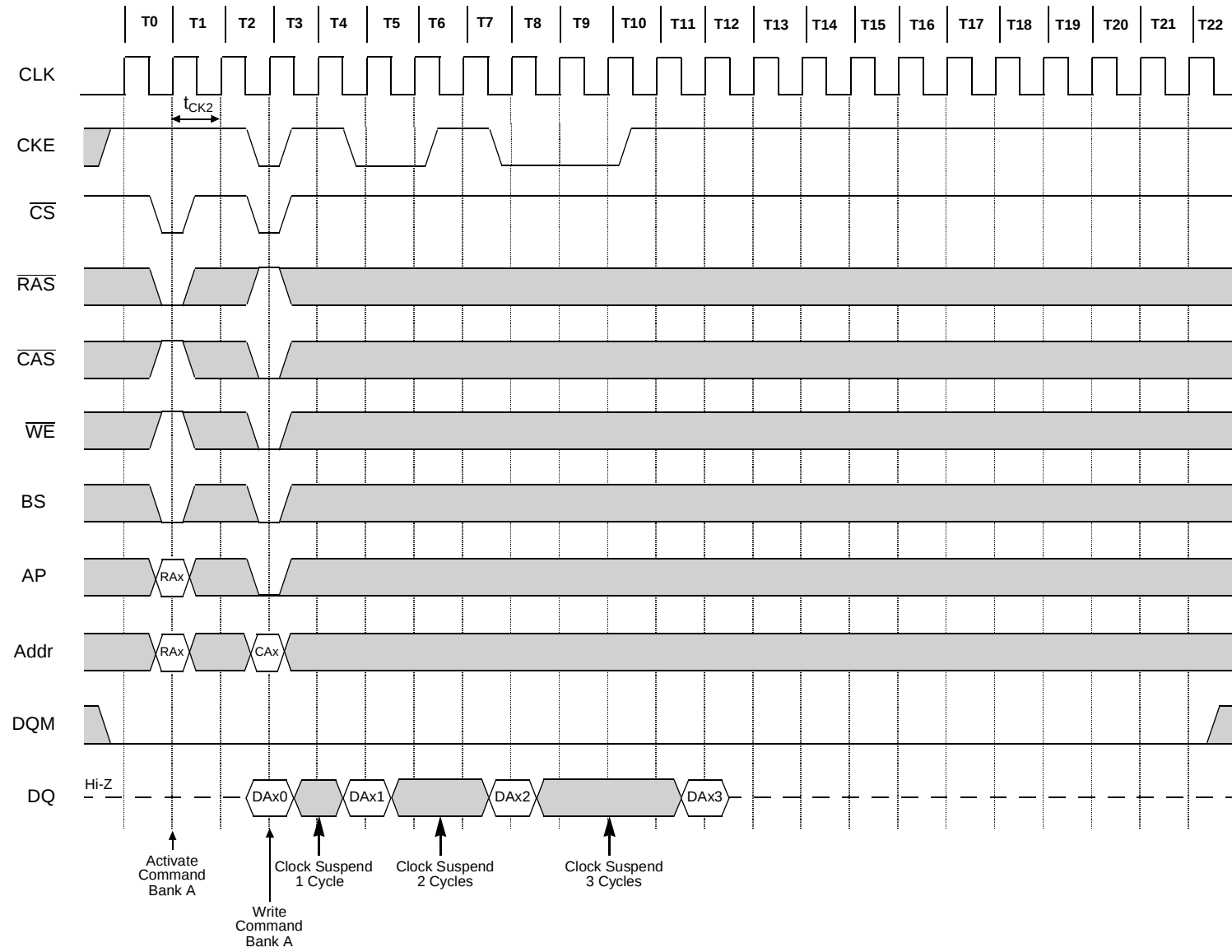
Burst Length = 4, $\overline{\text{CAS}}$ Latency = 3



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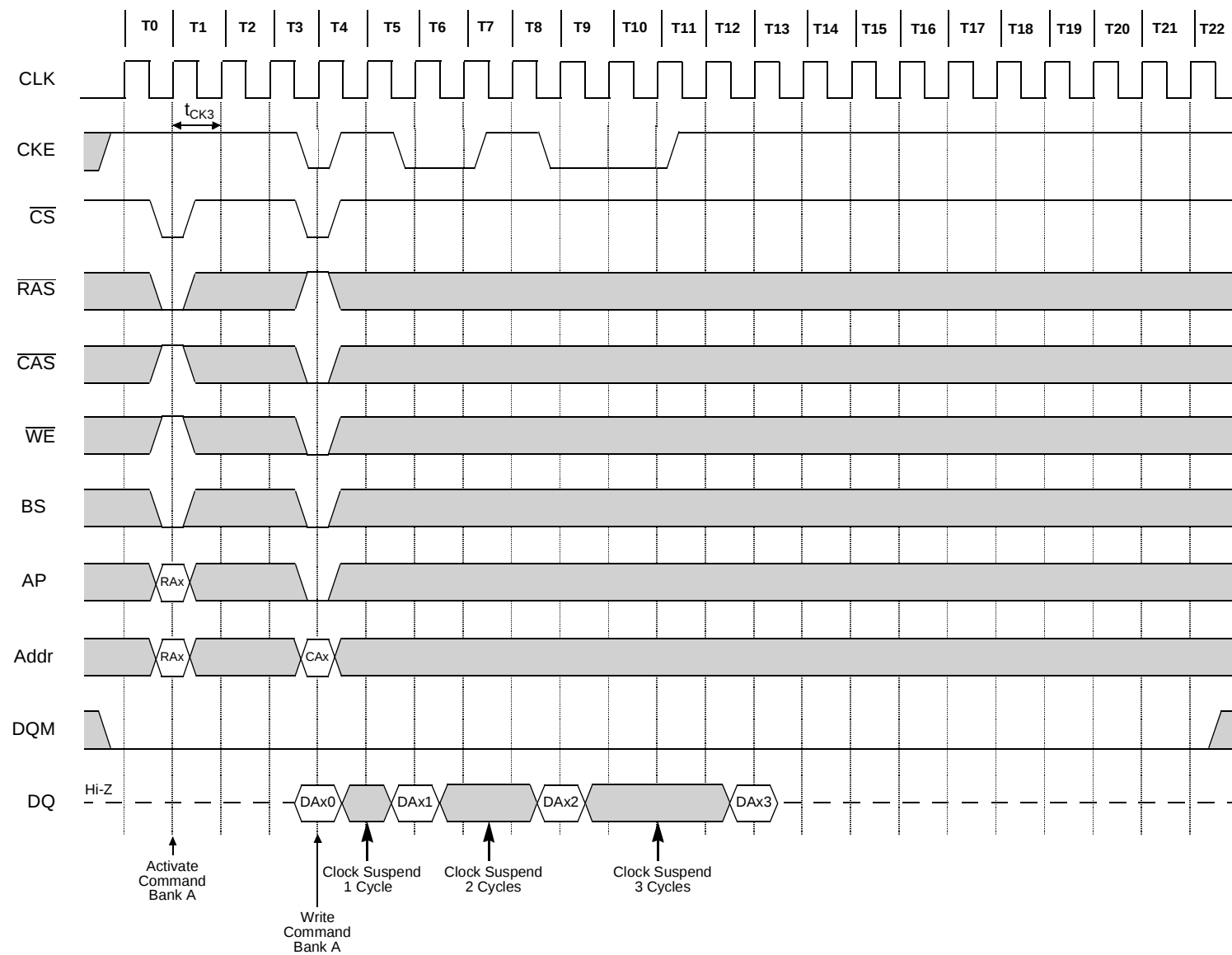
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12.3 Clock Suspension During Burst Write (Using CKE)

Burst Length = 4, $\overline{\text{CAS}}$ Latency = 2

12.4 Clock Suspension During Burst Write (Using CKE)

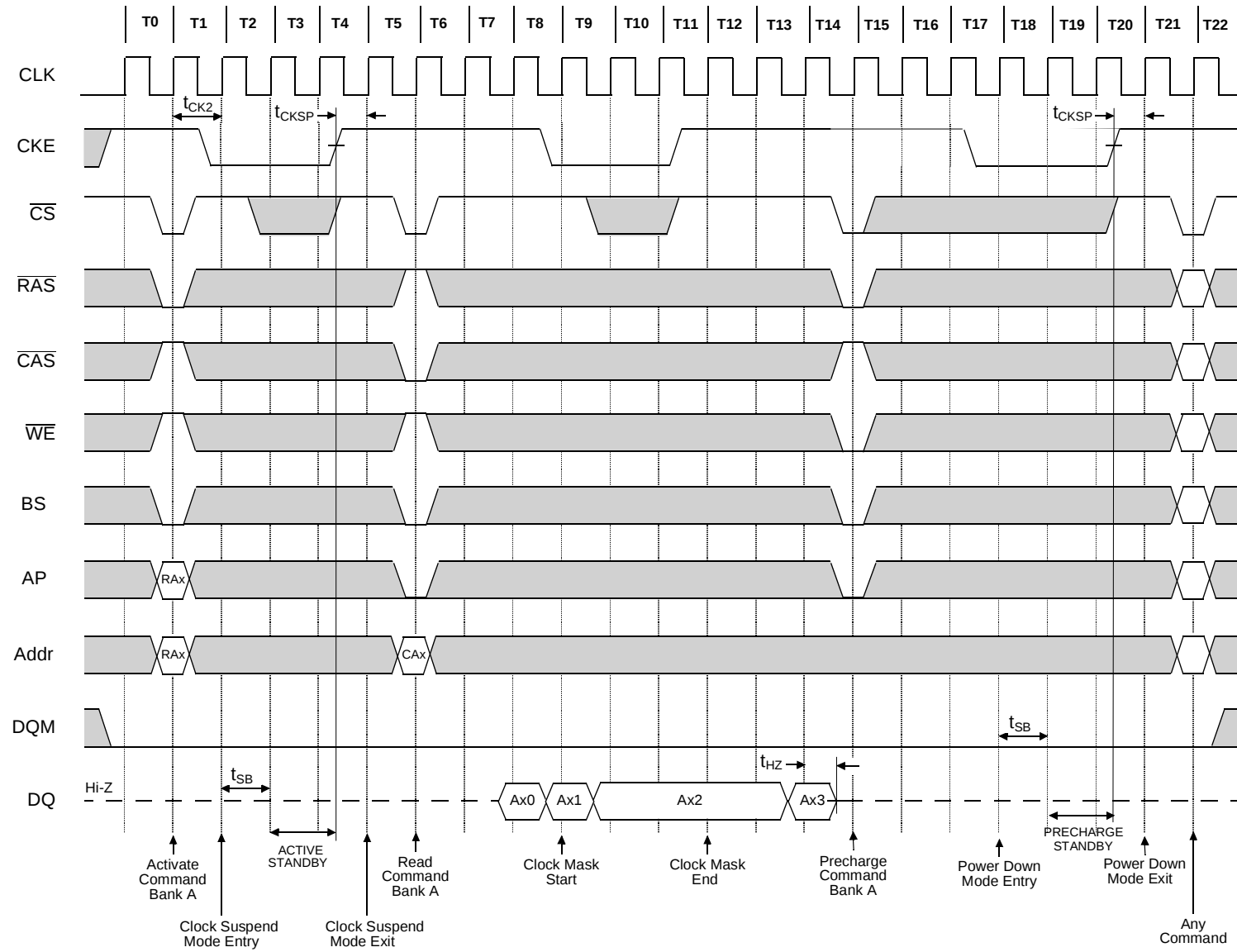
Burst Length = 4, $\overline{\text{CAS}}$ Latency = 3



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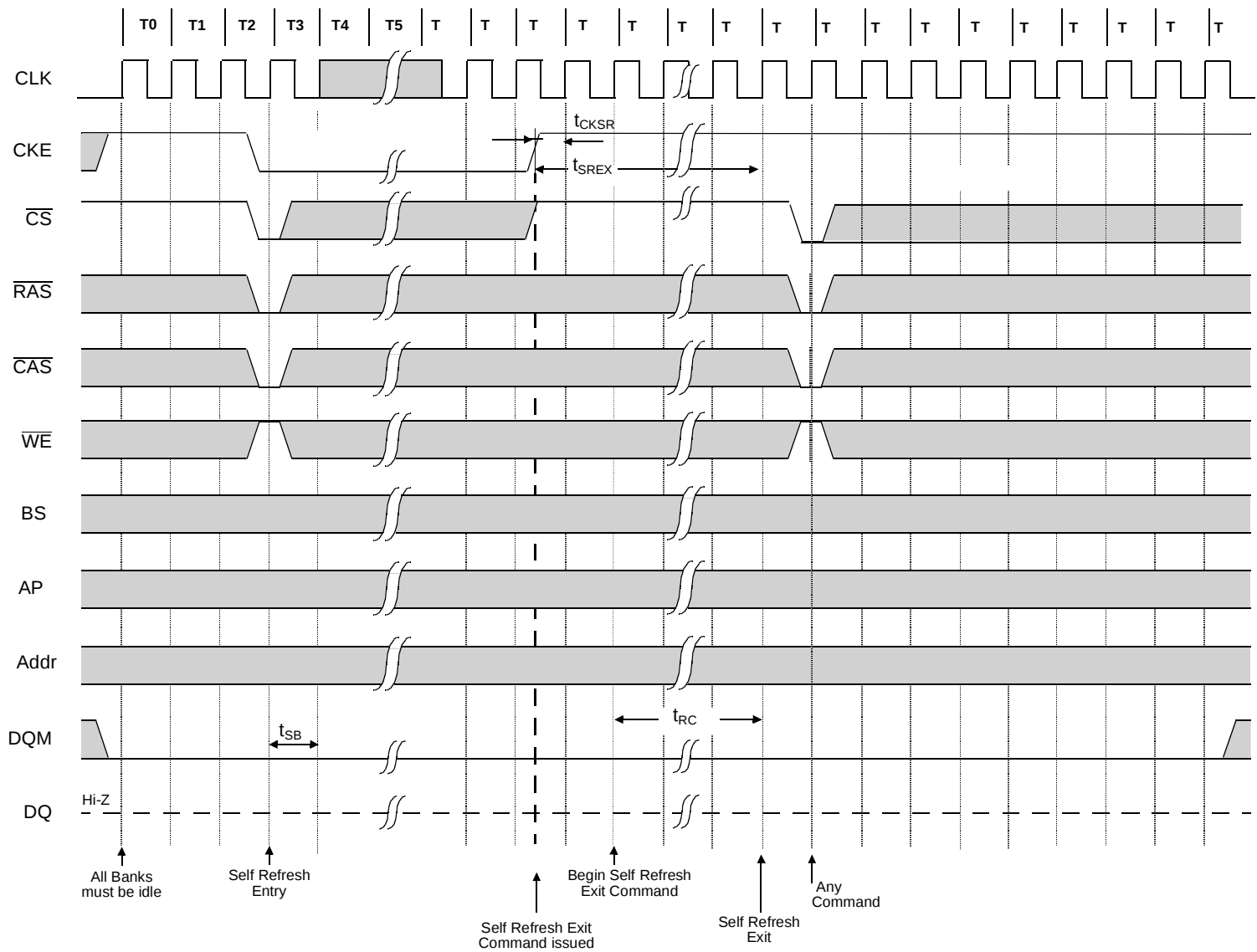
13. Power Down Mode and Clock Suspend

Burst Length = 4, $\overline{\text{CAS}}$ Latency = 2

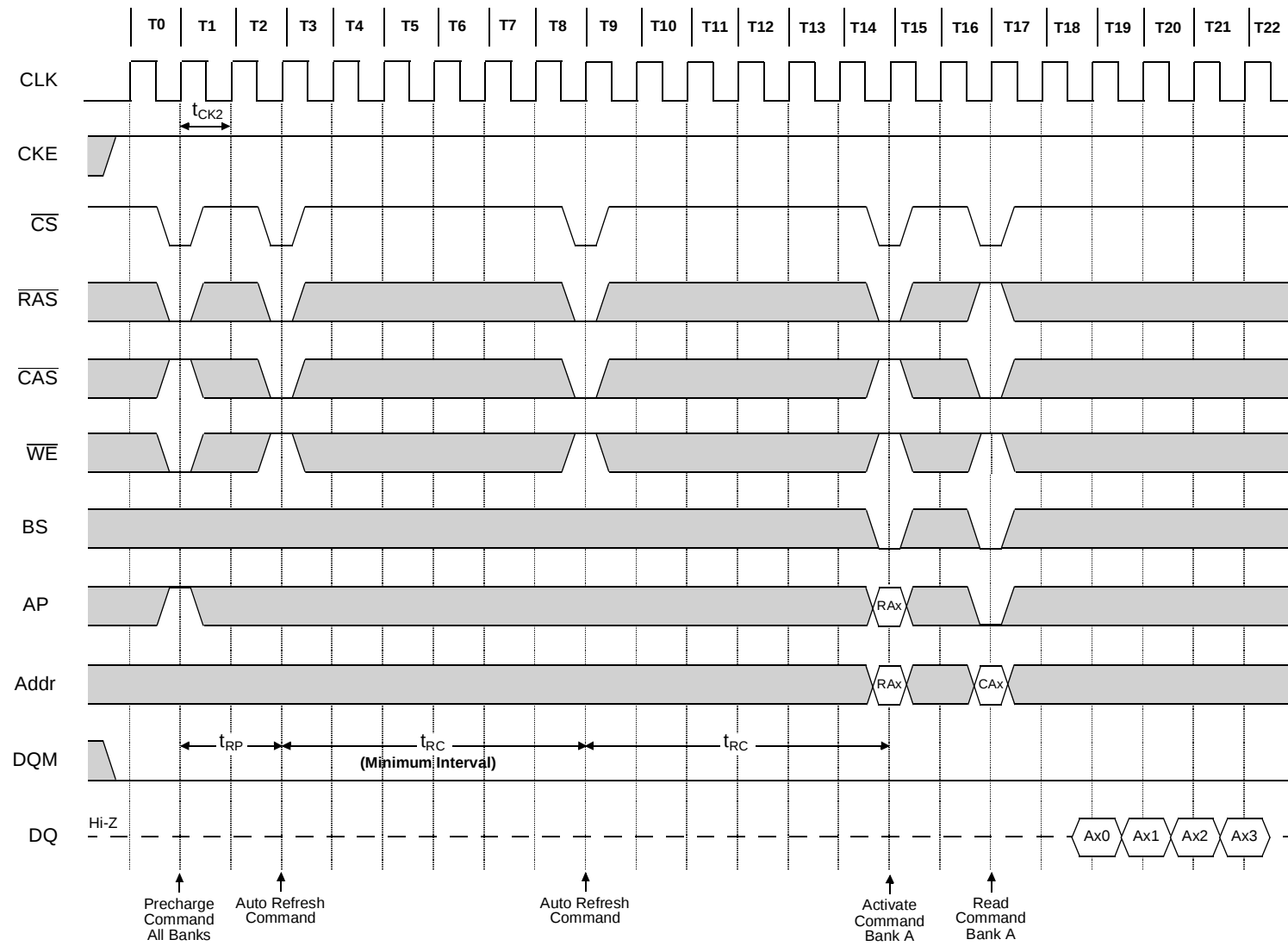
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15. Self Refresh (Entry and Exit)

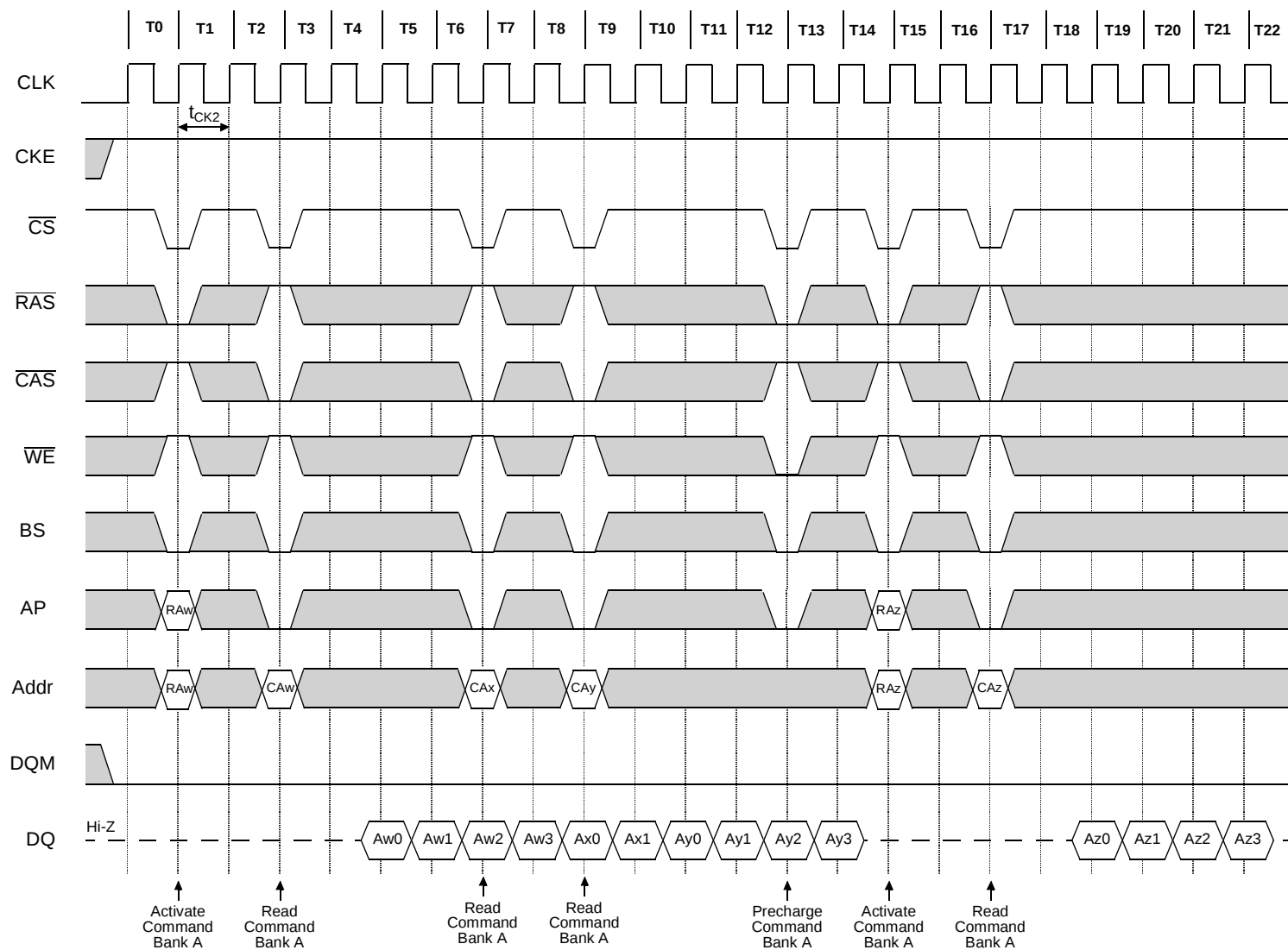


15. Auto Refresh (CBR)

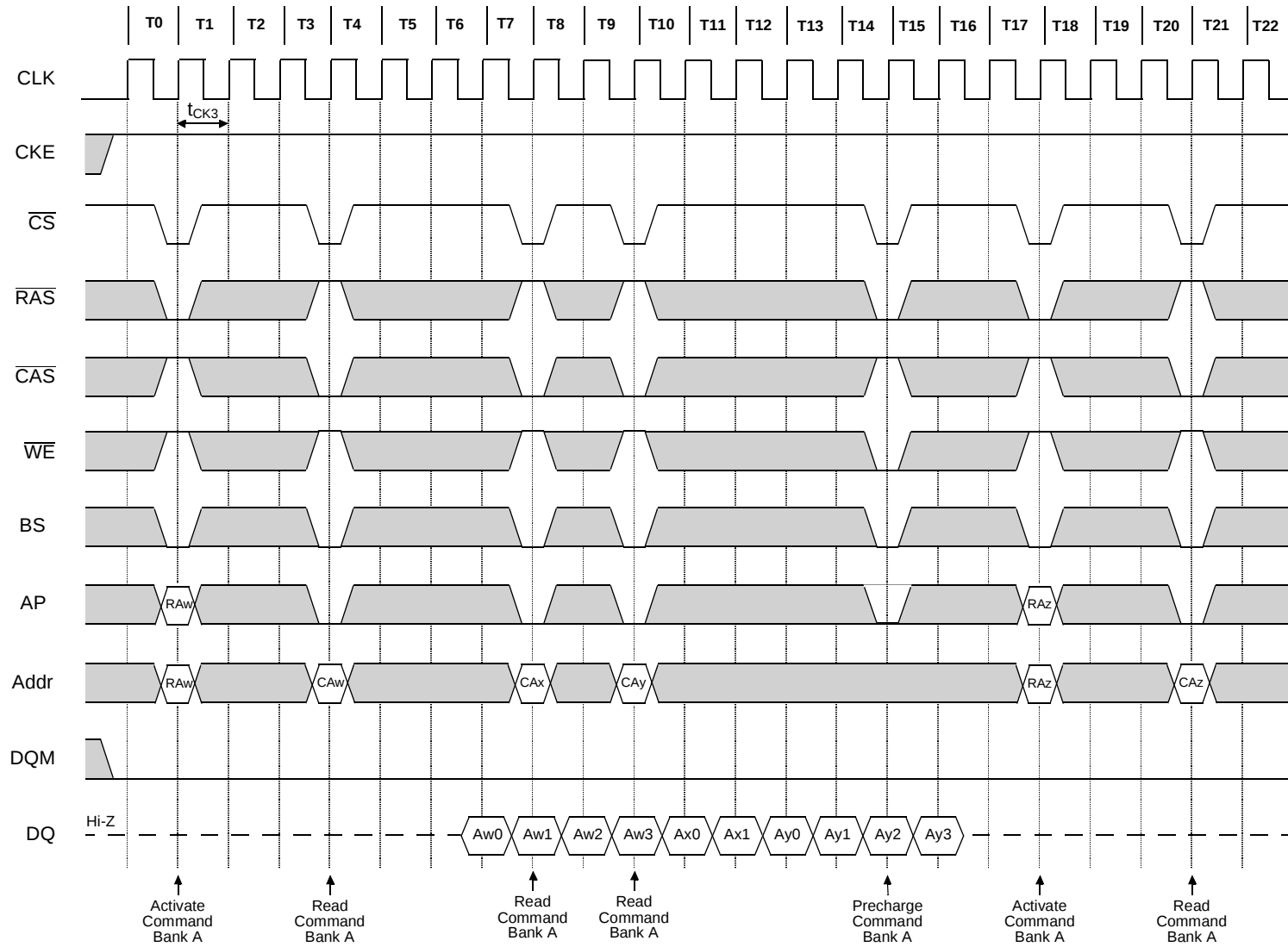
Burst Length = 4, $\overline{\text{CAS}}$ Latency = 2**SIEMENS****HYB39S6440x/80x/16xT
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16.1 Random Column Read (Page within same Bank)

Burst Length = 4, $\overline{\text{CAS}}$ Latency = 2

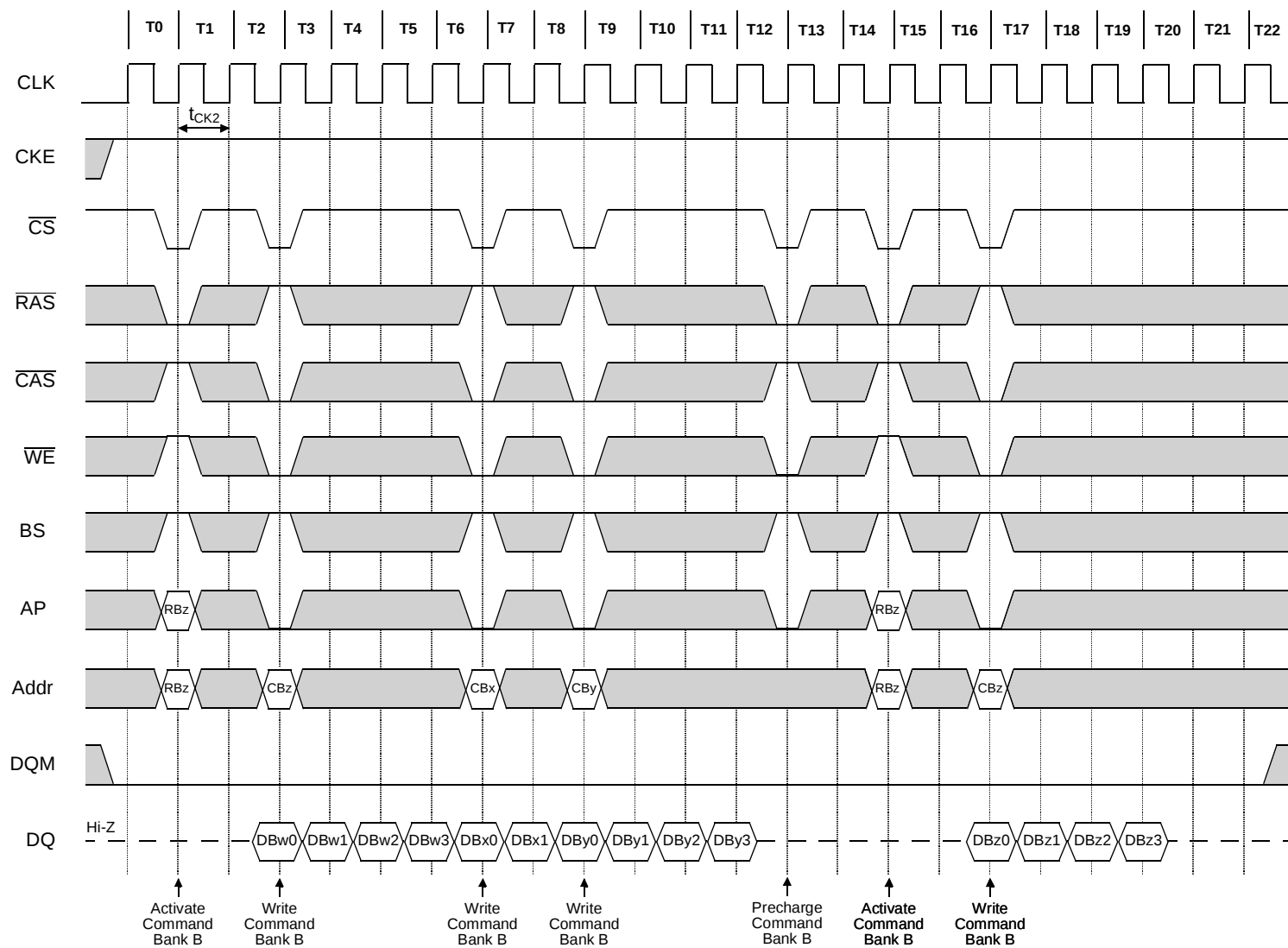


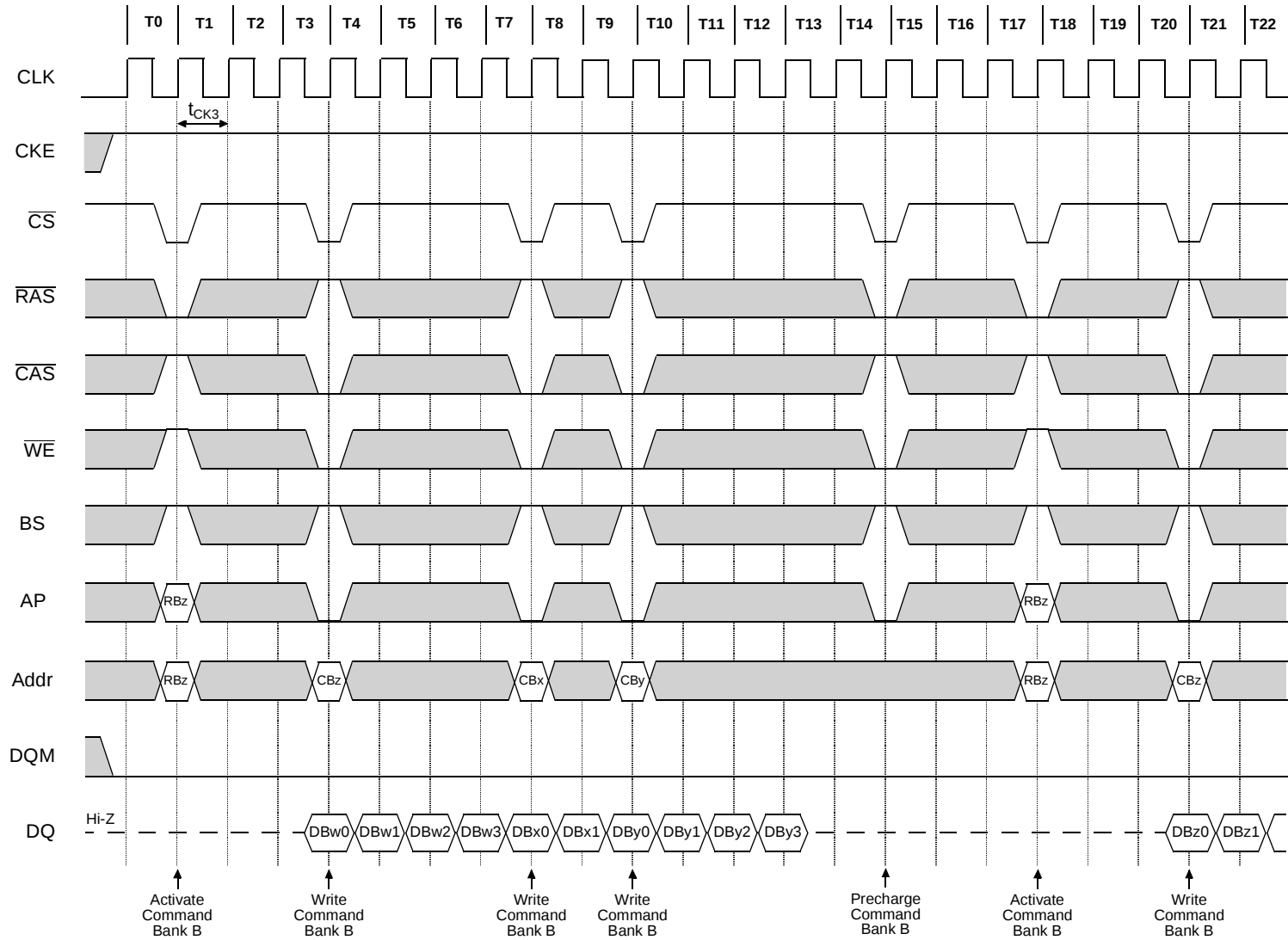
16.2 Random Column Read (Page within same Bank)

Burst Length = 4, $\overline{\text{CAS}}$ Latency = 3

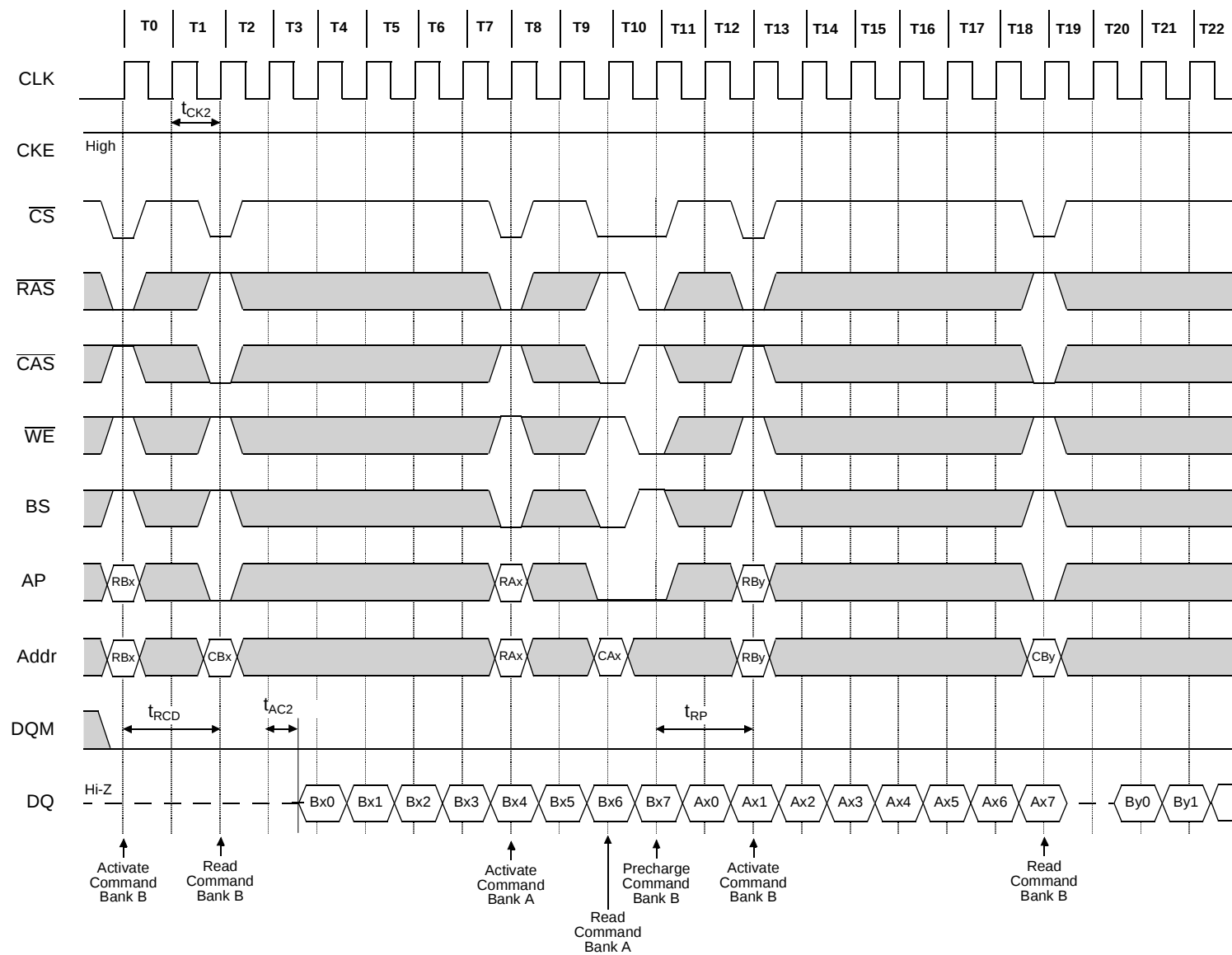
17.1 Random Column Write (Page within same Bank)

Burst Length = 4, $\overline{\text{CAS}}$ Latency = 2



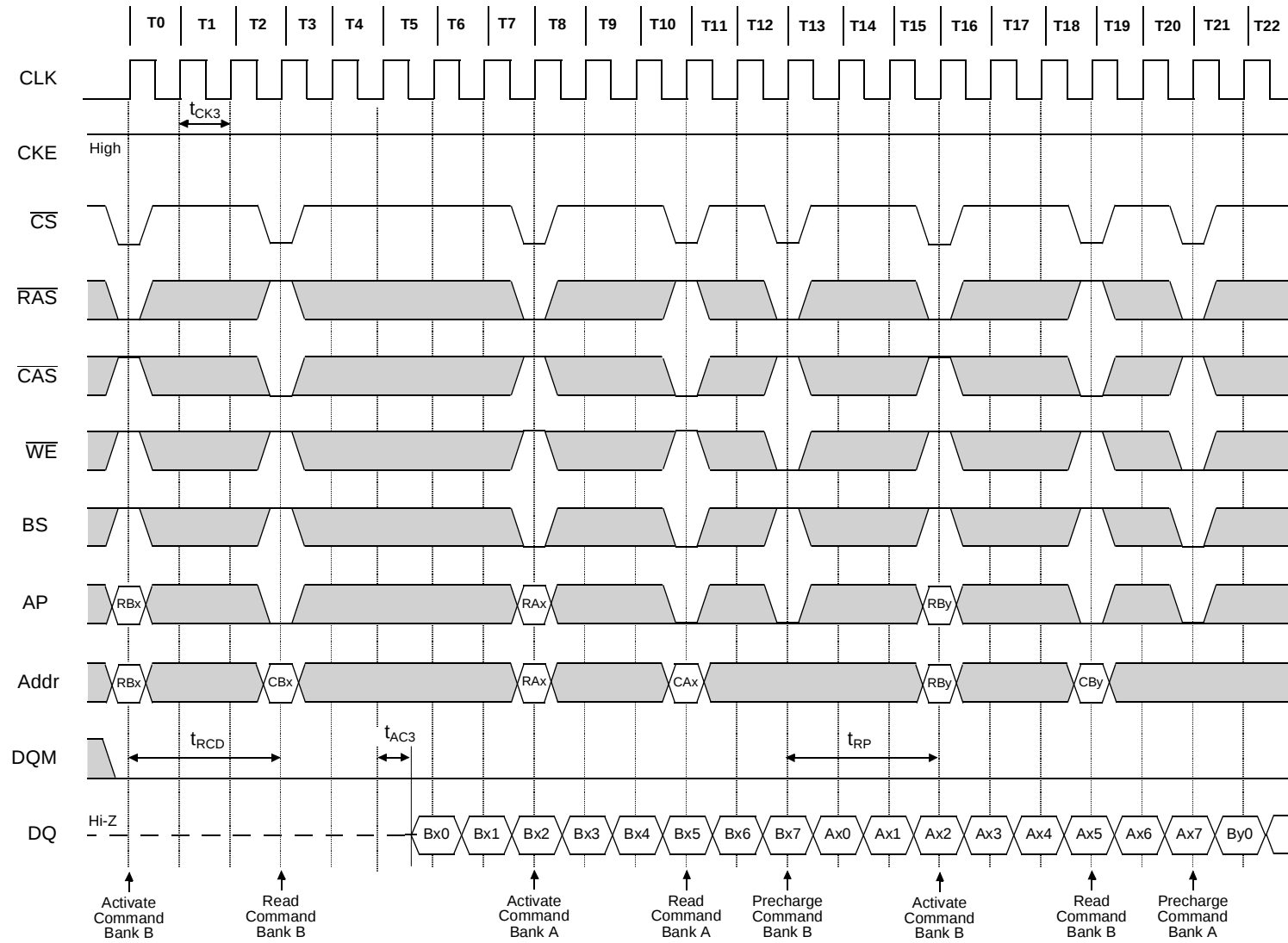
17.2 Random Column Write (Page within same Bank)Burst Length = 4, $\overline{\text{CAS}}$ Latency = 3

18.1 Random Row Read (Interleaving Banks) with Precharge

Burst Length = 8, $\overline{\text{CAS}}$ Latency = 2

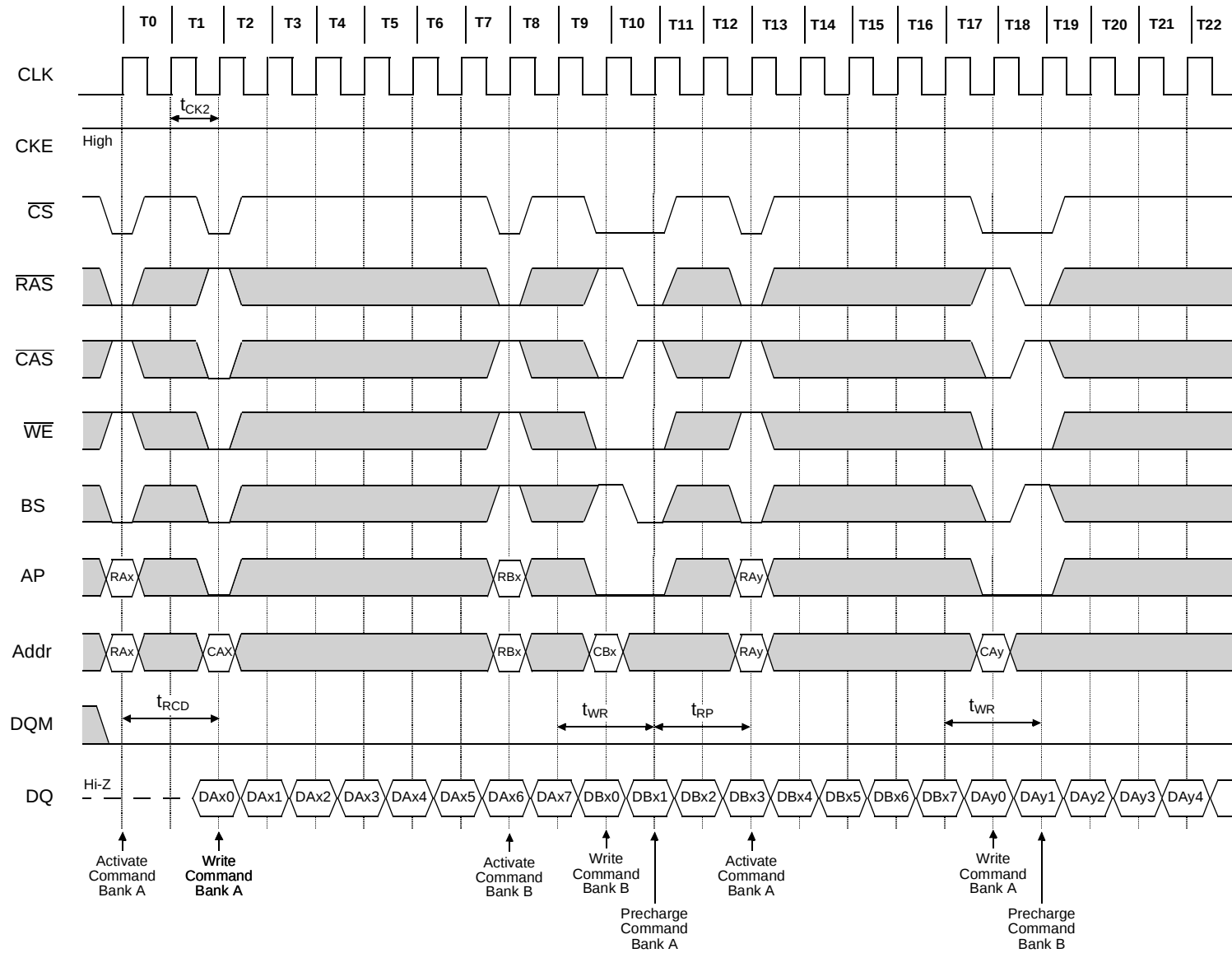
18.2 Random Row Read (Interleaving Banks) with Precharge

Burst Length = 8, $\overline{\text{CAS}}$ Latency = 3



19.1 Random Row Write (Interleaving Banks) with Precharge

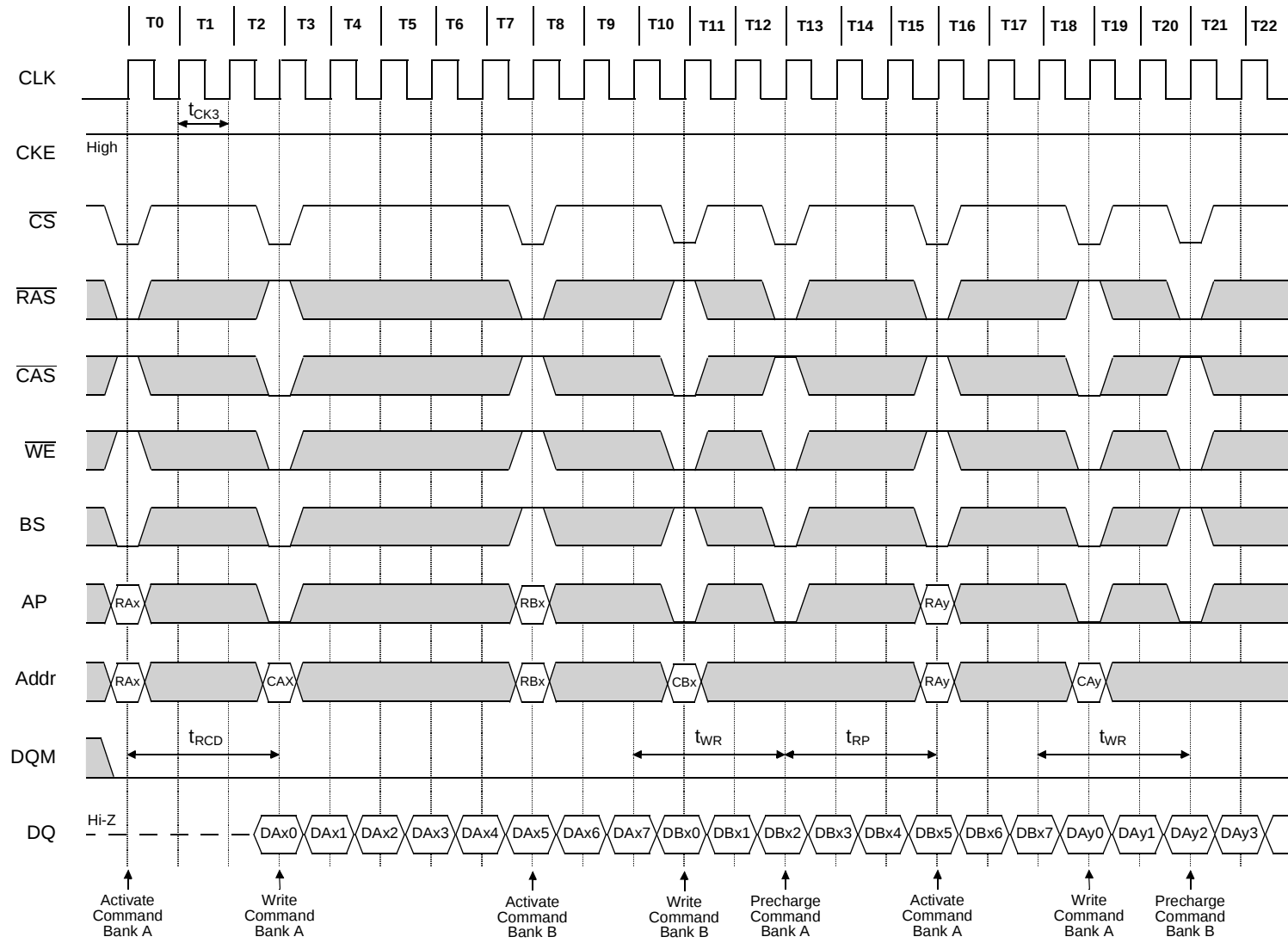
Burst Length = 8, $\overline{\text{CAS}}$ Latency = 2



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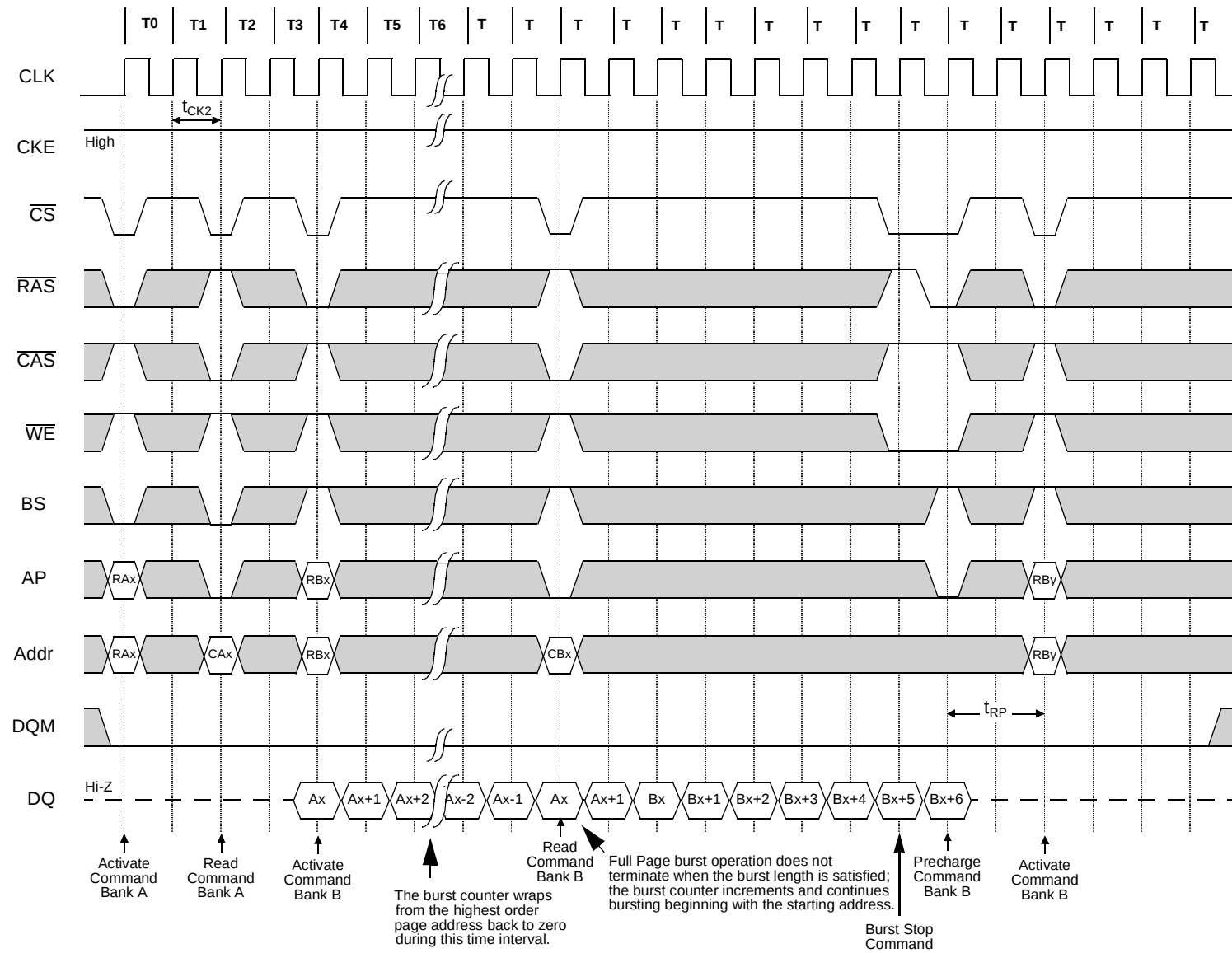
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19.2 Random Row Write (Interleaving Banks) with Precharge

Burst Length = 8, $\overline{\text{CAS}}$ Latency = 3

20.1 Full Page Read Cycle

Burst Length = Full Page, $\overline{\text{CAS}}$ Latency = 2

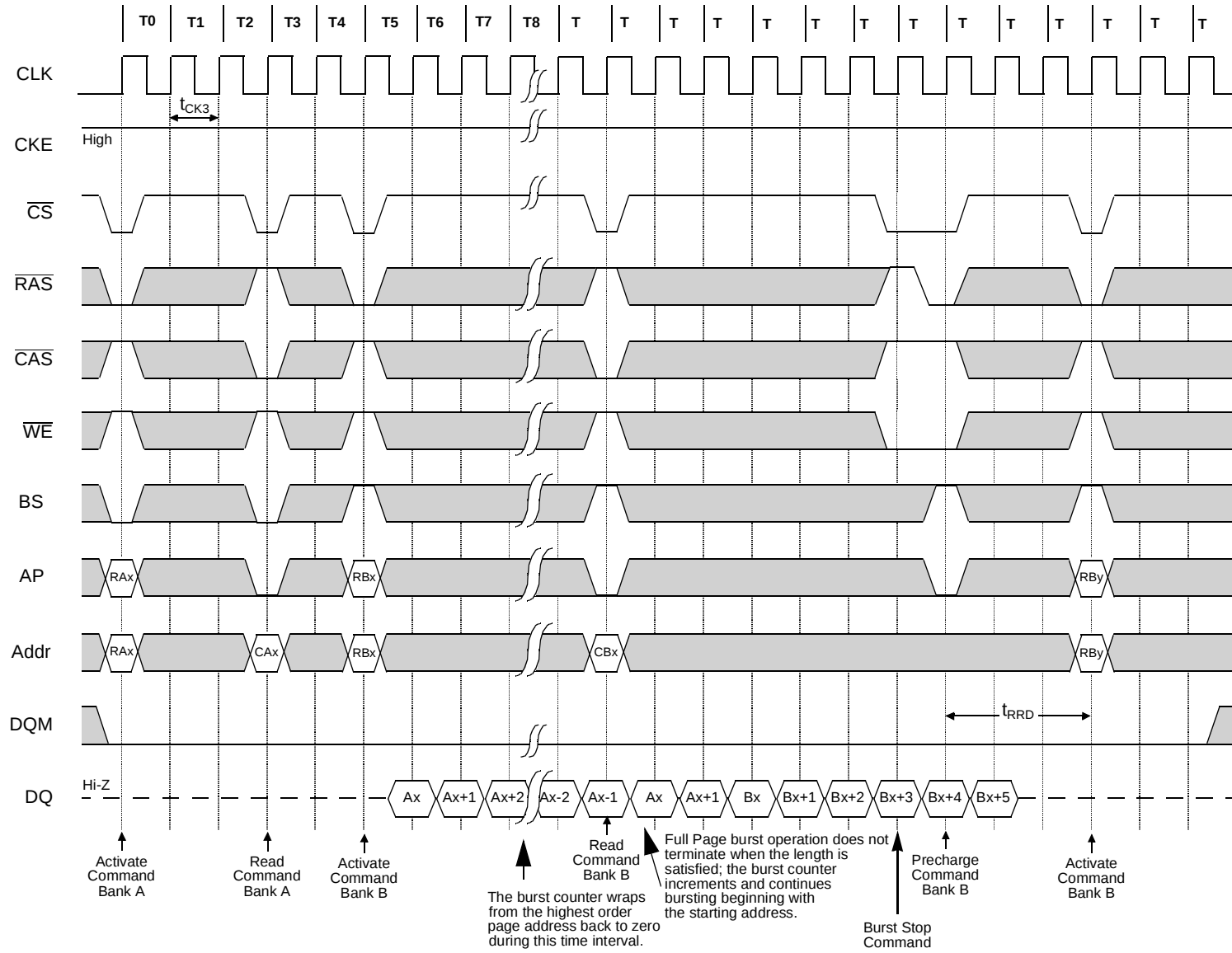


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20.2 Full Page Read Cycle

Burst Length = Full Page, $\overline{\text{CAS}}$ Latency = 3

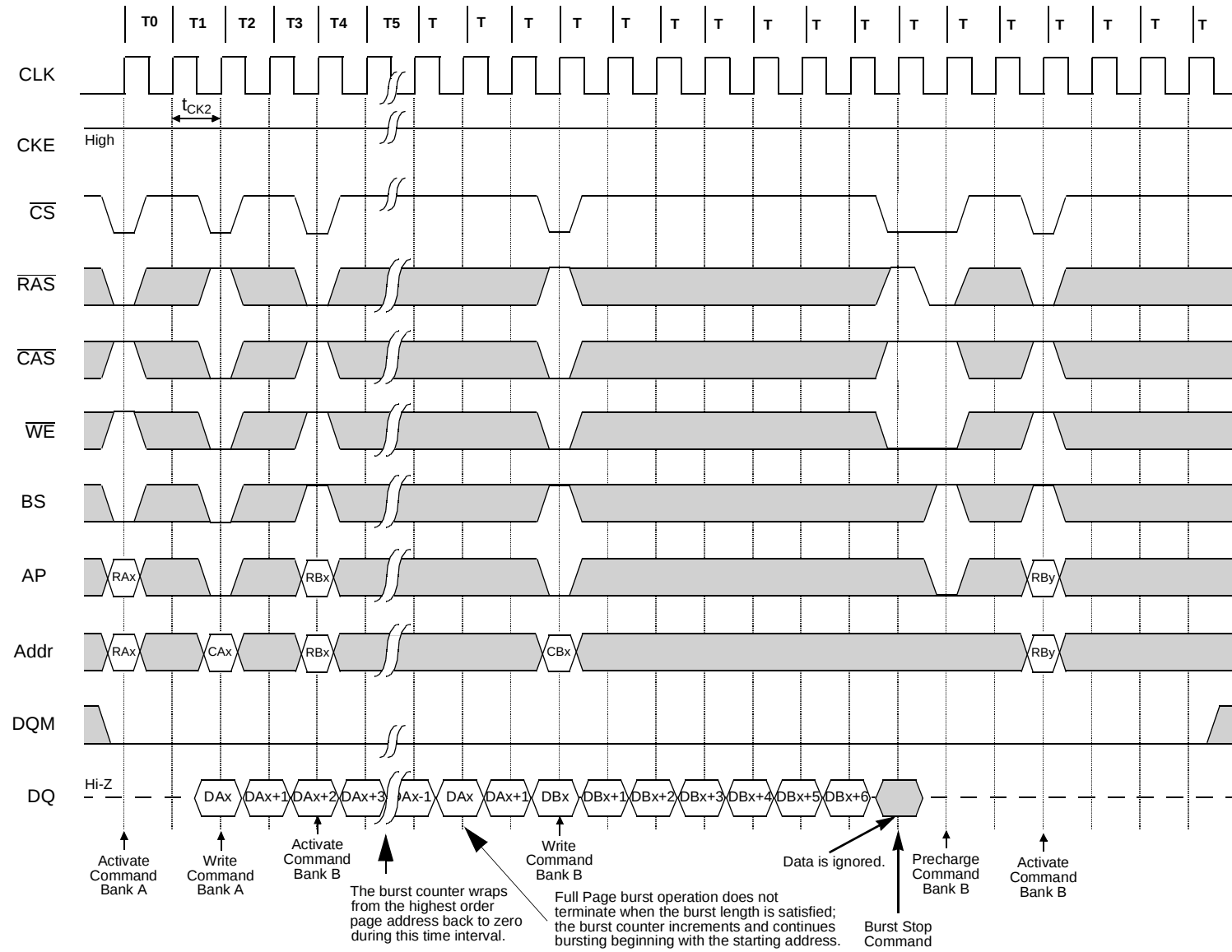


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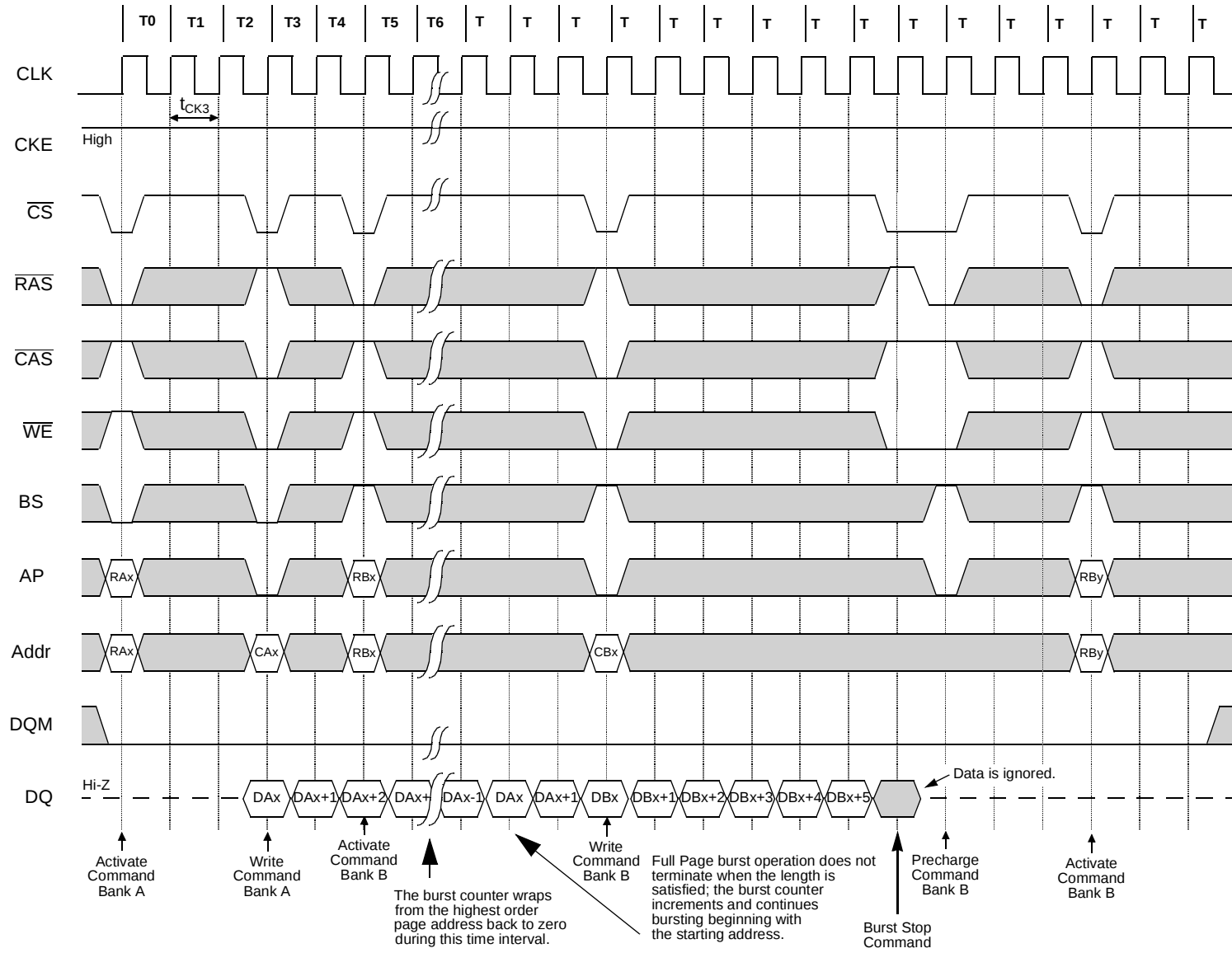
21.1 Full Page Write Cycle

Burst Length = Full Page, $\overline{\text{CAS}}$ Latency = 2



21.2 Full Page Write Cycle

Burst Length = Full Page, $\overline{\text{CAS}}$ Latency = 3



Burst Length = 8 or Full Page, $\overline{\text{CAS}}$ Latency = 2