16 MBit Synchronous DRAM (second generation)

Advanced Information

- High Performance:

$\overline{\text{CAS}}$ latency = 3	-8	-10	Units
fCK	125	100	MHz
tCK3	8	10	ns
tAC3	7	8	ns

- Single Pulsed $\overline{\text{RAS}}$ Interface
- Fully Synchronous to Positive Clock Edge
- 0 to 70 °C operating temperature
- Dual Banks controlled by A11 (Bank Select)
- Programmable $\overline{\text{CAS}}$ Latency : 1, 2, 3
- Programmable Wrap Sequence : Sequential or Interleave
- Programmable Burst Length:
  1, 2, 4, 8 and full page for Sequential type
  1, 2, 4, 8 for Interleave Type
- Multiple Burst Read with Single Write Operation
- Automatic and Controlled Precharge Command
- Data Mask for Read / Write control (x4, x8)
- Dual Data Mask for byte control (x16)
- Auto Refresh (CBR) and Self Refresh
- Suspend Mode and Power Down Mode
- 4096 refresh cycles / 64 ms
- Random Column Address every CLK (1-N Rule)
- Single 3.3V +/- 0.3V Power Supply
- LVTTL and SSTL_3 (Class II) Interface versions
- Plastic Packages:
  P-TSOPI-44 400mil width (x4, x8)
  P-TSOPII -50 400 mil width (x 16)

The HYB39S1640x/80x/16xAT are dual bank Synchronous DRAMs based on the die revisions „B“ and „C“ and organized as 2 banks x 2MBit x4, 2 banks x 1MBit x8 and 2 banks x 512kbit x16 respectively. These synchronous devices achieve high speed data transfer rates up to 125 MHz by employing a chip architecture that prefetches multiple bits and then synchronizes the output data to a system clock. The chip is fabricated with SIEMENS' advanced 16MBit DRAM process technology.

The device is designed to comply with all JEDEC standards set for synchronous DRAM products, both electrically and mechanically. All of the control, address, data input and output circuits are synchronized with the positive edge of an externally supplied clock.

Operating the two memory banks in an interleaved fashion allows random access operation to occur at higher rate than is possible with standard DRAMs. A sequential and gapless data rate of up to 125 MHz is possible depending on burst length, $\overline{\text{CAS}}$ latency and speed grade of the device.

Auto Refresh (CBR) and Self Refresh operation are supported. These devices operate with a single 3.3V +/- 0.3V power supply and are available in TSOPII packages.

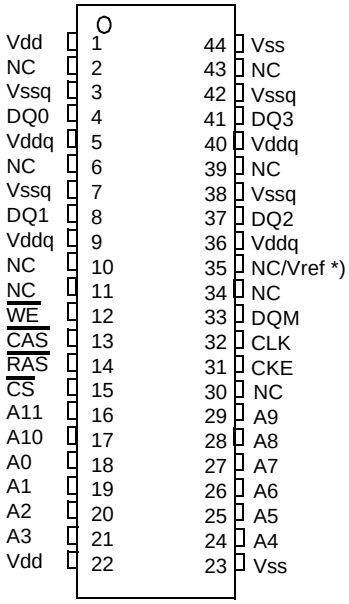
These Synchronous DRAM devices are available with either LV-TTL or SSTL-3 interfaces.

Ordering Information

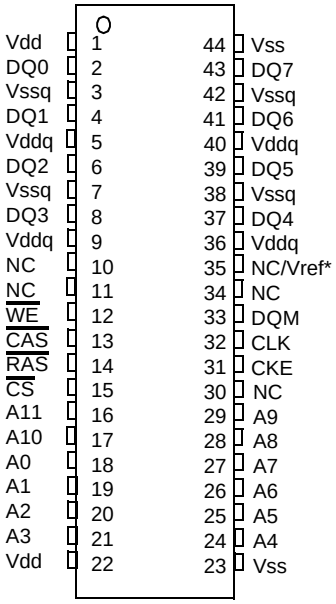
Type	Ordering Code	Package	Description
LVTTL-version:			
HYB 39S16400AT-8	Q67100-Q1333	P-TSOPII-44 (400mil)	125MHz 2B x 2M x 4 SDRAM
HYB 39S16400AT-10	Q67100-Q1323	P-TSOPII-44-(400mil)	100MHz 2B x 2M x 4 SDRAM
HYB 39S16800AT-8	Q67100-Q1335	P-TSOPII-44-(400mil)	125MHz 2B x 1M x 8 SDRAM
HYB 39S16800AT-10	Q67100-Q1327	P-TSOPII-44 (400mil)	100MHz 2B x 1M x 8 SDRAM
HYB 39S16160AT-8	Q67100-Q1337	P-TSOPII-50 (400mil)	125MHz 2B x 512k x 16 SDRAM
HYB 39S16160AT-10	Q67100-Q1331	P-TSOPII-50-(400mil)	100MHz 2B x 512k x 16 SDRAM
SSTL (Class II) -version:			
HYB 39S16402T-8	Q67100-Q1277	P-TSOPII-44 (400mil)	125MHz 2B x 2M x 4 SDRAM
HYB 39S16402AT-10	Q67100-Q1283	P-TSOPII-44 (400mil)	100MHz 2B x 2M x 4 SDRAM
HYB 39S16802AT-8	Q67100-Q1279	P-TSOPII-44 (400mil)	125MHz 2B x 1M x 8 SDRAM
HYB 39S16802AT-10	Q67100-Q1284	P-TSOPII-44 (400mil)	100MHz 2B x 1M x 8 SDRAM
HYB 39S16162AT-8	Q67100-Q1280	P-TSOPII-50 (400mil)	125MHz 2B x 512k x 16 SDRAM
HYB 39S16162AT-10	Q67100-Q1286	P-TSOPII-50 (400mil)	100MHz 2B x 512k x 16 SDRAM

Pin Description and Pinouts:

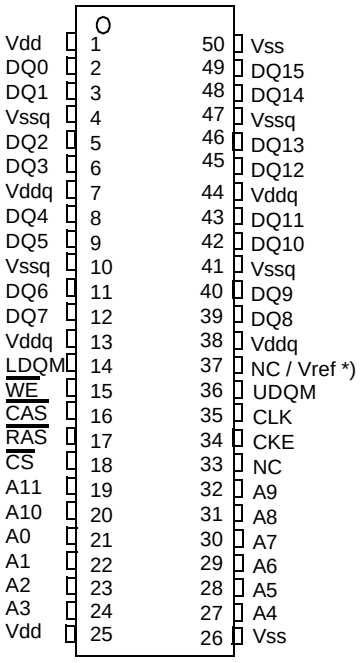
CLK	Clock Input	**DQ**	Data Input /Output
CKE	Clock Enable	**DQM, LDQM, UDQM**	Data Mask
$\overline{\text{CS}}$	Chip Select	**Vdd**	Power (+3.3V)
$\overline{\text{RAS}}$	Row Address Strobe	**Vss**	Ground
$\overline{\text{CAS}}$	Column Address Strobe	**Vddq**	Power for DQ's (+ 3.3V)
$\overline{\text{WE}}$	Write Enable	**Vssq**	Ground for DQ's
A0-A10	Address Inputs	**NC**	not connected
A11 (BS)	Bank Select	**Vref**	Reference Voltage (SSTL version only)



HYB39S16400AT / HYB39S16402AT
2 Bank x 2MBit x 4
TSOPII-44
(400 mil x 725 mil)



HYB39S16800AT / HYB39S16802AT
2 Bank x 1MBit x 8
TSOPII-44
(400 mil x 725 mil)

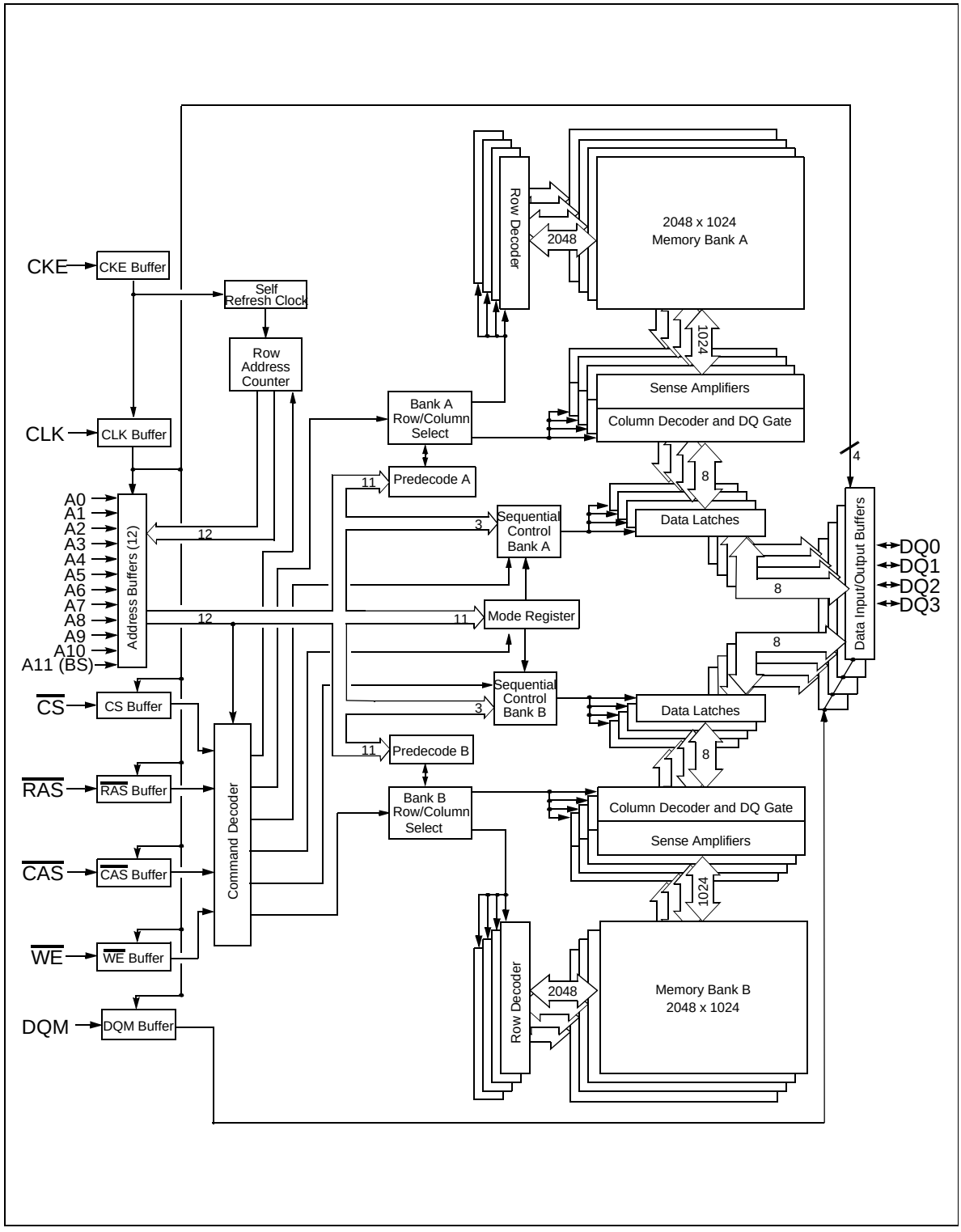


HYB39S16160AT / HYB39S16162AT
2 Bank x 512kbit x 16
TSOPII-50
(400 mil x 825 mil)

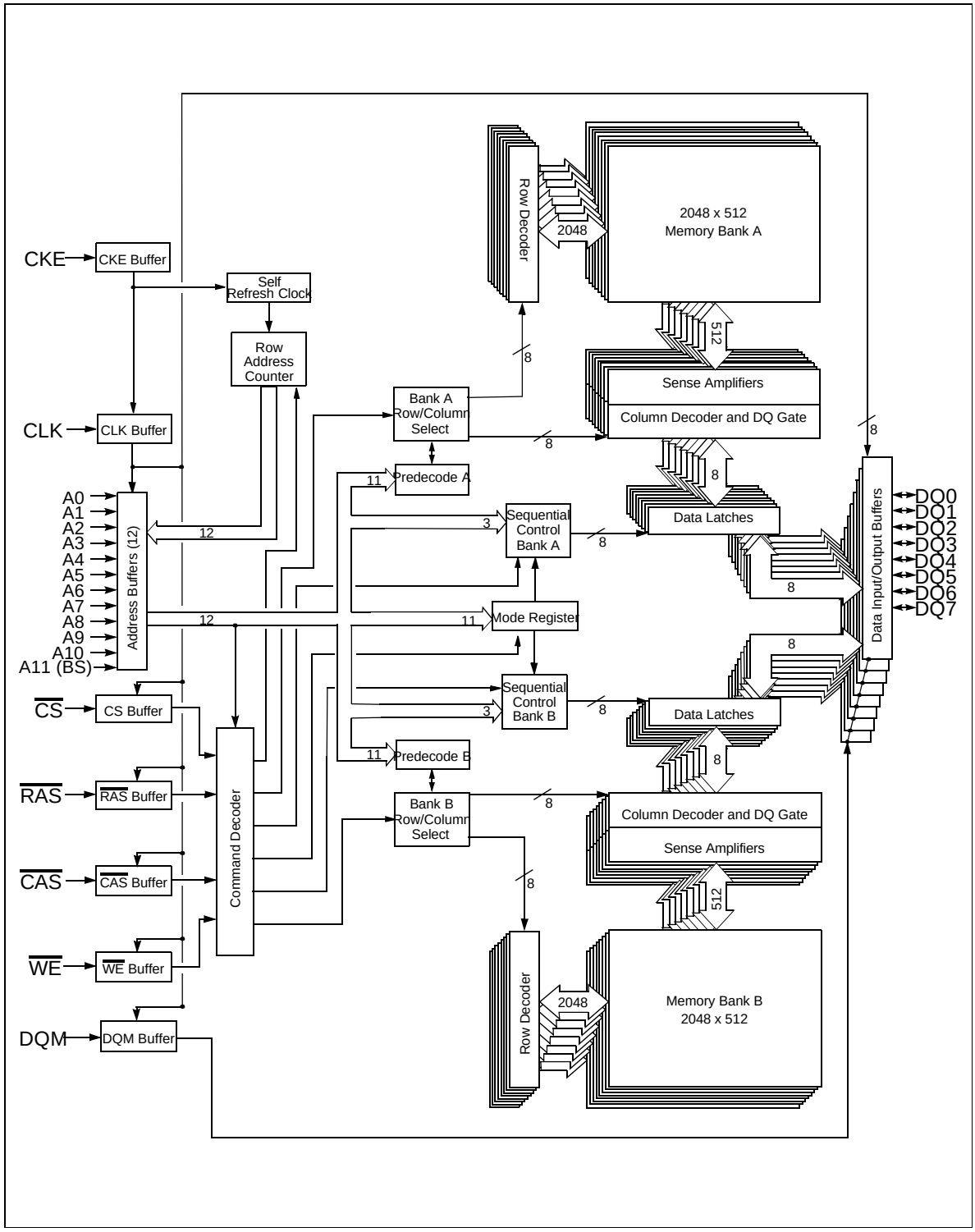
***) This pin is NC for the LV-TTL versions and Vref for the SSTL versions**

Signal Pin Description

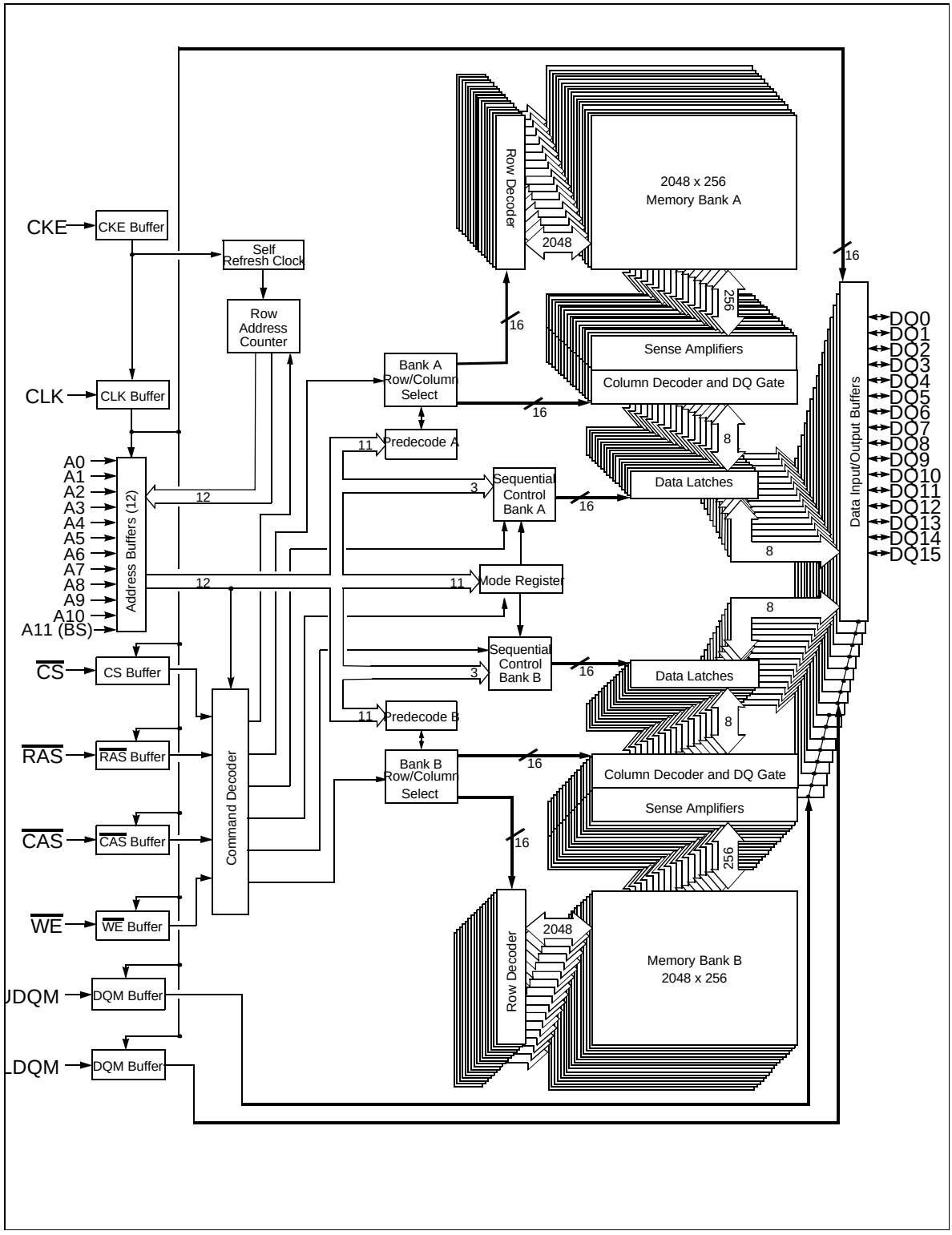
Pin	Type	Signal	Polarity	Function
CLK	Input	Pulse	Positive Edge	The system clock input. All of the SDRAM inputs are sampled on the rising edge of the clock.
CKE	Input	Level	Active High	Activates the CLK signal when high and deactivates the CLK signal when low, thereby inititiates either the Power Down mode, Suspend mode or the Self Refresh mode.
$\overline{CS}$	Input	Pulse	Active Low	$\overline{CS}$ enables the command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
$\overline{RAS}$, $\overline{CAS}$ $\overline{WE}$	Input	Pulse	Active Low	When sampled at the positive rising edge of the clock, $\overline{CAS}$, $\overline{RAS}$, and $\overline{WE}$ define the command to be executed by the SDRAM.
A0 - A10	Input	Level	—	During a Bank Activate command cycle, A0-A10 defines the row address (RA0-RA10) when sampled at the rising clock edge. During a Read or Write command cycle, A0-A9 defines the column address (CA0-CAn) when sampled at the rising clock edge.CAn depends from the SDRAM organisation. 4M x 4 SDRAM CAn = CA9 2M x 8 SDRAM CAn = CA8 1M x 16 SDRAM CAn = CA7 In addition to the column address, A10 is used to invoke autoprecharge operation at the end of the burst read or write cycle. If A10 is high, autoprecharge is selected and A11 defines the bank to be precharged (low=bank A, high=bank B). If A10 is low, autoprecharge is disabled. During a Precharge command cycle, A10 is used in conjunction with A11 to control which bank(s) to precharge. If A10 is high, both bank A and bank B will be precharged regardless of the state of A11. If A10 is low, then A11 is used to define which bank to precharge.
A11 (BS)	Input	Level	—	Selects which bank is to be active. A11 low selects bank A and A11 high selects bank B.
DQx	Input Output	Level	—	Data Input/Output pins operate in the same manner as on conventional DRAMs.
DQM LDQM UDQM	Input	Pulse	Active High	The Data Input/Output mask places the DQ buffers in a high impedance state when sampled high. In Read mode, DQM has a latency of two clock cycles and controls the output buffers like an output enable. In Write mode, DQM has a latency of zero and operates as a word mask by allowing input data to be written if it is low but blocks the write operation if DQM is high.
VDD, VSS	Supply			Power and ground for the input buffers and the core logic.
VDDQ VSSQ	Supply	—	—	Isolated power supply and ground for the output buffers to provide improved noise immunity.
Vref	Input	Level	—	Reference voltage for SDRAM versions supporting SSTL interface



Block Diagram for HYB39S16400AT (2 banks x 4M x 4 SDRAM)



Block Diagram for HYB39S16800AT (2 banks x 1M x 8 SDRAM)



Block Diagram for HYB39S16160AT (2 banks x 512k x 16 SDRAM)

Operation Definition

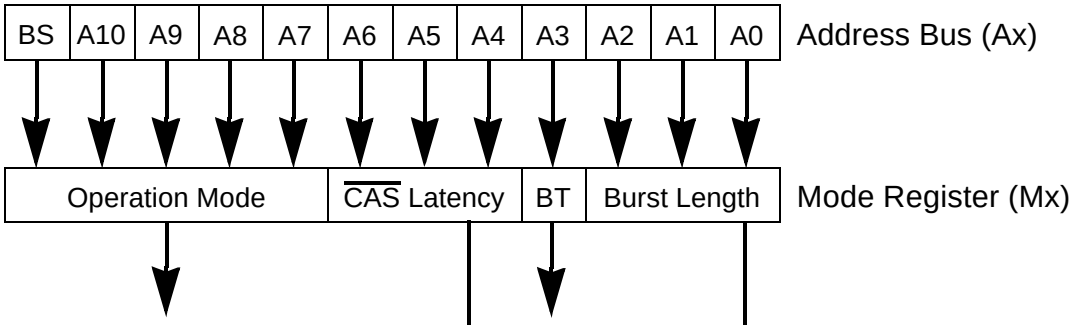
All of SDRAM operations are defined by states of control signals $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, and DQM at the positive edge of the clock. The following list shows the most important operation commands.

Operation	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	(L/U)DQM
Standby, Ignore $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and Address	H	X	X	X	X
Row Address Strobe and Activating a Bank	L	L	H	H	X
Column Address Strobe and Read Command	L	H	L	H	X
Column Address Strobe and Write Command	L	H	L	L	X
Precharge Command	L	L	H	L	X
Burst Stop Command	L	H	H	L	X
Self Refresh Entry	L	L	L	H	X
Mode Register Set Command	L	L	L	L	X
Write Enable/Output Enable	X	X	X	X	L
Write Inhibit/Output Disable	X	X	X	X	H
No Operation (NOP)	L	H	H	H	X

Mode Register

For application flexibility, a $\overline{CAS}$ latency, a burst length, and a burst sequence can be programmed in the SDRAM mode register. The mode set operation must be done before any activate command after the initial power up. Any content of the mode register can be altered by re-executing the mode set command. Both banks must be in precharged state and CKE must be high at least one clock before the mode set operation. After the mode register is set, a Standby or NOP command is required. Low signals of $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ at the positive edge of the clock activate the mode set operation. Address input data at this timing defines parameters to be set as shown in the following table.

Address Input for Mode Set (Mode Register Operation)



Operation Mode

M11	M10	M9	M8	M7	Mode
0	0	0	0	0	Normal
X	X	1	0	0	Multiple Burst with Single Write

Burst Type

M3	Type
0	Sequential
1	Interleave

$\overline{\text{CAS}}$ Latency

M6	M5	M4	Latency
0	0	0	Reserve
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	Reserve
1	0	1	Reserve
1	1	0	Reserve
1	1	1	Reserve

Burst Length

M2	M1	M0	Length	
			Sequential	Interleave
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserve	Reserve
1	0	1	Reserve	Reserve
1	1	0	Reserve	Reserve
1	1	1	Full Page	Reserve

Sequential Burst Addressing								Interleave Burst Addressing							
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
1	2	3	4	5	6	7	0	1	0	3	2	5	4	7	6
2	3	4	5	6	7	0	1	2	3	0	1	6	7	4	5
3	4	5	6	7	0	1	2	3	2	1	0	7	6	5	4
4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3
5	6	7	0	1	2	3	4	5	4	7	6	1	0	3	2
6	7	0	1	2	3	4	5	6	7	4	5	2	3	0	1
7	0	1	2	3	4	5	6	7	6	5	4	3	2	1	0

Read and Write Access Mode

When $\overline{RAS}$ is low and both $\overline{CAS}$ and $\overline{WE}$ are high at the positive edge of the clock, a RAS cycle starts. According to address data, a word line of the selected bank is activated and all of sense amplifiers associated to the word line are fired. A CAS cycle is triggered by setting $\overline{RAS}$ high and $\overline{CAS}$ low at a clock timing after a necessary delay, tRCD, from the RAS timing. $\overline{WE}$ is used to define either a read ($\overline{WE}$ = H) or a write ($\overline{WE}$ = L) at this stage.

SDRAM provides a wide variety of fast access modes. In a single CAS cycle, serial data read or write operations are allowed at up to a 125 MHz data rate. The numbers of serial data bits are the burst length programmed at the mode set operation, i.e., one of 1, 2, 4, 8 and full page. Column addresses are segmented by the burst length and serial data accesses are done within this boundary. The first column address to be accessed is supplied at the CAS timing and the subsequent addresses are generated automatically by the programmed burst length and its sequence. For example, in a burst length of 8 with interleave sequence, if the first address is '2', then the rest of the burst sequence is 3, 0, 1, 6, 7, 4, and 5 .

Full page burst operation is only possible using the sequential burst type and page length is a function of the I/O organisation and column addressing. Full page burst operation do not self terminate once the burst length has been reached. In other words, unlike burst length of 2, 3 or 8, full page burst continues until it is terminated using another command.

Similar to the page mode of conventional DRAM's, burst read or write accesses on any column address are possible once the $\overline{RAS}$ cycle latches sense amplifiers. The maximum tRAS or the refresh interval time limits the number of random column accesses. A new burst access can be done even before the previous burst ends. The interrupt operation at every clock cycles is supported. When the previous burst is interrupted, the remaining addresses are overridden by the new address with the full burst length. An interrupt which accompanies with an operation change from a read to a write is possible by exploiting DQM to avoid bus contention.

When two banks are activated sequentially, interleaved bank read or write operations are possible. With the programmed burst length, alternate access and precharge operations on two banks can realize fast serial data access modes among many different pages. Once two banks are activated, column to column interleave operation can be done between two different pages.

Refresh Mode

SDRAM has two refresh modes, a $\overline{CAS}$ before $\overline{RAS}$ (CBR) automatic refresh and a self refresh. All of banks must be precharged before applying any refresh mode. An on-chip address counter increments the word and the bank addresses and no bank information is required for both refresh modes. The chip enters the automatic refresh mode, when $\overline{RAS}$ and $\overline{CAS}$ are held low and CKE and $\overline{WE}$ are held high at a clock timing. The mode restores word line after the refresh and no external precharge command is necessary. A minimum tRC time is required between two automatic refreshes in a burst refresh mode. The same rule applies to any access command after the automatic refresh operation.

The chip has an on-chip timer and the self refresh mode is available. It enters the mode when $\overline{RAS}$, $\overline{CAS}$, and CKE are low and $\overline{WE}$ is high at a clock timing. All of external control signals including the clock are disabled. Returning CKE to high enables the clock and initiates the refresh exit operation. After the exit command, at least one tRC delay is required prior to any access command.

DQM Function

DQM has two functions for data I/O read write operations. During reads, when it turns to high at a clock timing, data outputs are disabled and become high impedance after two clock delay (DQM Data Disable Latency t_{DQZ}). It also provides a data mask function for writes. When DQM is activated, the write operation at the next clock is prohibited (DQM Write Mask Latency t_{DQW} = zero clocks).

Suspend Mode

During normal access mode, CKE is held high and CLK is enabled. When CKE is low, it freezes the internal clock and extends data read and write operations. One clock delay is required for mode entry and exit (Clock Suspend Latency t_{CSL}).

Power Down

In order to reduce standby power consumption, a power down mode is available. Bringing CKE low enters the power down mode and all of receiver circuits are gated. All banks must be precharged before entering this mode. One clock delay is required for mode entry and exit. The Power Down mode does not perform any refresh operation.

Auto Precharge

Two methods are available to precharge SDRAMs. In an automatic precharge mode, the CAS timing accepts one extra address, CA10, to determine whether the chip restores or not after the operation. If CA10 is high when a Read Command is issued, the **Read with Auto-Precharge** function is initiated. The SDRAM automatically enters the precharge operation one clock after the Read Command is registered for $\overline{CAS}$ latencies of 1 and 2, and two clocks for $\overline{CAS}$ latencies of 3. If CAS10 is high when a Write Command is issued, the **Write with Auto-Precharge** function is initiated. The SDRAM automatically enters the precharge operation one clock delay form the last data-in for $\overline{CAS}$ latencies of 1 and 2 and two clocks for $\overline{CAS}$ latencies of 3. This delay is referenced as t_{DPL} .

Precharge Command

If CA10 is low, the chip needs another way to precharge. In this mode, a separate precharge command is necessary. When $\overline{RAS}$ and $\overline{WE}$ are low and $\overline{CAS}$ is high at a clock timing, it triggers the precharge operation. Two address bits, A10 and A11, are used to define banks as shown in the following list. The precharge command may be applied coincident with the last of burst reads for CAS Latency = 1 and with the second to the last read data for CAS Latencies = 2 & 3. Writes require a time t_{DPL} from the last burst data to apply the precharge command.

Bank Selection by Address Bits

	A10	A11
Bank A Only	Low	Low
Bank B Only	Low	High
Both A and B	High	Dont Care

Burst Termination

Once a burst read or write operation has been initiated, there are several methods in which to terminate the burst operation prematurely. These methods include using another Read or Write Command to interrupt an existing burst operation, use a Precharge Command to interrupt a burst cycle and close the active bank, or using the Burst Stop Command to terminate the existing burst operation but leave the bank open for future Read or Write Commands to the same page of the active bank. When interrupting a burst with another Read or Write Command care must be taken to avoid DQ contention. The Burst Stop Command, however, has the fewest restrictions making it the easiest method to use when terminating a burst operation before it has been completed. If a Burst Stop command is issued during a burst write operation, then any residual data from the burst write cycle will be ignored. Data that is presented on the DQ pins before the Burst Stop Command is registered will be written to the memory.

Power Up Procedure

All Vdd and Vddq must reach the specified voltage no later than any of input signal voltages. An initial pause of 200 µsec is required after power on. All banks have to be precharged and a minimum of 2 auto-refresh cycles are required prior to the mode register set operation.

Absolute Maximum Ratings

Operating temperature range ..... 0 to + 70 °C
Storage temperature range..... – 55 to + 150 °C
Input/output voltage ..... – 0.5 to min(Vcc+0.5, 4.6) V
Power supply voltage VDD / VDDQ..... – 1.0 to + 4.6 V
Power Dissipation..... .....1 W
Data out current (short circuit) ..... 50 mA

Note: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Recommended Operation and Characteristics for LV-TTL versions:
T_A = 0 to 70 °C; V_{SS} = 0 V; $V_{DD,}V_{DDQ}$ = 3.3 V ± 0.3 V

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Input high voltage	V_{IH}	2.0	Vcc+0.3	V	1, 2
Input low voltage	V_{IL}	– 0.3	0.8	V	1, 2
Output high voltage (I_{OUT} = – 2.0 mA)	V_{OH}	2.4	–	V	
Output low voltage (I_{OUT} = 2.0 mA)	V_{OL}	–	0.4	V	
Input leakage current, any input (0 V < V_{IN} < Vddq, all other inputs = 0 V)	$I_{I(L)}$	– 10	10	µA	
Output leakage current (DQ is disabled, 0 V < V_{OUT} < V_{CC})	$I_{O(L)}$	– 10	10	µA	

Notes:
1. All voltages are referenced to VSS.
2. Vih may overshoot to Vcc + 2.0 V for pulse width of < 4ns with 3.3V. Vil may undershoot to -2.0 V for pulse width < 4.0 ns with 3.3V. Pulse width measured at 50% points with amplitude measured peak to DC reference.

Capacitance
T_A = 0 to 70 °C; V_{DD} = 3.3 V ± 0.3 V, f = 1 MHz

Parameter	Symbol	max. Values	Unit
Input capacitance (A0 to A11)	C_{I1}	4	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$, CLK, CKE, DQM)	C_{I2}	4	pF
Output capacitance (DQ)	C_{IO}	5	pF
Vref	C_{Ref}	8	pF

Recommended Operation and DC Characteristics for SSTL versions:
T_A = 0 to 70 °C; V_{SS} = 0 V;

Parameter	Symbol	Limit Values			Unit	Notes
		min.	nom.	max.		
Device supply voltage	V_{DD}	3.0	3.3	3.6	V	
Output supply voltage	V_{DDQ}	3.0	3.3	3.6	V	3
Input reference voltage	V_{REF}	1.3	1.5	1.7	V	4

Input logic levels and output current drives conditions for SSTL versions:
T_A = 0 to 70 °C; V_{SS} = 0 V;

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
DC input logic high levels	$V_{IH\ (DC)}$	Vref + 0.2	Vddq + 0.3	V	
AC input logic high levels	$V_{IH\ (AC)}$	Vref + 0.4		V	5
DC input logic low levels	$V_{IL\ (DC)}$	-0.3	Vref - 0.2	V	
AC input logic low levels	$V_{IL\ (AC)}$		Vref - 0.4	V	5
Ouput minimum source dc current	Ioh (dc)	16		mA	
Ouput minimum sink dc current	Iol (dc)	16		mA	

Notes:

3. Under all conditions VDDQ must be less than or equal to VDD
4. The value of Vref may be selected by the user to provide optimum noise margin in the system. Vref has to be in the range between 0.43 * VDDQ and 0.47 * VDDQ and is expected to track variations in VDDQ
5. Vih may overshoot to VDD, VDDQ + 1.2V for pulse width < 5ns and Vil may undershoot to VSS, VSSQ - 1.2 V for pulse widht < 5ns.

Operating Currents (T_A = 0 to 70°C, VCC = 3.3V ± 0.3V

(Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test Condition	$\overline{CAS}$ Latency	-8 max.	-10 max.		Note
Operating Current	Icc1	Burst Length = 4 trc>=trc (min.) tck>=tck(min.), Io = 0mA 2 bank interleave operation	1 2 3	80 115 125	65 90 100	mA mA mA	1, 2
Precharge Standby Current in Power Down Mode	Icc2P	CKE<=VIL(max), tck>=tck(min.)		3	3	mA	
	Icc2PS	CKE<=VIL(max), tCK=infinite		2	2	mA	
Precharge Standby Current in Non-power down Mode	Icc2N	CKE>=VIH(min), tck>=tck(min.) input signals changed once in 3 cycles		20	20	mA	$\overline{CS}$= High
	Icc2NS	CKE>=VIH(min), tCK=infinite, input signals are stable		10	10	mA	
Active Standby Current in Power Down Mode	Icc3P	CKE<=VIL(max), tck>=tck(min.)		3	3	mA	
	Icc3PS	CKE<=VIL(max), tCK=infinite, inpit signals are stable		2	2	mA	
Active Standby Current in Non-power Down Mode	Icc3N	CKE>=VIH(min), tck>=tck(min.), changed once in 3 cycles		25	25	mA	$\overline{CS}$= High, 1
	Icc3NS	CKE>=VIH(min), tCK=infinite, input signals are stable		15	15	mA	
Burst Operating Current	Icc4	Burst Length = full page trc = infinite tck >= tck (min.), IO = 0 mA 2 banks activated	1 2 3	50 80 120	40 65 95	mA	1, 2
Auto (CBR) Refresh Current	Icc5	trc>=trc(min)	1 2 3	75 95 115	60 75 90	mA mA mA	1, 2
Self Refresh	Icc6	CKE=<0,2V		2	2	mA	1, 2

Notes:

1. The specified values are valid when addresses are changed no more than three times during trc(min.) and when No Operation commands are registered on every rising clock edge during tRC(min).
2. The specified values are valid when data inputs (DQs) are stable during tRC(min.).

AC Characteristics 1)2)

T_A = 0 to 70 °C; V_{SS} = 0 V; V_{CC} = 3.3 V ± 0.3 V, t_T = 1 ns

Parameter	Symbol	Limit Values				Unit	Note
		-8		-10			
		min	max	min	max		
Clock and Clock Enable							
Clock Cycle Time	t_{CK}						
$\overline{CAS}$ Latency = 3		8		10		ns	
$\overline{CAS}$ Latency = 2		12		15		ns	
$\overline{CAS}$ Latency = 1		24		30		ns	
System frequency	t_{CK}						
$\overline{CAS}$ Latency = 3			125		100	MHz	
$\overline{CAS}$ Latency = 2			83		66	MHz	
$\overline{CAS}$ Latency = 1			41		33	MHz	
Clock Access Time	t_{AC}						
$\overline{CAS}$ Latency = 3		–	7	–	8	ns	3
$\overline{CAS}$ Latency = 2		–	8	–	9	ns	
$\overline{CAS}$ Latency = 1			21	–	27	ns	
Clock High Pulse Width	t_{CH}	3	–	3.5	–	ns	
Clock Low Pulse Width	t_{CL}	3	–	3.5	–	ns	
Transition time (rise and fall)	t_T	1	30	1	30	ns	
Setup and Hold Times							
Command Setup time	t_{CS}	2.5	–	3	–	ns	4
Address Setup Time	t_{AS}	2.5	–	3	–	ns	4
Data In Setup Time	t_{DS}	2.5	–	3	–	ns	4
CKE Setup Time	t_{CKS}	2.5	–	3	–	ns	4
CKE Set-up Time (Power down mode)	t_{CKSP}	2.5	–	3	–	ns	4
CKE Set-up Time (Self Refresh Exit)	t_{CKSR}	8	–	8	–	ns	
Command Hold Time	t_{CH}	1	–	1	–	ns	4
Address Hold Time	t_{AH}	1	–	1	–	ns	4
Data In Hold Time	t_{DH}	1	–	1	–	ns	4
CKE Hold Time	t_{CKH}	1	–	1	–	ns	4

Parameter	Symbol	Limit Values				Unit	Note
		-8		-10			
		min	max	min	max		
Common Parameters							
Row to Column Delay Time	t_{RCD}	24	–	30	–	ns	
Row Active Time	t_{RAS}	36	120k	45	120k	ns	
Precharge Time	t_{RP}	24	–	30	–	ns	
Row Cycle Time	t_{RC}	60	120k	75	120k	ns	
Bank to Bank Delay Time	t_{RRD}	16	–	20	–	ns	
$\overline{CAS}$ to $\overline{CAS}$ delay time (same bank)	t_{CCD}	1	–	1	–	CLK	
Refresh Cycle							
Self Refresh Exit Time	t_{SREX}	$2CLK+t_{RC}$				ns	6
Refresh Period (4096 cycles)	t_{REF}	–	64	–	64	ms	5
Read Cycle							
Data Out Hold Time	t_{OH}	3	–	3	–	ns	
Data Out to Low Impedance Time	t_{LZ}	0	–	0	–	ns	
Data Out to High Impedance Time	t_{HZ}						7
$\overline{CAS}$ Latency = 3		–	5	–	6	ns	
$\overline{CAS}$ Latency = 2		–	7	–	8	ns	
$\overline{CAS}$ Latency = 1		–	19	–	25	ns	
DQM Data Out Disable Latency	t_{DQZ}	2	–	2	–	CLK	
Write Cycle							
Last Data-Input to Precharge (Write Recovery Latency)							
CL = 1, 2	t_{DPL}	1	–	1	–	CLK	
CL = 3 .		2	–	2	–	CLK	
DQM Write Mask Latency	t_{DQW}	0	–	0	–	CLK	

Notes:

1. An initial pause of 200µs is required after power-up, then a Precharge All Banks command must be given followed by 8 Auto Refresh (CBR) cycles before the Mode Register Set Operation can begin.
2. AC timing tests for LV-TTL versions have V_{il} = 0.4V and V_{ih} = 2.4V with the timing referenced to the 1.4 V crossover point. The transition time is measured between V_{ih} and V_{il}. All AC measurements assume t_T=1ns with the AC output load circuit shown in fig.1.
   AC timing tests for SSTL versions have to be performed according to the JEDEC standard for „Stub Series Terminated Logic for 3.3Volts (SSTL_3)."
3. If clock rising time is longer than 1ns, (t_T/2 -0.5) ns has to be added to this parameter.
4. If t_T is longer than 1 ns, a time (t_T-1) ns has to be added to this parameter.
5. Any time that the refresh Period has been exceeded, a minimum of two Auto (CBR) Refresh commands must be given to "wake-up"the device.
6. Self Refresh Exit is a synchronous operation and begins on the 2nd positive clock edge after CKE returns high. Self Refresh Exit is not complete until a time period equal to tRC is satisfied once the Self Refresh Exit command is registered.
7. Referenced to the time which the output achieves the open circuit condition, not to output voltage levels..

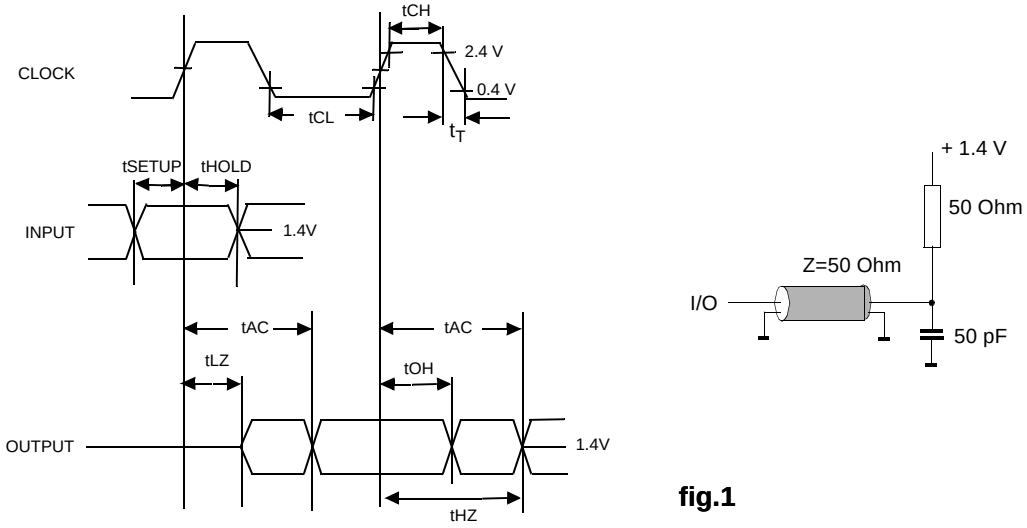


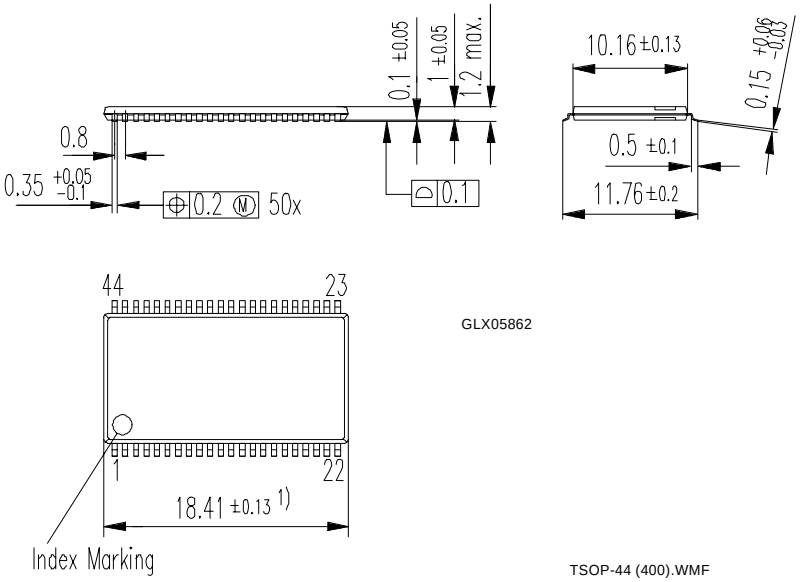
fig.1

Clock Frequency and Latency

Parameter		Symbol	Speed Sort				Unit
			-8		-10		
Clock Frequency	max.	t_{CK}	**125**	**83**	**100**	**66**	MHz
Clock Cycle Time	min.	t_{CK}	8	12	10	15	ns
$\overline{CAS}$ Latency	min.	t_{AA}	3	2	3	2	CLK
Row to Column Delay	min.	t_{RCD}	3	2	3	2	CLK
$\overline{RAS}$ Latency	min.	t_{RL}	6	4	6	4	CLK
Row Active Time	min.	t_{RAS}	5	3	5	3	CLK
	max.	t_{RAS}	120	120	120	120	µs
Row Precharge Time	min.	t_{RP}	3	2	3	2	CLK
Row Cycle time	min.	t_{RC}	8	5	8	5	CLK
Last Data-In to Precharge (Write Recovery)	min.	t_{DPL}	2	1	2	1	CLK
Last Data-In to Active / Refresh	min.	t_{DPL} + t_{RP}	5	3	5	3	CLK
Bank to Bank Delay Time	min.	t_{RRD}	2	2	2	2	CLK
$\overline{CAS}$ to $\overline{CAS}$ delay time	min.	t_{CCD}	1	1	1	1	CLK
Write Latency	fixed	t_{WL}	0	0	0	0	CLK
DQM Write Mask Latency	fixed	t_{DQW}	0	0	0	0	CLK
DQM Data Disable Latency	fixed	t_{DQZ}	2	2	2	2	CLK
Clock Suspend Latency	fixed	t_{CSL}	1	1	1	1	CLK

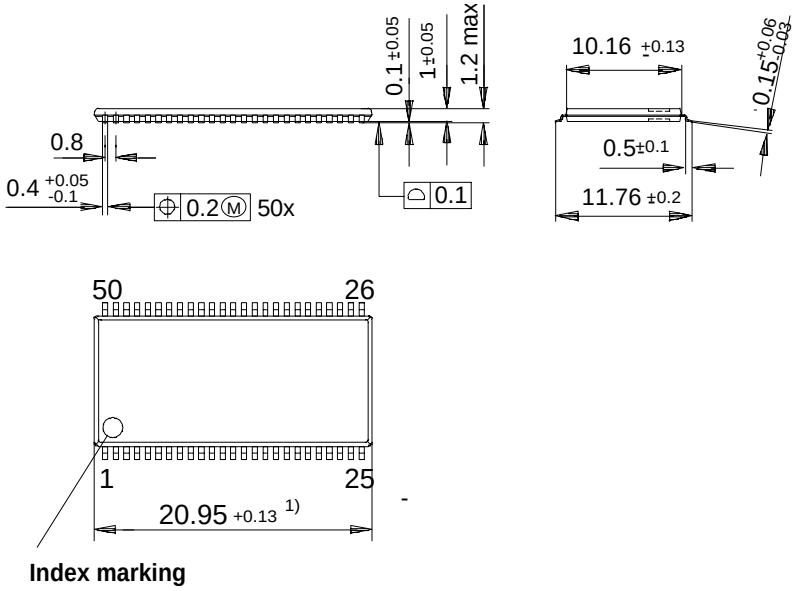
Package Outlines:

Plastic Package P-TSOPII-44 (400mil, 0.8mm lead pitch)
Thin small outline package, SMD



1) Does not include plastic or metal protrusion of 0.15 max. per side

Plastic Package P-TSOPII-50 (400mil, 0.8mm lead pitch)
Thin small outline package, SMD



1) Does not include plastic or metal protusion of 0.25 max. per side

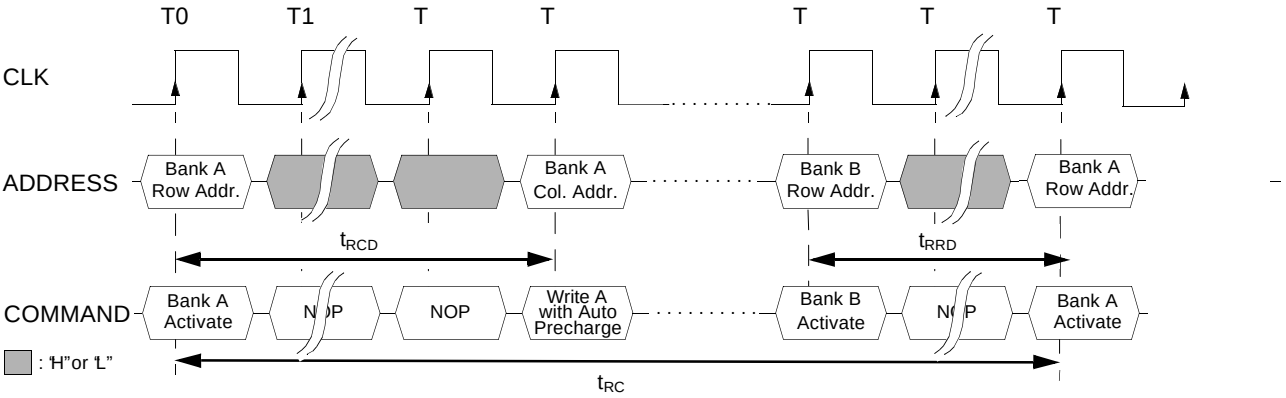
Timing Diagrams

Timing Diagrams (cont'd)

18. Random Row Read (Interleaving Banks)
    - 18.1 $\overline{\text{CAS}}$ Latency = 1
    - 18.2 $\overline{\text{CAS}}$ Latency = 2
    - 18.3 $\overline{\text{CAS}}$ Latency = 3
19. Random Row Write (Interleaving Banks)
    - 19.1 $\overline{\text{CAS}}$ Latency = 1
    - 19.2 $\overline{\text{CAS}}$ Latency = 2
    - 19.3 $\overline{\text{CAS}}$ Latency = 3
20. Full Page Read Cycle (optional feature)
    - 20.1 $\overline{\text{CAS}}$ Latency = 1
    - 20.2 $\overline{\text{CAS}}$ Latency = 2
    - 20.3 $\overline{\text{CAS}}$ Latency = 3
21. Full Page Write Cycle (optional feature)
    - 21.1 $\overline{\text{CAS}}$ Latency = 1
    - 21.2 $\overline{\text{CAS}}$ Latency = 2
    - 21.3 $\overline{\text{CAS}}$ Latency = 3
22. Precharge Termination of a Burst
    - 22.1 $\overline{\text{CAS}}$ Latency = 1
    - 22.2 $\overline{\text{CAS}}$ Latency = 2
    - 22.3 $\overline{\text{CAS}}$ Latency = 3

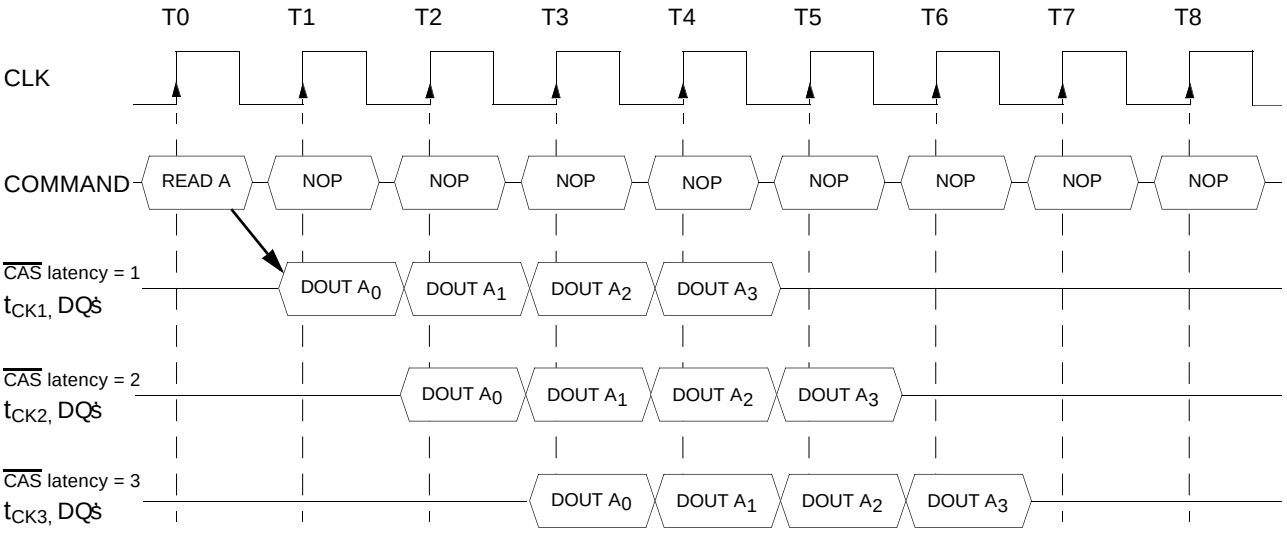
1. Bank Activate Command Cycle

($\overline{\text{CAS}}$ latency = 3)



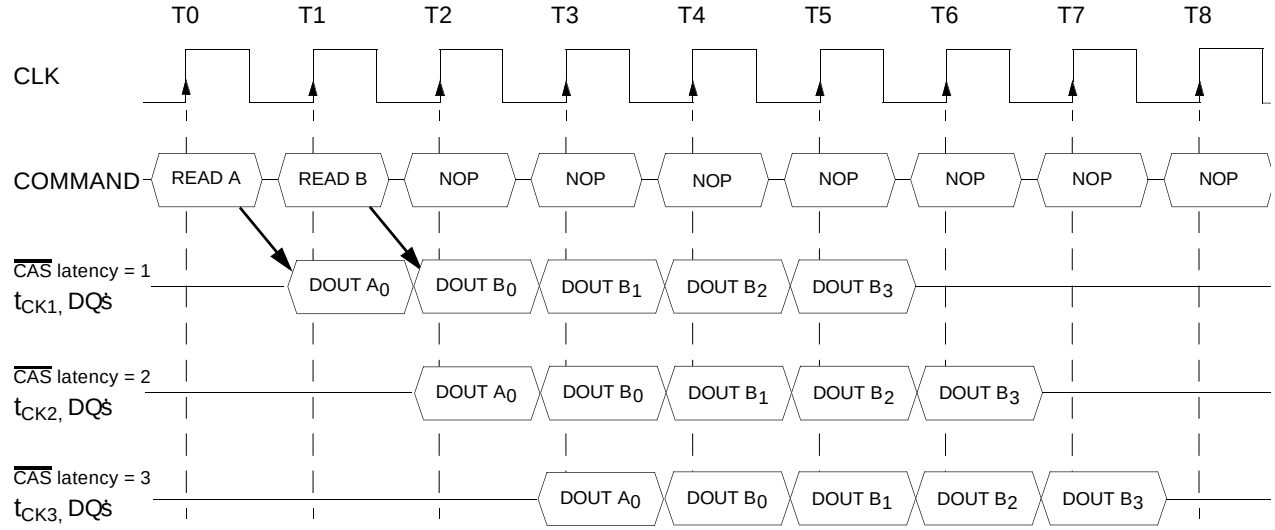
2. Burst Read Operation

(Burst Length = 4, $\overline{\text{CAS}}$ latency = 1, 2, 3)



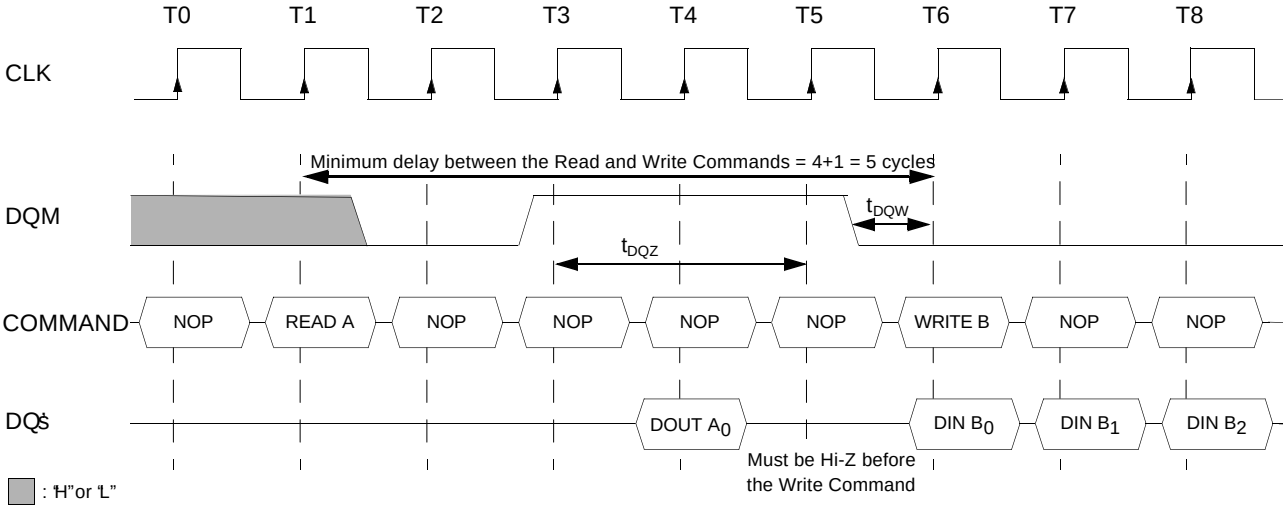
3. Read Interrupted by a Read

(Burst Length = 4, $\overline{CAS}$ latency = 1, 2, 3)



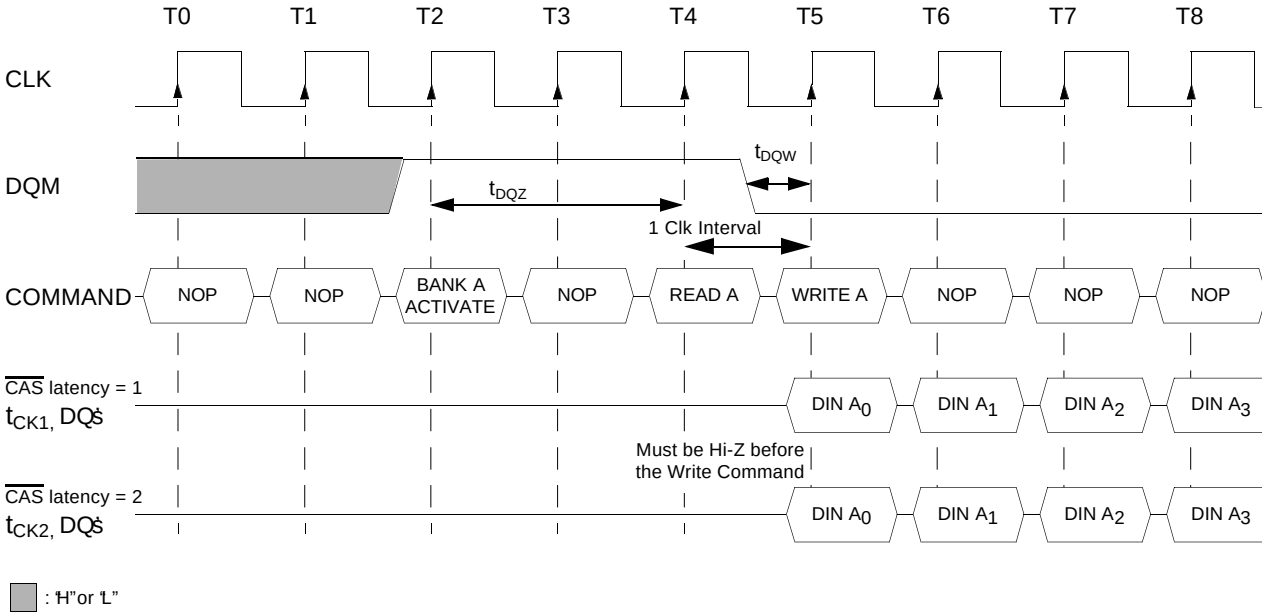
4.1 Read to Write Interval

(Burst Length = 4, $\overline{CAS}$ latency = 3)



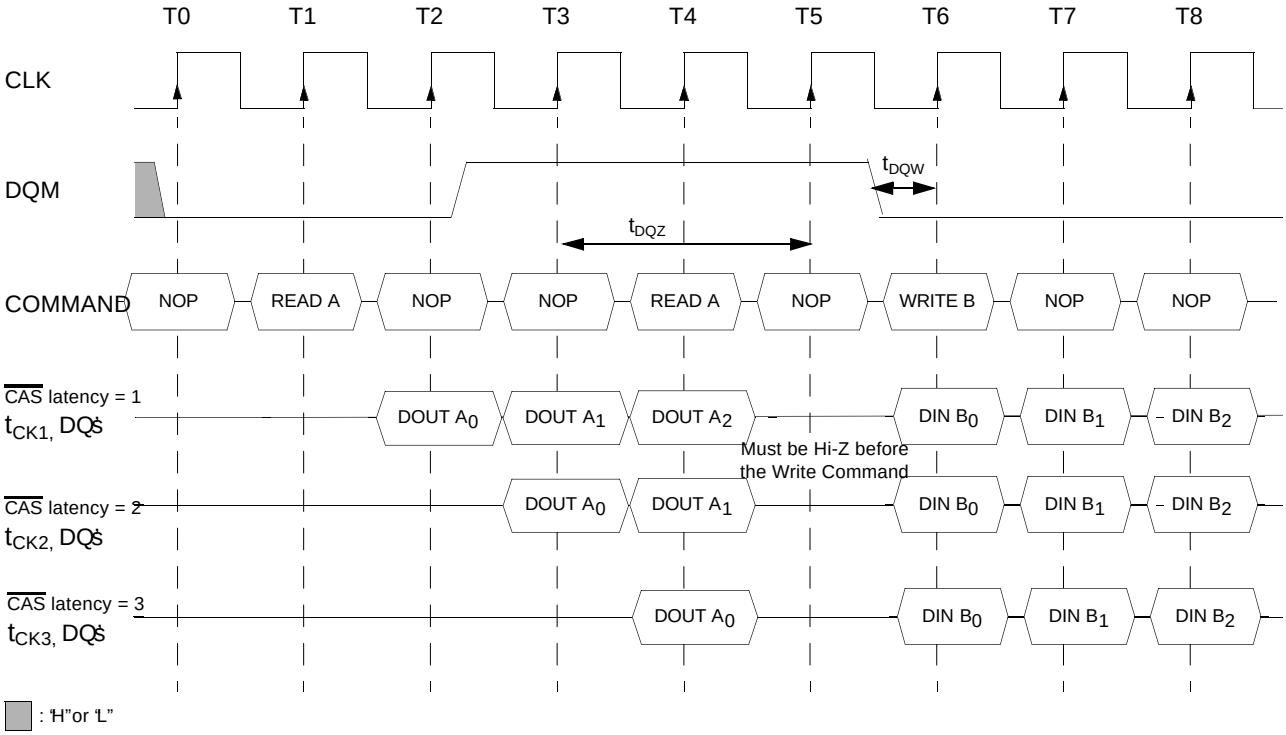
4 2. Minimum Read to Write Interval

(Burst Length = 4, $\overline{CAS}$ latency = 1, 2)



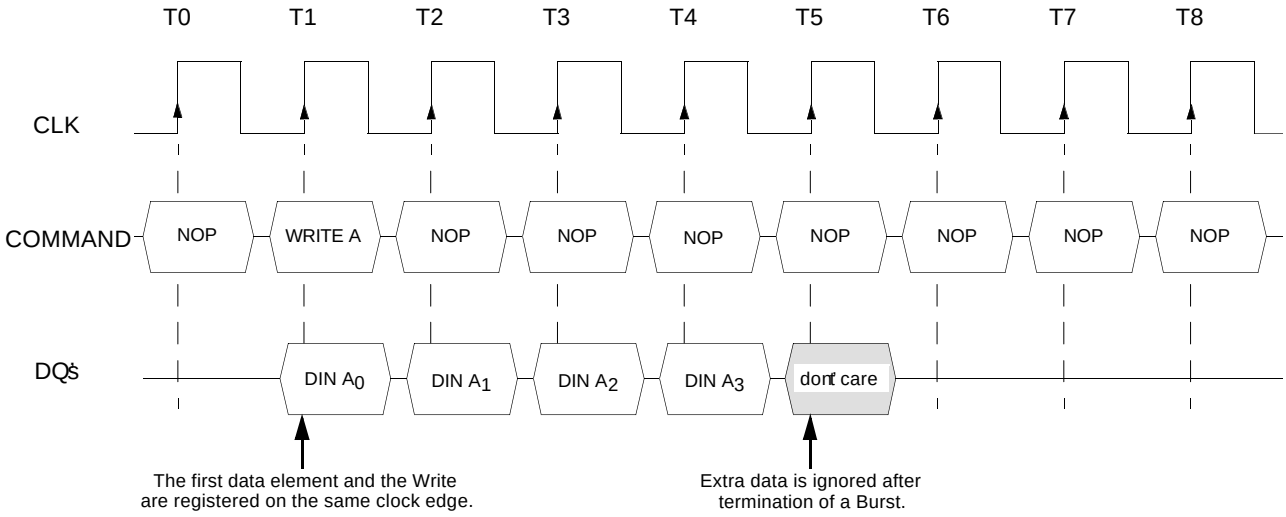
4. 3. Non-Minimum Read to Write Interval

(Burst Length = 4, $\overline{CAS}$ latency = 3



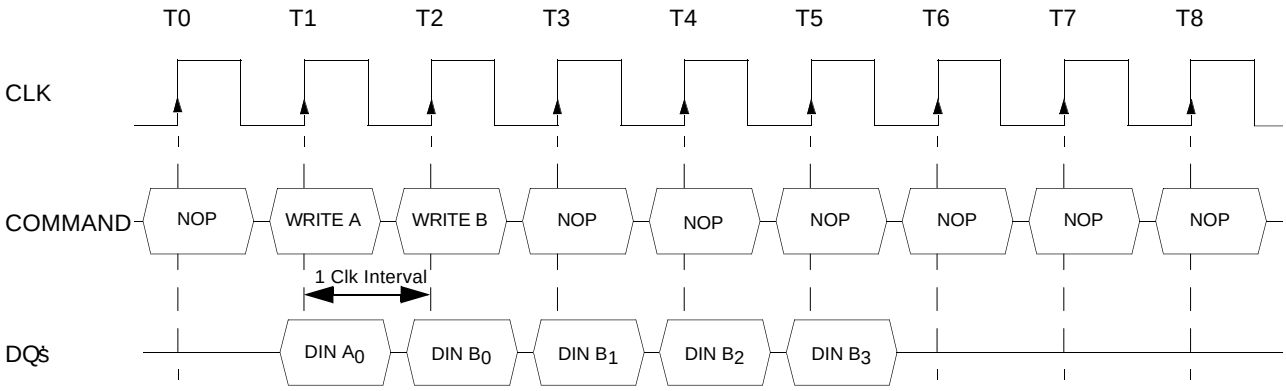
5. Burst Write Operation

(Burst Length = 4, $\overline{\text{CAS}}$ latency = 1, 2, or 3)



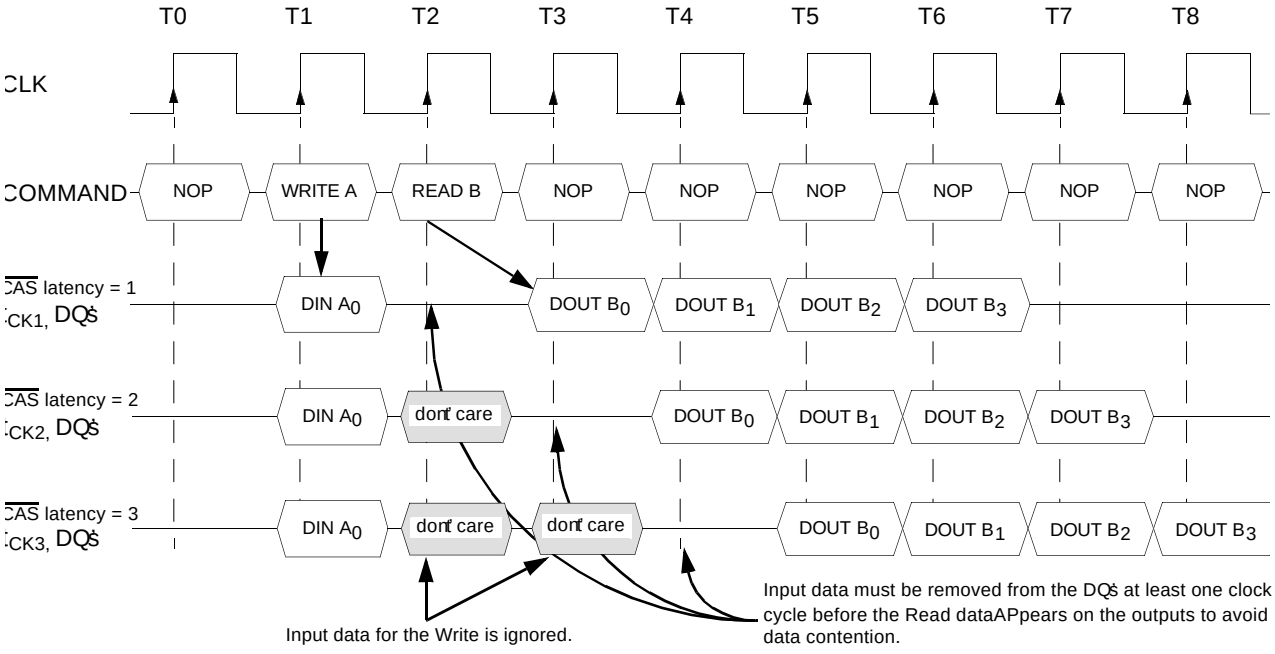
6.1 Write Interrupted by a Write

(Burst Length = 4, $\overline{\text{CAS}}$ latency = 1, 2, or 3)



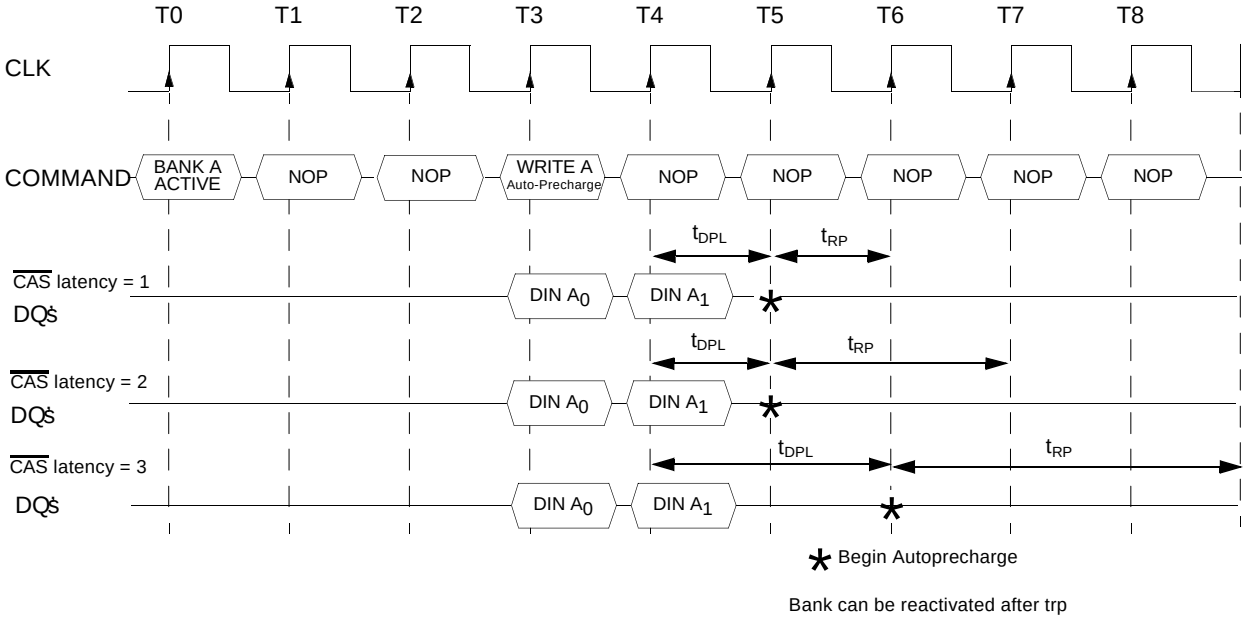
6.2 Write Interrupted by a Read

(Burst Length = 4, $\overline{\text{CAS}}$ latency = 1, 2, 3)



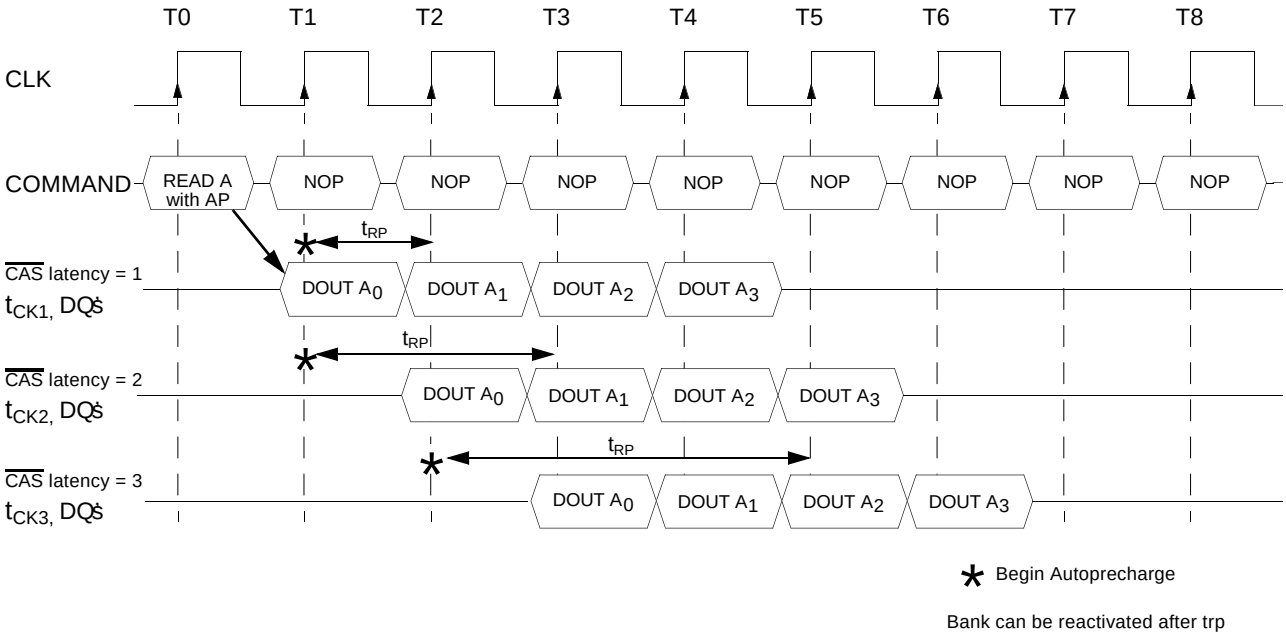
7.1 Burst Write with Auto-Precharge

Burst Length = 2, $\overline{\text{CAS}}$ latency = 1, 2, 3)



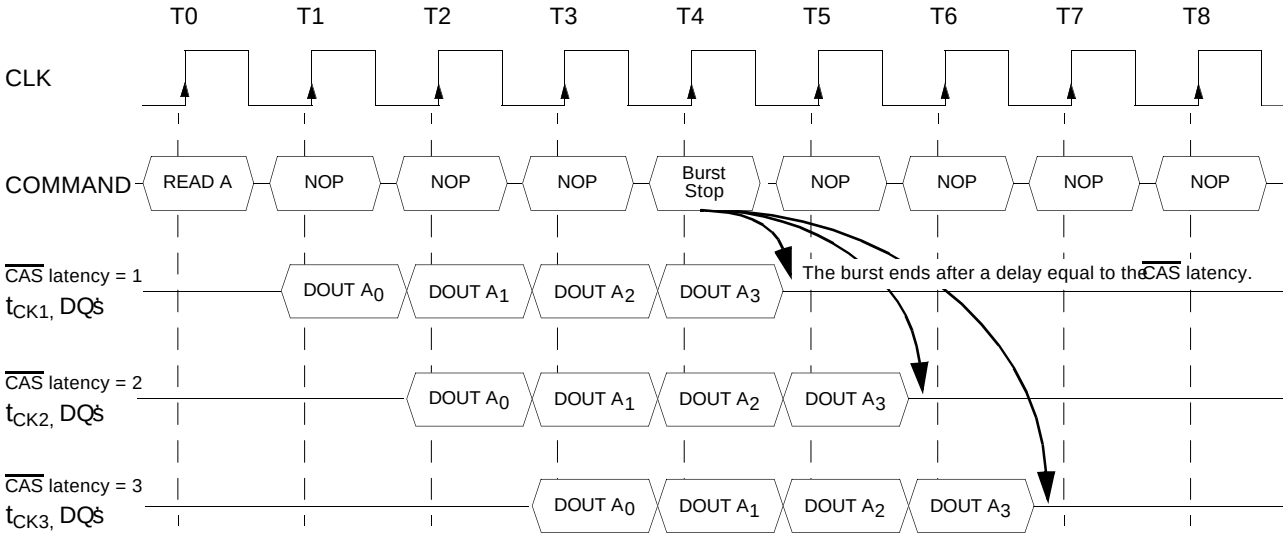
7.2 Burst Read with Auto-Precharge

(Burst Length = 4, $\overline{\text{CAS}}$ latency = 1, 2, 3)



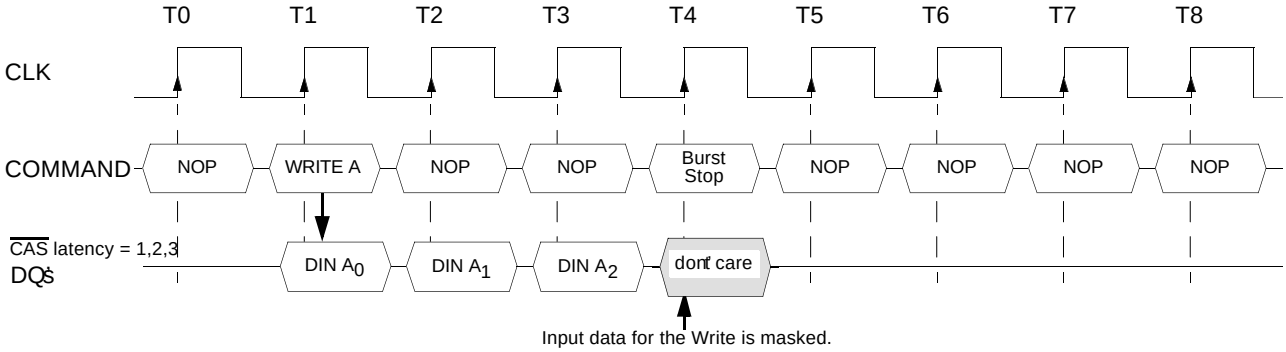
8.1 Termination of a Burst Read Operation

($\overline{\text{CAS}}$ latency = 1, 2, 3 / Burst Length = 8)

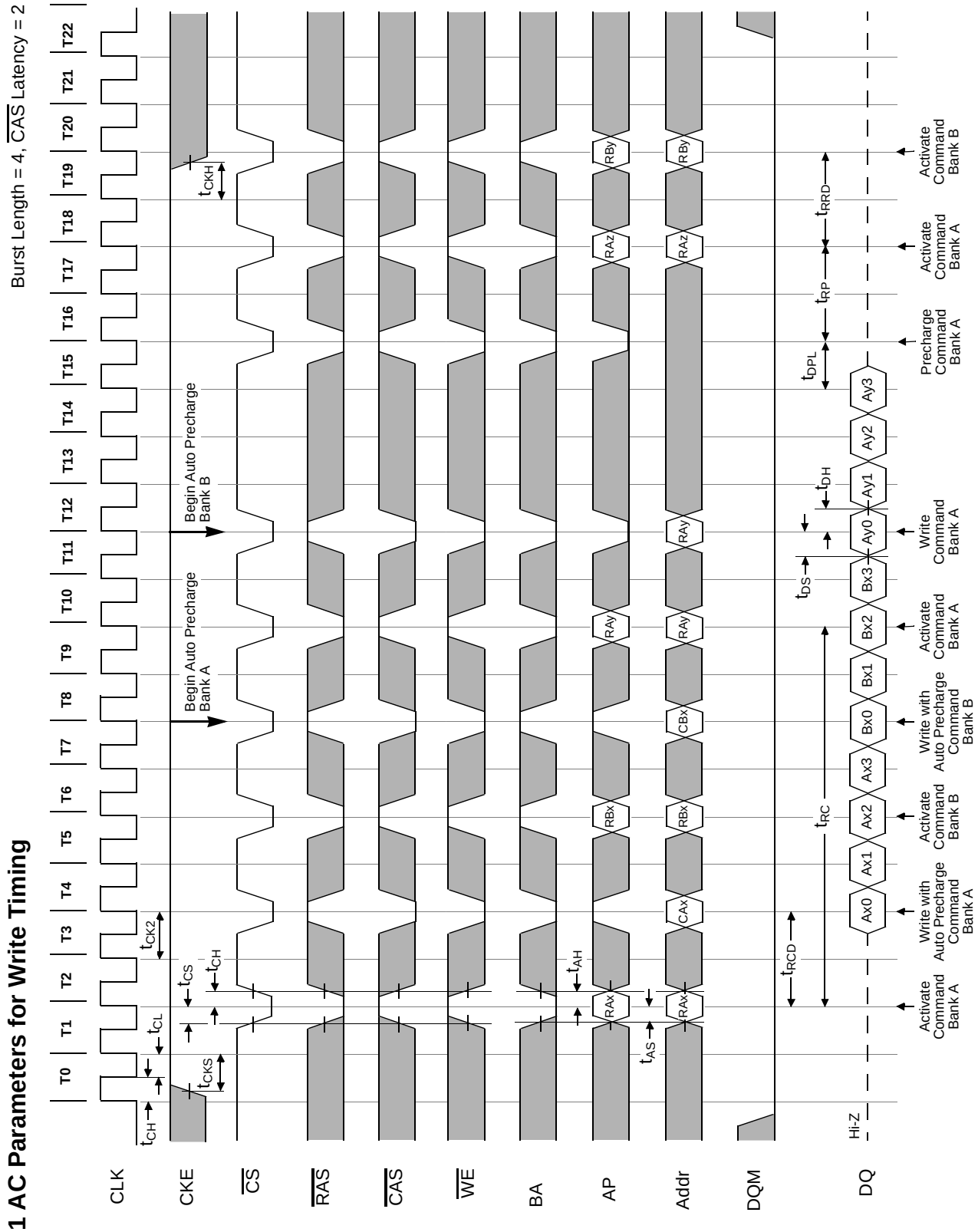


8.2 Termination of a Burst Write Operation

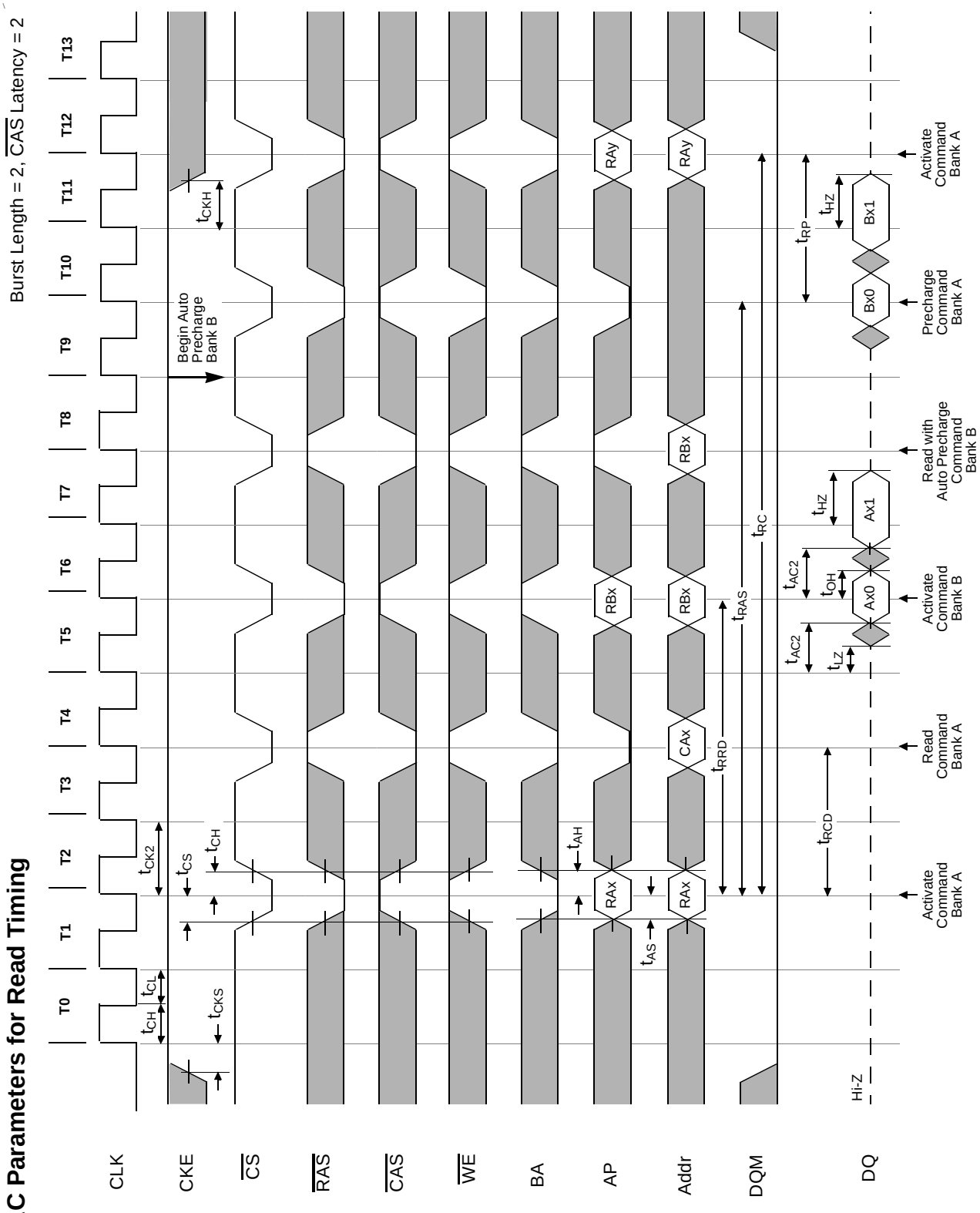
(CAS Laency = 1, 2, 3, Burst Length = 8)



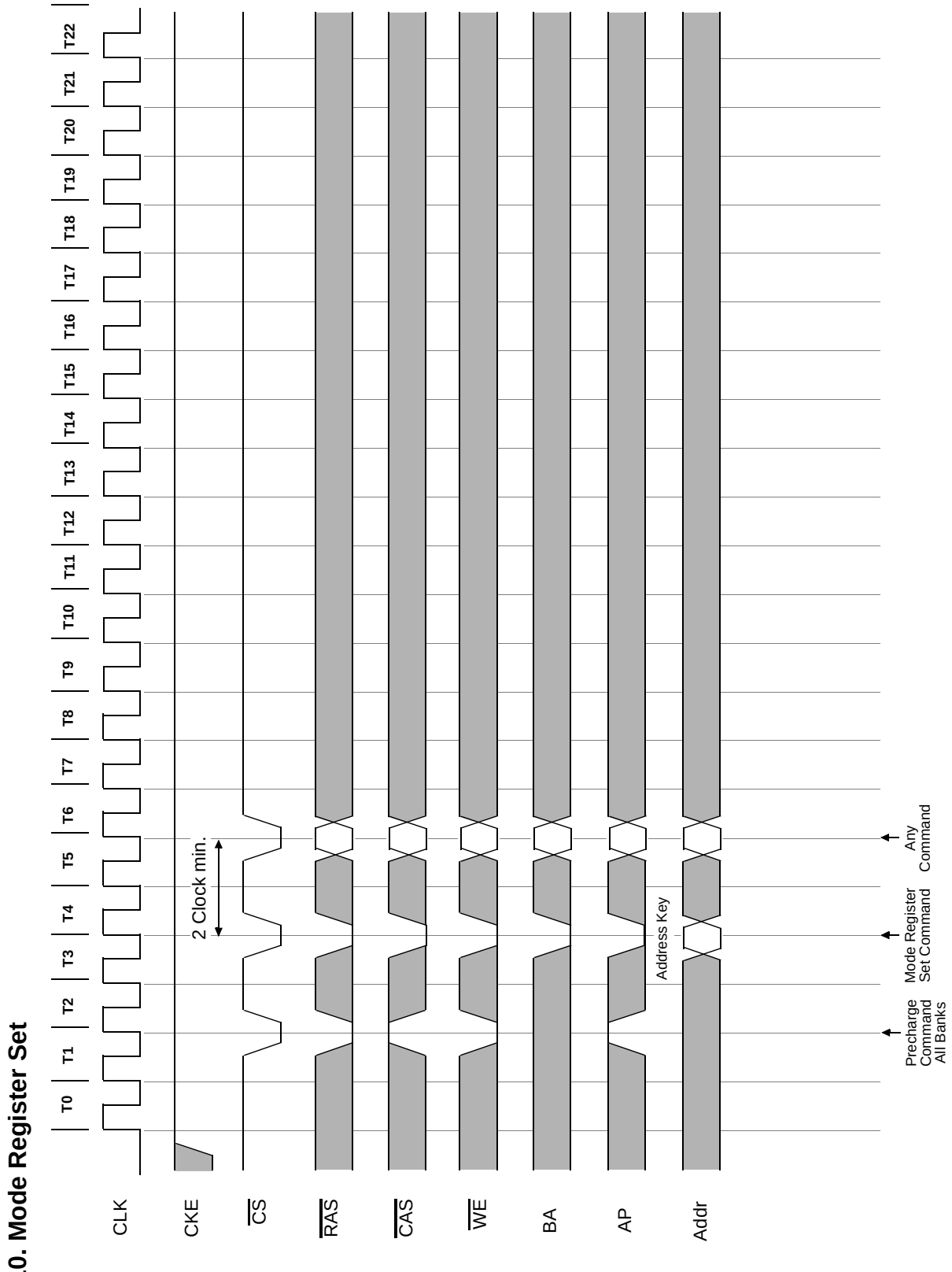
9.1 AC Parameters for Write Timing



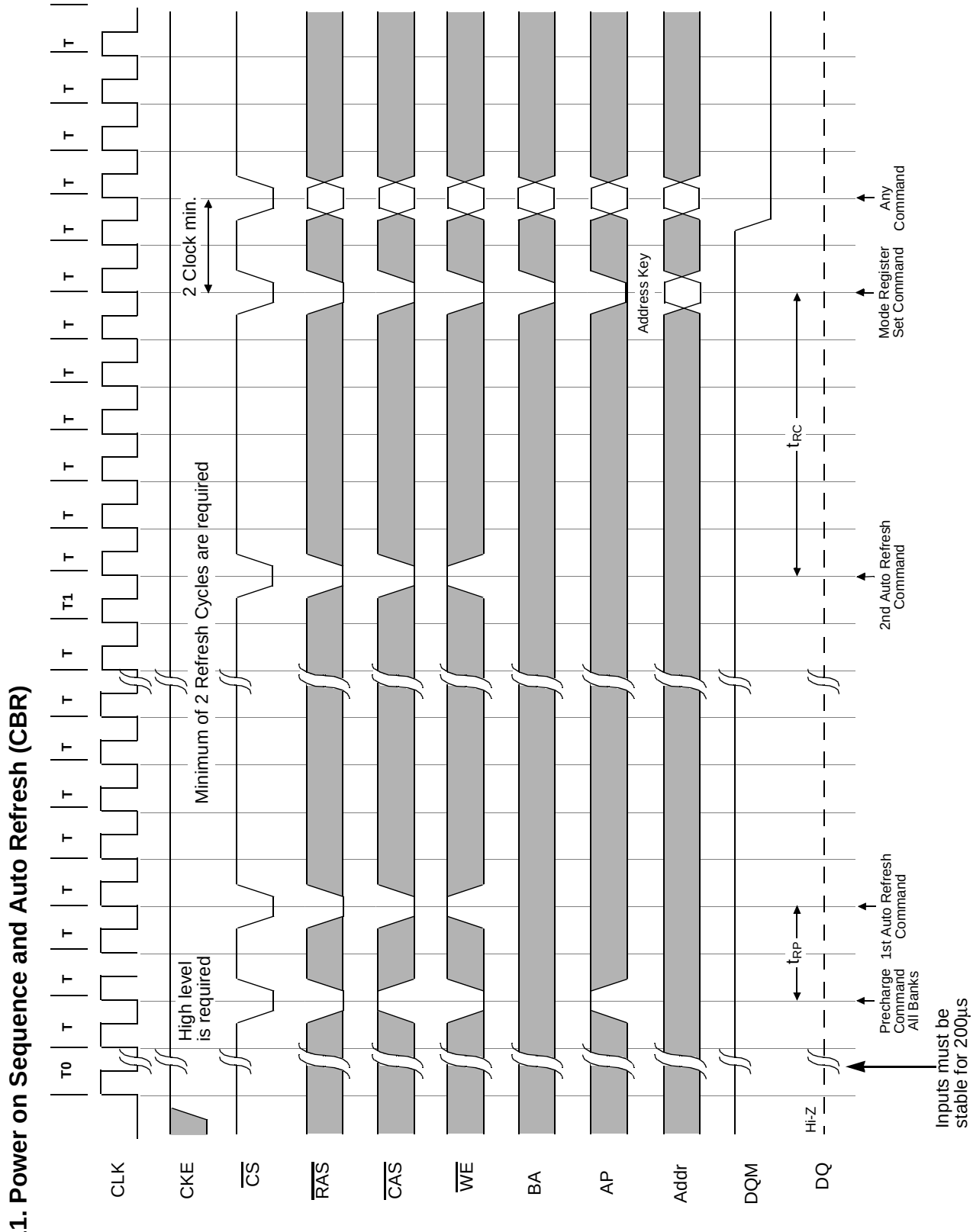
9.2 AC Parameters for Read Timing



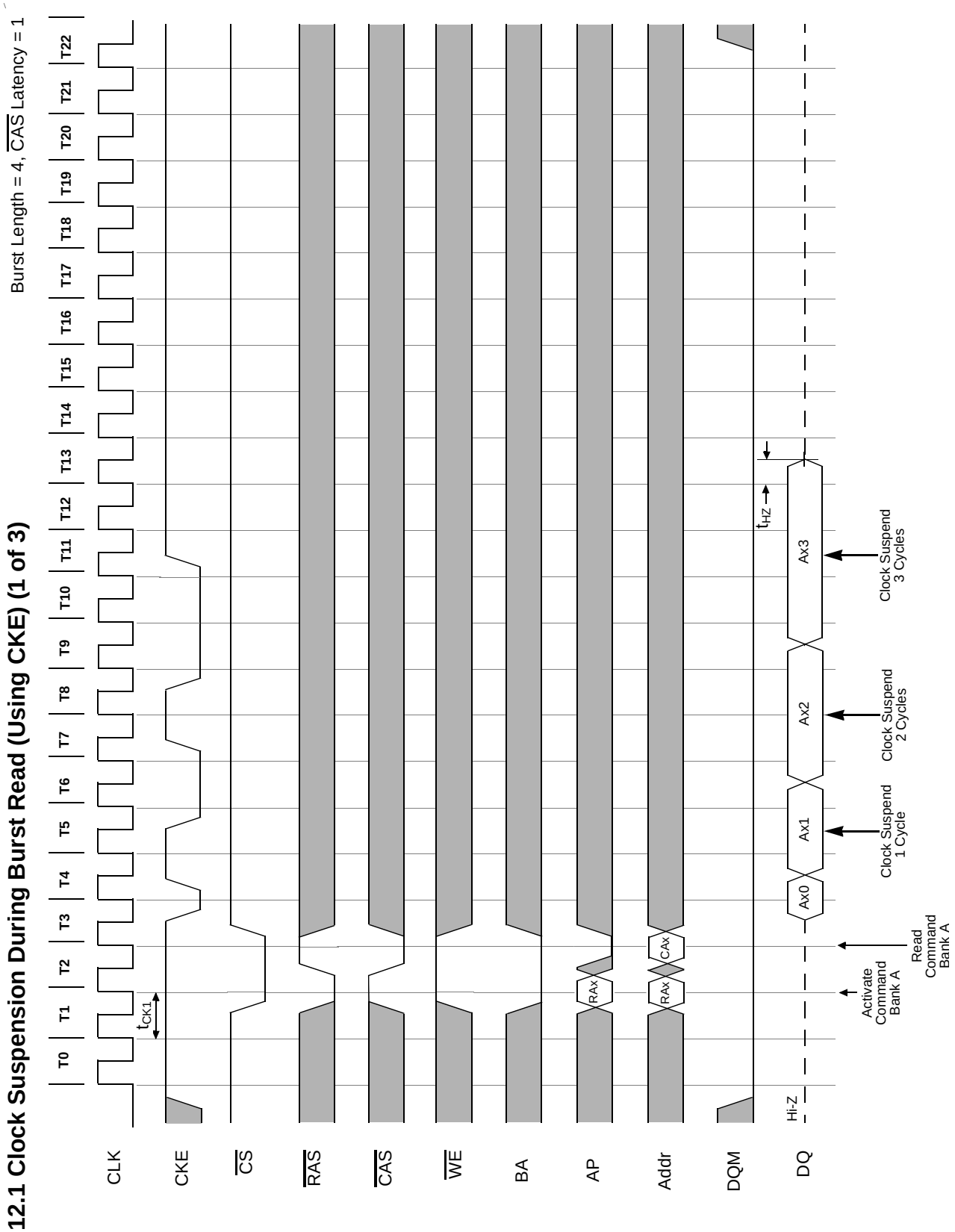
10. Mode Register Set



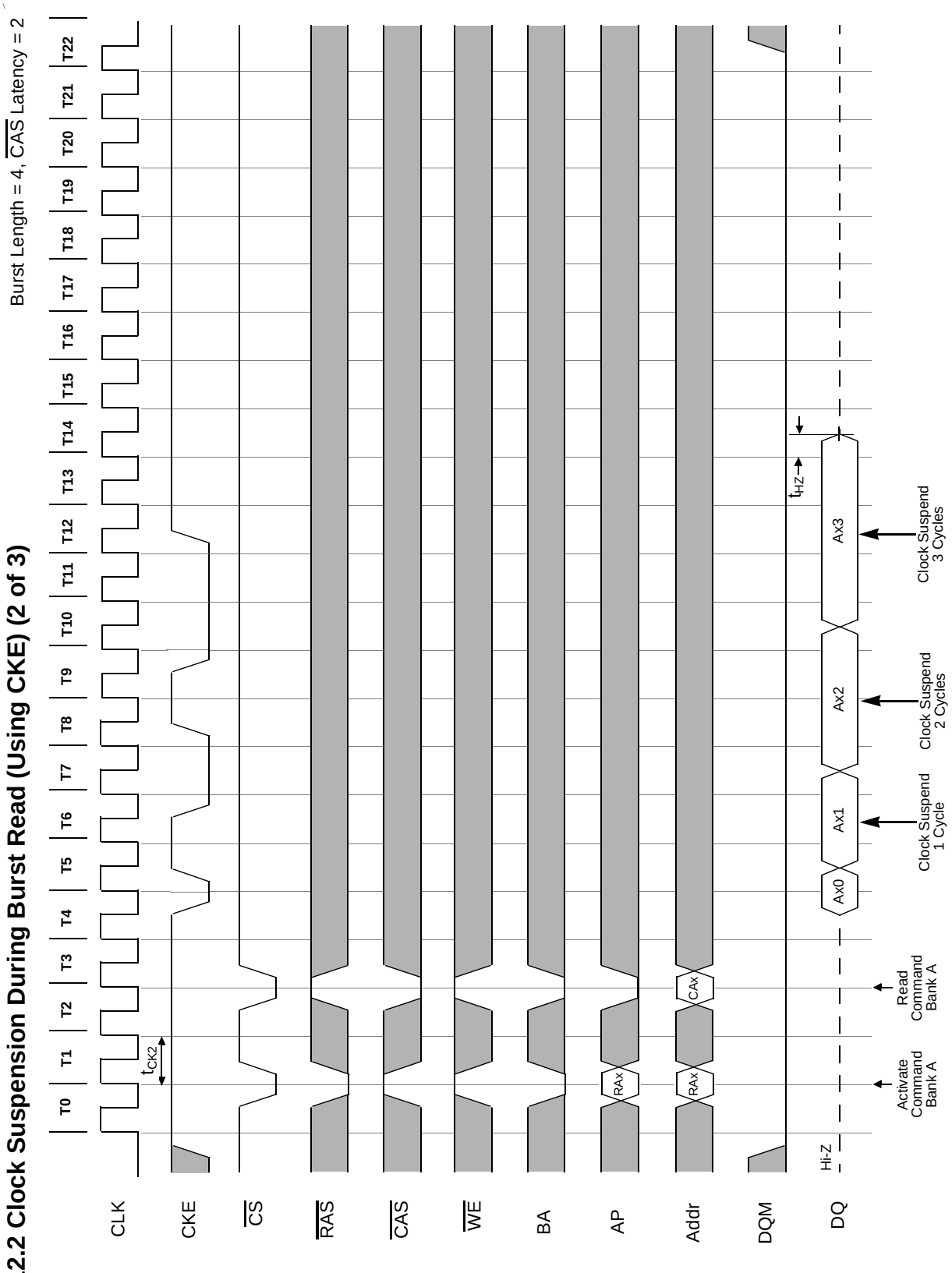
11. Power on Sequence and Auto Refresh (CBR)



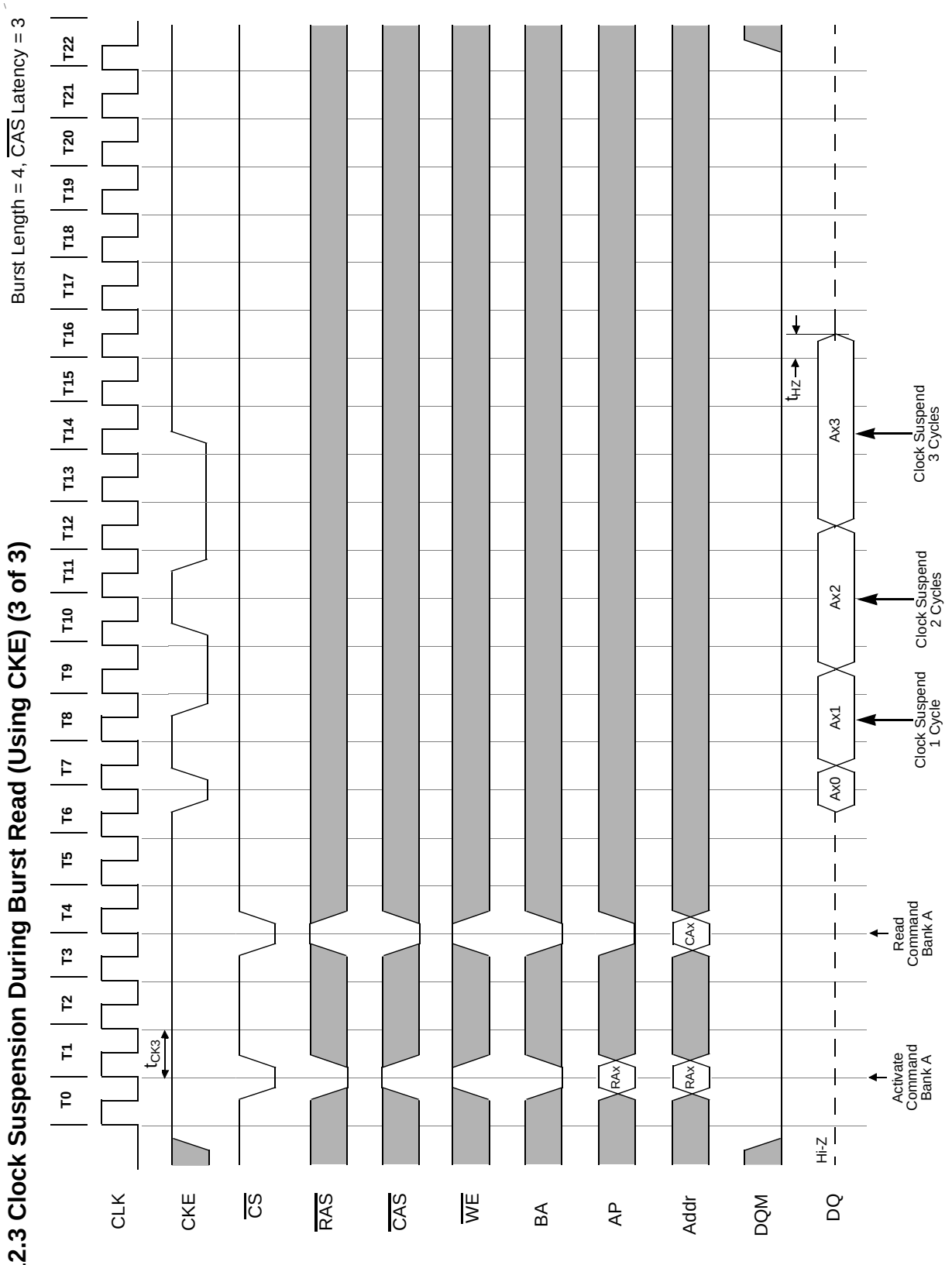
12.1 Clock Suspension During Burst Read (Using CKE) (1 of 3)



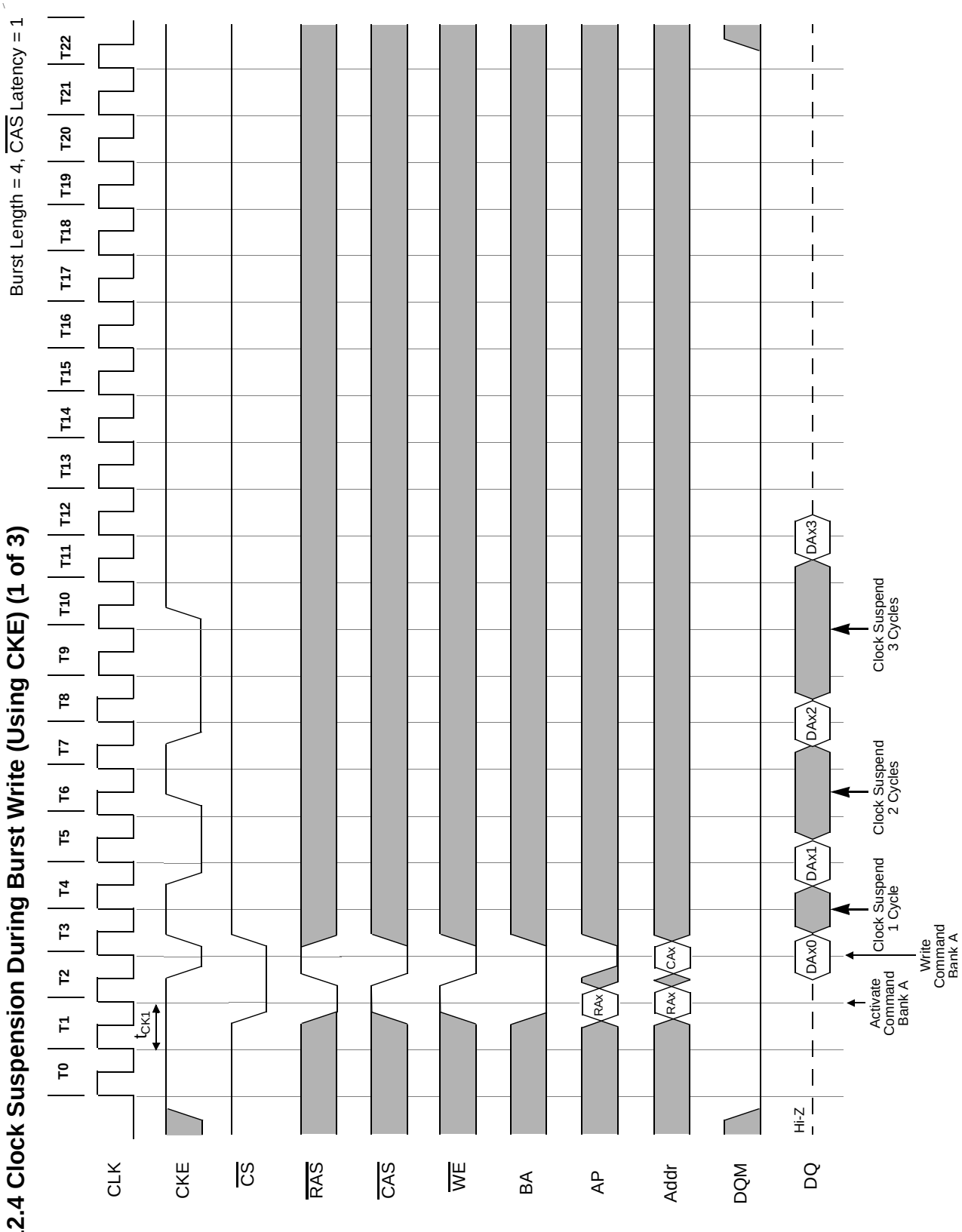
12.2 Clock Suspension During Burst Read (Using CKE) (2 of 3)



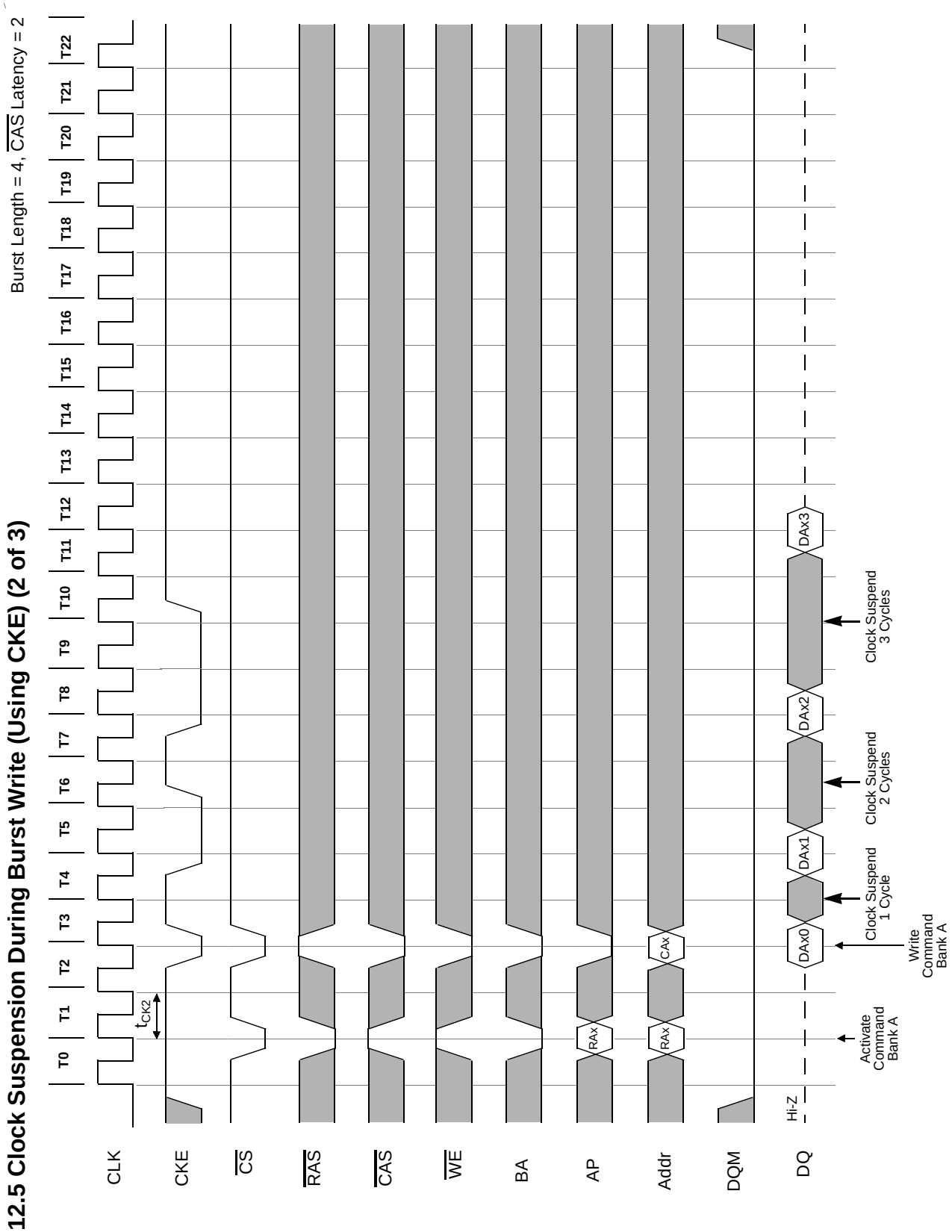
12.3 Clock Suspension During Burst Read (Using CKE) (3 of 3)



12.4 Clock Suspension During Burst Write (Using CKE) (1 of 3)

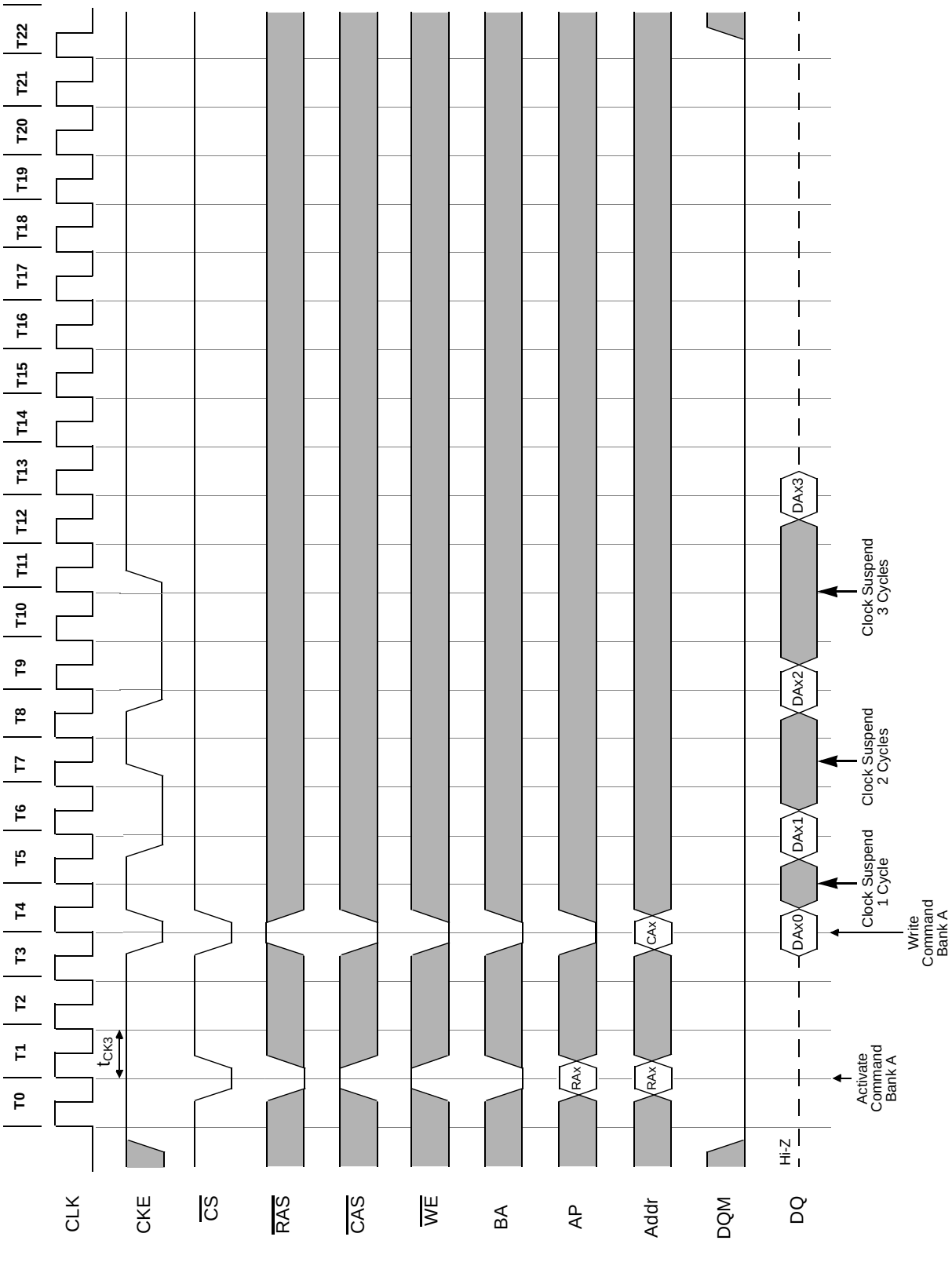


12.5 Clock Suspension During Burst Write (Using CKE) (2 of 3)

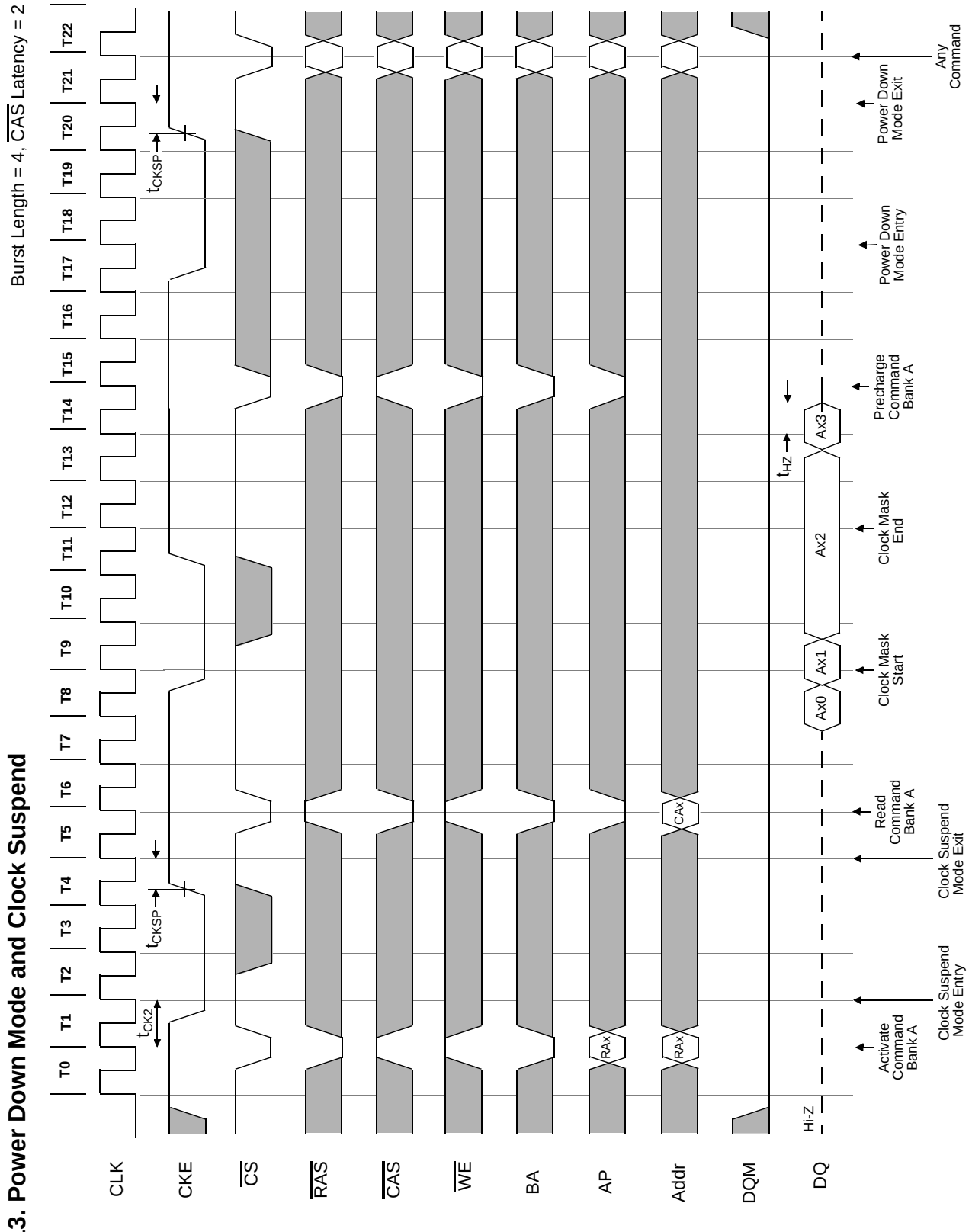


12.6 Clock Suspension During Burst Write (Using CKE) (3 of 3)

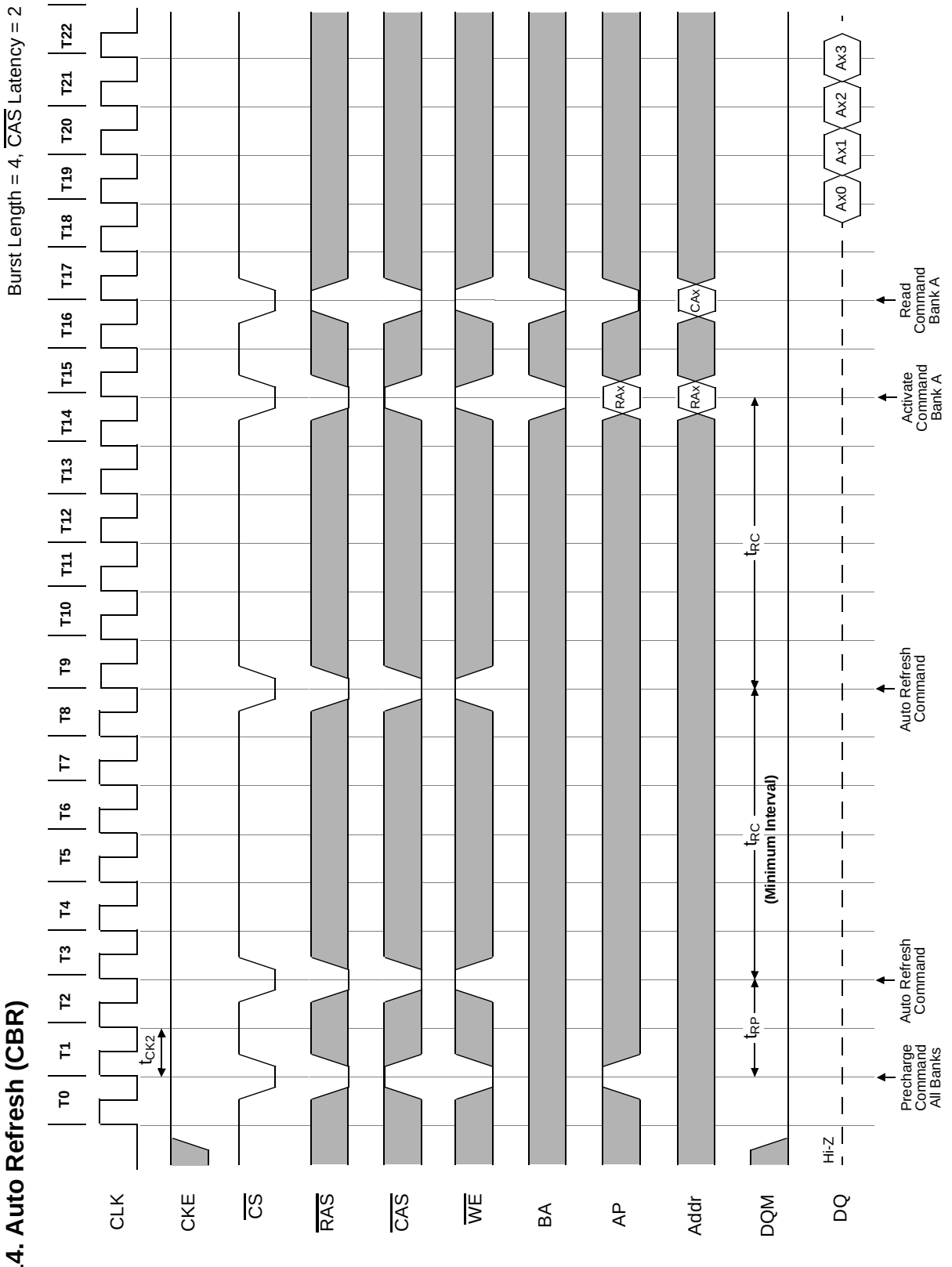
Burst Length = 4, $\overline{CAS}$ Latency = 3



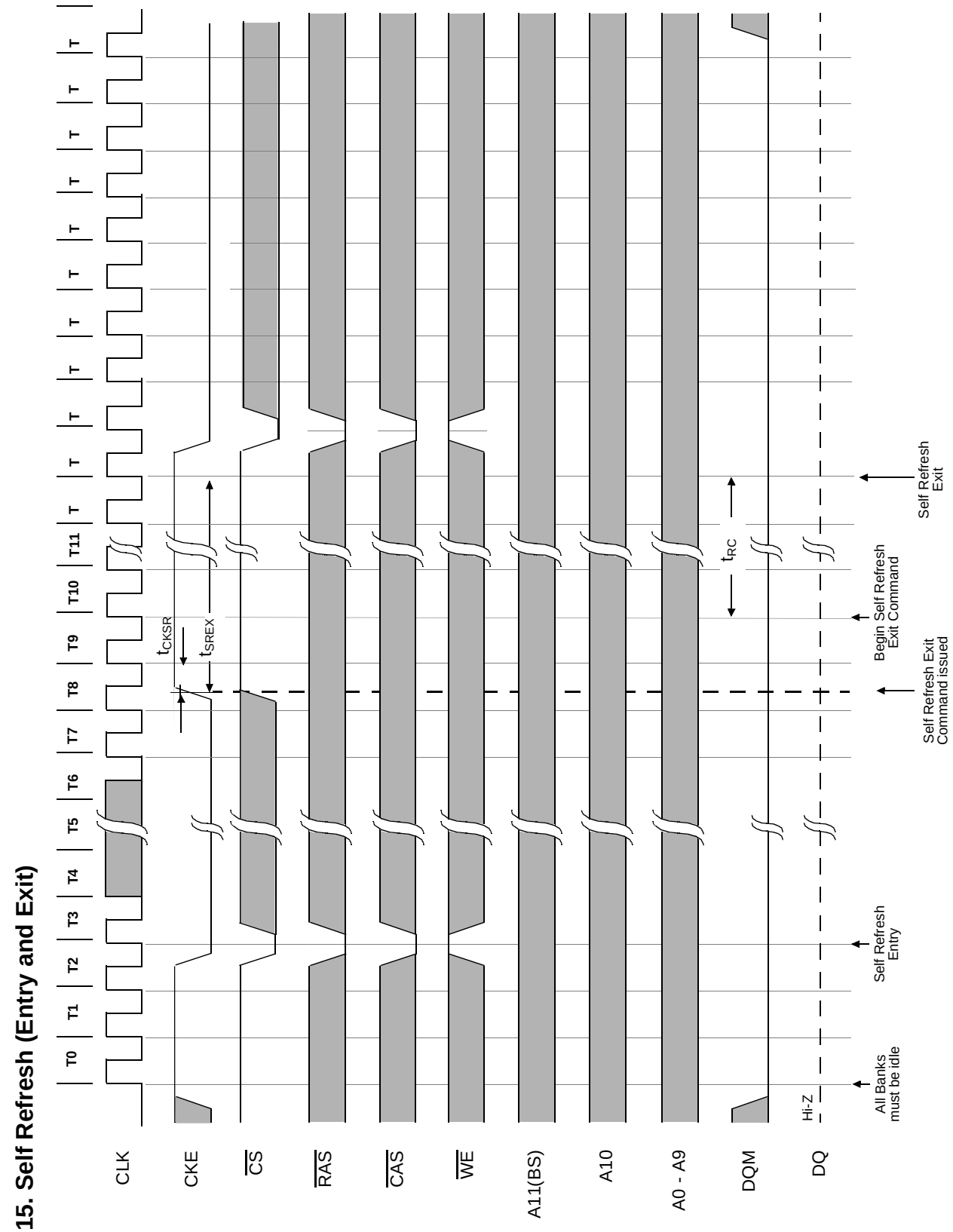
13. Power Down Mode and Clock Suspend



14. Auto Refresh (CBR)

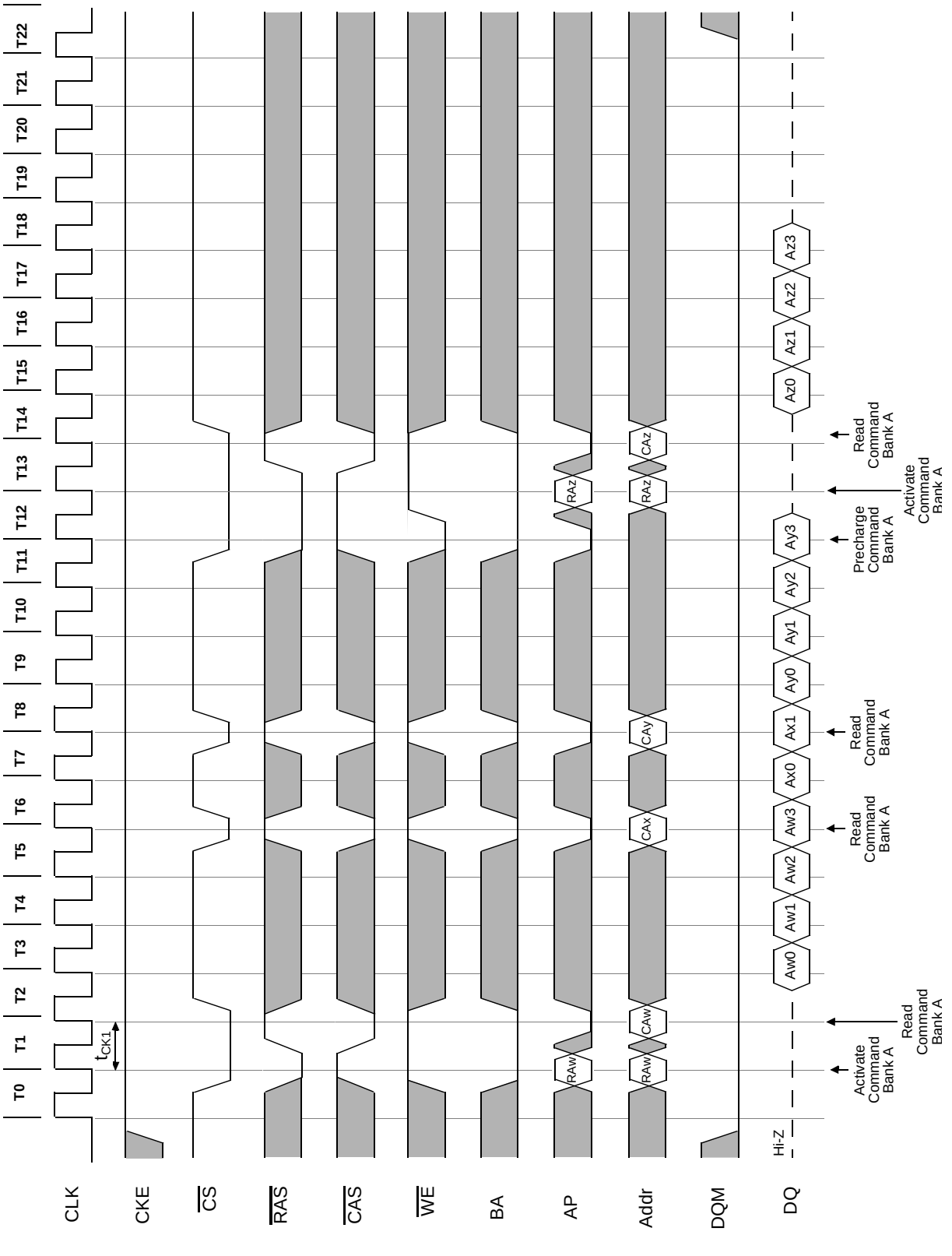


15. Self Refresh (Entry and Exit)



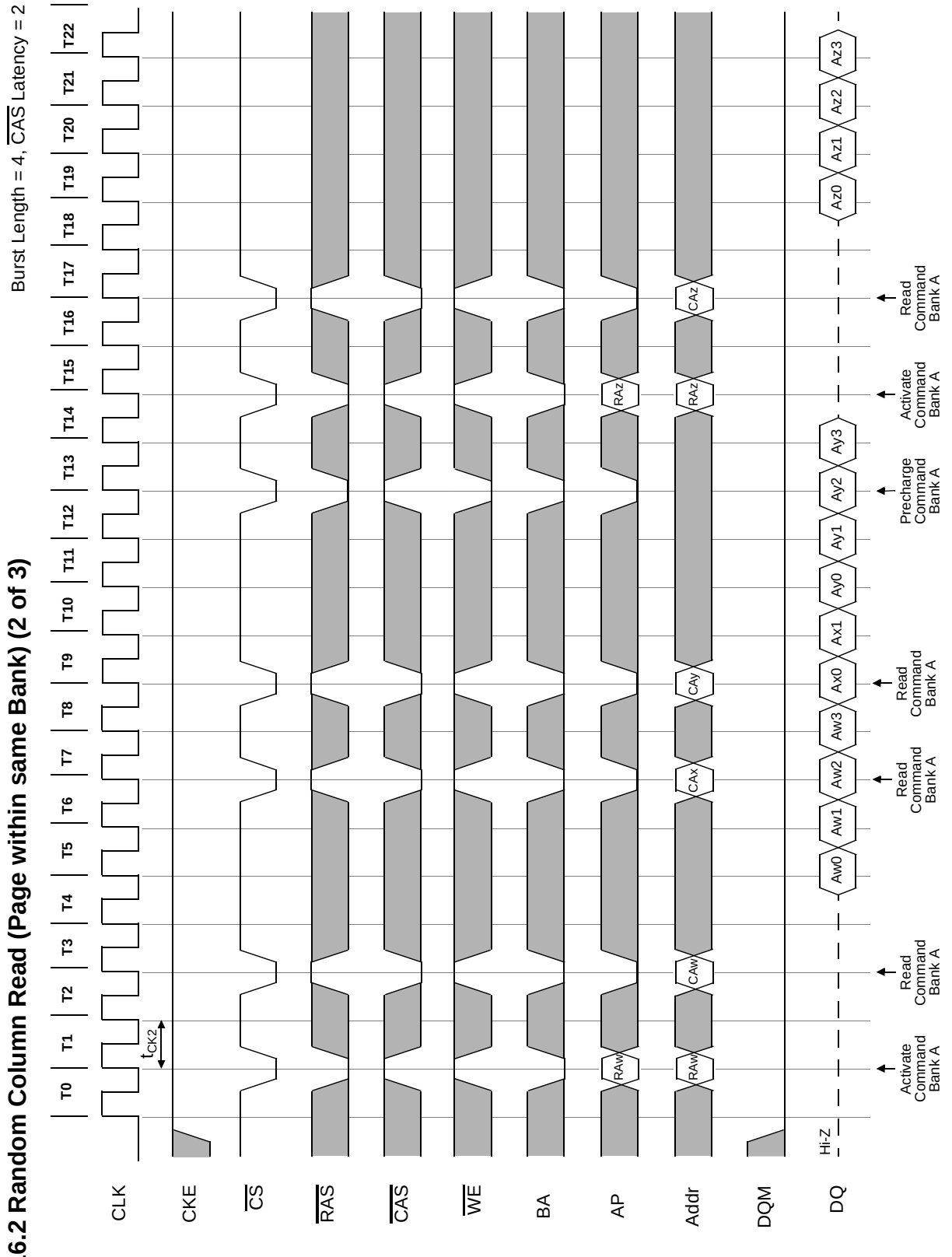
16.1 Random Column Read (Page within same Bank) (1 of 3)

Burst Length = 4, $\overline{CAS}$ Latency = 1



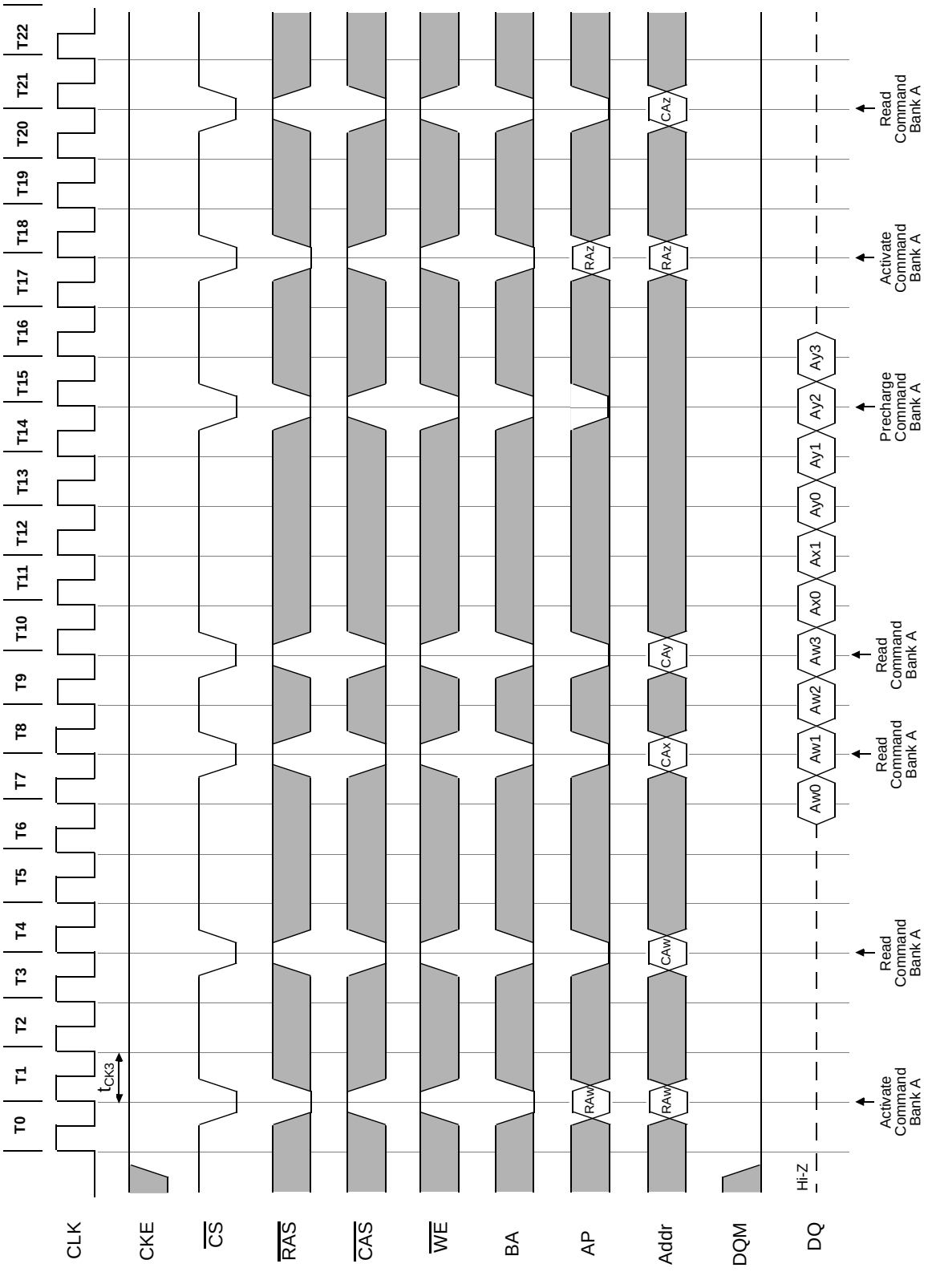
16.2 Random Column Read (Page within same Bank) (2 of 3)

Burst Length = 4, $\overline{CAS}$ Latency = 2



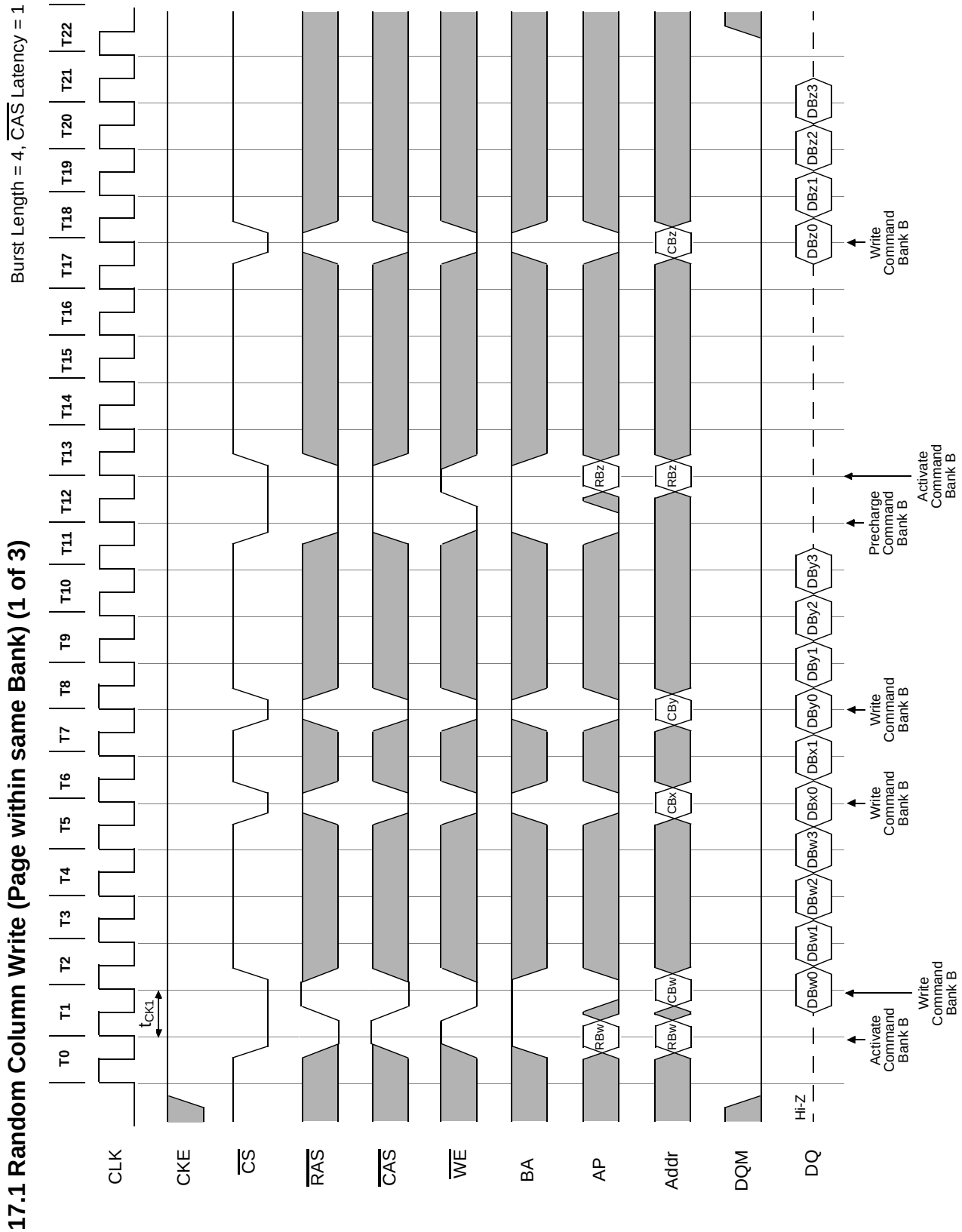
16.3 Random Column Read (Page within same Bank) (3 of 3)

Burst Length = 4, $\overline{CAS}$ Latency = 3

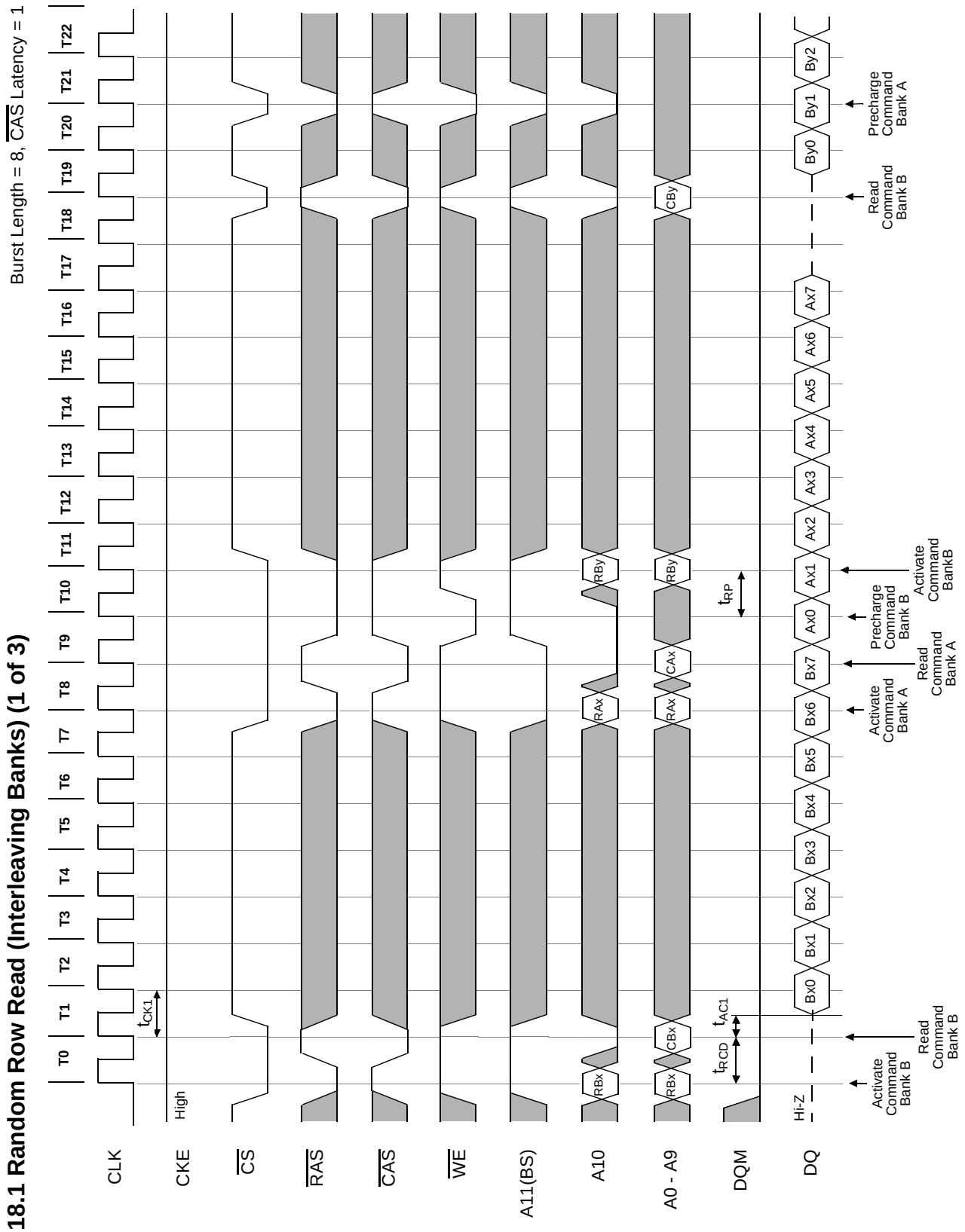


17.1 Random Column Write (Page within same Bank) (1 of 3)

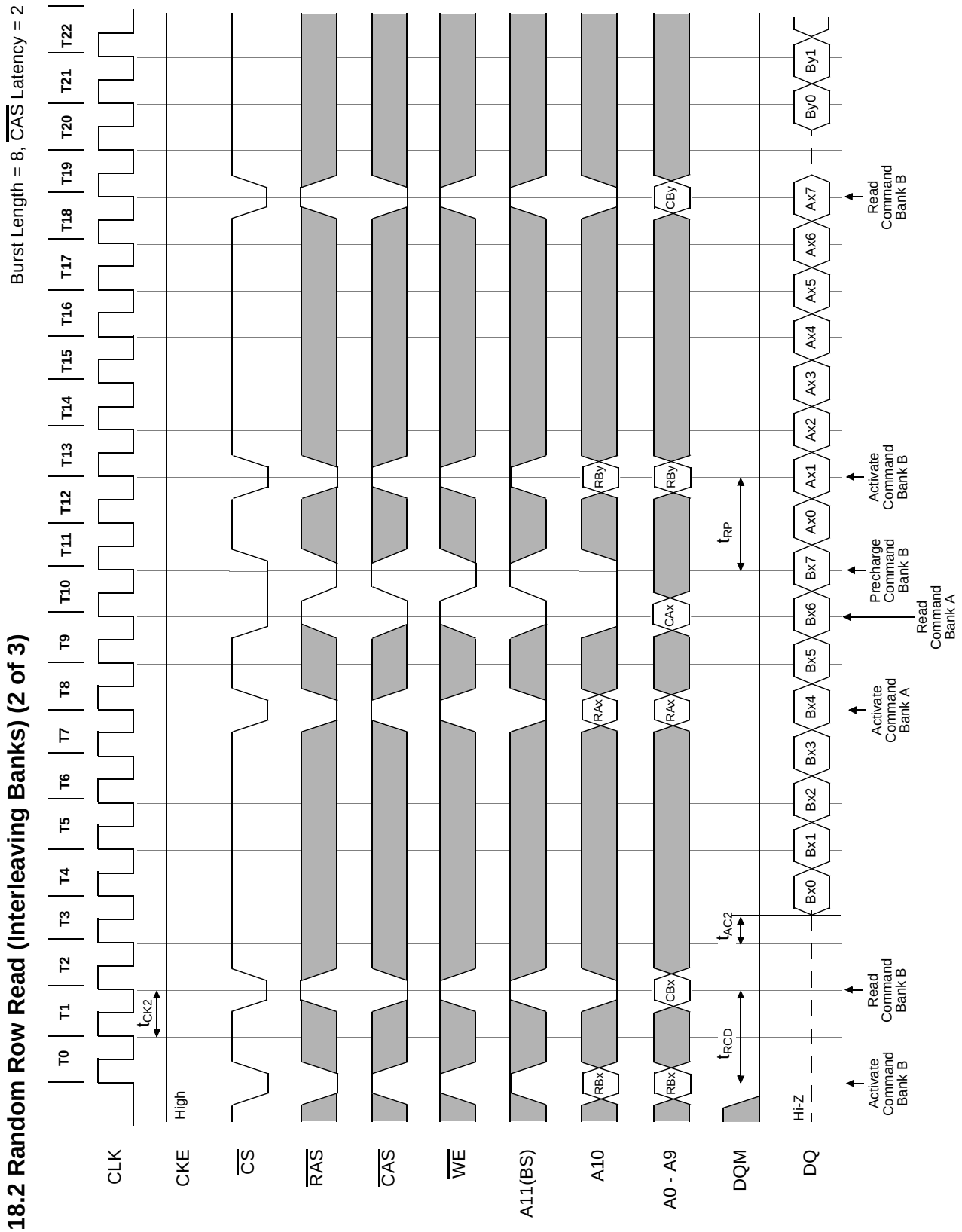
Burst Length = 4, $\overline{CAS}$ Latency = 1



18.1 Random Row Read (Interleaving Banks) (1 of 3)

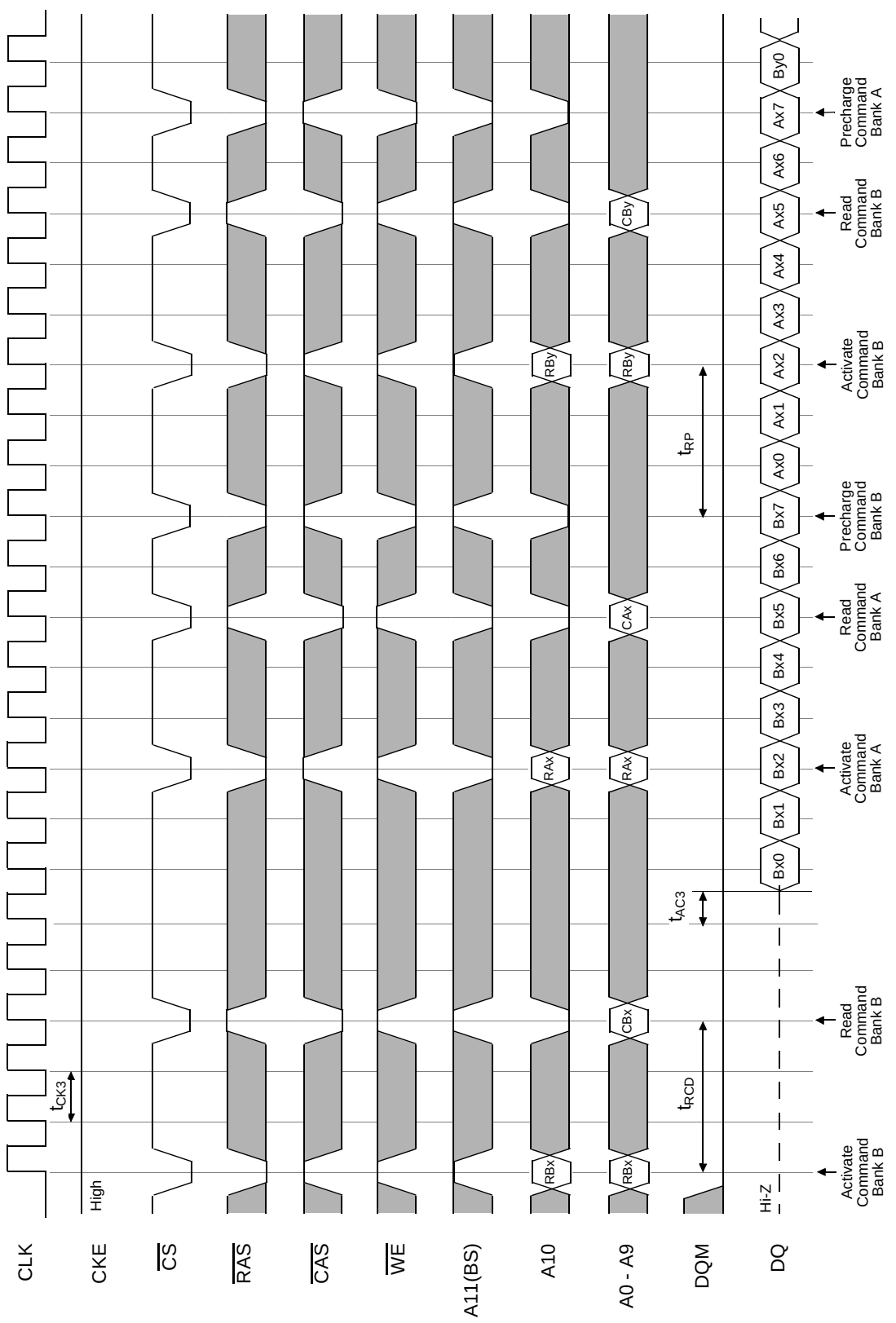


18.2 Random Row Read (Interleaving Banks) (2 of 3)



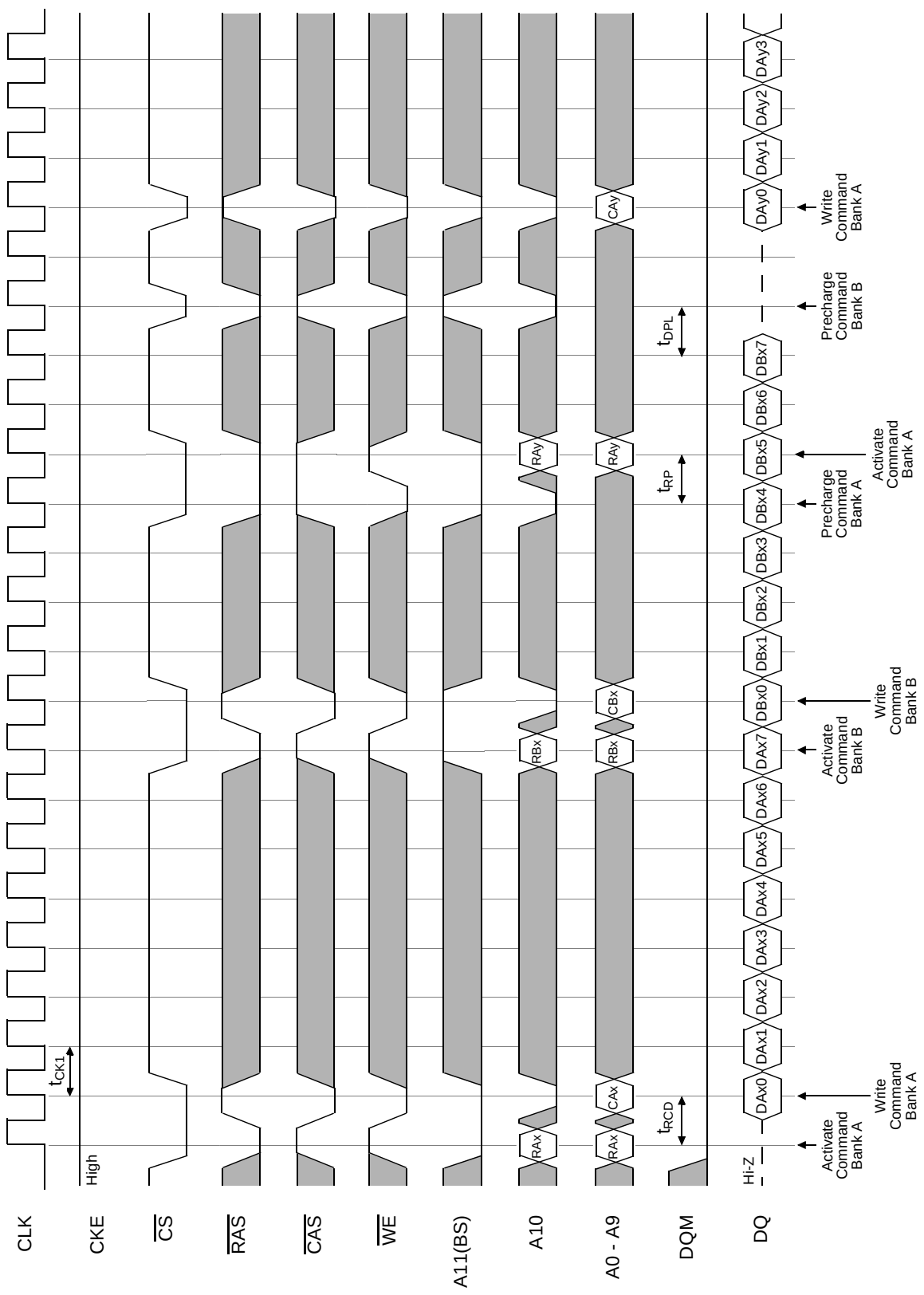
18. 3 Random Row Read (Interleaving Banks) (3 of 3)

Burst Length = 8, $\overline{CAS}$ Latency = 3



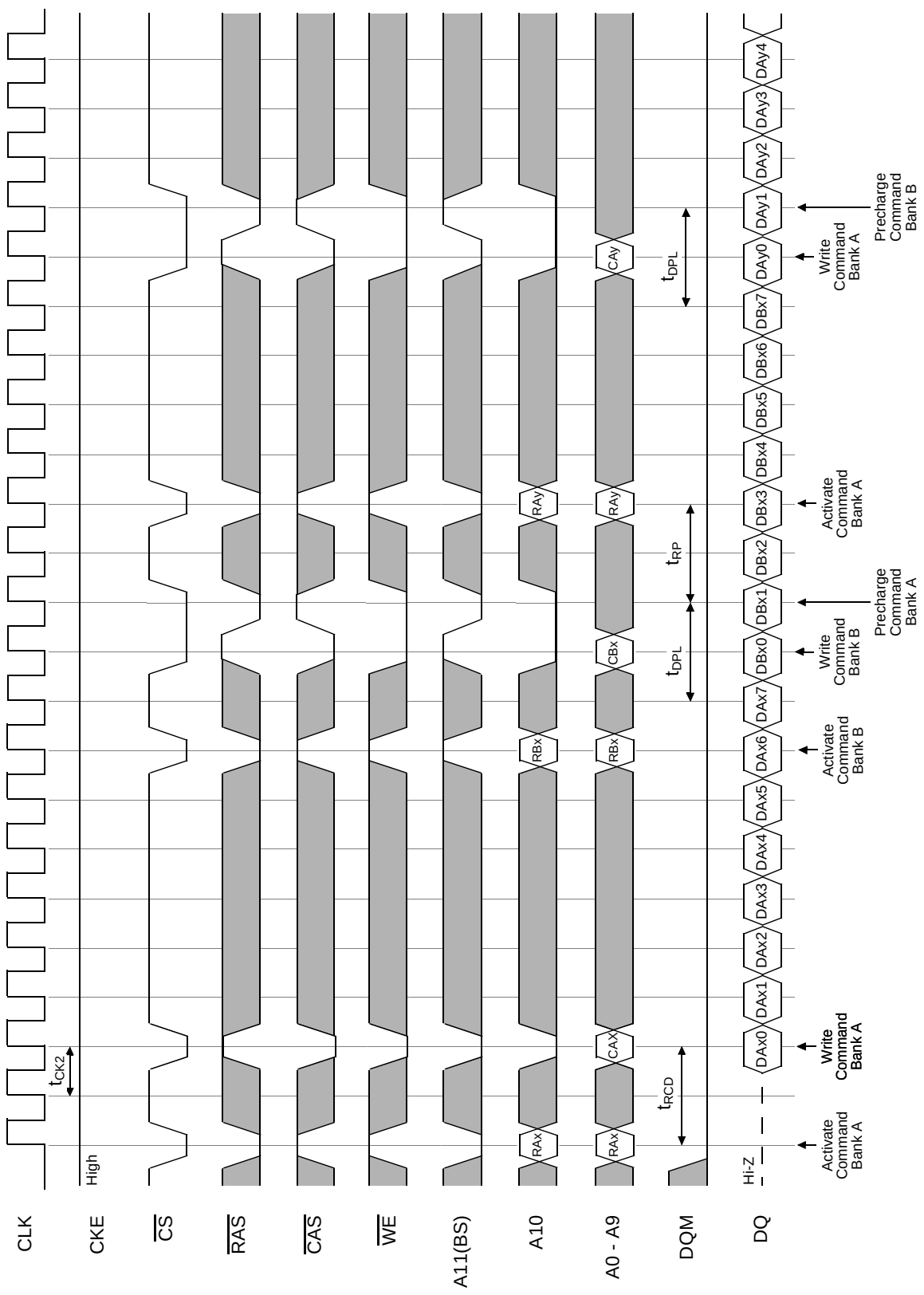
19.1 Random Row Write (Interleaving Banks) (1 of 3)

Burst Length = 8, $\overline{CAS}$ Latency = 1



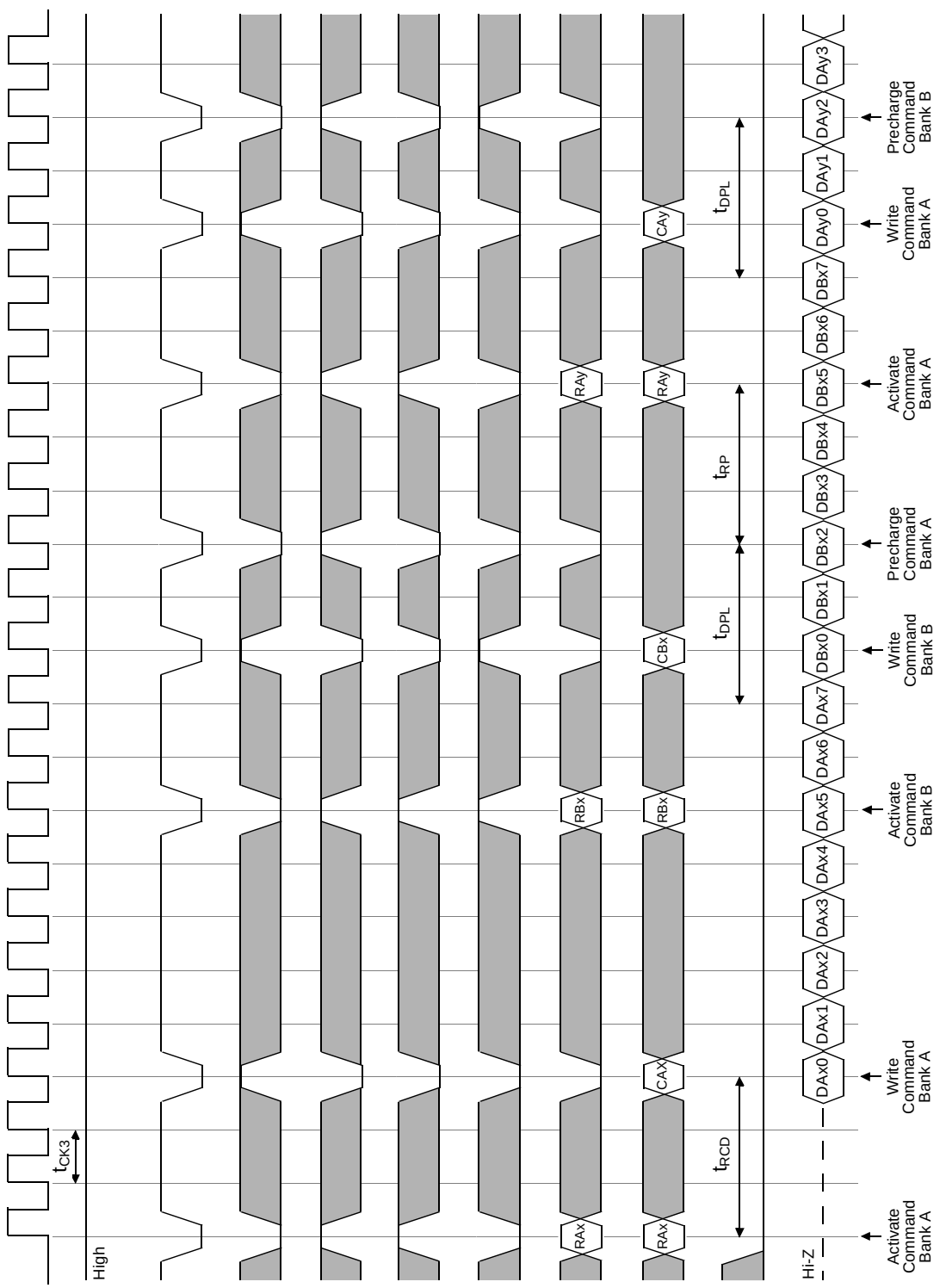
19.2 Random Row Write (Interleaving Banks) (2 of 3)

Burst Length = 8, $\overline{CAS}$ Latency = 2



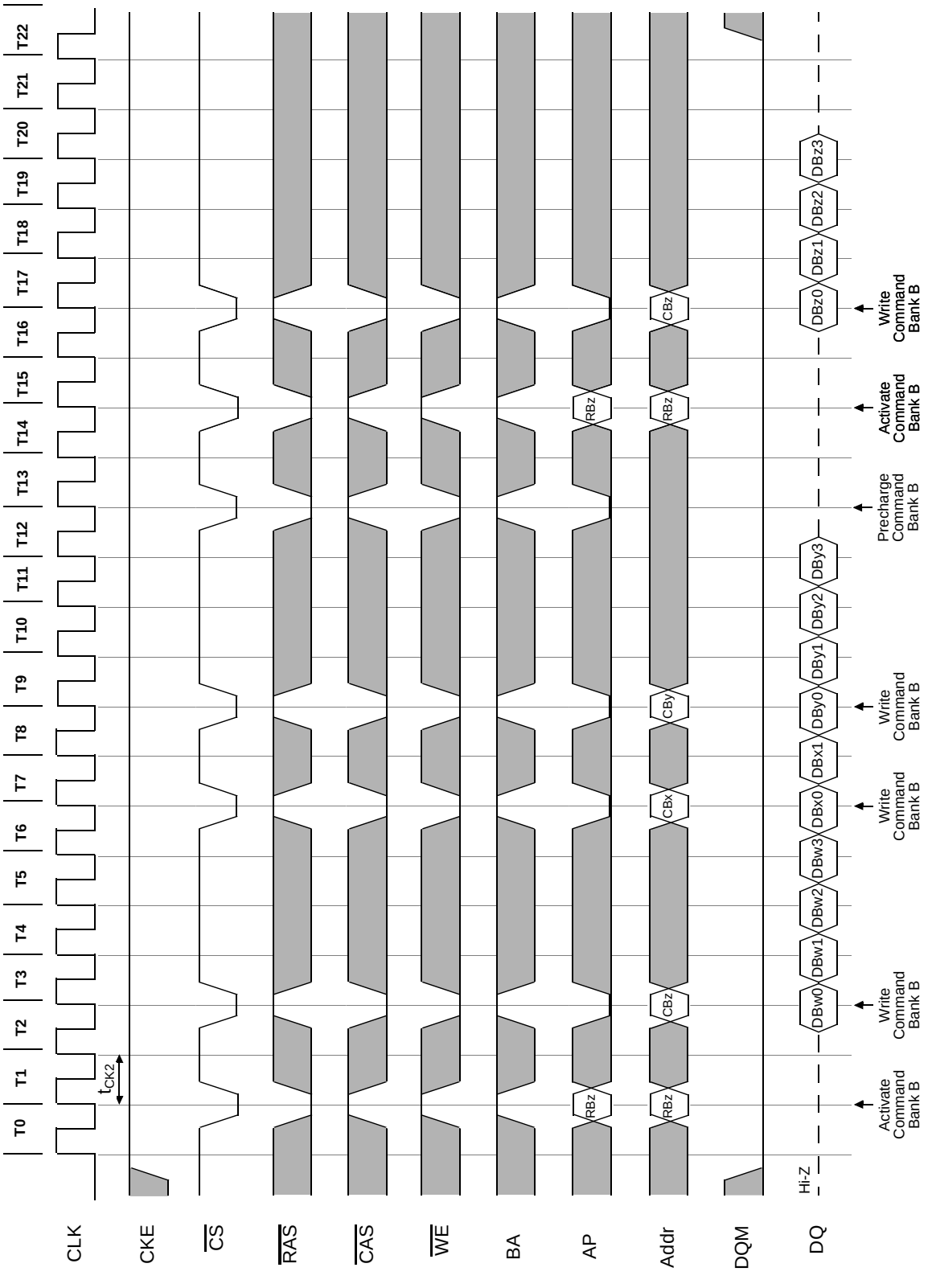
19.3 Random Row Write (Interleaving Banks) (3 of 3)

Burst Length = 8, $\overline{CAS}$ Latency = 3



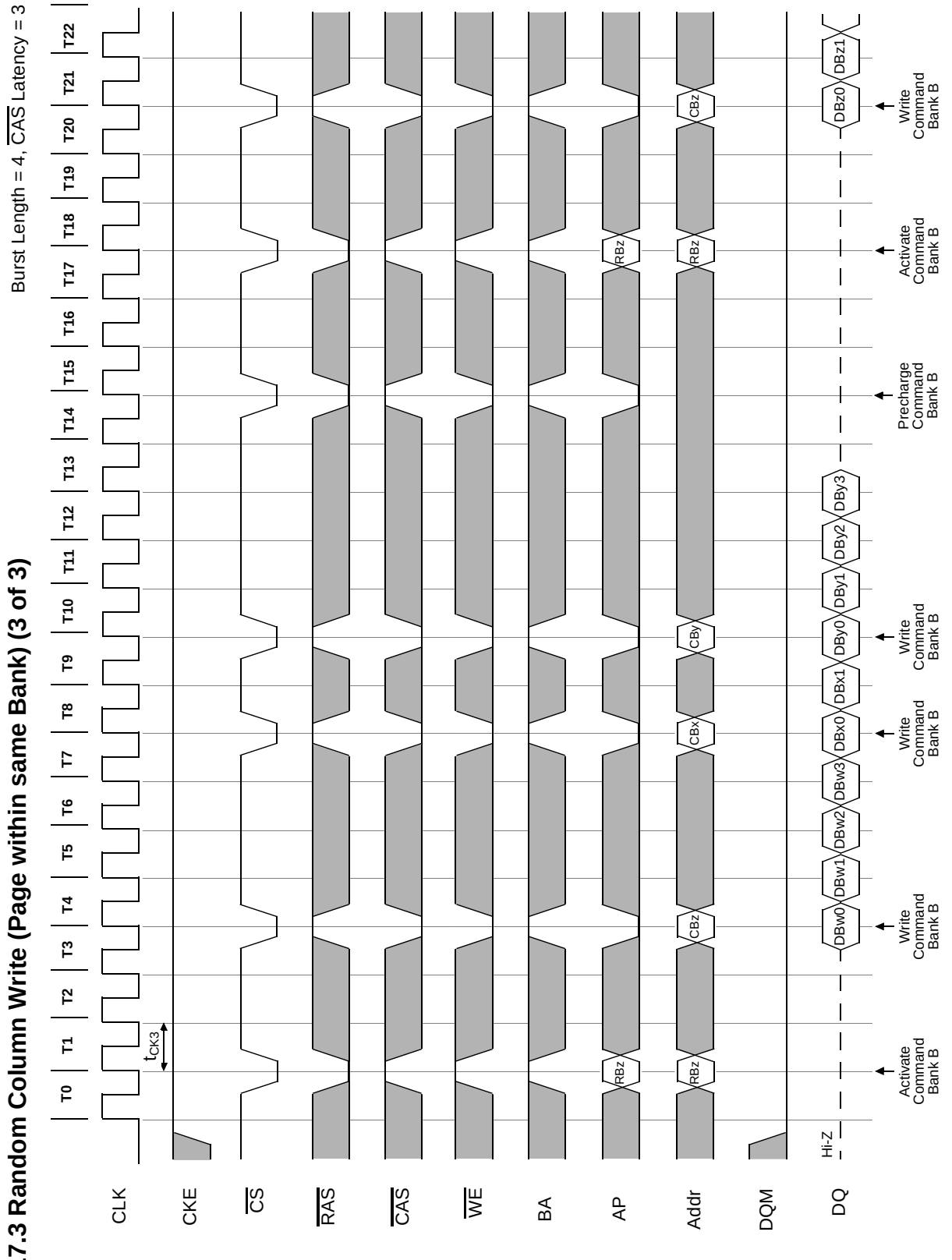
17.2 Random Column Write (Page within same Bank) (2 of 3)

Burst Length = 4, $\overline{CAS}$ Latency = 2

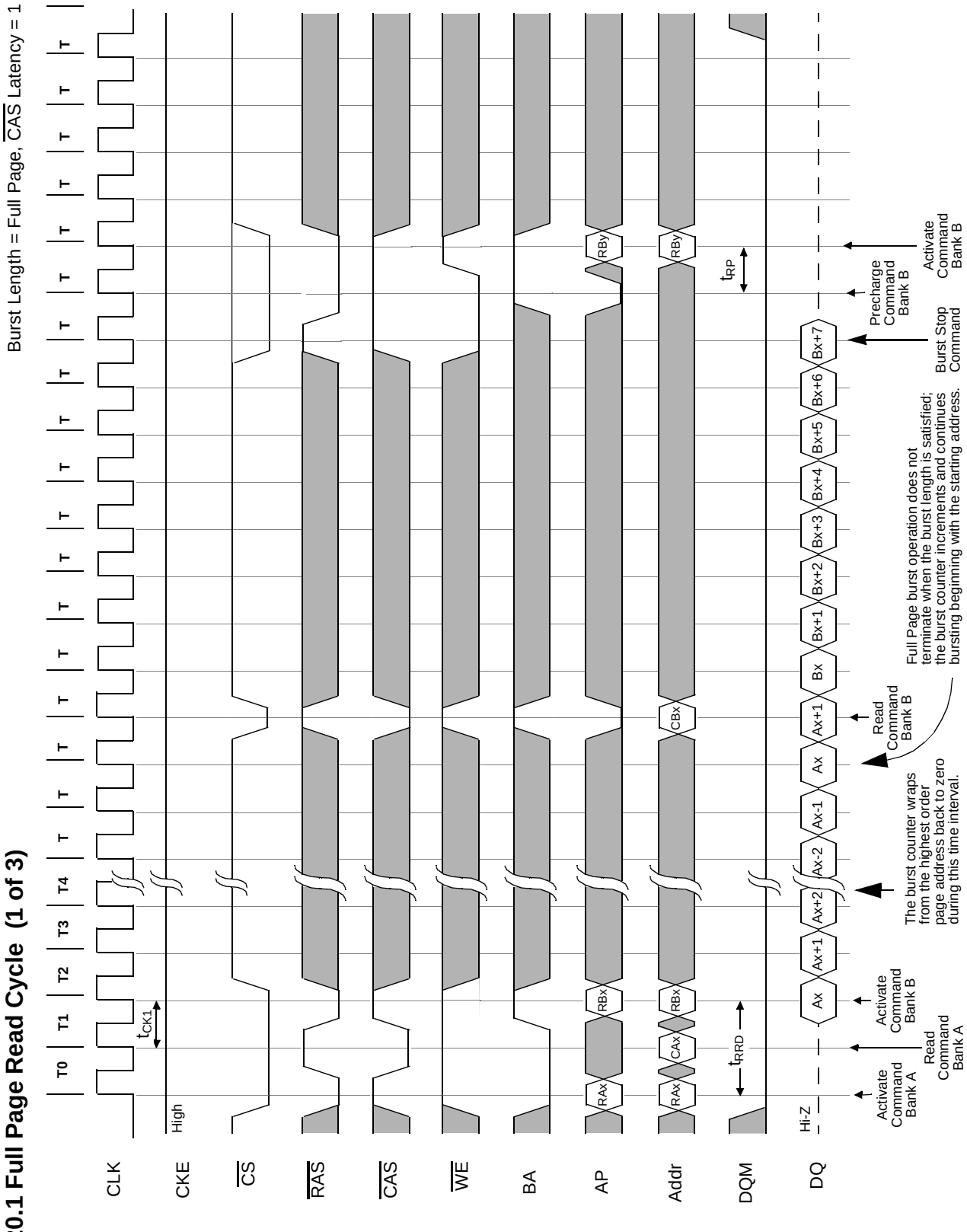


17.3 Random Column Write (Page within same Bank) (3 of 3)

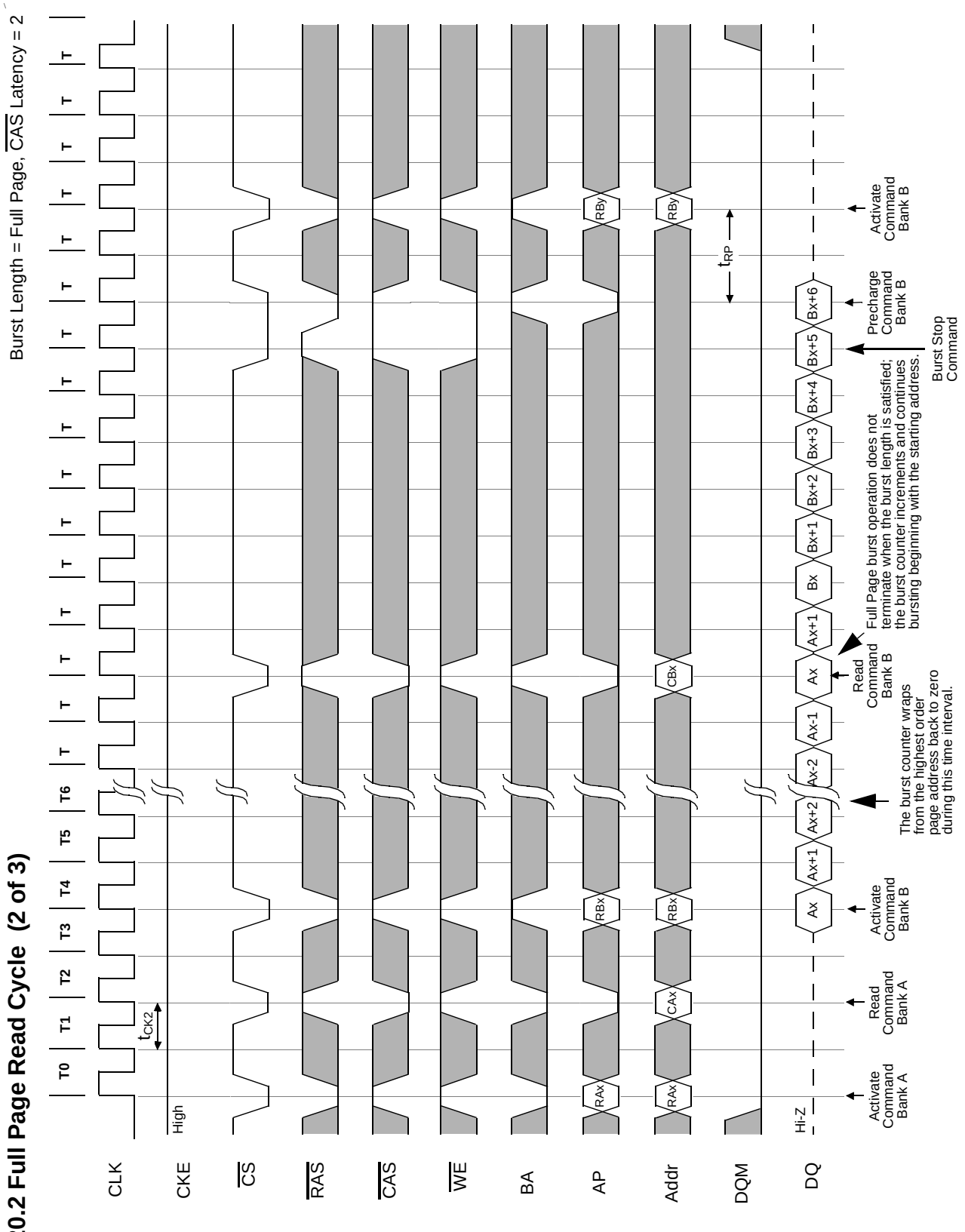
Burst Length = 4, $\overline{CAS}$ Latency = 3



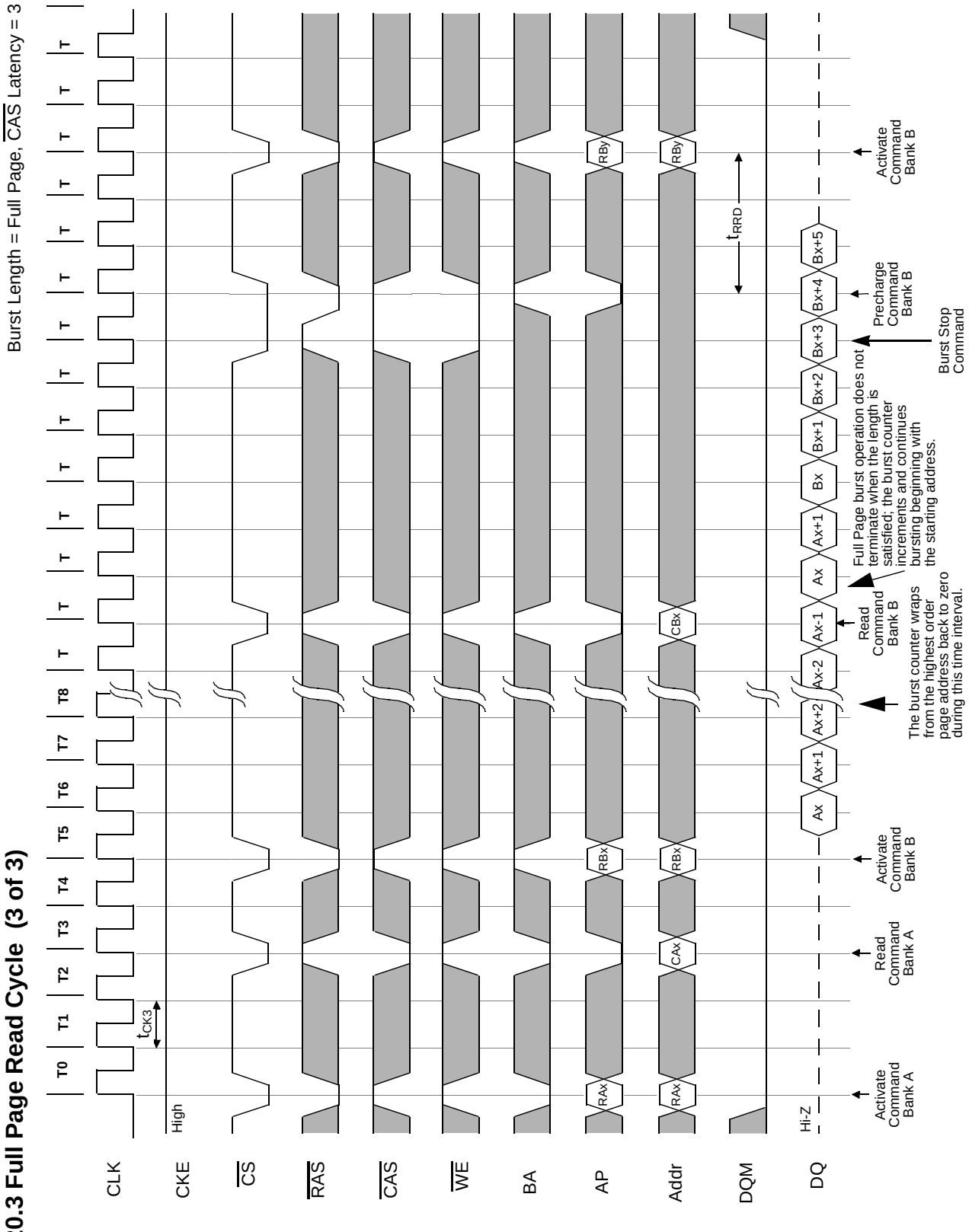
20.1 Full Page Read Cycle (1 of 3)



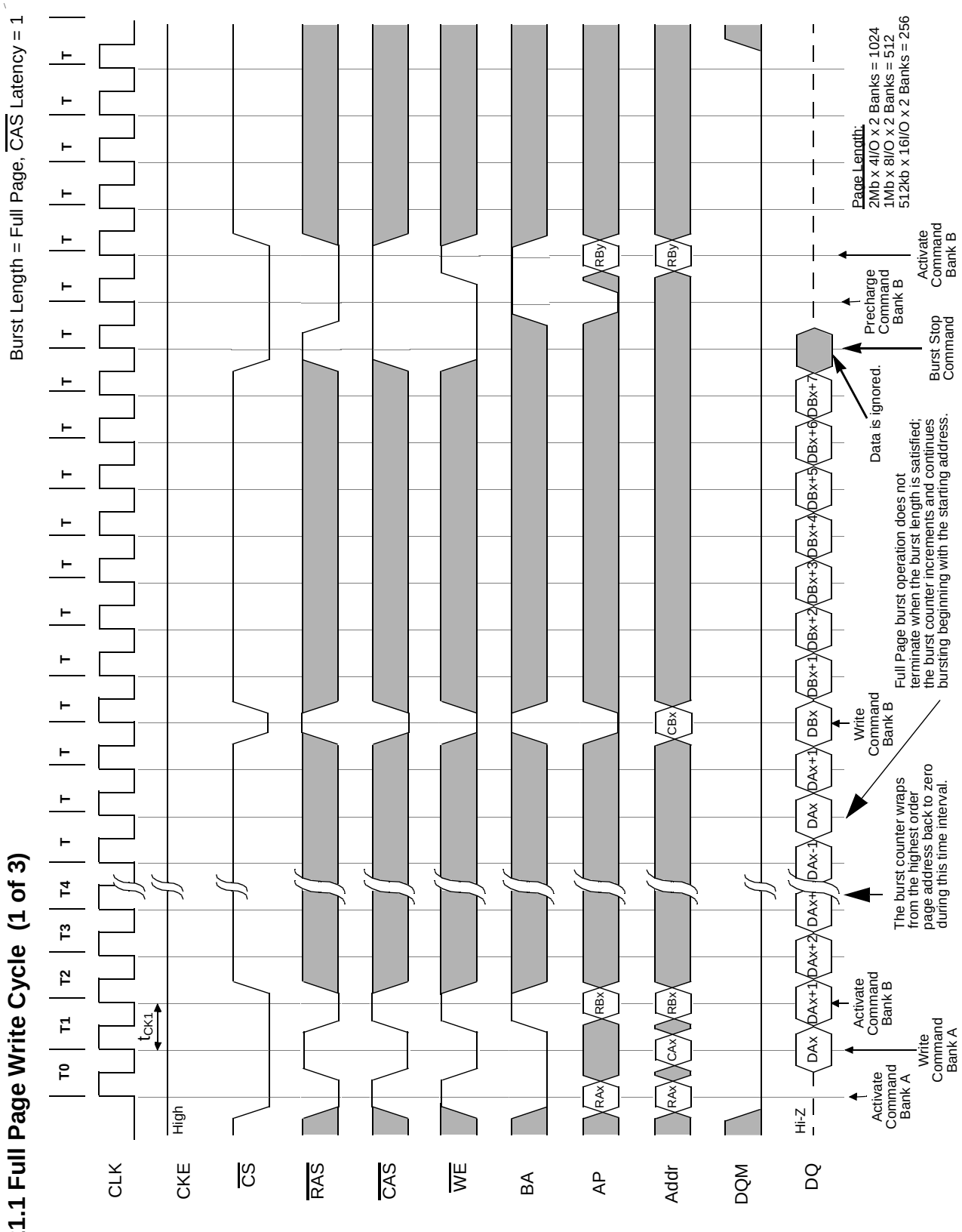
20.2 Full Page Read Cycle (2 of 3)



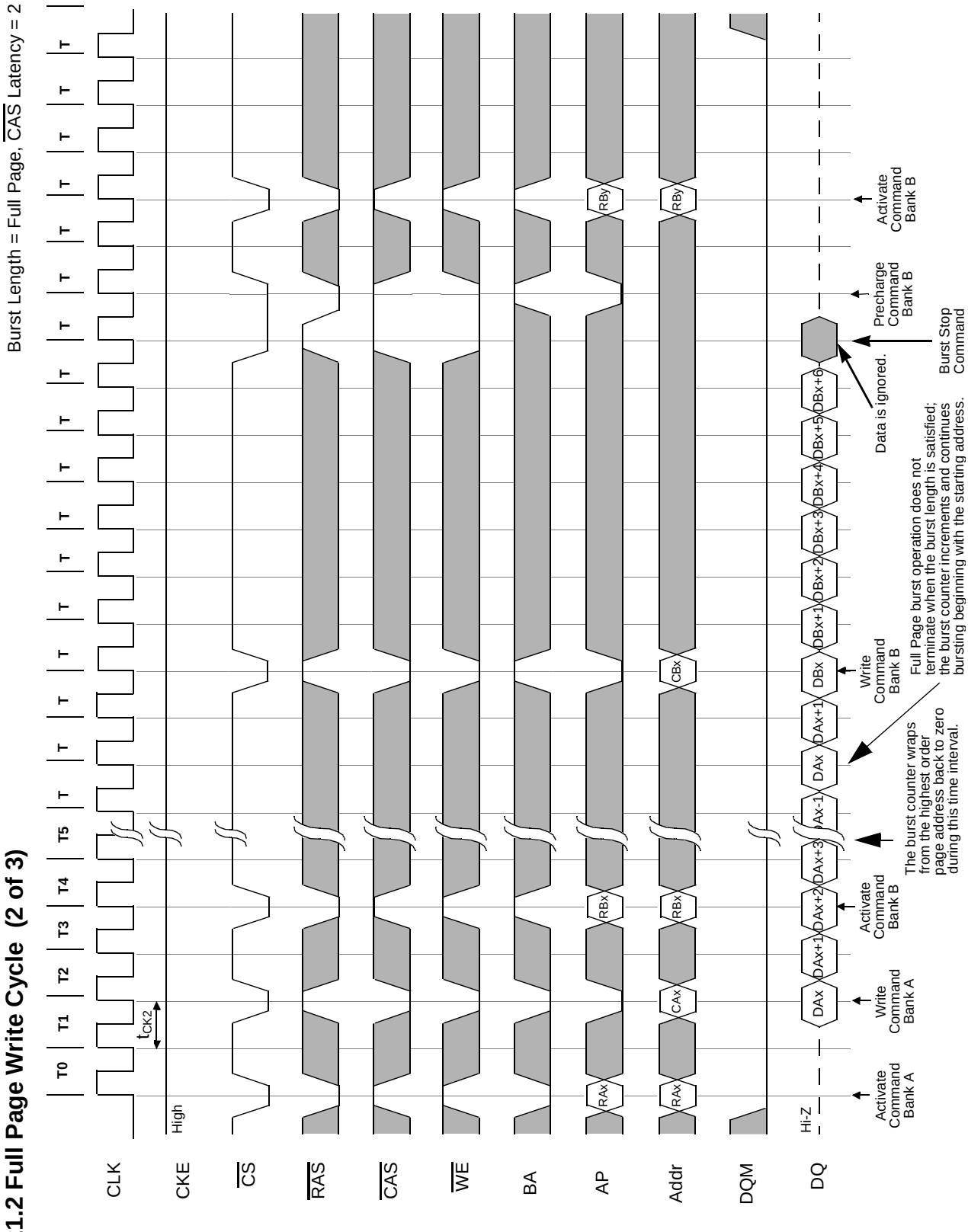
20.3 Full Page Read Cycle (3 of 3)



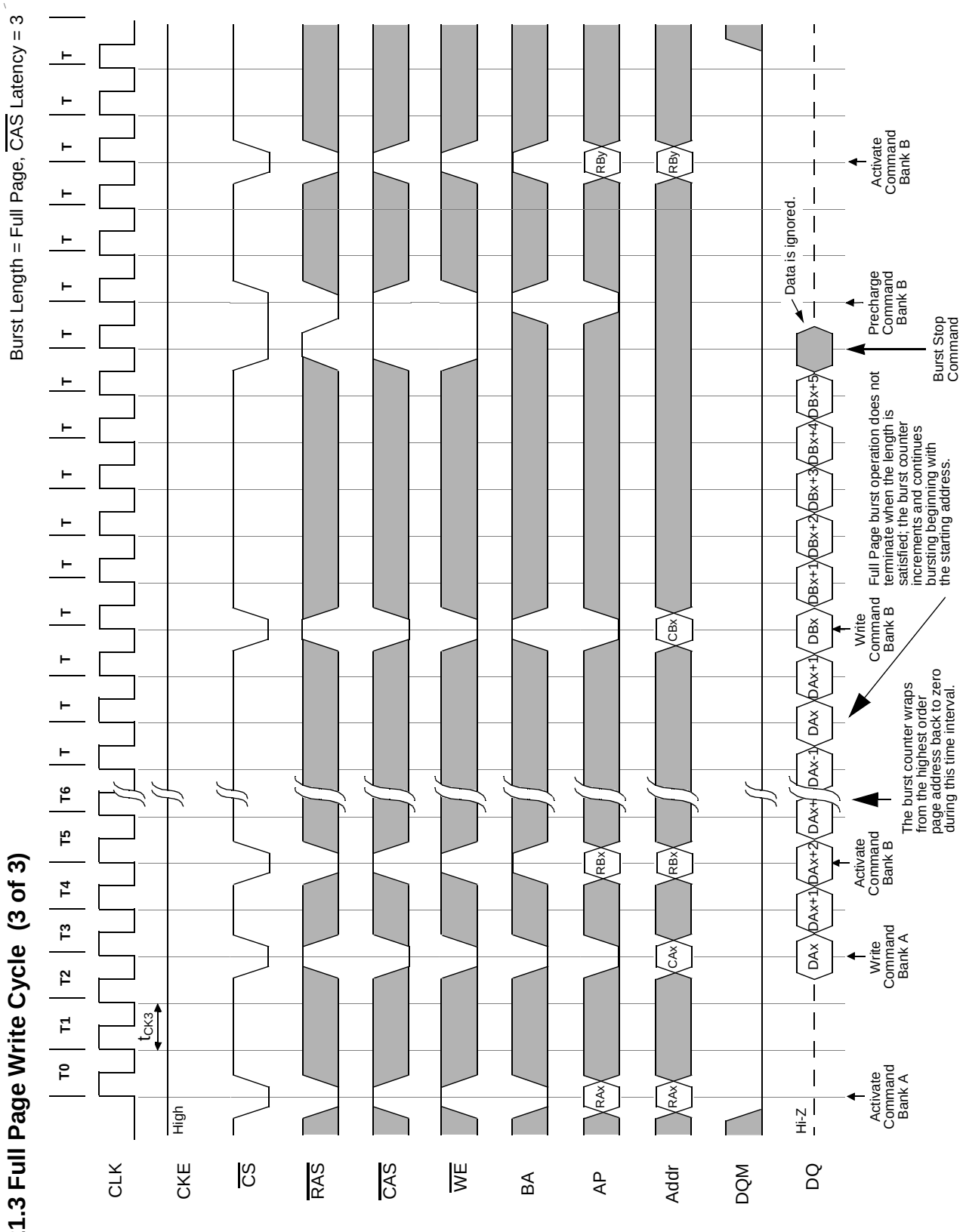
21.1 Full Page Write Cycle (1 of 3)



21.2 Full Page Write Cycle (2 of 3)

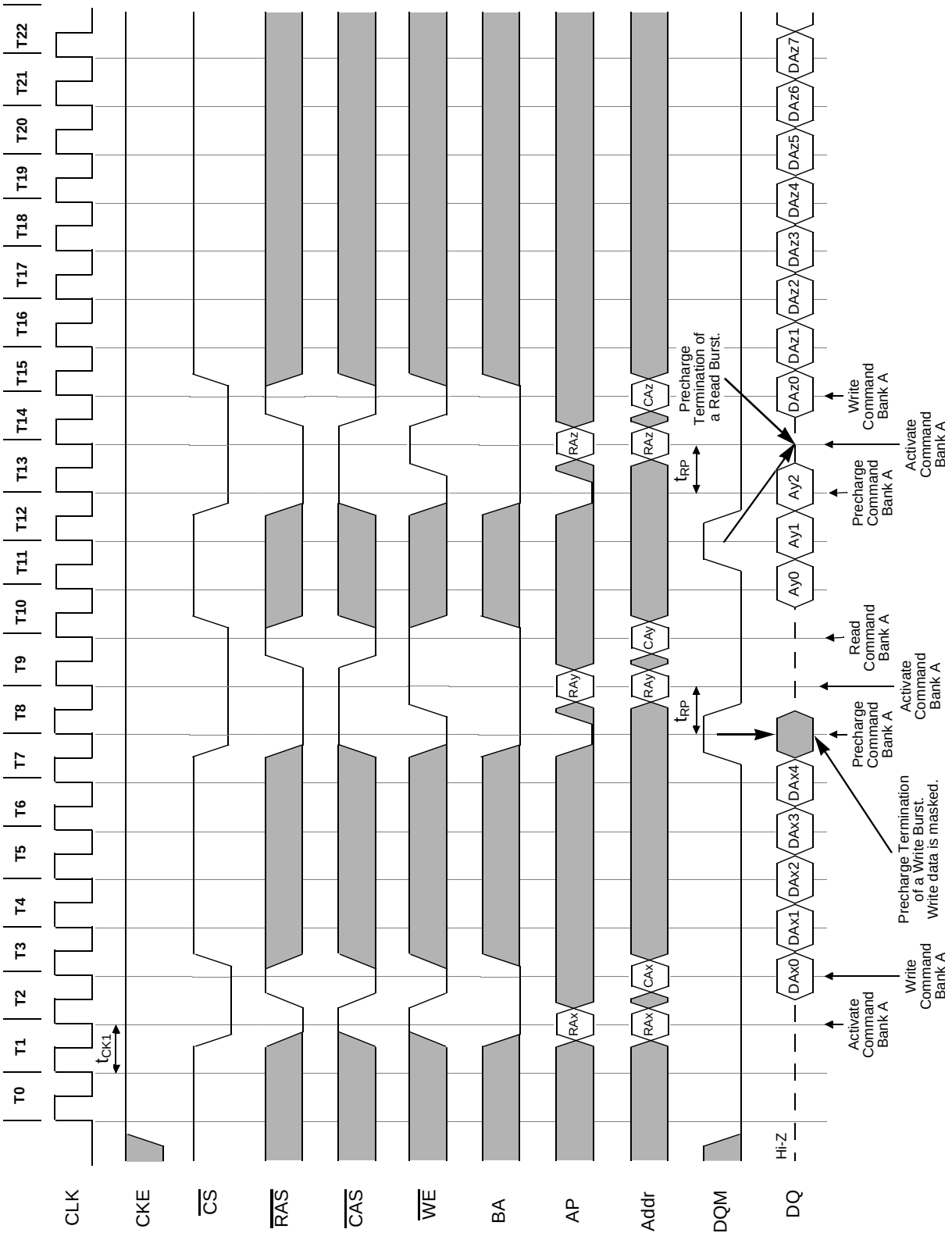


21.3 Full Page Write Cycle (3 of 3)

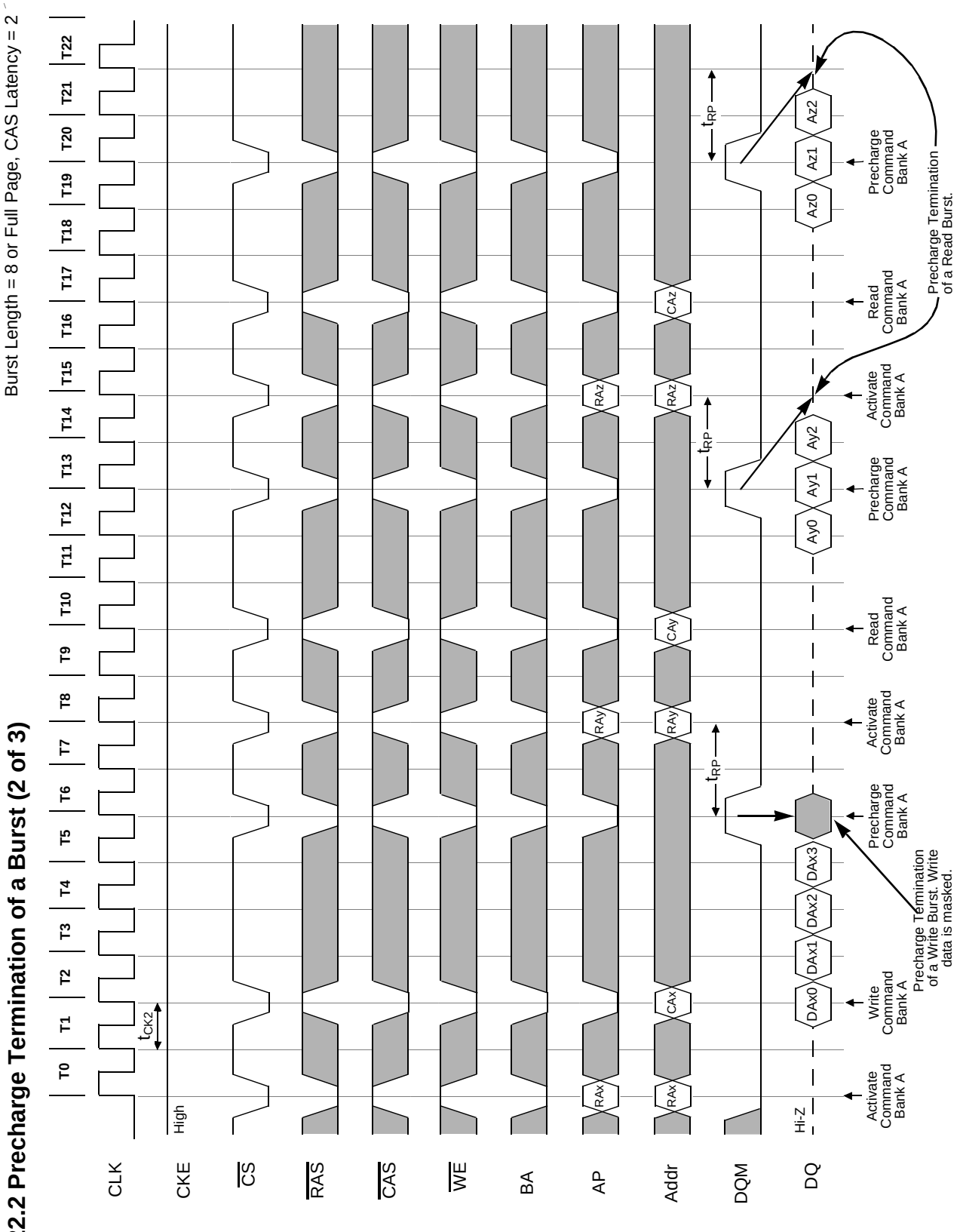


22.1 Precharge Termination of a Burst (1 of 3)

Burst Length = Full Page, CAS Latency = 1

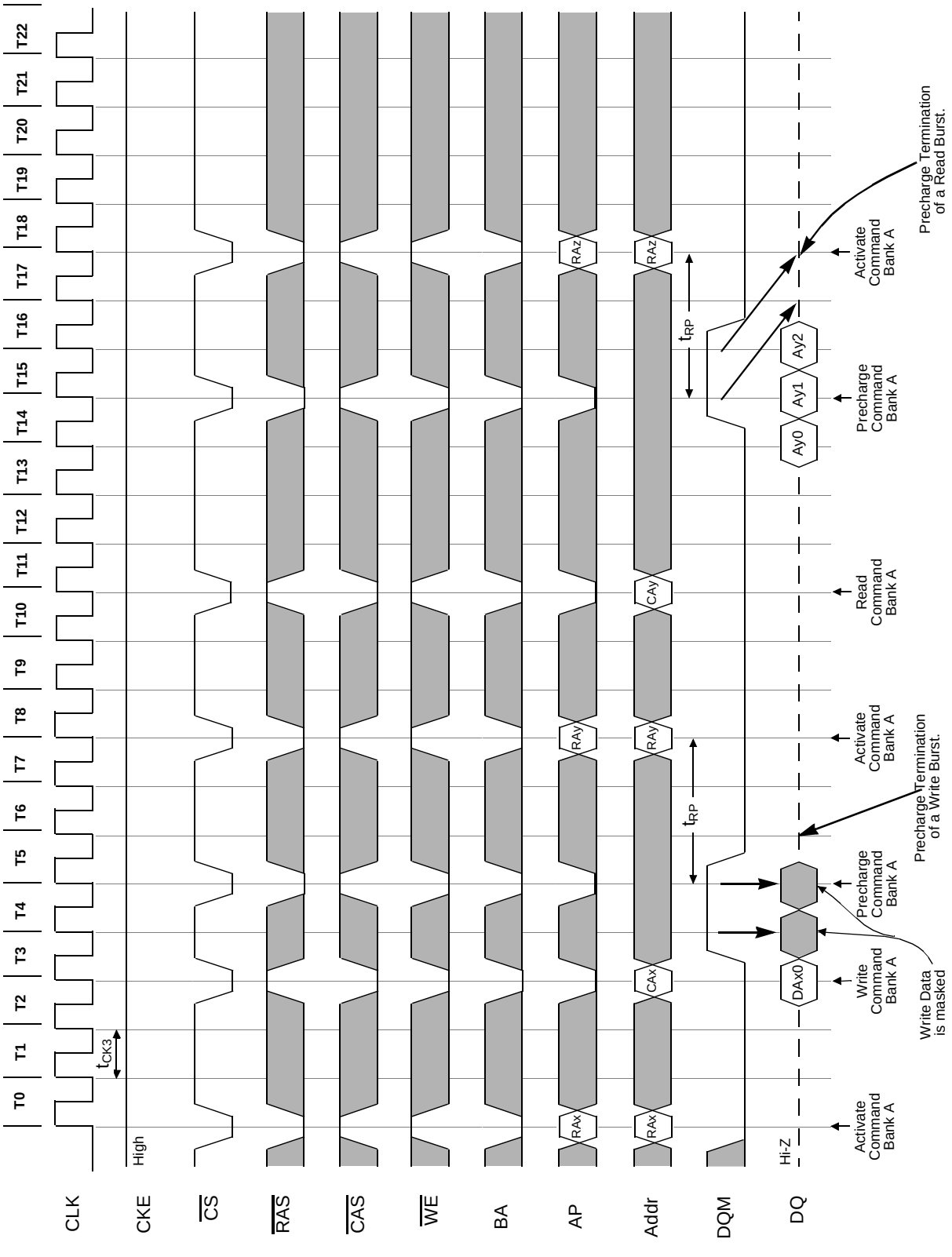


22.2 Precharge Termination of a Burst (2 of 3)



22.3 Precharge Termination of a Burst (3 of 3)

Burst Length = 4,8 or Full Page, CAS Latency = 3



Complete List of Operation Commands

SDRAM FUNCTION TRUTH TABLE

CURRENT STATE[1]	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BS	Addr	ACTION
Idle	H	X	X	X	X	X	NOP or Power Down
	L	H	H	H	X	X	NOP
	L	H	H	L	BS	X	ILLEGAL[2]
	L	H	L	X	BS	X	ILLEGAL[2]
	L	L	H	H	BS	RA	Row (&Bank) Active; Latch Row Address
	L	L	H	L	BS	AP	NOP[4]
	L	L	L	H	X	X	Auto-Refresh or Self-Refresh[5]
	L	L	L	L	Op-	Code	Mode reg. Access[5]
Row Active	H	X	X	X	X	X	NOP
	L	H	H	X	X	X	NOP
	L	H	L	H	BS	CA,AP	Begin Read; Latch CA; Determine AP
	L	H	L	L	BS	CA,AP	Begin Write; Latch CA; Determine AP
	L	L	H	H	BS	X	ILLEGAL[2]
	L	L	H	L	BS	AP	Precharge
	L	L	L	X	X	X	ILLEGAL
Read	H	X	X	X	X	X	NOP (Continue Burst to End;>Row Active)
	L	H	H	H	X	X	NOP (Continue Burst to End;>Row Active)
	L	H	H	L	BS	X	Burst Stop Command > Row Active
	L	H	L	H	BS	CA,AP	Term Burst, New Read, Determine AP[3]
	L	H	L	L	BS	CA,AP	Term Burst, Start Write, Determine AP[3]
	L	L	H	H	BS	X	ILLEGAL[2]
	L	L	H	L	BS	AP	Term Burst, Precharge
	L	L	L	X	X	X	ILLEGAL
Write	H	X	X	X	X	X	NOP (Continue Burst to End;>Row Active)
	L	H	H	H	X	X	NOP (Continue Burst to End;>Row Active)
	L	H	H	L	BS	X	Burst Stop Command > Row Active
	L	H	L	H	BS	CA,AP	Term Burst, Start Read, Determine AP[3]
	L	H	L	L	BS	CA,AP	Term Burst, New Write, Determine AP[3]
	L	L	H	H	BS	X	ILLEGAL[2]
	L	L	H	L	BS	AP	Term Burst, Precharge[3]
	L	L	L	X	X	X	ILLEGAL
Read with Auto Precharge	H	X	X	X	X	X	NOP (Continue Burst to End;> Precharge)
	L	H	H	H	X	X	NOP (Continue Burst to End;> Precharge)
	L	H	H	L	BS	X	ILLEGAL[2]
	L	H	L	H	BS	X	ILLEGAL[2]
	L	H	L	L	X	X	ILLEGAL
	L	L	H	H	BS	X	ILLEGAL[2]
	L	L	H	L	BS	AP	ILLEGAL[2]
	L	L	L	X	X	X	ILLEGAL

SDRAM FUNCTION TRUTH TABLE(continued)

CURRENT STATE[1]	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{BS}$	Addr	ACTION
Write	H	X	X	X	X	X	NOP (Continue Burst to End;> Precharge)
with	L	H	H	H	X	X	NOP (Continue Burst to End;> Precharge)
Auto	L	H	H	L	BS	X	ILLEGAL[2]
Precharge	L	H	L	H	BS	X	ILLEGAL[2]
	L	H	L	L	X	X	ILLEGAL
	L	L	H	H	BS	X	ILLEGAL[2]
	L	L	H	L	BS	AP	ILLEGAL[2]
	L	L	L	X	X	X	ILLEGAL
Precharging	H	X	X	X	X	X	NOP;> Idle after tRP
	L	H	H	H	X	X	NOP;> Idle after tRP
	L	H	H	L	BS	X	ILLEGAL[2]
	L	H	L	X	BS	X	ILLEGAL[2]
	L	L	H	H	BS	X	ILLEGAL[2]
	L	L	H	L	BS	AP	NOP[4]
	L	L	L	X	X	X	ILLEGAL
Row	H	X	X	X	X	X	NOP;> Row Active after tRCD
Activating	L	H	H	H	X	X	NOP;> Row Active after tRCD
	L	H	H	L	BS	X	ILLEGAL[2]
	L	H	L	X	BS	X	ILLEGAL[2]
	L	L	H	H	BS	X	ILLEGAL[2]
	L	L	H	L	BS	AP	ILLEGAL[2]
	L	L	L	X	X	X	ILLEGAL
Write	H	X	X	X	X	X	NOP
Recovering	L	H	H	H	X	X	NOP
	L	H	H	L	BS	X	ILLEGAL[2]
	L	H	L	X	BS	X	ILLEGAL[2]
	L	L	H	H	BS	X	ILLEGAL[2]
	L	L	H	L	BS	AP	ILLEGAL[2]
	L	L	L	X	X	X	ILLEGAL
Refreshing	H	X	X	X	X	X	NOP;> Idle after tRC
	L	H	H	X	X	X	NOP;> Idle after tRC
	L	H	L	X	X	X	ILLEGAL
	L	L	H	X	X	X	ILLEGAL
	L	L	L	X	X	X	ILLEGAL
Mode	H	X	X	X	X	X	NOP
Register	L	H	H	H	X	X	NOP
	L	H	H	L	X	X	ILLEGAL
Accessing	L	H	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	ILLEGAL

CLOCK ENABLE (CKE) TRUTH TABLE:

STATE(n)	CKE n-1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Addr	ACTION
Self-Refresh[6]	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	EXIT Self-Refresh, Idle after tRC
	L	H	L	H	H	H	X	EXIT Self-Refresh, Idle after tRC
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP (Maintain Self-Refresh)
Power-Down	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	EXIT Power-Down, > Idle.
	L	H	L	H	H	H	X	EXIT Power-Down, > Idle.
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP (Maintain Low-Power Mode)
All. Banks Idle[7]	H	H	X	X	X	X	X	Refer to the function truth table
	H	L	H	X	X	X	X	Enter Power- Down
	H	L	L	H	H	H	X	Enter Power- Down
	H	L	L	H	H	L	X	ILLEGAL
	H	L	L	H	L	X	X	ILLEGAL
	H	L	L	L	H	X	X	ILLEGAL
	H	L	L	L	L	H	X	Enter Self-Refresh
	H	L	L	L	L	L	X	ILLEGAL
	L	L	X	X	X	X	X	NOP
Any State other than listed above	H	H	X	X	X	X	X	Refer to the function truth table
	H	L	X	X	X	X	X	Begin Clock Suspend next cycle[8]
	L	H	X	X	X	X	X	Exit Clock Suspend next cycle[8].
	L	L	X	X	X	X	X	Maintain Clock Suspend.

ABBREVIATIONS:

RA = Row Address BS = Bank Address

CA = Column Address AP = Auto Precharge

Notes for SDRAM function truth table :

1. Current State is state of the bank determined by BS. All entries assume that CKE was active (HIGH) during the preceding clock cycle.
2. Illegal to bank in specified state; Function may be legal in the bank indicated by BS, depending on the state of that bank.
3. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
4. NOP to bank precharging or in Idle state. May precharge bank(s) indicated by BS (andAP).
5. Illegal if any bank is not Idle.
6. CKE Low to High transition will re-enable CLK and other inputs asynchronously. A minimum setup time must be satisfied before any command other than EXIT.
7. Power-Down and Self-Refresh can be entered only from the All Banks Idle State.
8. Must be legal command as defined in the SDRAM function truth table.