

2M x 8 - Bit Dynamic RAM 2k Refresh (Fast Page Mode)

HYB5117800BJ/BSJ-50/-60
HYB3117800BJ(L)/BSJ(L)-50/-60

Advanced Information

- 2 097 152 words by 8-bit organization
- 0 to 70 °C operating temperature
- Fast Page Mode operation
- Performance:

		-50	-60	
t _{RAC}	$\overline{\text{RAS}}$ access time	50	60	ns
t _{CAC}	$\overline{\text{CAS}}$ access time	13	15	ns
t _{AA}	Access time from address	25	30	ns
t _{RC}	Read/Write cycle time	84	104	ns
t _{PC}	Fast page mode cycle time	35	40	ns

- Low power dissipation:

	HYB5117800		HYB3117800		
	-50	-60	-50	-60	
Power Supply	5 ± 10%		3.3 ± 0.3 V		
Active	440	385	288	252	mW
TTL Standby	11		7,2		mW
CMOS Standby	5,5		3,6		mW
CMOS Standby (L-version)	1,1		0,72		mW

- Read, write, read-modify-write, $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ -only refresh, hidden refresh, test mode
- Self Refresh (L-versions only)
- All inputs, outputs and clocks fully TTL (5V versions) and LV-TTL (3.3V version)-compatible
- 2048 refresh cycles / 32 ms (2k-Refresh) / 2048 refresh cycles / 128 ms for L- version
- Plastic Package: P-SOJ-28-3 400 mil & P-SOJ-28-4 300mil

The HYB 5(3)117800 are 16 MBit dynamic RAMs based on the die revisions „G“ & „F“ and organized as 2 097 152 words by 8-bits. The HYB 5(3)117800 utilizes a submicron CMOS silicon gate process technology, as well as advanced circuit techniques to provide wide operating margins, both internally and for the system user. Multiplexed address inputs permit the HYB 5(3)117800 to be packaged in a standard SOJ 28 plastic package. Packages with both 300 mil and 400 mil width are available. These packages provide high system bit densities and are compatible with commonly used automatic testing and insertion equipment. The HYB53117800BJL/BSJL („L-versions“) have a very low power „sleep mode“ supported by Self Refresh.

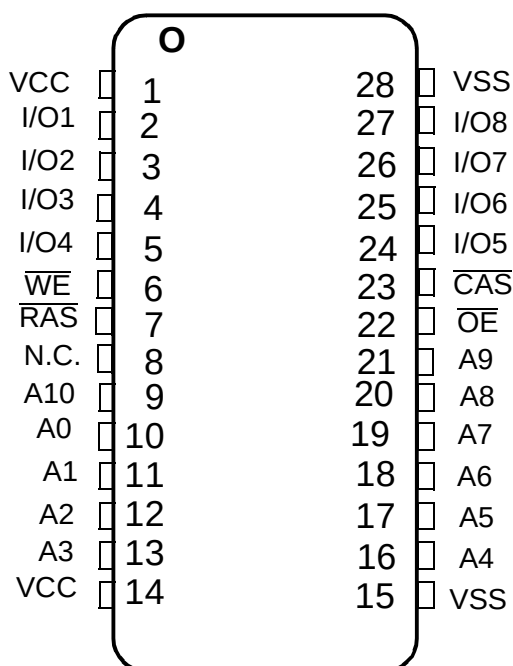
Ordering Information

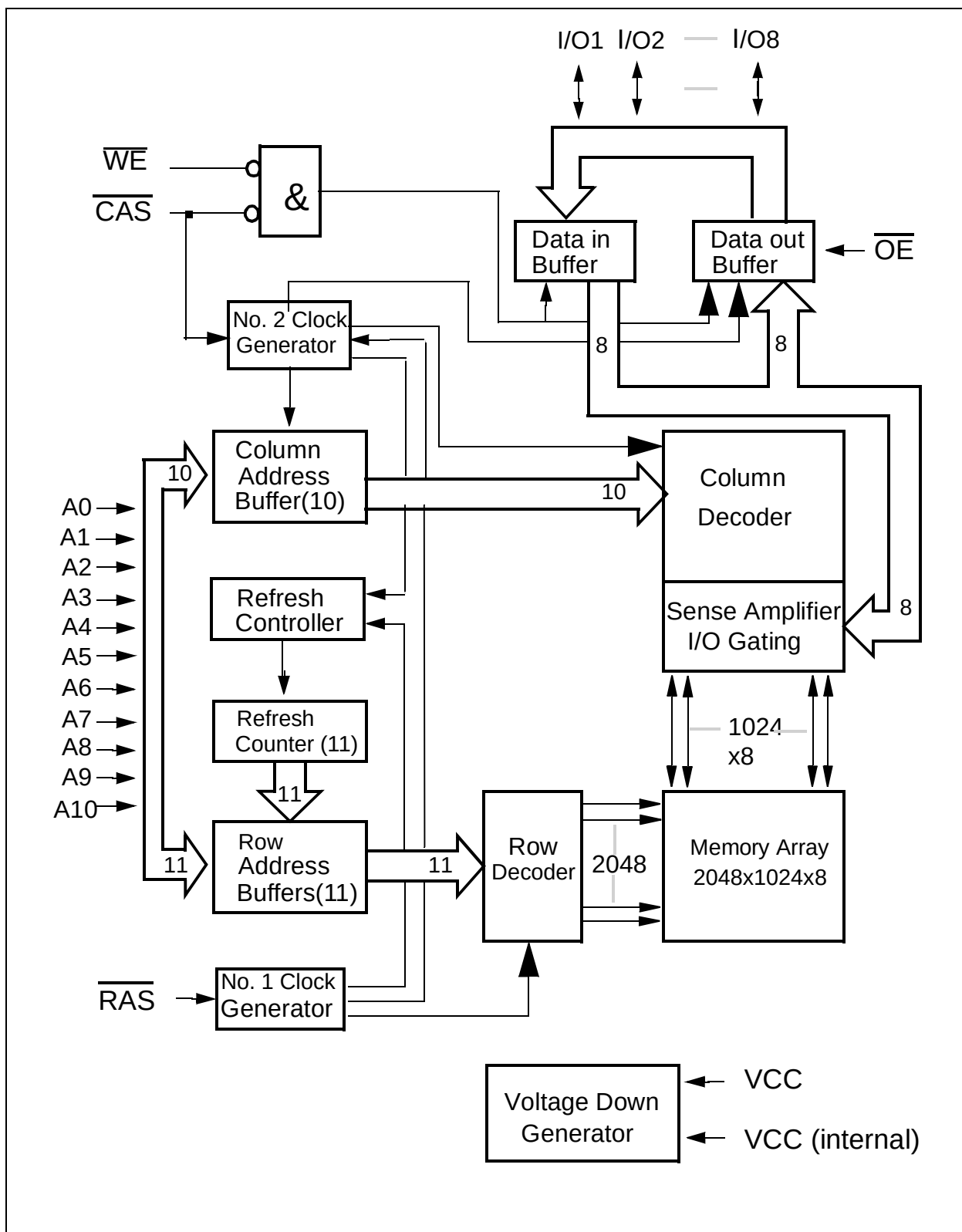
Type	Ordering Code	Package	Descriptions
HYB 5117800BJ-50	Q67100-	P-SOJ-28-4 300 mil	5V 50ns FPM - DRAM
HYB 5117800BJ-60	Q67100-	P-SOJ-28-4 300 mil	5V 60ns FPM-DRAM
HYB 3117800BJ-50	Q67100-	P-SOJ-28-4 300 mil	3.3V 50ns FPM-DRAM
HYB 3117800BJ-60	Q67100-	P-SOJ-28-4 300 mil	3.3V 60ns FPM-DRAM
HYB 3117800BJL-50	Q67100-	P-SOJ-28-4 300 mil	3.3V 50ns LP-FPM-DRAM
HYB 3117800BJL-60	Q67100-	P-SOJ-28-4 300 mil	3.3V 60ns LP-FPM-DRAM
HYB 5117800BSJ-50	Q67100-	P-SOJ-28-3 400 mil	5V 50ns FPM - DRAM
HYB 5117800BSJ-60	Q67100-	P-SOJ-28-3 400 mil	5V 60ns FPM-DRAM
HYB 3117800BSJ-50	Q67100-	P-SOJ-28-3 400 mil	3.3V 50ns FPM-DRAM
HYB 3117800BSJ-60	Q67100-	P-SOJ-28-3 400 mil	3.3V 60ns FPM-DRAM
HYB 3117800BSJL-50	Q67100-	P-SOJ-28-3 400 mil	3.3V 50ns LP-FPM-DRAM
HYB 3117800BSJL-60	Q67100-	P-SOJ-28-3 400 mil	3.3V 60ns LP-FPM-DRAM

Pin Names and Configuration:

A0-A10	Row Address Inputs
A0-A9	Column Address Inputs
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{OE}}$	Output Enable
I/O1-I/O8	Data Input/Output
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{WE}}$	Read/Write Input
V_{CC}	Power Supply + 5 V for HYB5117800 +3.3V for HYB3117800
V_{SS}	Ground (0 V)
N.C.	not connected

P-SOJ-28-3 300 & 400 mil





Block Diagram

Absolute Maximum Ratings :

Operating temperature range	0 to 70 °C
Storage temperature range.....	– 55 to 150 °C
Input/output voltage (5V versions)	-0.5 to min (V _{CC} +0.5,7.0) V
Input/output voltage (3.3V versions)	-0.5 to min (V _{CC} +0.5,4.6) V
Power supply voltage (5V versions)	-1.0V to 7.0 V
Power supply voltage (3.3V versions)	-1.0V to 4.6 V
Power dissipation(5V versions)	1.0 W
Power dissipation (3.3V versions)	0.5 W
Data out current (short circuit)	50 mA

Note:

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

$T_A = 0$ to 70 °C, $V_{SS} = 0$ V, $t_T = 2$ ns

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		

5V versions:

Power supply voltage	V_{CC}	4.5	5.5	V	
Input high voltage	V_{IH}	2.4	V _{CC} +0.5	V	1)
Input low voltage	V_{IL}	– 0.5	0.8	V	1)
Output high voltage ($I_{OUT} = -5$ mA)	V_{OH}	2.4	–	V	1)
Output low voltage ($I_{OUT} = 4.2$ mA)	V_{OL}	–	0.4	V	1)

3.3V versions:

Power supply voltage	V_{CC}	3.0	3.6	V	
Input high voltage	V_{IH}	2.0	V _{CC} +0.5	V	1)
Input low voltage	V_{IL}	– 0.5	0.8	V	1)
TTL Output high voltage ($I_{OUT} = -2$ mA)	V_{OH}	2.4	–	V	1)
TTL Output low voltage ($I_{OUT} = 2$ mA)	V_{OL}	–	0.4	V	1)
CMOS Output high voltage ($I_{OUT} = -100$ uA)	V_{OH}	V _{CC} -0.2	–	V	
CMOS Output low voltage ($I_{OUT} = 100$ uA)	V_{OL}	–	0.2	V	

DC Characteristics (cont'd)

$T_A = 0$ to 70 °C, $V_{SS} = 0$ V, $t_T = 2$ ns

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Common Parameters:					
Input leakage current (0 V ≤ V _{IH} ≤ Vcc + 0.3V, all other pins = 0 V)	I _{I(L)}	− 10	10	μA	1)
Output leakage current (DO is disabled, 0 V ≤ V _{OUT} ≤ Vcc + 0.3V)	I _{O(L)}	− 10	10	μA	1)
Average V _{CC} supply current: -50 ns version -60 ns version (RAS, CAS, address cycling: t _{RC} = t _{RC} min.)	I _{CC1}	− −	80 70	mA mA	2) 3) 4) 2) 3) 4)
Standby V _{CC} supply current ($\overline{\text{RAS}} = \overline{\text{CAS}} = V_{IH}$)	I _{CC2}	−	2	mA	−
Average V _{CC} supply current, during $\overline{\text{RAS}}$ -only refresh cycles: -50 ns version -60 ns version ($\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}} = V_{IH}$, t _{RC} = t _{RC} min.)	I _{CC3}	− −	80 70	mA mA	2) 4) 2) 4)
Average V _{CC} supply current, during fast page mode : -50 ns version -60 ns version ($\overline{\text{RAS}} = V_{IL}$, $\overline{\text{CAS}}$, address cycling: t _{PC} = t _{PC} min.)	I _{CC4}	− −	25 20	mA mA	2) 3) 4) 2) 3) 4)
Standby V _{CC} supply current ($\overline{\text{RAS}} = \overline{\text{CAS}} = V_{CC} - 0.2 \text{ V}$)	I _{CC5}	−	1 200	mA μA	1) L-Version
Average V _{CC} supply current, during $\overline{\text{CAS}}$ -before-RAS refresh mode: -50 ns version -60 ns version ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$ cycling: t _{RC} = t _{RC} min.)	I _{CC6}	− −	80 70	mA mA	2) 4) 2) 4)
Average Self Refresh Current (CBR cycle with tRAS>TRASSmin., $\overline{\text{CAS}}$ held low, $\overline{\text{WE}}$ =Vcc-0.2V, Address and Din=Vcc - 0.2V or 0.2V)	I _{CC7}	−	250	μA	L-Version only

Capacitance

$T_A = 0$ to 70 °C, $V_{CC} = 5 \text{ V} \pm 10 \%$, $f = 1 \text{ MHz}$

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A10)	C_{I1}	-	5	pF
Input capacitance ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$)	C_{I2}	-	7	pF
I/O capacitance (I/O1-I/O8)	C_{IO}	-	7	pF

AC Characteristics ⁵⁾⁶⁾

16FP/FG

$T_A = 0$ to $70\text{ }^{\circ}\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$ / $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, $t_T = 5\text{ ns}$

Parameter	Symbol	Limit Values				Unit	Note
		-50		-60			
		min.	max.	min.	max.		

common parameters

Random read or write cycle time	t_{RC}	90	—	110	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	30	—	40	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10k	60	10k	ns	
$\overline{CAS}$ pulse width	t_{CAS}	13	10k	15	10k	ns	
Row address setup time	t_{ASR}	0	—	0	—	ns	
Row address hold time	t_{RAH}	8	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	ns	
Column address hold time	t_{CAH}	10	—	15	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	18	37	20	45		
$\overline{RAS}$ to column address delay time	t_{RAD}	13	25	15	30	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	50		60	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	—	5	—	ns	
Transition time (rise and fall)	t_T	3	50	3	50	ns	7
Refresh period	t_{REF}	—	32	—	32	ms	
Refresh period for L-version	t_{REF}	—	128	—	128	ms	

Read Cycle

Access time from $\overline{RAS}$	t_{RAC}	—	50	—	60	ns	8, 9
Access time from $\overline{CAS}$	t_{CAC}	—	13	—	15	ns	8, 9
Access time from column address	t_{AA}	—	25	—	30	ns	8,10
$\overline{OE}$ access time	t_{OEA}	—	13	—	15	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	25	—	30	—	ns	
Read command setup time	t_{RCS}	0	—	0	—	ns	
Read command hold time	t_{RCH}	0	—	0	—	ns	11
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0	—	0	—	ns	11
$\overline{CAS}$ to output in low-Z	t_{CLZ}	0	—	0	—	ns	8
Output buffer turn-off delay	t_{OFF}	0	13	0	15	ns	12

AC Characteristics (cont'd) ⁵⁾⁶⁾

16FP/FG

 $T_A = 0 \text{ to } 70 \text{ }^\circ\text{C}, V_{CC} = 5 \text{ V} \pm 10 \% / V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}, t_T = 5 \text{ ns}$

Parameter	Symbol	Limit Values				Unit	Note
		-50		-60			
		min.	max.	min.	max.		
Output buffer turn-off delay from $\overline{\text{OE}}$	t_{OEZ}	0	13	0	15	ns	12
Data to $\overline{\text{OE}}$ low delay	t_{DZO}	0	–	0	–	ns	13
$\overline{\text{CAS}}$ high to data delay	t_{CDD}	13	–	15	–	ns	14
$\overline{\text{OE}}$ high to data delay	t_{ODD}	13	–	15	–	ns	14

Write Cycle

Write command hold time	t_{WCH}	8	–	10	–	ns	
Write command pulse width	t_{WP}	8	–	10	–	ns	
Write command setup time	t_{WCS}	0	–	0	–	ns	15
Write command to $\overline{\text{RAS}}$ lead time	t_{RWL}	13	–	15	–	ns	
Write command to $\overline{\text{CAS}}$ lead time	t_{CWL}	13	–	15	–	ns	
Data setup time	t_{DS}	0	–	0	–	ns	16
Data hold time	t_{DH}	10	–	10	–	ns	16
Data to $\overline{\text{CAS}}$ low delay	t_{DZC}	0	–	0	–	ns	13

Read-Modify-Write Cycle

Read-write cycle time	t_{RWC}	126	–	150	–	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ delay time	t_{RWD}	68	–	80	–	ns	15
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ delay time	t_{CWD}	31	–	35	–	ns	15
Column address to $\overline{\text{WE}}$ delay time	t_{AWD}	43	–	50	–	ns	15
$\overline{\text{OE}}$ command hold time	t_{OEH}	13	–	15	–	ns	

Fast Page Mode Cycle

Fast page mode cycle time	t_{PC}	35	–	40	–	ns	
$\overline{\text{CAS}}$ precharge time	t_{CP}	10	–	10	–	ns	
Access time from $\overline{\text{CAS}}$ precharge	t_{CPA}	–	30	–	35	ns	7
$\overline{\text{RAS}}$ pulse width	t_{RAS}	50	200k	60	200k	ns	
$\overline{\text{CAS}}$ precharge to $\overline{\text{RAS}}$ Delay	t_{RHPC}	30	–	35	–	ns	

AC Characteristics (cont'd) ⁵⁾⁶⁾

16FP/FG

 $T_A = 0 \text{ to } 70 \text{ }^\circ\text{C}, V_{CC} = 5 \text{ V} \pm 10 \% / V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}, t_T = 5 \text{ ns}$

Parameter	Symbol	Limit Values				Unit	Note
		-50		-60			
		min.	max.	min.	max.		

Fast Page Mode Read-Modify-Write Cycle

Fast page mode read-write cycle time	t_{PRWC}	71	—	80	—	ns	
CAS precharge to WE	t_{CPWD}	48	—	55	—	ns	

$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Cycle

$\overline{\text{CAS}}$ setup time	t_{CSR}	10	—	10	—	ns	
$\overline{\text{CAS}}$ hold time	t_{CHR}	10	—	10	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	t_{RPC}	5	—	5	—	ns	
Write to $\overline{\text{RAS}}$ precharge time	t_{WRP}	10	—	10	—	ns	
Write hold time referenced to $\overline{\text{RAS}}$	t_{WRH}	10	—	10	—	ns	

$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Counter Test Cycle

$\overline{\text{CAS}}$ precharge time	t_{CPT}	35	—	40	—	ns	
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Test Mode

$\overline{\text{CAS}}$ hold time	t_{CHRT}	30	—	30	—	ns	
Write command setup time	t_{WTS}	10	—	10	—	ns	
Write command hold time	t_{WTH}	10	—	10	—	ns	
RAS hold time in test mode	t_{RAHT}	30	—	30	—	ns	

Self Refresh Cycle

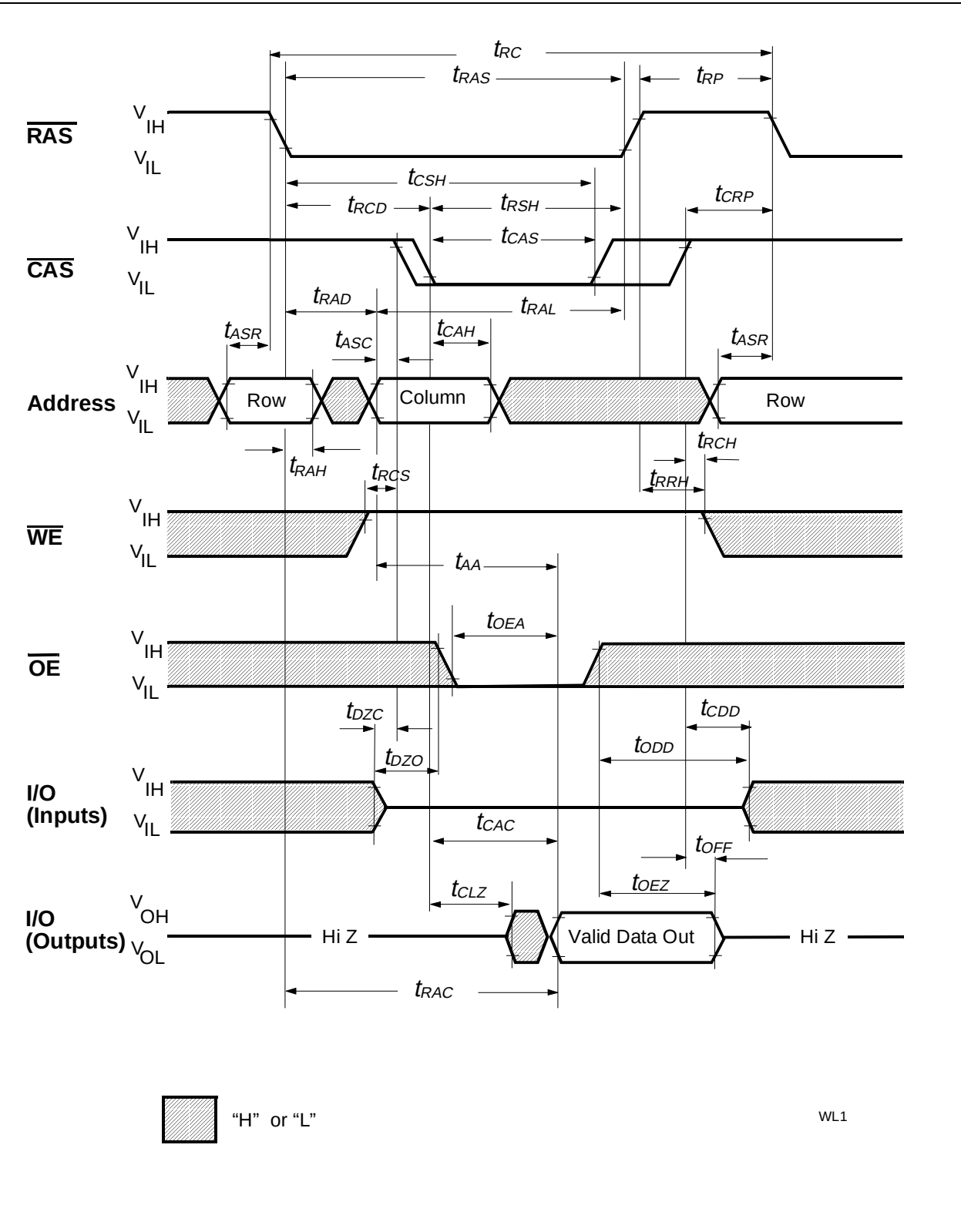
$\overline{\text{RAS}}$ pulse width	t_{RASS}	100k	—	100k	—	ns	17
$\overline{\text{RAS}}$ precharge time	t_{RPS}	95	—	110	—	ns	17
$\overline{\text{CAS}}$ hold time	t_{CHS}	-50	—	-50	—	ns	17

Notes:

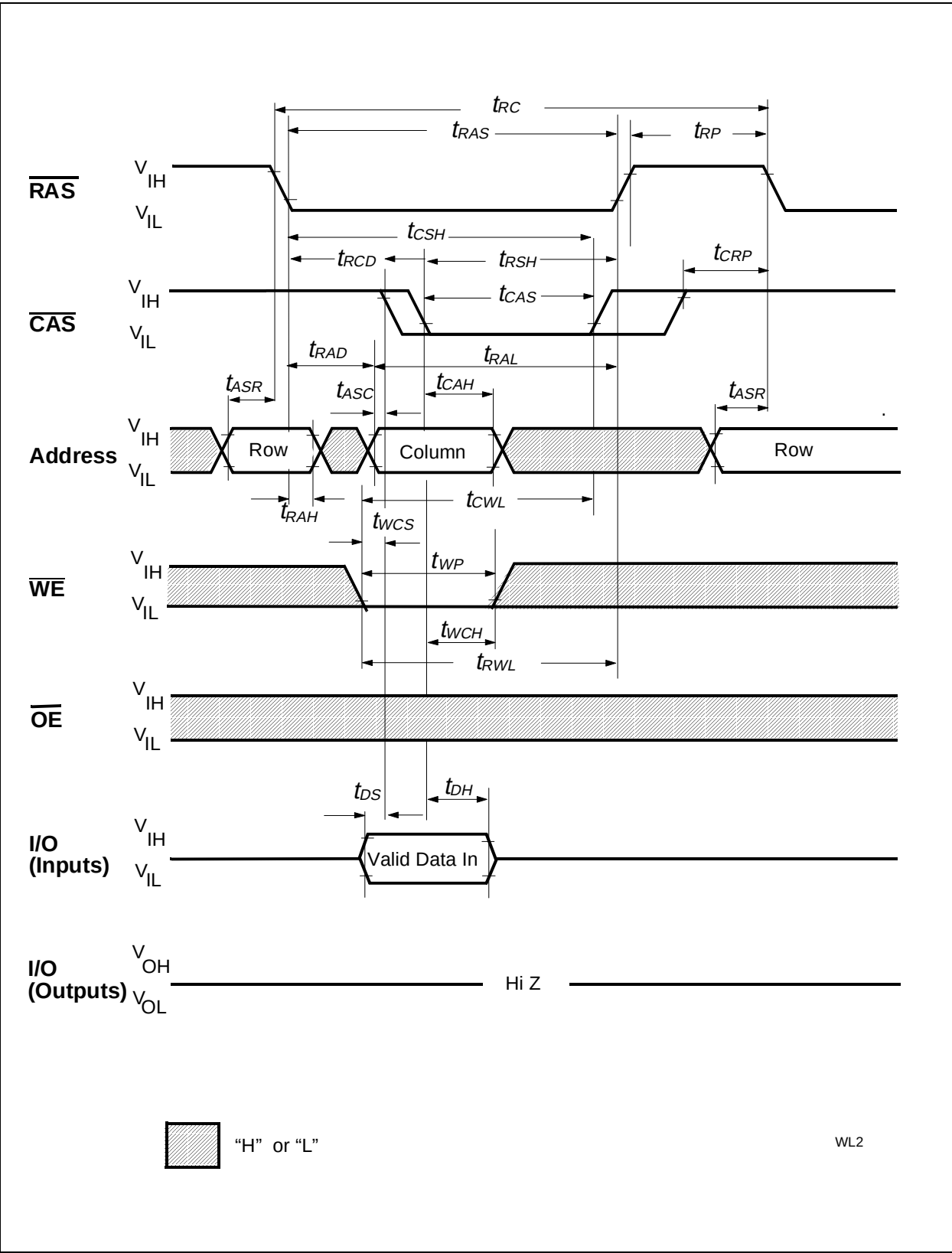
- 1) All voltages are referenced to VSS.
- 2) ICC1, ICC3, ICC4 and ICC6 depend on cycle rate.
- 3) ICC1 and ICC4 depend on output loading. Specified values are measured with the output open.
- 4) Address can be changed once or less while $\overline{\text{RAS}} = \text{VIL}$. In the case of ICC4 it can be changed once or less during a fast page mode cycle (tPC).
- 5) An initial pause of 200 ms is required after power-up followed by 8 RAS cycles of which at least one cycle has to be a refresh cycle, before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CAS-before-RAS initialization cycles instead of 8 RAS cycles are required.
- 6) AC measurements assume $t_T = 5 \text{ ns}$.
- 7) VIH (min.) and VIL (max.) are reference levels for measuring timing of input signals. Transition times are also measured between VIH and VIL.
- 8) Measured with a load equivalent to 2 TTL loads and 100 pF.
- 9) Operation within the tRCD (max.) limit ensures that tRAC (max.) can be met. tRCD (max.) is specified as a reference point only: If tRCD is greater than the specified tRCD (max.) limit, then access time is controlled by tCAC.
- 10) Operation within the tRAD (max.) limit ensures that tRAC (max.) can be met. tRAD (max.) is specified as a reference point only: If tRAD is greater than the specified tRAD (max.) limit, then access time is controlled by tAA.
- 11) Either tRCH or tRRH must be satisfied for a read cycle.
- 12) tOFF (max.) and tOEZ (max.) define the time at which the outputs achieve the open-circuit condition and are not referenced to output voltage levels.
- 13) Either tDZC or tDZO must be satisfied.
- 14) Either tCDD or tODD must be satisfied.
- 15) tWCS, tRWD, tCWD, tAWD and tCPWD are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $tWCS > tWCS(\text{min.})$, the cycle is an early write cycle and the I/O pin will remain open-circuit (high impedance) through the entire cycle; if $tRWD > tRWD(\text{min.})$, $tCWD > tCWD(\text{min.})$, $tAWD > tAWD(\text{min.})$ and $tCPWD > tCPWD(\text{min.})$, the cycle is a read-write cycle and I/O pins will contain data read from the selected cells. If neither of the above sets of conditions is satisfied, the condition of the I/O pins (at access time) is indeterminate.
- 16) These parameters are referenced to the CAS leading edge in early write cycles and to the WE leading edge in read-write cycles.
- 17) When using Self Refresh mode, the following refresh operations must be performed to ensure proper DRAM operation:

If row addresses are being refreshed on an evenly distributed manner over the refresh interval using CBR refresh cycles, then only one CBR cycle must be performed immediately after exit from Self Refresh.

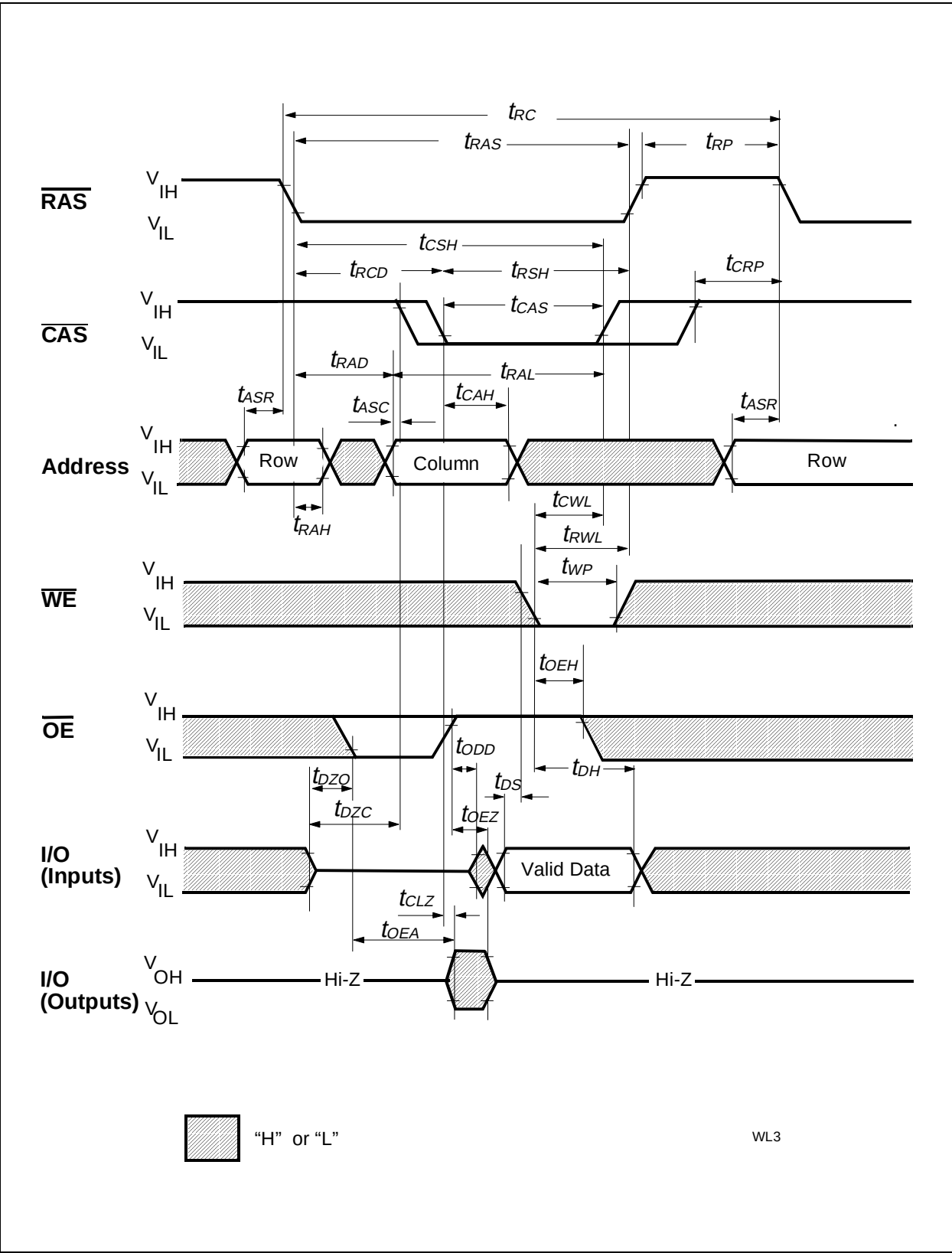
If row addresses are being refreshed in any other manner (ROR - Distributed/Burst; or CBR-Burst) over the refresh interval, then a full set of row refreshes must be performed immediately before entry to and immediately after exit from Self Refresh.



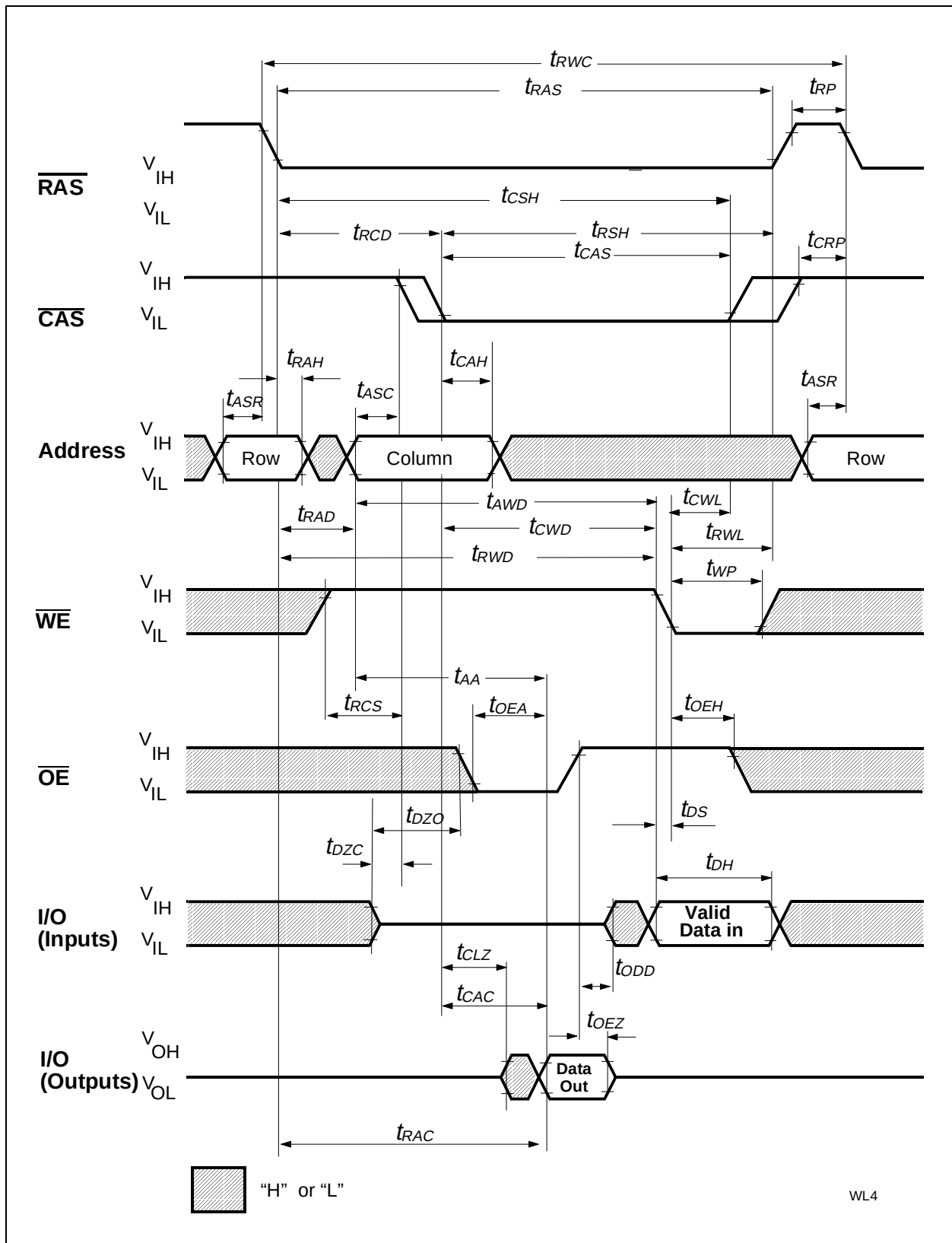
Read Cycle



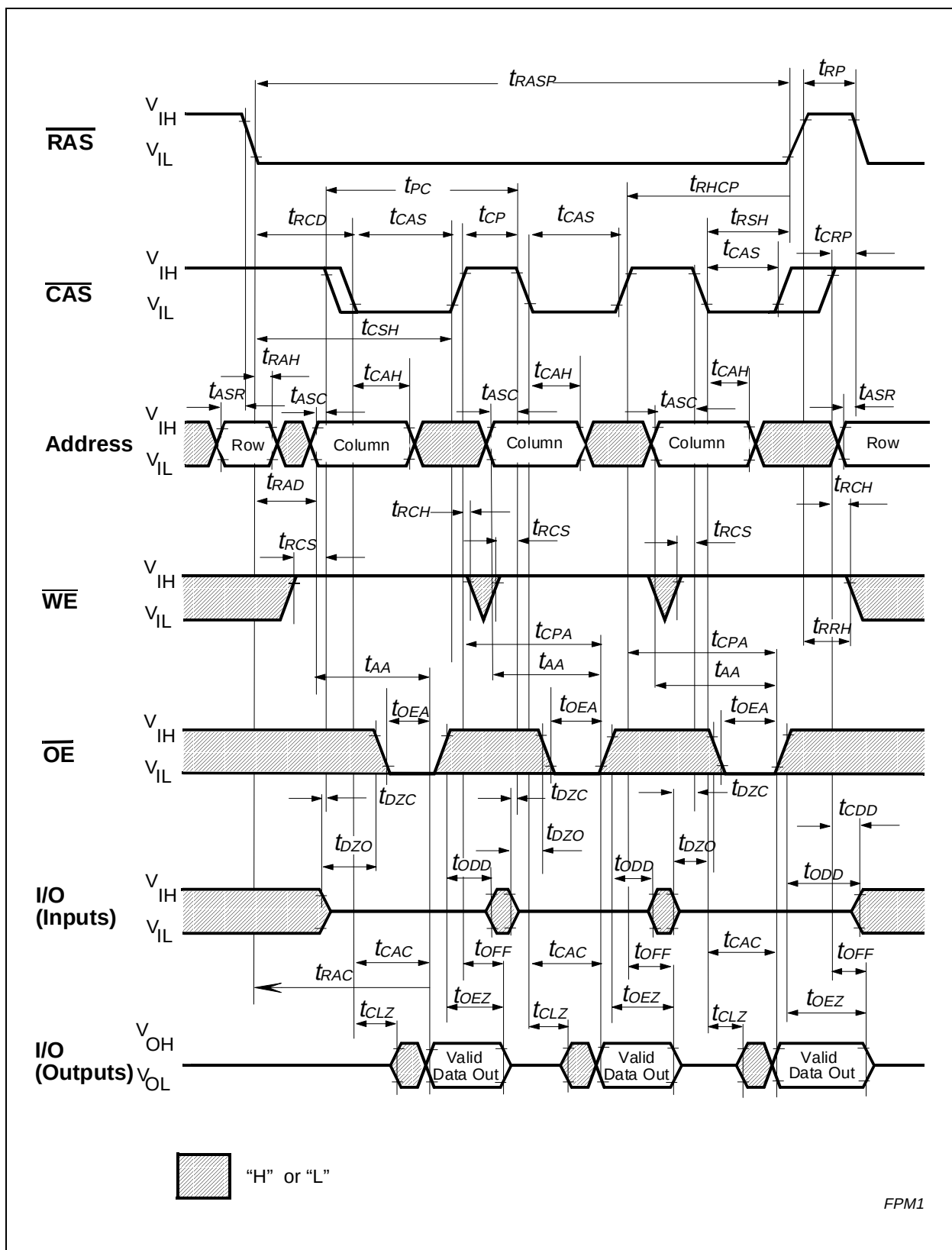
Write Cycle (Early Write)



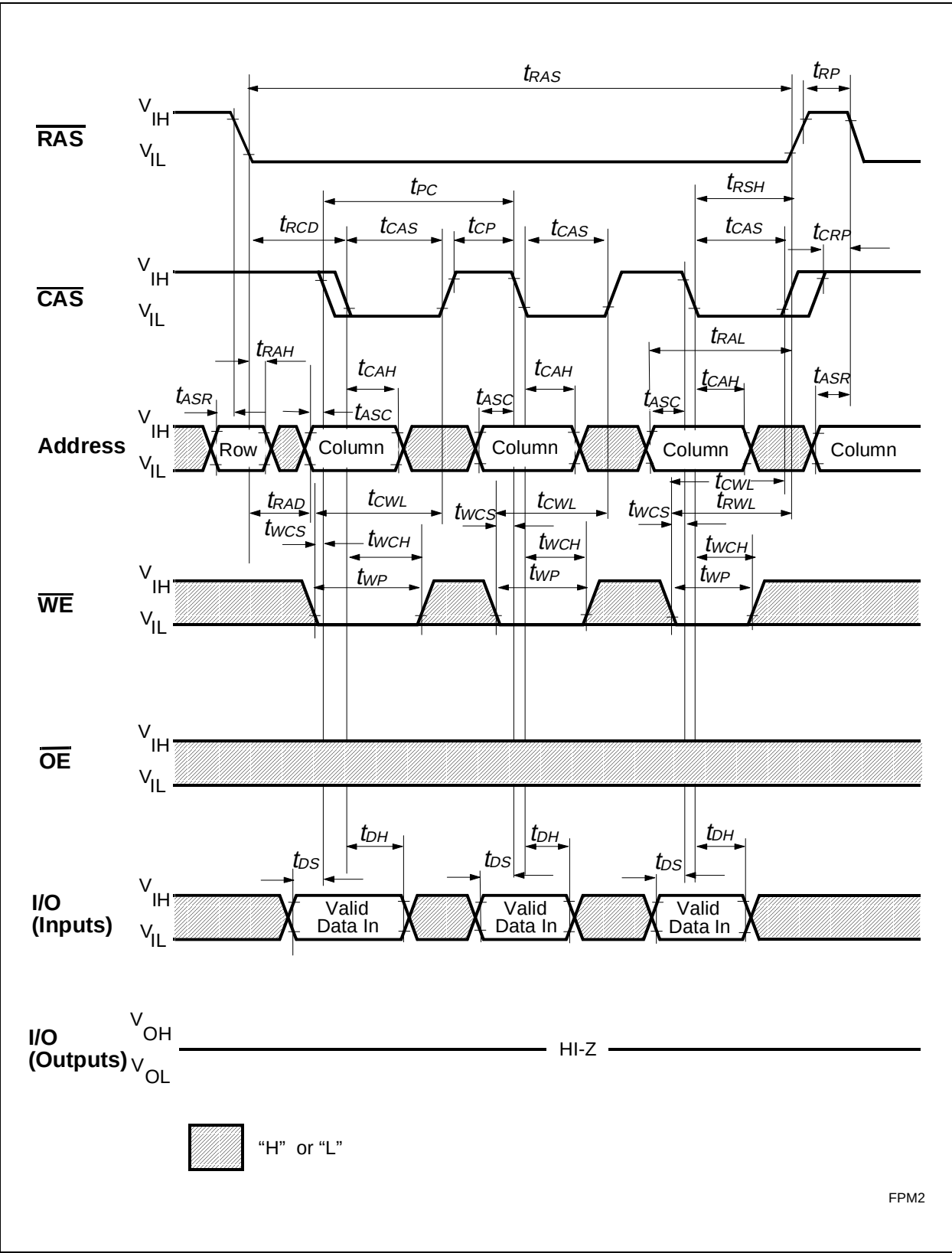
Write Cycle ($\overline{OE}$ Controlled Write)



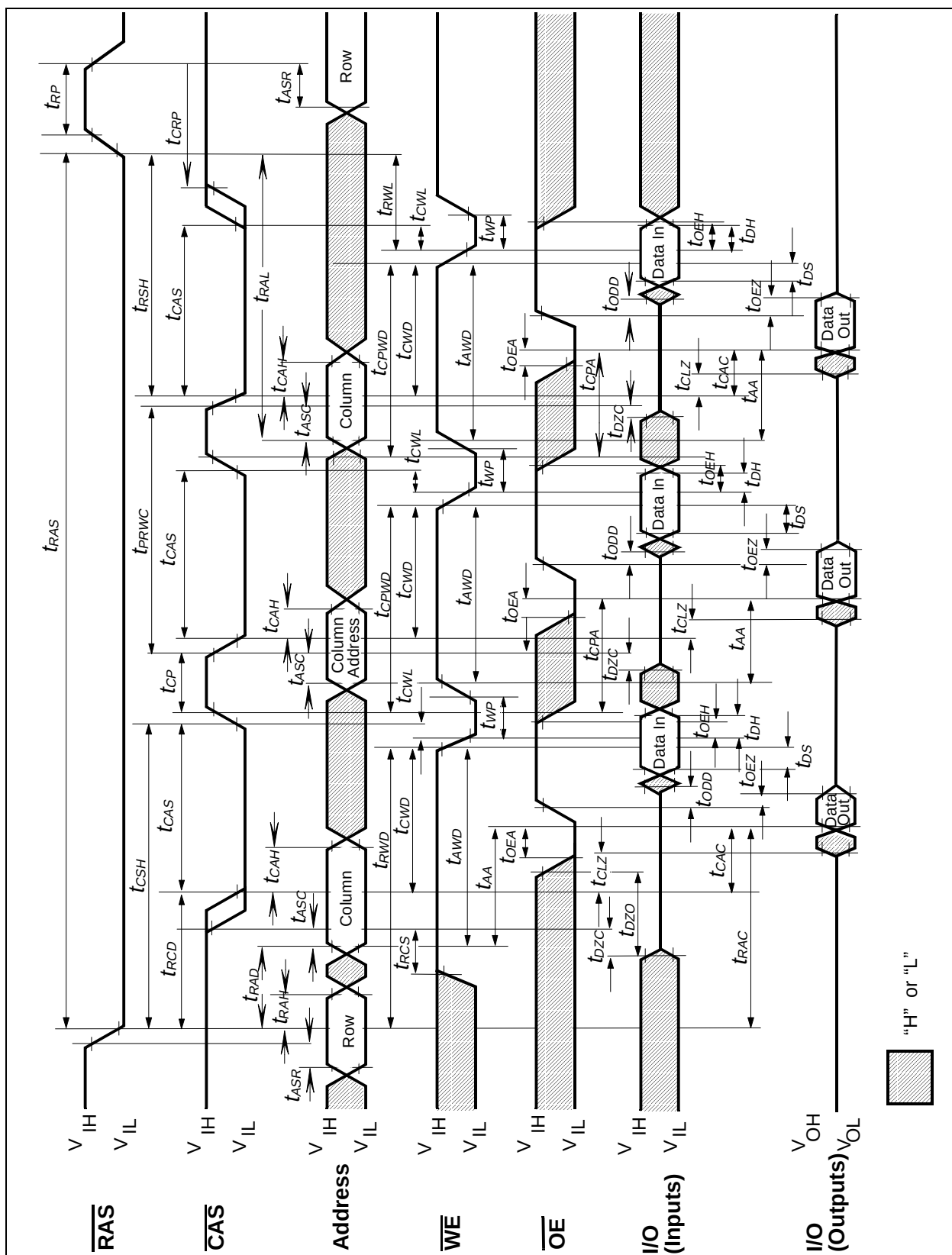
Read-Write (Read-Modify-Write) Cycle



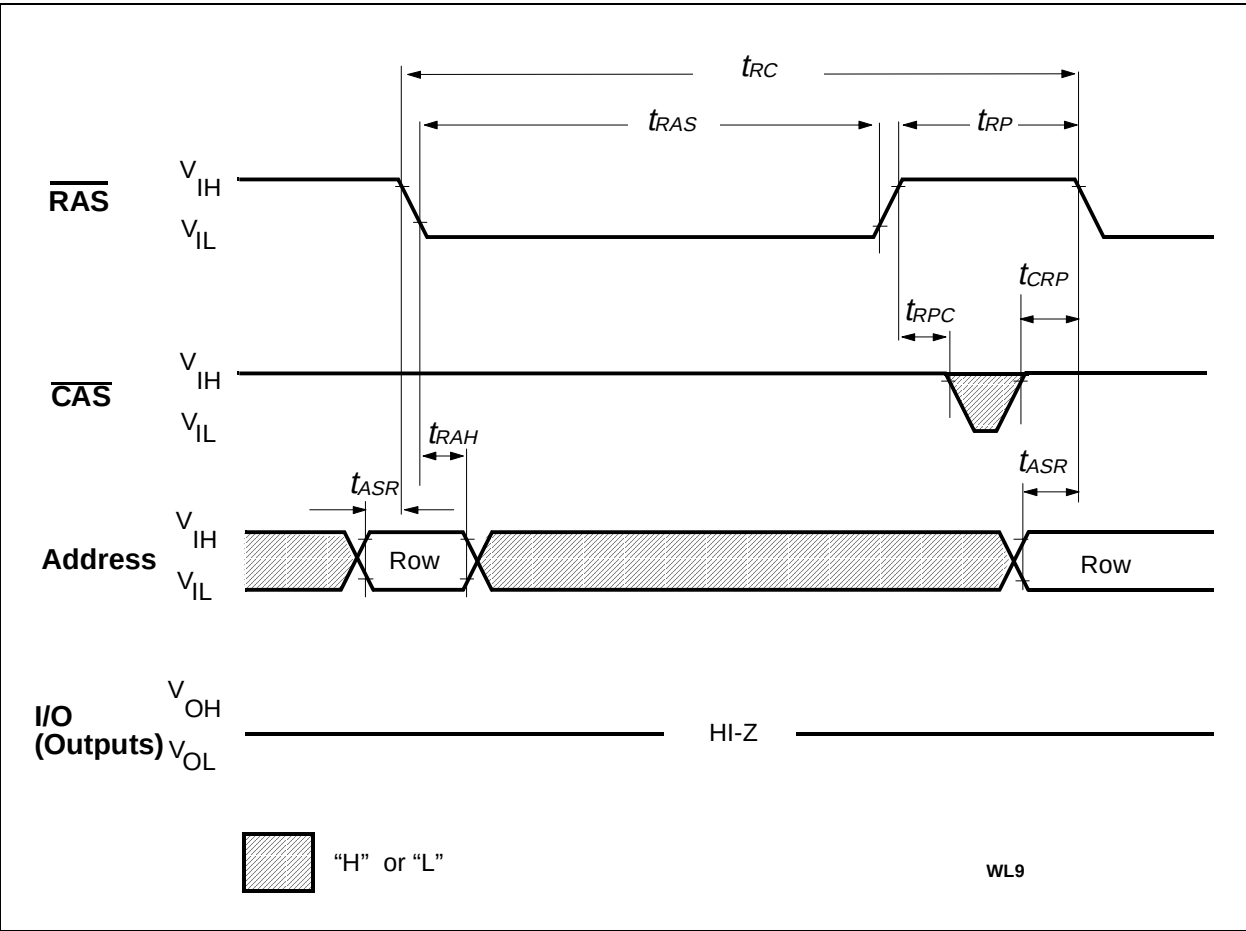
Fast Page Mode Read Cycle



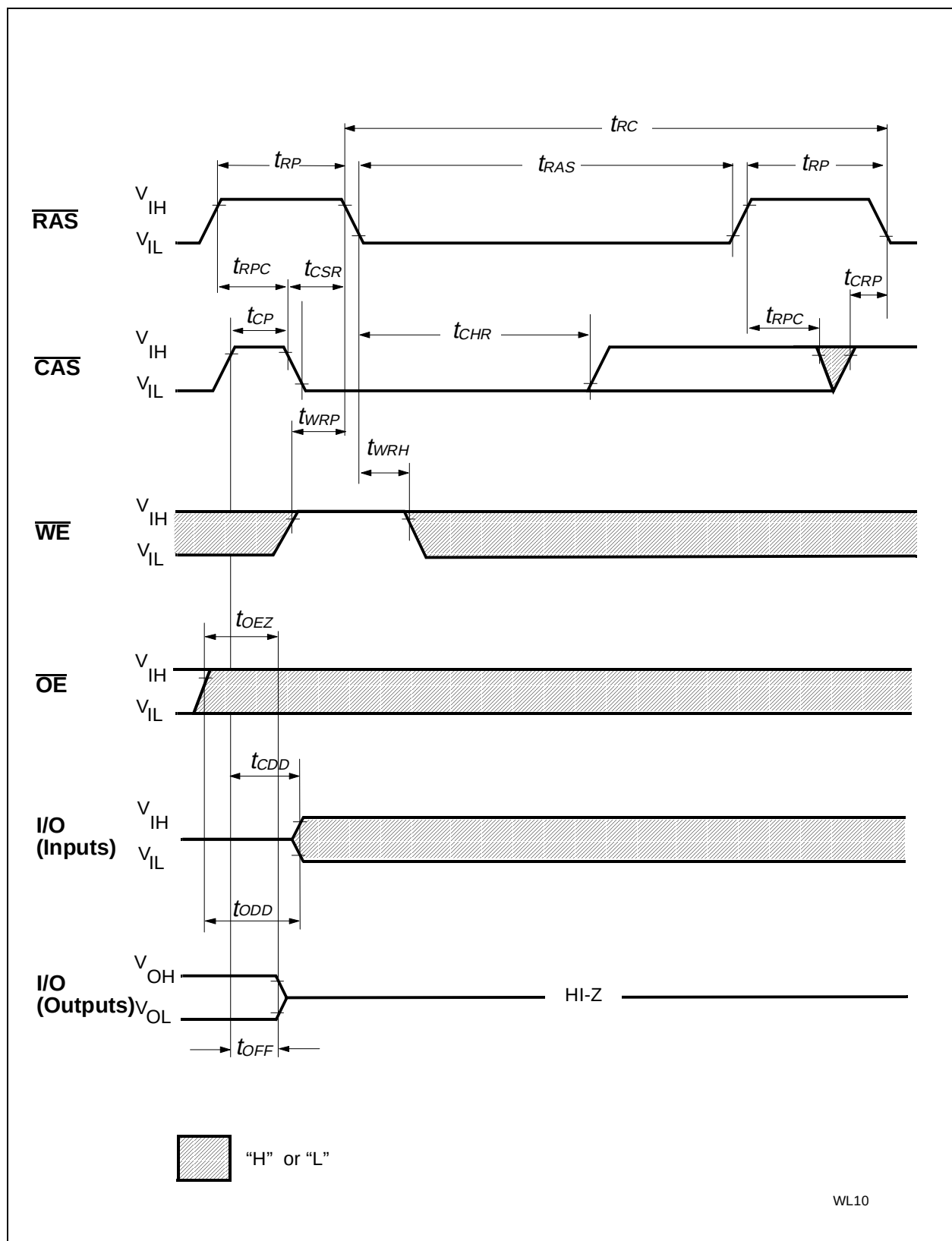
Fast Page Mode Early Write Cycle



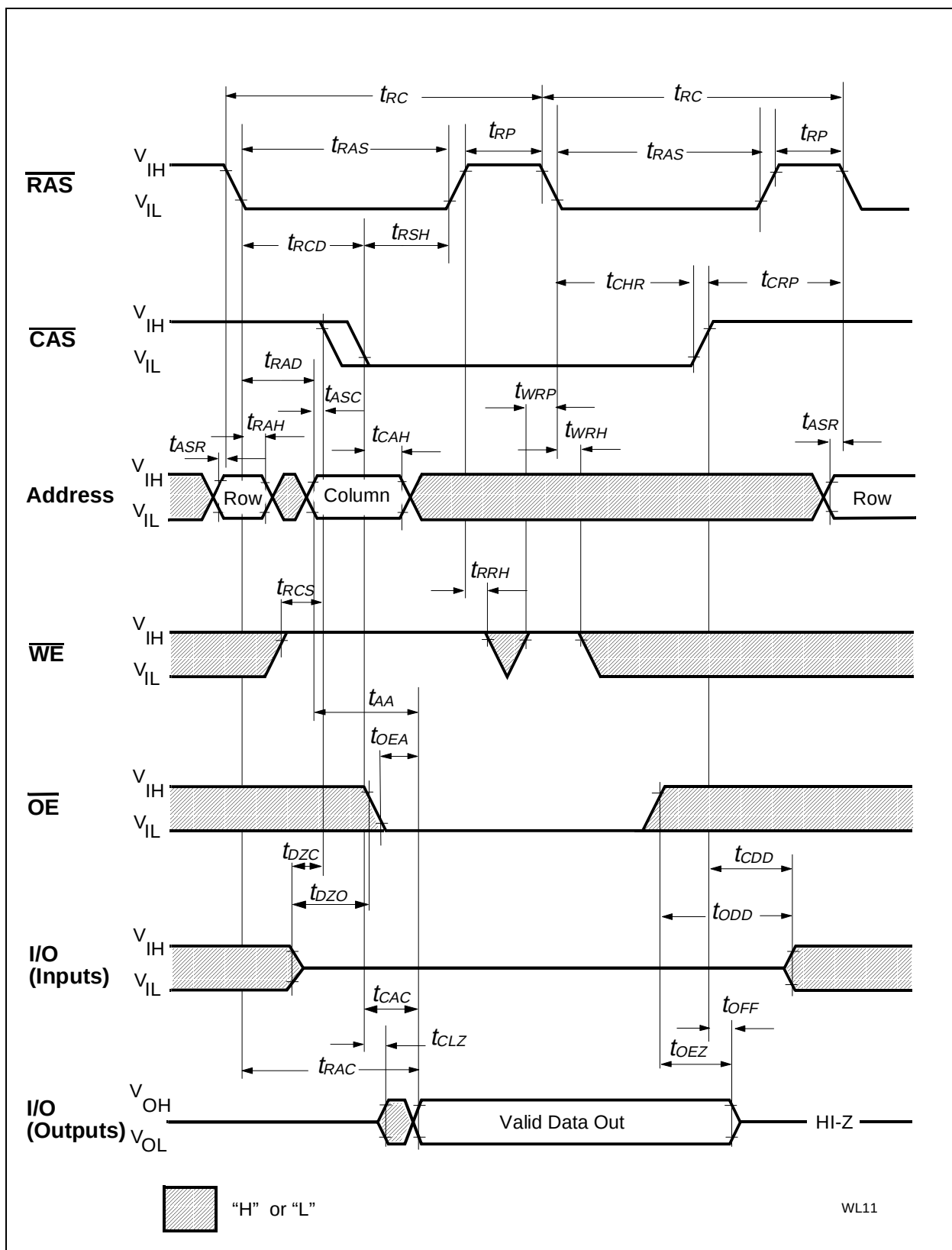
Fast Page Mode Late Write and Read-Modify Write Cycle



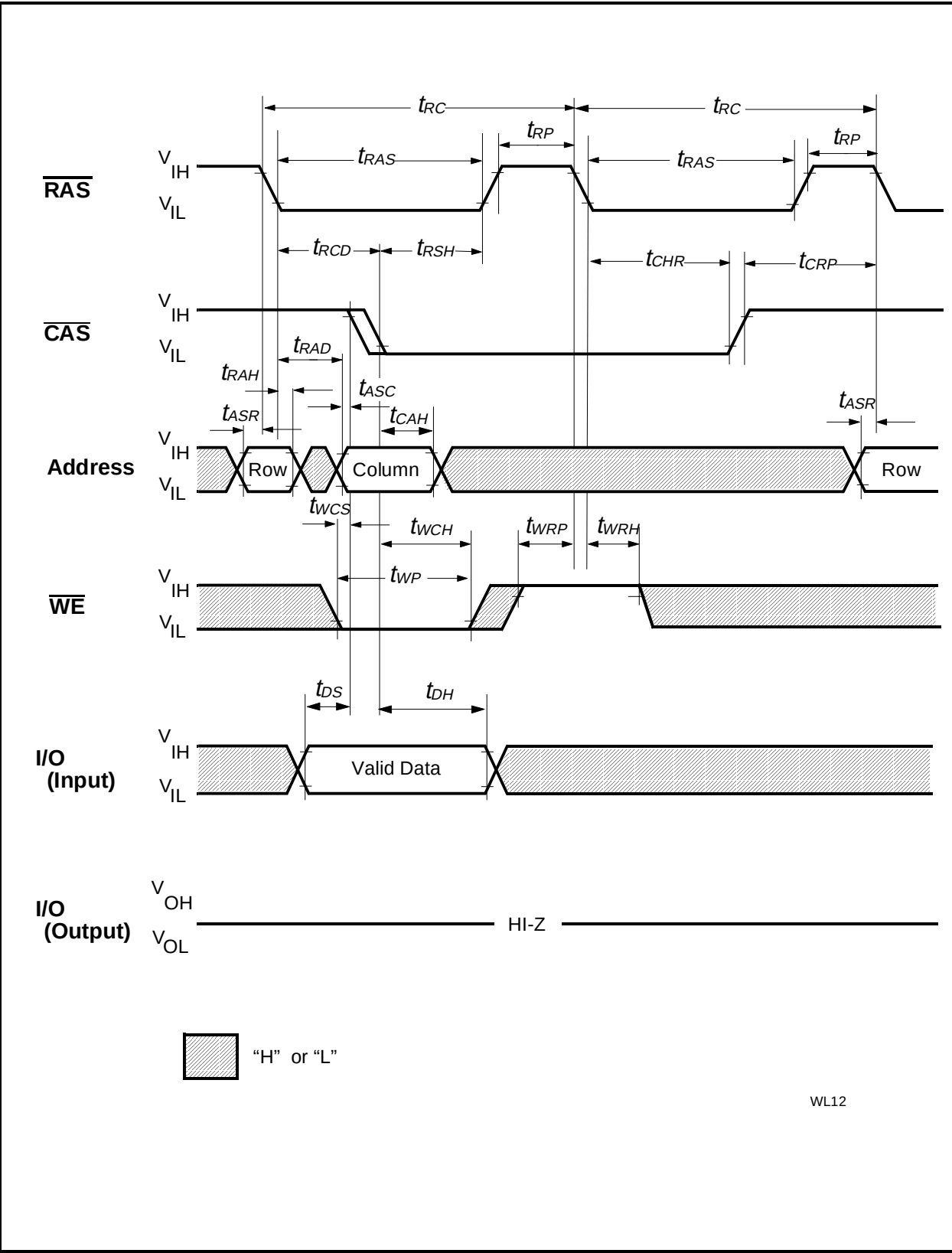
$\overline{\text{RAS}}$ -Only Refresh Cycle



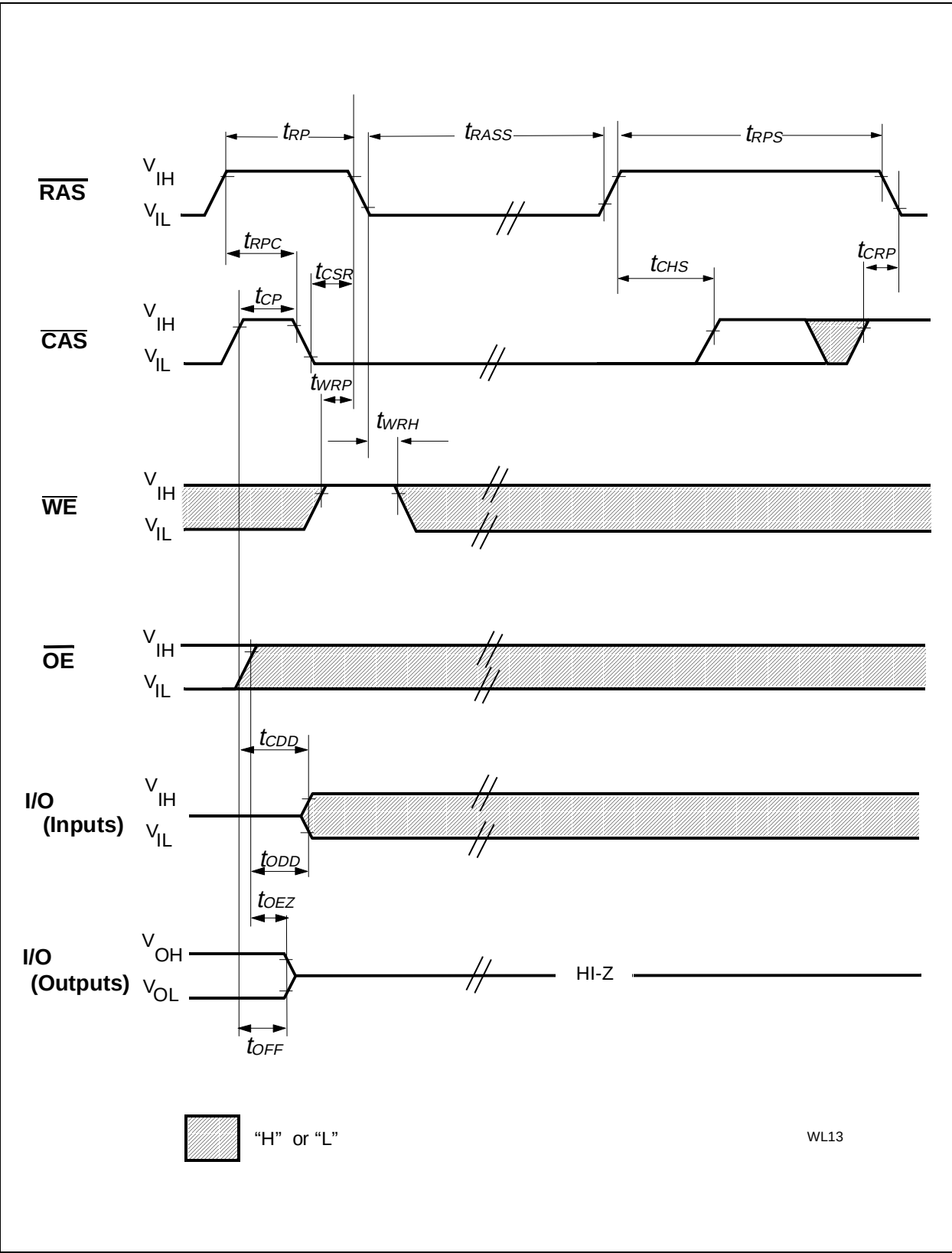
CAS-Before-RAS Refresh Cycle



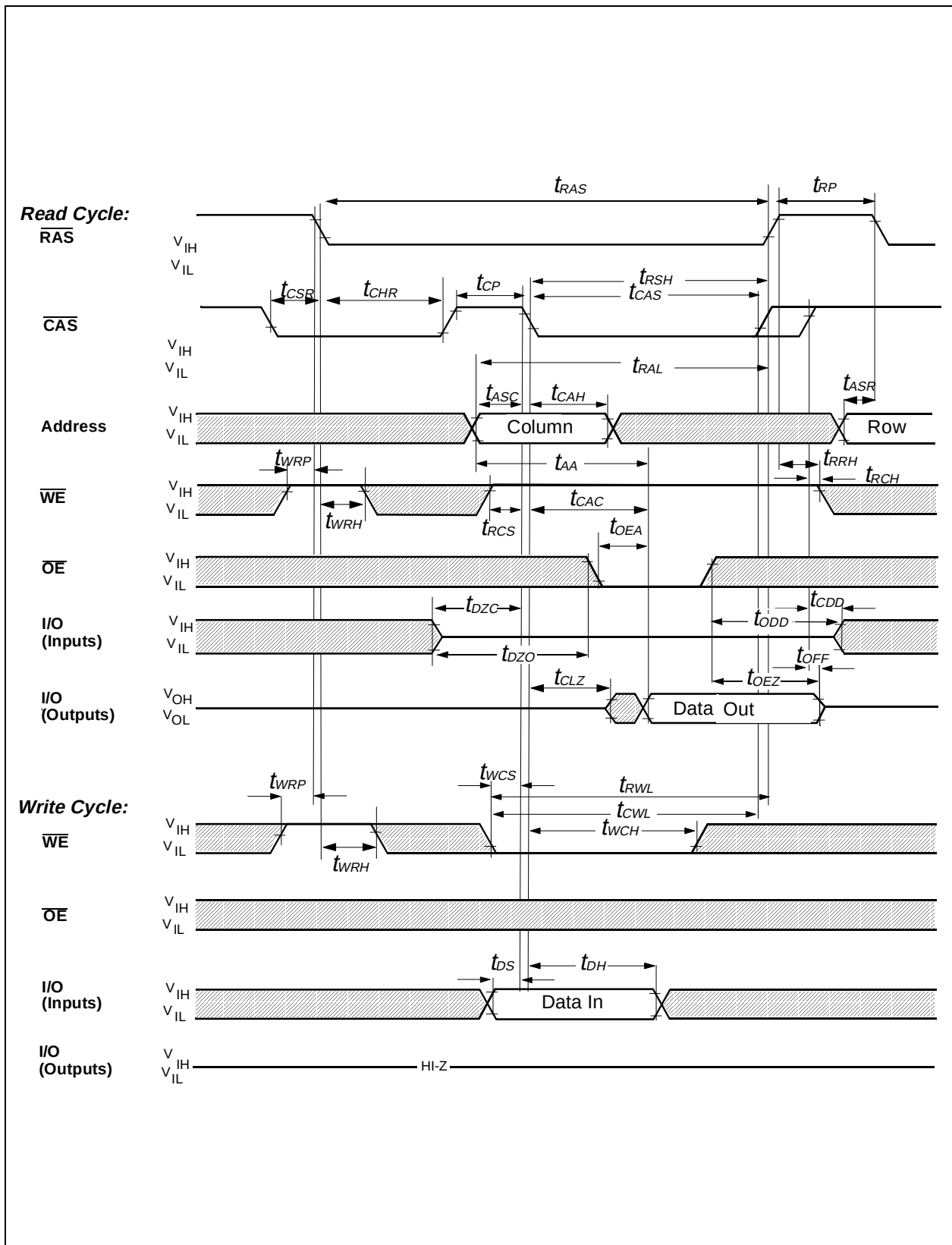
Hidden Refresh Cycle (Read) Cycle



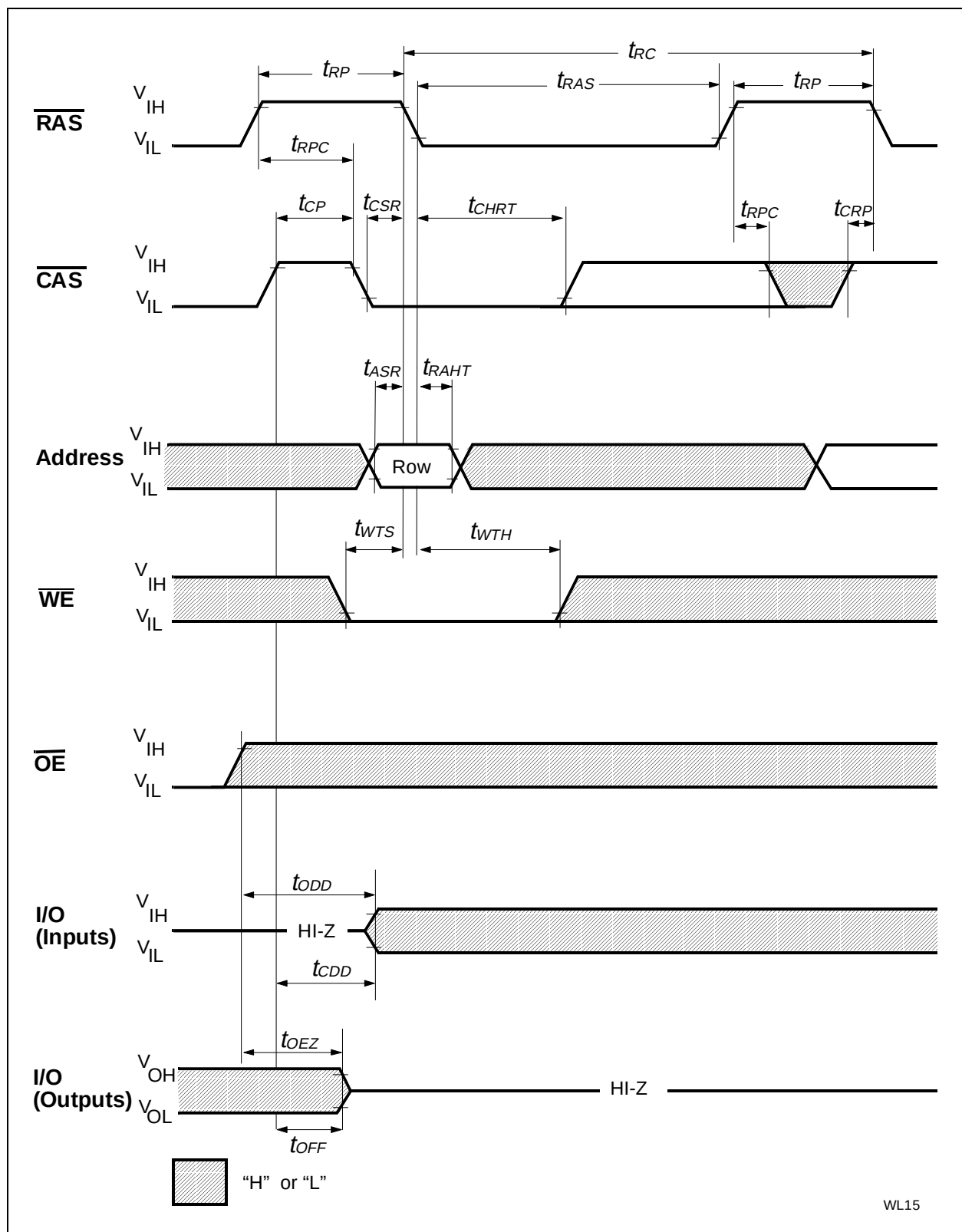
Hidden Refresh Early Write Cycle



Self Refresh



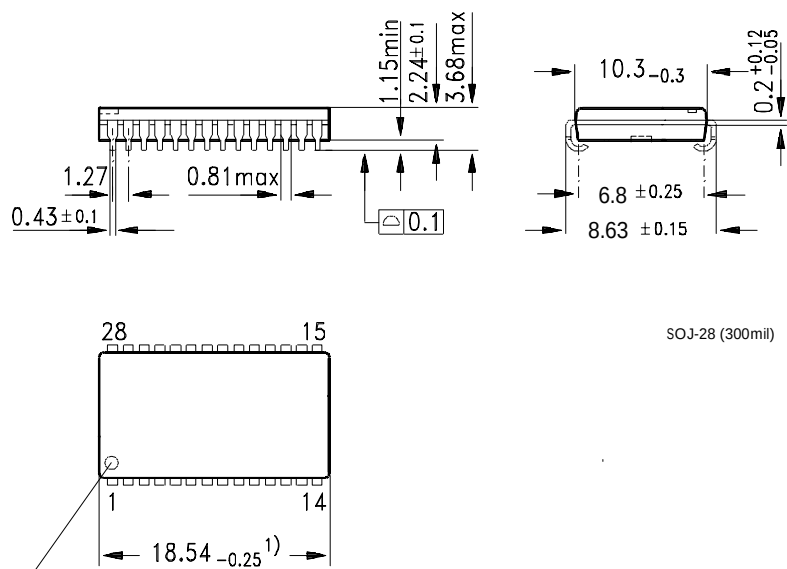
CAS-Before-RAS Refresh Counter Test Cycle



Test Mode Entry

Plastic Package P-SOJ-28-4 (300mil)

(Small Outline J-lead, SMD)

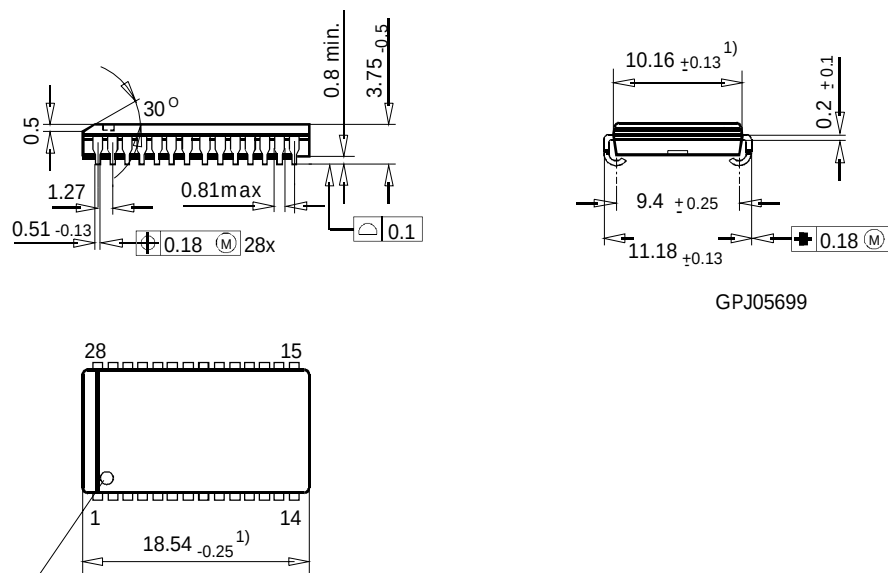


Index Marking

1) Does not include plastic or metal protrusion of 0.15 max per side

Plastic Package P-SOJ-28-3 (400mil)

(Small Outline J-lead, SMD)



Index Marking

1) Does not include plastic or metal protrusion of 0.15 max. per side

Package Outline