Data Sheet

gmZ1

DAT-0001-D

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gmZ1 Data Sheet

DAT-0001-D

(supersedes gmZ1 Data Sheet DAT-0001-C)

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DAT-0001-D	Changed reference to “multiscan” on page 3. Added Table 3 - D_BYPASS Mode signals. Added note to Section 5.7	August 1998

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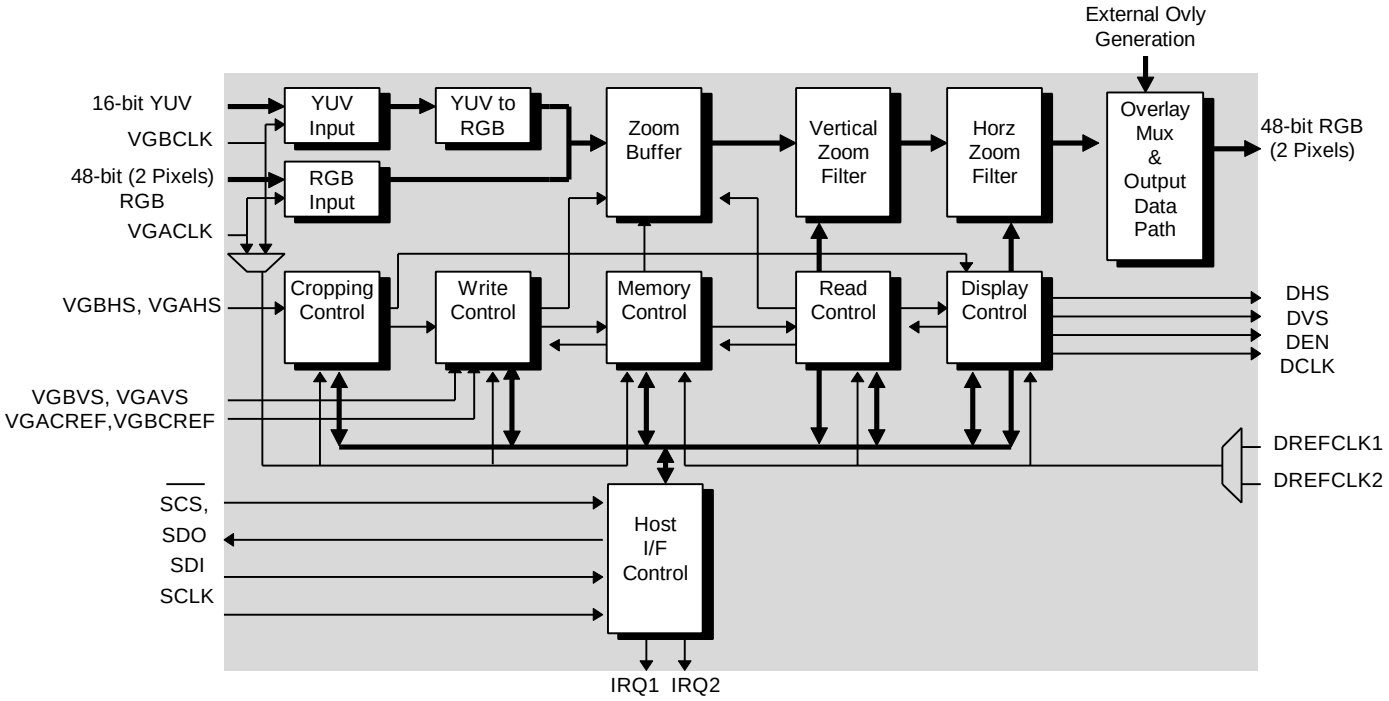
1. Overview

The gmZ1 is a highly-integrated IC producing real-time, high-quality, scaled digital video or computer graphics images. Three separate data channels have been integrated into the gmZ1, allowing complete images to be resized using a single device. The gmZ1 performs image magnification (zoom) on 24-bit RGB or 16-bit YUV input data streams. The RGB video ports support single width (24-bit) or double width (48-bit) pixel transfers.

The gmZ1 performs advanced interpolation and finite impulse response (FIR) filtering independently in both the vertical and horizontal directions. The output image's spatial frequency response is automatically adjusted to preserve image bandwidth and to minimize imaging artifacts, resulting in the highest image quality.

Both graphics and status overlay information can be displayed on top of the scaled video data by means of an overlay port. A "transparent" capability exists for viewing zoomed video within and around any alpha-numeric or graphics overlay.

Figure 1: Functional Block Diagram



2. Features & Applications

High quality advanced zoom-only engine:

- Fully programmable zoom ratios
- Independent Horizontal/Vertical zoom
- An advanced zoom algorithm provides pristine image quality

Spatial de-interlacing of video inputs

- Corrected spatial positioning of odd and even input lines

Built-in display timing generator

- Can be used to drive AMLCD panels
- Special support for DMD engines
- Fully programmable timing parameters

YUV inputs:

- 16-bit YUV input video
- Clock rates up to 45MHz
- NTSC/PAL square pixels/CCIR601
- Glue-less connection to many color decoders, ex. Philips SAA7110/7111
- Built-in YUV to RGB color space converter

RGB inputs:

- Single 24-bit RGB pixels @ 84MHz
- 48-bit RGB pixel @ 42MHz
- Programmable input port

Output Pixel Modes supported:

- 1 and 2 pixel/clock panel support
- Single 24 bit RGB pixel/clock @ 84MHz
- Dual 48 bit RGB pixels/clock @ 42 MHz
- Dithering logic to enhance pixel color depth for 18-bit panels
- Compliant with proposed **VESA FPDI-2** standard via direct connect to NSC, C&T, SII LVDS transceivers

Operating Modes

- Bypass mode with no filtering
- 1:1 scaling
- Non-interlaced zoom
- De-interlacing zoom

Display Synchronization Modes

- Frame Sync - input & output frame periods are forced to synchronize
- Line Sync - display line rate synthesized from the input line rate
- Free Run - input and output rates are not synchronized - ideal for frame-rate conversions

Simplicity of design speeds time to market

- Single-chip zoom-only solution
- No external memory required
- Programmable horizontal and vertical front and back porches on input data
- Input active window region decoded
- Active window framing signal requests pixels 2 clocks before sampling time
- Using line request and pixel request signals, pipelined video data I/F can be easily designed
- Overlay menus supported via dedicated port, control, and data lines
- 4-wire or 3-wire serial host interface for easy connection to Intel/Motorola MCUs

Applications

- Projection Systems based on AMLCDs, DMDs
- Fixed-resolution Pixelated Display devices
- Multiscan LCD Panels for CRT replacement
- Standards conversion
- Scan doublers/quadruplers/converters
- Home theater
- Video Walls

3. General Operation

The gmZ1 has been designed to simplify connection to both digital video and graphics data streams. Once the gmZ1 is programmed, high quality zoom processing is performed using independently adjustable ADVANCED ZOOM filtering in the vertical and horizontal directions. All filter coefficients are generated internally without additional programming.

The gmZ1 scales the selected input video by a 1X or larger zoom ratio to create an output image of equal or greater size. The gmZ1 requires no external frame buffer when the input and output formats have equal frame rates and the vertical active periods are synchronized. Magnification plus frame-rate conversion may be performed using the Genesis gmFC1 Frame Rate Converter chip along with the gmZ1 (see Application Note MSD-0016).

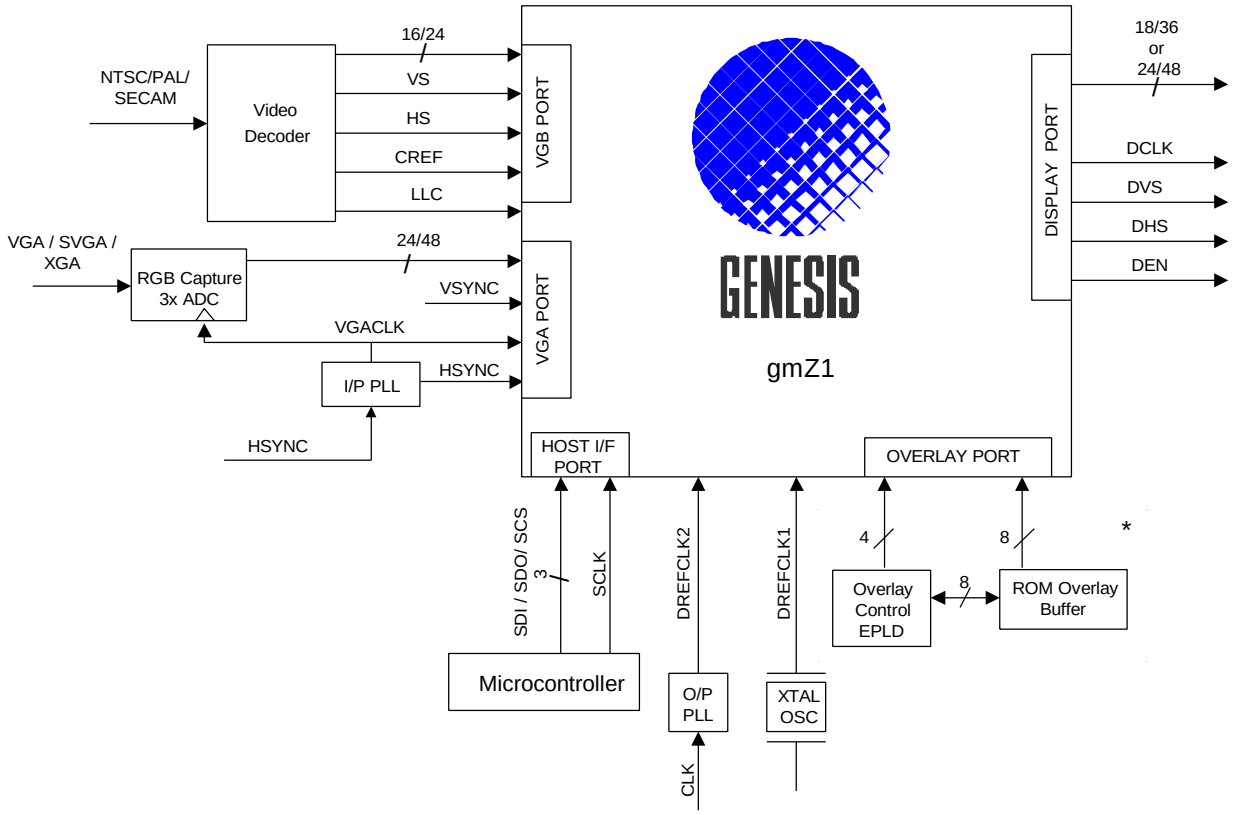
The video input data is transferred to the gmZ1 at the selected video input pixel clock rate and stored in an internal zoom buffer. Data is read from the zoom buffer for processing by the on-chip scaler and subsequent display at the display pixel clock rate. The selected input and output display clocks can run at different frequencies.

An overlay port outputs programmable overlay timing information to external overlay circuitry that generates 8-bit overlay color select data (See Application Note MSD-0008). Two independent overlay display regions may be displayed on top of the scaled output. Pixel-by-pixel enabling control provides “transparent” capability for viewing zoomed video within and around any alpha numeric or graphics overlay.

The gmZ1 can be initialized by an external micro-controller to program the control, status, filter parameter, and timing parameter registers via a serial interface port. All registers can be accessed using read, write, burst-read, and burst-write I/O cycles. The gmZ1 provides status and video timing information to the system through a status register and programmable interrupts.

A gmZ1 Programming Cable and software is available from Genesis Microchip to help speed up gmZ1 designs. This Cable Module allows a PC to access and program gmZ1 registers directly (See Application Note MSD-0004). What’sOn Software is also available to help in calculating gmZ1 register parameters (See The What’sOn User Guide SED-0015).

Figure 2: gmZ1 System Block Diagram



* Overlay control may be simplified using a single chip OSD device such as the Motorola 141544DW. See Genesis Application Note MSD-0008.

4. Pinout

Figure 3: gmZ1 Pinout

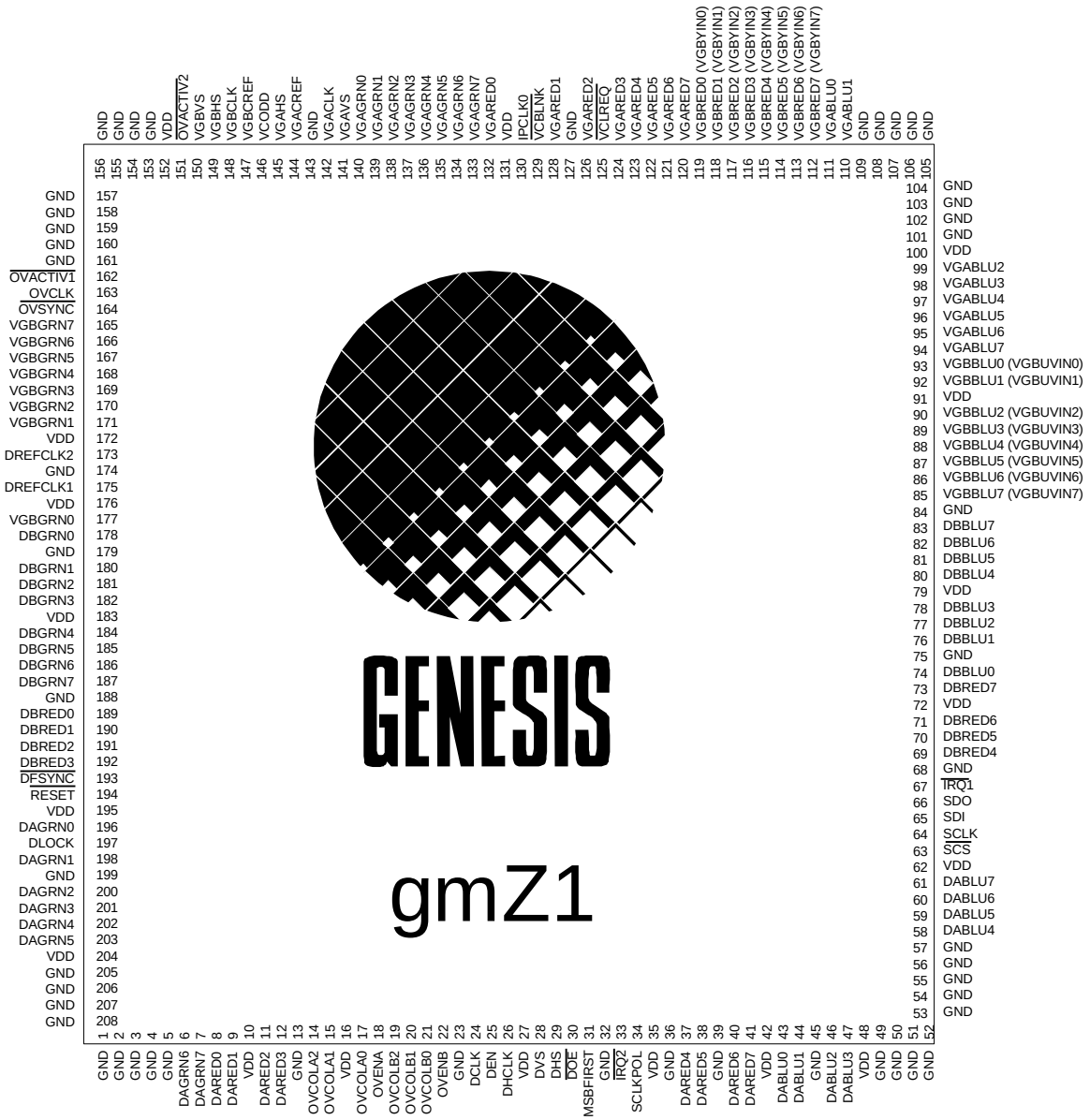


Table 1: gmZ1 Pinout

"VGB" Input Port (YUV or RGB Data) *- Input Signals*

PIN #	Symbol	I/O	Description
148	VGBCLK	I	Video input system clock
147	VGBCREF	I	Input pixel clock qualifier - programmable active high or low
150	VGBVS	I	Vertical sync - programmable active high or low
149	VGBHS	I	Horizontal sync - programmable active high or low
119	VGBRED0/VGBYIN0	I	Red input data /Input data for Y - LSBit
118	VGBRED1/VGBYIN1	I	Red input data /Input data for Y
117	VGBRED2/VGBYIN2	I	Red input data /Input data for Y
116	VGBRED3/VGBYIN3	I	Red input data /Input data for Y
115	VGBRED4/VGBYIN4	I	Red input data /Input data for Y
114	VGBRED5/VGBYIN5	I	Red input data /Input data for Y
113	VGBRED6/VGBYIN6	I	Red input data /Input data for Y
112	VGBRED7/VGBYIN7	I	Red input data /Input data for Y - MSBit
177	VGBGRN0	I	Green input data - LSBit
171	VGBGRN1	I	Green input data
170	VGBGRN2	I	Green input data
169	VGBGRN3	I	Green input data
168	VGBGRN4	I	Green input data
167	VGBGRN5	I	Green input data
166	VGBGRN6	I	Green input data
165	VGBGRN7	I	Green input data - MSBit
93	VGBBLU0/VGBUVIN0	I	Blue input data /Input data for UV - LSBit
92	VGBBLU1/VGBUVIN1	I	Blue input data /Input data for UV
90	VGBBLU2/VGBUVIN2	I	Blue input data /Input data for UV
89	VGBBLU3/VGBUVIN3	I	Blue input data /Input data for UV
88	VGBBLU4/VGBUVIN4	I	Blue input data /Input data for UV
87	VGBBLU5/VGBUVIN5	I	Blue input data /Input data for UV
86	VGBBLU6/VGBUVIN6	I	Blue input data /Input data for UV
85	VGBBLU7/VGBUVIN7	I	Blue input data /Input data for UV - MSBit

Note: VGB port input data represents the Right pixel of a pixel pair in double wide mode

"VGA" Input Port (RGB Data) *- Input Signals*

PIN #	Symbol	I/O	Description
142	VGACLK	I	Video graphics input system clock
144	VGACREF	I	Video graphics input system clock enable - programmable active high or low
141	VGAVS	I	Vertical sync - programmable active high or low
145	VGAHS	I	Horizontal sync - programmable active high or low
132	VGARED0	I	Red input data - LSBit
128	VGARED1	I	Red input data
126	VGARED2	I	Red input data
124	VGARED3	I	Red input data
123	VGARED4	I	Red input data
122	VGARED5	I	Red input data
121	VGARED6	I	Red input data
120	VGARED7	I	Red input data - MSBit
140	VGAGRN0	I	Green input data - LSBit
139	VGAGRN1	I	Green input data
138	VGAGRN2	I	Green input data
137	VGAGRN3	I	Green input data
136	VGAGRN4	I	Green input data
135	VGAGRN5	I	Green input data
134	VGAGRN6	I	Green input data
133	VGAGRN7	I	Green input data - MSBit
111	VGABLU0	I	Blue input data - LSBit
110	VGABLU1	I	Blue input data
99	VGABLU2	I	Blue input data
98	VGABLU3	I	Blue input data
97	VGABLU4	I	Blue input data
96	VGABLU5	I	Blue input data
95	VGABLU6	I	Blue input data
94	VGABLU7	I	Blue input data - MSBit

Note: VGA port input data represents the Left pixel of a pixel pair in double wide mode

Input Port Control Signals *- Common Control signals for "VGB" and "VGA" ports.*

PIN #	Symbol	I/O	Description
146	VCODD	I	Interlace Mode Field status, programmable active high or low. Default 1=odd field, 0=even field
125	$\overline{\text{VCLREQ}}$	O	Line request signal indicates the gmZ1 is ready to accept input lines
129	$\overline{\text{VCBLNK}}$	O	When de-asserted, blanking output indicates active capture window for the selected (VGA or VGB) video input

Overlay Port

PIN #	Symbol	I/O	Description
163	OVCLK	O	Clock for external overlay circuit (operates at half the display pixel rate).
164	$\overline{\text{OVSYNC}}$	O	Overlay vertical synchronization pulse indicates start of new frame of display overlay data.
162	$\overline{\text{OVACTIV1}}$	O	Overlay status indicates active overlay window region #1
151	$\overline{\text{OVACTIV2}}$	O	Overlay status indicates active overlay window region #2
18	OVENA	I	Enables overlay "A" color.
17	OVCOLA0	I	Overlay "A" color select - Blue
15	OVCOLA1	I	Overlay "A" color select - Green
14	OVCOLA2	I	Overlay "A" color select - Red
22	OVENB	I	Enables overlay "B" color.
21	OVCOLB0	I	Overlay "B" color select - Blue
20	OVCOLB1	I	Overlay "B" color select - Green
19	OVCOLB2	I	Overlay "B" color select - Red

Display Port

PIN #	Symbol	I/O	Description
30	$\overline{\text{DOE}}$	I	Display Port Output Enable. A logic "1" tri-states all Display Output Port clock, control and data output signals.
175	DREFCLK1	I	Display timing reference clock #1
173	DREFCLK2	I	Display timing reference clock #2
24	DCLK	O	Display output clock. Programmable phase.
26	DHCLK	O	Half rate display output clock. Programmable phase.
28	DVS	O	Display vertical sync. Programmable active high or low.
29	DHS	O	Display horizontal sync. Programmable active high or low.

PIN #	Symbol	I/O	Description
25	DEN	O	Display enable (specifies active area of display). Programmable active high or low.
8	DARED0	O	Red output data - LSBit
9	DARED1	O	Red output data
11	DARED2	O	Red output data
12	DARED3	O	Red output data
37	DARED4	O	Red output data
38	DARED5	O	Red output data
40	DARED6	O	Red output data
41	DARED7	O	Red output data - MSBit
196	DAGRN0	O	Green output data - LSBit
198	DAGRN1	O	Green output data
200	DAGRN2	O	Green output data
201	DAGRN3	O	Green output data
202	DAGRN4	O	Green output data
203	DAGRN5	O	Green output data
6	DAGRN6	O	Green output data
7	DAGRN7	O	Green output data - MSBit
43	DABLU0	O	Blue output data - LSBit
44	DABLU1	O	Blue output data
46	DABLU2	O	Blue output data
47	DABLU3	O	Blue output data
58	DABLU4	O	Blue output data
59	DABLU5	O	Blue output data
60	DABLU6	O	Blue output data
61	DABLU7	O	Blue output data - MSBit
189	DBRED0	O	Red output data - LSBit
190	DBRED1	O	Red output data
191	DBRED2	O	Red output data
192	DBRED3	O	Red output data
69	DBRED4	O	Red output data
70	DBRED5	O	Red output data
71	DBRED6	O	Red output data
73	DBRED7	O	Red output data - MSBit
178	DBGRN0	O	Green output data - LSBit
180	DBGRN1	O	Green output data
181	DBGRN2	O	Green output data
182	DBGRN3	O	Green output data
184	DBGRN4	O	Green output data
185	DBGRN5	O	Green output data
186	DBGRN6	O	Green output data

PIN #	Symbol	I/O	Description
187	DBGRN7	O	Green output data - MSBit
74	DBBLU0	O	Blue output data - LSBit
76	DBBLU1	O	Blue output data
77	DBBLU2	O	Blue output data
78	DBBLU3	O	Blue output data
80	DBBLU4	O	Blue output data
81	DBBLU5	O	Blue output data
82	DBBLU6	O	Blue output data
83	DBBLU7	O	Blue output data - MSBit

Note: DA output data represents the Left pixel of a pixel pair in double wide mode.
DB output data represents the Right pixel of a pixel pair in double wide mode.

Host Interface Control Signals

PIN #	Symbol	I/O	Description
194	$\overline{\text{RESET}}$	I	Reset input for initializing the device
31	MSBFIRST	I	Selects data bit order MSB or LSB first operation, 0=LSBit First; 1=MSBit First.
34	SCLKPOL	I	0=SDI sampled on SCLK rising edge, SDO clock out on SCLK falling edge.
63	$\overline{\text{SCS}}$	I	Serial Control I/F Chip select
64	SCLK	I	Serial Control I/F Clock
65	SDI	I	Serial Control I/F Input Data
66	SDO	O	Serial Control I/F Output Data

Miscellaneous Interface Signals

PIN #	Symbol	I/O	Description
67	$\overline{\text{IRQ1}}$	O	Interrupt or status output to host controller. Programmable to indicate IPVsync, OPVsync, Zoom buffer Error (over/under flow).
33	$\overline{\text{IRQ2}}$	O	Interrupt or status output to host controller. Programmable to indicate IPVsync, OPVsync, Zoom buffer Error (over/under flow).
197	DLOCK	I	Display REFCLK lock status
193	$\overline{\text{DFSYNC}}$	I	Display Timing Forced Synchronization - forces the Display Timing Generation to a programmable location within the blanking interval when a falling edge is detected.
130	IPCLKO	O	Selected input pixel port clock (VGBCLK or VGACLK). For use as reference to external display clock synthesis PLL which generates DREFCLK1 or DREFCLK2.

Power and Ground

Power Supply, +3.3V [18 pins]	10, 16, 27, 35, 42,48, 62, 72,79, 91, 100, 131,152, 172, 176, 183, 195, 204
Ground [51 pins]	1, 2, 3, 4, 5, 13, 23, 32, 36, 39, 45, 49, 50, 51, 52, 53,54, 55, 56, 57, 68, 75, 84, 101, 102, 103, 104 105, 106, 107, 108, 109, 127, 143, 153, 154, 155 156, 157, 158, 159, 160, 161, 174, 179, 188, 199 205, 206, 207, 208

5. FUNCTIONAL DESCRIPTION

5.1. Power-on Reset

A Power-on Reset cycle is required to place the gmZ1 into a defined state, and should be initiated after any power supply excursion outside of the range specified in Table 26. If a Power-on Reset cycle is not performed, the operation of the gmZ1 cannot be guaranteed and the output image data may be corrupted.

A Power-on Reset cycle is performed by asserting $\overline{\text{RESET}}$ for at least 100 nsec. This forces all internal programmable registers to be set to zero. SCLK must be asserted (logic high) for a minimum of 50 nsec during the $\overline{\text{RESET}}$ pulse.

After the $\overline{\text{RESET}}$ pulse, the selected input and display clocks (VGBCLK and DREFCLK1 by default) must receive a minimum of 8 rising clock edges before normal operation will commence.

5.2. System Clocks

There are master clocks for each of the gmZ1's four ports: the Input Port, the Display Port, the Overlay Port, and the Host Interface Port.

5.2.1. Input Port Clock

The Input Port is divided into the VGA Port and the VGB Port.

5.2.1.1. VGACLK & VGACREF - VGA Input Port (RGB Data)

The VGACLK signal provides the master clock for the VGA Input Port. This clock supports operating speeds up to 84 MHz. VGACLK synchronizes data on the input buses and the writing of data to the gmZ1. The active edge of VGACLK is programmable through the host interface.

The VGACREF (VGA Port Clock Reference) signal provides a clock by clock enable (or stall) capability when transferring data and control information into the VGA Input Port. VGACREF must be asserted during the selected edge of VGACLK for control and data information to be sampled.

5.2.1.2. VGBCLK & VGBCREF - VGB Input Port (YUV or RGB Data)

VGBCLK is the master clock for the VGB Input Port, which accepts YUV or RGB data. This clock is connected to a 1X or 2X pixel clock in the external system with operating frequencies up to a maximum of 45 MHz when in YUV mode, or 84 MHz when in RGB mode. The active edge of VGBCLK is programmable through the Host Interface.

The VGBCREF (VGB Port Clock Reference) signal provides a clock-by-clock enable (or stall) capability when transferring data and control information into the VGB Input Port. VGBCREF must be asserted during the selected edge of VGBCLK to enable the sampling of control and data information.

5.2.2. Display Port Clock

5.2.2.1. DREFCLK1 DREFCLK2, DCLK and DHCLK

Two separate display reference clocks (DREFCLK1 and DREFCLK2) are supported to allow systems to easily integrate both a free-running crystal oscillator and an external Phase Lock Loop (PLL) generated clock for display timing. The PLL display clock can be synchronized to the external video input to achieve frame lock through clock synchronization.

DREFCLK1: This clock input is driven by an external free running crystal oscillator source and is the default clock source during power-up-reset. *It must always be driven by a free-running clock for the gmZ1 device to reset properly.*

DREFCLK2: This clock input is driven from an external crystal oscillator source or PLL. The gmZ1 can be programmed to use DREFCLK2 as the display timing master clock by setting the HOSTCTRL: DREFCLK2_EN control bit.

DREFCLK1 and DREFCLK2 control all display timing. A buffered version of the enabled clock is output on the DCLK pin. A separate DHCLK signal operating at half the DCLK rate is output and available to systems using Double Pixel Mode.

The Display Port data and control outputs are sampled by any external device using the DCLK and DHCLK outputs. These clocks provide controlled set-up and hold times for sampling the data outputs. The DCLK and DHCLK active edge (rising/falling) is programmable and the clock phase relative to the data and control outputs is also software controlled. By default, DCLK and DHCLK are rising-edge aligned to the data and control outputs. (DCLK leads DHCLK which in turn leads the state changes on the control and data outputs to provide finite hold times for external devices.)

5.2.3. Overlay Port Clock

The overlay clock output, OVCLK, operates at the same frequency as DHCLK (one half of the display pixel clock rate) and must be used as the clock for any off-chip overlay generation circuitry. This clock is used by external overlay generation circuitry to latch the gmZ1 overlay output control signals and to clock the overlay color select and enable control signals into the gmZ1.

5.2.4. Host Interface Port Clock

The Serial Clock (SCLK) must be provided by the external system to clock input and output serial data. The active edge is determined by the Serial Clock Polarity (SCLKPOL) pin. Address and data transfers are composed of sixteen pulses of SCLK framed by an asserted $\overline{SCS}$ (Serial Chip Select). Each transfer cycle must consist of 16 SCLK cycles - valid control, address, or data bits must be provided with each SCLK.

5.3. Input Port

Table 2 summarizes the basic signal connections required for specific input data formats. The Reference Page gives the location of a detailed explanation for each item in this data sheet.

Table 2: Summary - I/O Interfacing to gmZ1

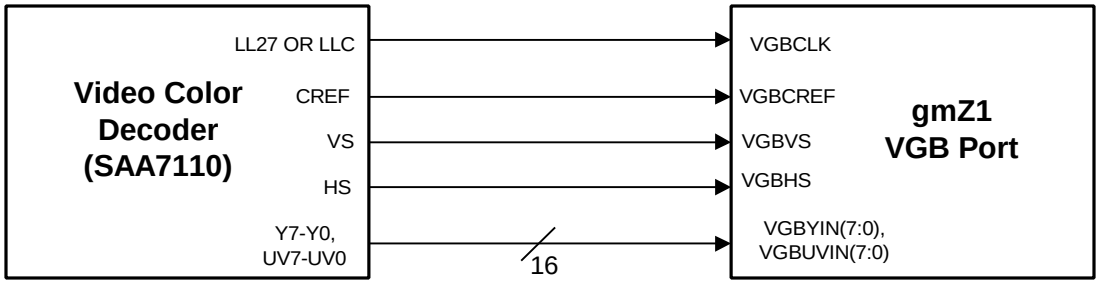
Input Data Format	Pixel Width	Required Signals	Reference Page
YUV Single Pixel	16-bit	*"VGB" Input Port*: VGBCLK, VGBCREF, VGBHS, VGBVS, VGBYIN[7:0] and VGBUVIN[7:0]. *Input Port Control Signals*: Use all signals.	16
RGB "VGB" Single Pixel	24-bit	*"VGB" Input Port*: Use all signals. *Input Port Control Signals*: Use all signals	16, 20
RGB "VGA" Single Pixel	24-bit	*"VGA" Input Port*: Use all signals. *Input Port Control Signals*: Use all signals	22, 24
RGB Double Pixel	48-bit	*"VGA" Input Port*: Use all signals. This port supports the 24-bits (Left pixel) of each 48-bit pixel pair. *"VGB" Input Port*: Use VGBRED[7:0], VGBGRN[7:0], VGBBLU[7:0]. This port supports the 24-bits (Right pixel) of each 48-bit pixel pair. This port is clocked and controlled by the VGA clock/control signals. *Input Port Control Signals*: Use all signals.	22, 25
RGB Double Pixel Offset	48-bit	*"VGA" Input Port*: Use all signals. This port supports the 24-bits of each 48-bit pixel pair. Pixels are latched when VGACREF = '1'. *"VGB" Input Port*: Use VGBRED[7:0], VGBGRN[7:0], VGBBLU[7:0]. This port supports the 24-bits (Right pixel) of each 48-bit pixel pair. This port is clocked and controlled by the VGA clock/control signals. Pixels are latched when VGACREF = '0'. *Input Port Control Signals*: Use all signals.	22, 26

5.3.1. VGB Input Port

The VGB Input Port supports interlaced and non-interlaced data streams and provides an easy direct connection to most common color decoder chips. As an example, a glueless connection from the Philips SAA7110 color decoder to the gmZ1 VGB Input Port is shown in Figure 4.

The VGB Input Port supports video timing for square pixel and CCIR601 formatted NTSC/PAL/SECAM, as well as non-standard data streams. The VGB port supports YUV and RGB data formats.

Figure 4: Video Color Decoder Connection to gmZ1



The gmZ1 always uses an even number of active Y and UV samples per line. Odd numbers of active samples are not supported, however the total number of pixel clocks (blanking and active) per line can be an odd value.

5.3.1.1. VGB Port I/O Signals (YUV Data)

VGBVS

The VGB Input Port samples VGBVS (VGB Port Vertical Sync) during qualified VGBCLK cycles, i.e. when VGBCREF is asserted during an active VGBCLK edge. When VGBVS assertion is detected, the gmZ1 begins processing a new input field. The VGBVS active state is programmable via the HOSTCTRL register.

VGBHS

The VGB Input Port samples VGBHS (VGB Port Horizontal Sync) during qualified VGBCLK cycles. Upon VGBHS assertion, the VGB Input Port prepares for the next incoming line of video data. The VGBHS active state is programmable via the HOSTCTRL register.

Note: VGBHS can be used to stall the gmZ1 on a "line-by-line" basis.

VCODD

The VCODD signal (Input ODD Field Indicator) determines the vertical start location of the active window. For interlaced video sources, VCODD selects one of two programmable vertical start locations. For non-interlaced video sources, this signal is ignored and all input frames are treated as "ODD" fields. VCODD is common to the VGB and VGA Input Ports.

VCODD must be valid during each field/frame's first active VGBHS pulse as defined by the IPV_STARTODD or IPV_STARTEVN programmable registers. Since VCODD determines the field polarity, it must assume its correct state before the lesser of the start odd or start even values. VCODD must remain valid for the entire vertical active region, i.e. during all active lines. The VCODD active state is programmable via the register set. (By default, VCODD = '1' indicates odd fields.)

$\overline{\text{VCBLNK}}$

$\overline{\text{VCBLNK}}$ (Input Port Composite Blanking Indicator) indicates that the gmZ1 device is sampling pixels in the Active Display Window region. This signal frames the active region when the gmZ1 accepts pixel data for zoom processing. This signal is common to the VGB/VGA Input Ports.

When required, the external system should sample $\overline{\text{VCBLNK}}$ during qualified clock edges (i.e. during a valid combination of VGBCLK edge and VGBCREF state). $\overline{\text{VCBLNK}}$ is de-asserted two qualified pixel clocks before the first input data is sampled, and can be used as a pixel request signal.

For applications where the external system is providing VGB Input Port data from a memory storage buffer (i.e. frame buffer, FIFO) , the predictive blanking signal allows the system one qualified clock edge to sample $\overline{\text{VCBLNK}}$, and the next qualified clock edge to output data to the VGB Port. This data is then sampled on the subsequent qualified clock edge by the gmZ1. For applications where the external system is providing free-running video and control signals to the Input Port, the $\overline{\text{VCBLNK}}$ signal does not provide any controlling function, but can be used to monitor the active samples accepted by the VGB Input Port.

$\overline{\text{VCLREQ}}$

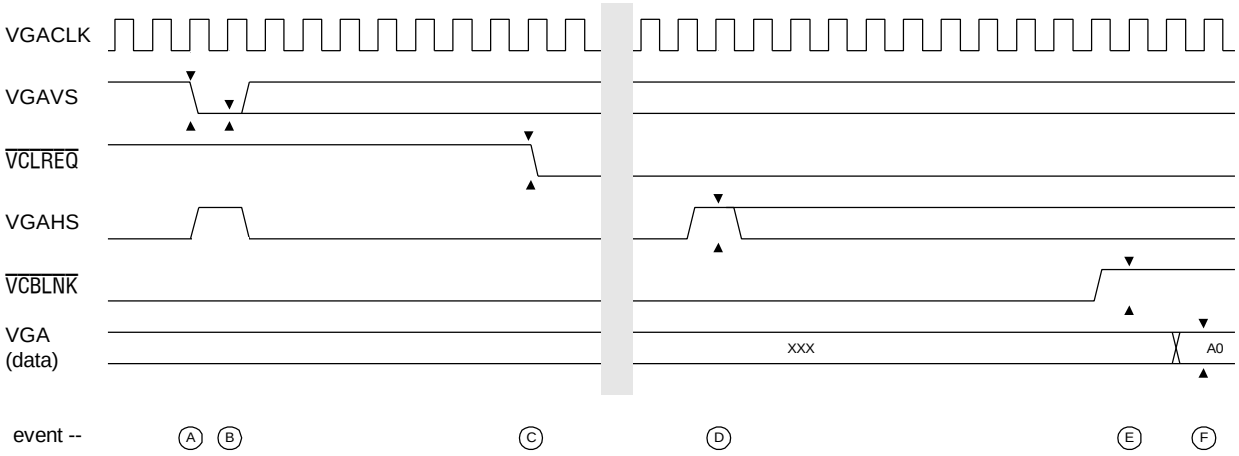
The Line Request, $\overline{\text{VCLREQ}}$ output signal that indicates the gmZ1 is ready for input video lines. This signal is common to the VGA/VGB Input Port.

If the external system is providing a free-running video source to the VGB Port, the $\overline{\text{VCLREQ}}$ signal is not typically utilized, since the flow of video data and control information cannot be stalled. However, $\overline{\text{VCLREQ}}$ can be monitored to determine the input lines accepted by the VGB Input Port.

If the external system is providing source data and control information from a memory device without periodic video line timing, the gmZ1 de-asserts $\overline{\text{VCLREQ}}$ at the end of each active video line until the VGB Port is ready for the next line. $\overline{\text{VCLREQ}}$ is always de-asserted between input video lines to stall the flow of input data while the gmZ1 is flushing internal pipelines. When $\overline{\text{VCLREQ}}$ is asserted to request the next input line, the system should always provide a VGBHS to initialize the gmZ1 for the next line. VGBHS should be followed by the programmed amount of blanking and valid data.

Once asserted to request data, $\overline{\text{VCLREQ}}$ will remain asserted until the programmed number of pixels have been transferred into the VGB Port. $\overline{\text{VCLREQ}}$ and $\overline{\text{VCBLNK}}$ are intended to be utilized by system frame buffer controllers to provide high-speed pipelined image/video data interfaces with minimal external glue logic.

Figure 5: VCLREQ, VCBLNK - Start of Frame



A - VSYNC occurs
B - VGA Port samples VGAVS to detect start of first line of a new field or frame. GmZ1 internal line # set to 1.
C - VCLREQ is asserted nine clocks after VGAVS assertion.
D - gmZ1 reaches vertical active region start value (IPV_ACTIV_STARTODD, IPV_ACTIV_STARTEVN)
E - VGA Port indicates pending start of active region, 2 pixels before IPH_ACTIV_START.
F - VGA Port samples first pixel of first line of frame. There are IPH_ACTIV_WIDTH active pixel samples per active line.

Note: VGAVS is programmed active low, VGAHS is programmed active high.

Figure 6: VCLREQ Operation

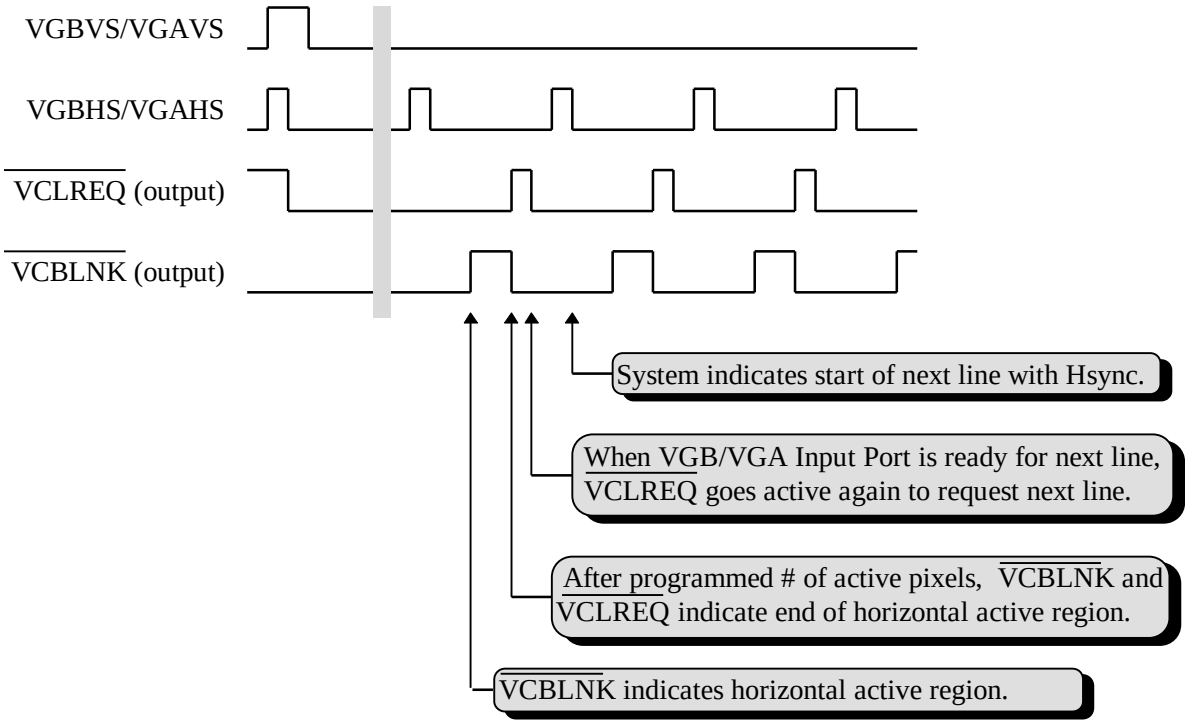
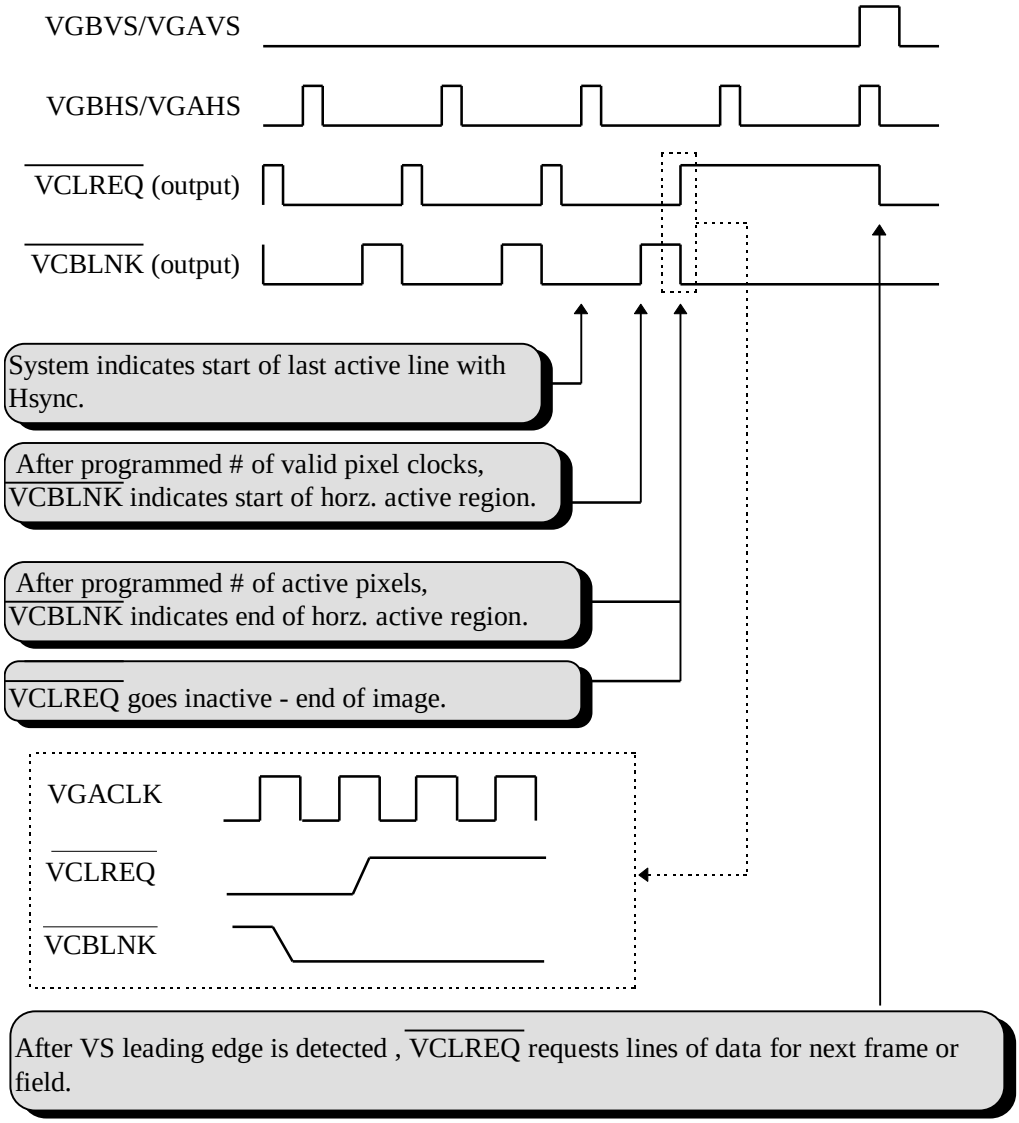


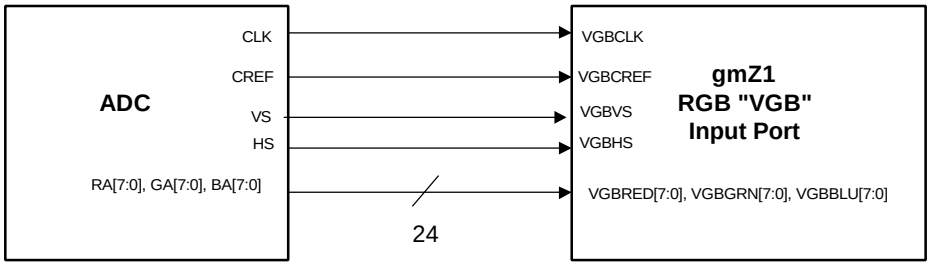
Figure 7: VCLREQ Operation During End of Frame/Field



5.3.1.2. VGB Port I/O Signals (RGB Data)

The VGB port supports RGB single pixel data on its own (up to 84MHz data rates), or double-pixel data streams in combination with the VGA port. The VGA port is described beginning with section 5.3.2. A connection to an RGB single-pixel source is shown below in Figure 8.

Figure 8: Single Pixel Mode - VGB Port Interfacing



The functionality of the control signals is identical whether the VGB port is processing YUV or RGB data.

5.3.1.3. Data Format

YUV input data is accepted through an 8-bit Y channel, and an 8-bit multiplexed UV (or Cb, Cr) channel. UV data is sub-sampled using standard 4:2:2 sampling. Y data values can be full range 0 - 255; however, they will be clamped by internal circuitry to be in the CCIR601 range (16 to 235). UV data values can be full range 0 - 255; however, they will be clamped by internal circuitry to be in the range 16 to 240. See Figure 9. The VGB port also accepts full scale RGB data on the VGBRED, VGBGRN, and VGBLU buses. *The gmZ1 contains a color space converter that always transforms 4:2:2 YUV data to 24-bit RGB.*

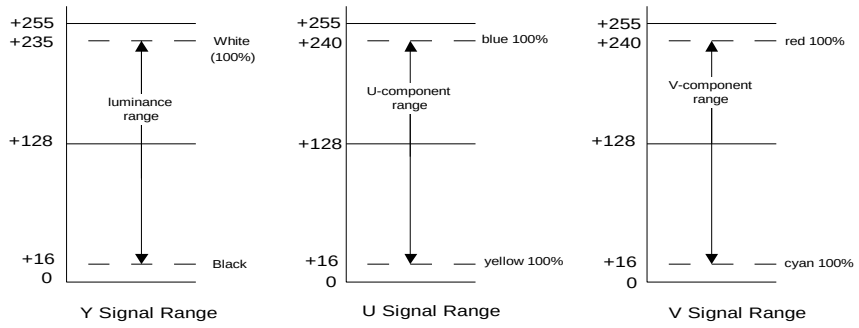
R = 1/256 [298Y + 409V - 57014]

G = 1/256 [298Y - 100U - 208V + 34692]

B = 1/256 [298Y + 517U + 1V - 70964]

Cb = U, Cr = V

Figure 9: CCIR 601 Signal Range



5.3.2. VGA Input Port

The VGA Input Port accepts real-time video graphics data and control signals (HSYNC, VSYNC, Pixel clock, Clock Qualifier). The VGA Input Port supports interlaced and non-interlaced video data streams with three different input modes: Single-Pixel, Double-Pixel and Double-Pixel-Offset.

5.3.2.1. VGA Port I/O Signals

VCODD

The VCODD signal (Input ODD Field Indicator) determines the vertical start location of the active window. For interlaced video sources, VCODD selects one of two programmable vertical start locations. For non-interlaced video sources, this signal is ignored and all input frames are treated as "ODD" fields. VCODD is common to the VGB and VGA Input Ports.

VCODD must be valid during each field/frame's first active VGAHS pulse as defined by the IPV_STARTODD or IPV_STARTEVN programmable registers. Since VCODD determines the field polarity, it must assume its correct state before the lesser of the start odd or start even values. VCODD must remain valid for the entire vertical active region i.e. during all active lines. The VCODD active state is programmable via the register set. (By default, VCODD = '1' indicates odd fields.)

$\overline{\text{VCBLNK}}$

$\overline{\text{VCBLNK}}$ (Input Port Composite Blanking Indicator) indicates that the gmZ1 device is sampling pixels in the Active Display Window region. This signal frames the active region when the gmZ1 accepts pixel data for zoom processing. This signal is common to the VGB/VGA Input Ports.

When required, the external system should sample $\overline{\text{VCBLNK}}$ during qualified clock edges (i.e. during a valid combination of VGBCLK edge and VGBCREF state). $\overline{\text{VCBLNK}}$ is de-asserted two qualified pixel clocks before the first input data is sampled, and can be used as a pixel request signal.

For applications where the external system is providing VGA Input Port data from a memory storage buffer (i.e. frame buffer, FIFO) , the predictive blanking signal allows the system one qualified clock edge to sample $\overline{\text{VCBLNK}}$, and the next qualified clock edge to output data to the VGA Port. This data is then sampled on the subsequent qualified clock edge by the gmZ1. For applications where the external system is providing free-running video and control signals to the Input Port, the $\overline{\text{VCBLNK}}$ signal does not provide any controlling function, but can be used to monitor the active samples accepted by the VGB Input Port.

$\overline{\text{VCLREQ}}$

The Line Request, $\overline{\text{VCLREQ}}$ output signal indicates the gmZ1 is ready for input video lines. This signal is common to the VGA/VGB Input Port.

For applications where the external system is providing a free-running video source to the VGA Port, the $\overline{\text{VCLREQ}}$ signal is not typically utilized, since the flow of video data and control information cannot be stalled. However, $\overline{\text{VCLREQ}}$ can be monitored to determine the input lines accepted by the VGA Input Port.

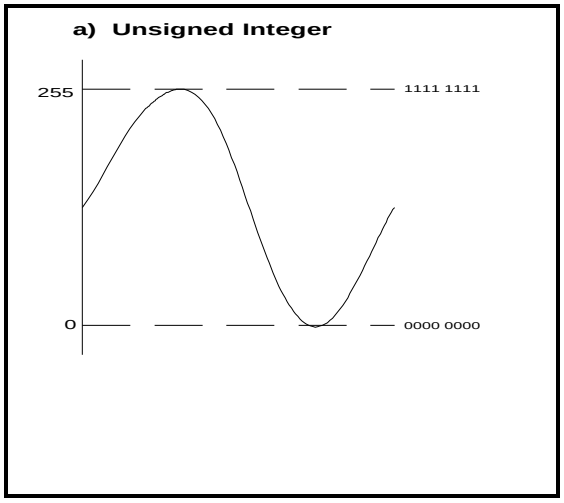
If the external system is providing source data and control information from a memory device without periodic video line timing, the gmZ1 de-asserts $\overline{\text{VCLREQ}}$ at the end of each active video line until the VGA Port is ready for the next line. $\overline{\text{VCLREQ}}$ is always de-asserted between input video lines to stall the flow of input data while the gmZ1 is flushing internal pipelines. When $\overline{\text{VCLREQ}}$ is asserted to request the next input line, the system should always provide a VGAHS to initialize the gmZ1 for the next line. VGAHS should be followed by the desired number of blanking and valid data.

Once asserted to request data, $\overline{\text{VCLREQ}}$ will remain asserted until the programmed number of pixels have been transferred into the VGA Port. $\overline{\text{VCLREQ}}$ and $\overline{\text{VCBLNK}}$ are intended to be utilized by system frame buffer controllers to provide high-speed pipelined image/video data interfaces with minimal external glue logic. See Figure 6 and Figure 7.

5.3.2.2. Data Format

The VGB port supports single pixel width (24 bit) and double pixel width (48 bit transfers). Each pixel consists of 8 bits for each color component: R (Red), G (Green), and B (Blue). Individual Red, Green, and Blue data values are full range 0 - 255.

Figure 10: Data Range



5.3.2.3. Pixel Width Control

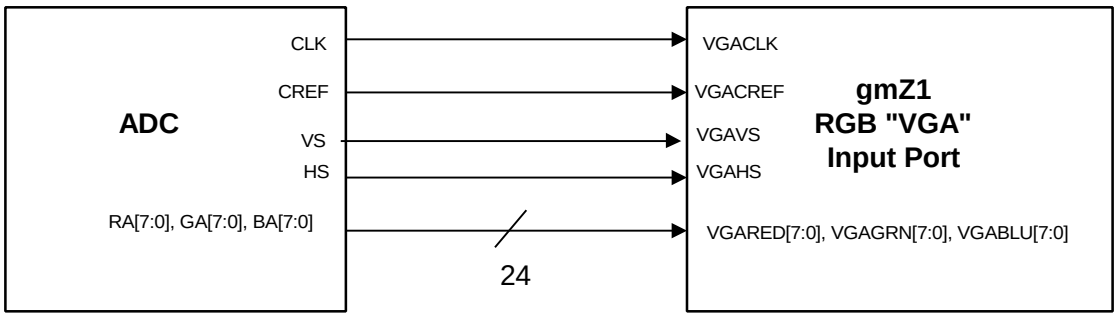
The three available pixel modes are selected by the IPCTRL register and IP2PIXWIDE_EN and IP2PIXOFFSET_EN bits.

Figure 11: Pixel Width Mode

Mode	IP2PIXWIDE_EN	IP2PIXOFFSET_EN	RGB_B_SEL	IP_RGB_EN
Single Pixel VGA Port	0	0	0	1
Single Pixel VGB Port	0	0	1	1
Double Pixel	1	0	0	1
Double Pixel Offset	0	1	0	1
YUV Single Pixel	0	0	0	0

5.3.2.3.1. Single Pixel Mode

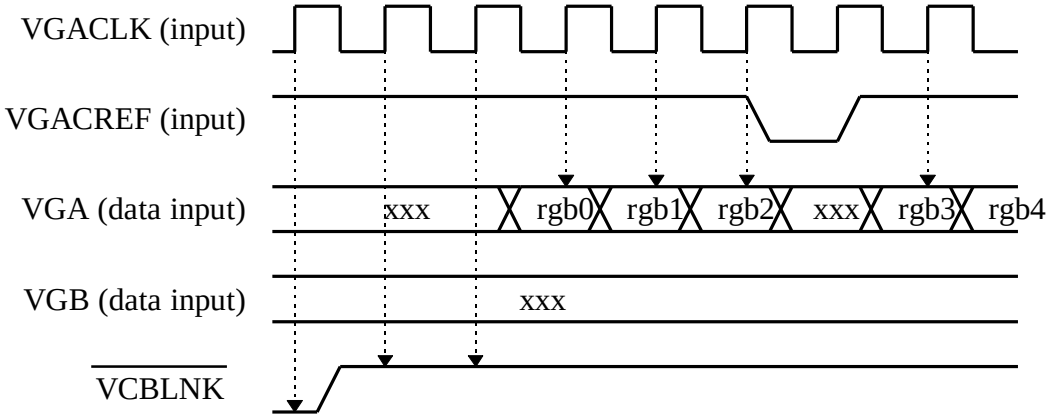
Figure 12: Single Pixel - RGB "VGA" Port Interfacing



In this mode, the Horizontal Active Window is programmable in single pixel increments. The sync and control signals are sampled by the gmZ1 every pixel clock when the pixel clock qualifier (VGACREF) is active. 24-bit RGB data is transferred into the gmZ1 only when VGACREF is asserted during the "active" region as indicated by $\overline{\text{VCBLNK}}$. There is a two clock latency between $\overline{\text{VCBLNK}}$ being de-asserted and data being accepted by the gmZ1.

- VGAVS (VGA Port Vertical Sync) is sampled during the selected edge of VGACLK when VGACREF is active.
- VGAHS is sampled during the selected edge of VGACLK when VGACREF is active.

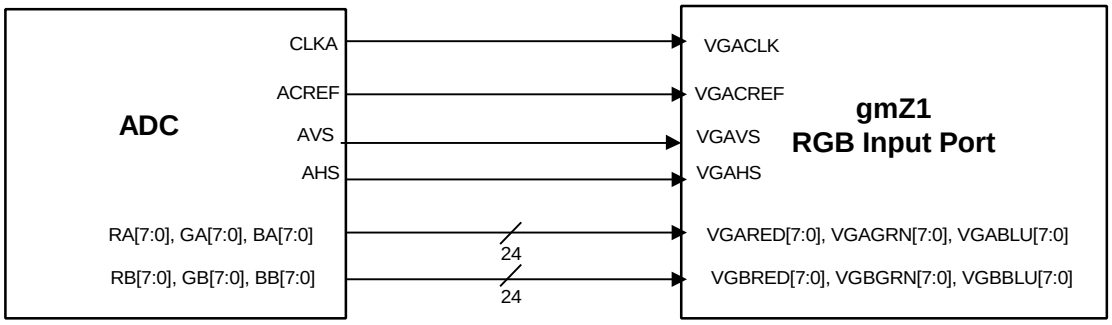
Figure 13: RGB Single Pixel Timing



Note: There is a two clock latency between the de-assertion of $\overline{\text{VCBLNK}}$ *and the gmZ1 accepting data. There is also a two clock latency at the end of a line between assertion of* $\overline{\text{VCBLNK}}$ *and the last data sample accepted by the gmZ1.*

5.3.2.3.2. Double Pixel Mode

Figure 14: Double Pixel - VGA and VGB Ports Interfacing



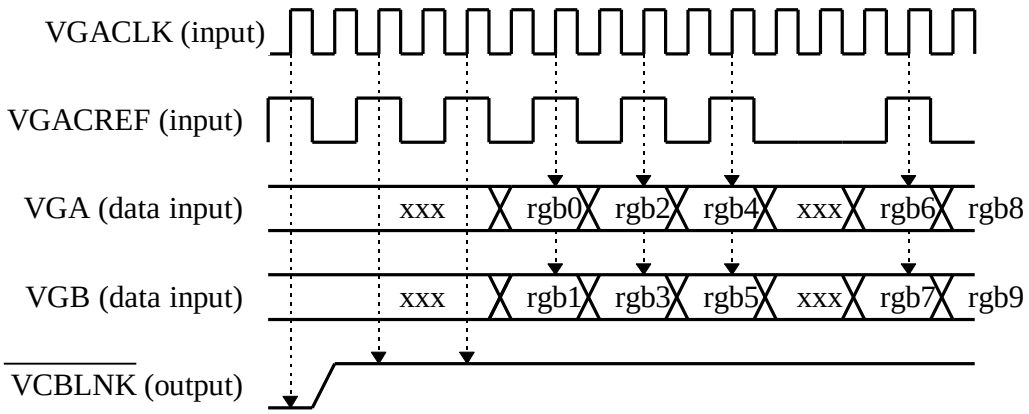
In this mode, the Horizontal Active Window is programmable in double pixel increments. The gmZ1 samples the sync and control signals every pixel clock when the pixel clock qualifier (VGACREF) is active. Note that only pixel clocks where VGACREF is active are counted.
Both the VGA and VGB buses are sampled on every qualified pixel clock during the active region indicated by the $\overline{\text{VCBLNK}}$ signal.

Note that the maximum transfer rate is one pixel pair every two pixel clocks. VGACREF must be inactive for at least 1 clock period every other pixel clock. Data is not sampled when the pixel

clock qualifier is in-active. Therefore in Double Pixel Mode the sync inputs always correspond to 2 pixels.

- VGAVS (VGA Port Vertical Sync) is sampled during the selected edge of VGACLK when VGACREF is active.
- VGAHS is sampled during the selected edge of VGACLK when VGACREF is active

Figure 15: RGB Double Pixel Timing



Note: There is a two clock latency between the de-assertion of $\overline{\text{VCBLNK}}$ *and the gmZ1 accepting data. There is also a two clock latency at the end of a line between the assertion of* $\overline{\text{VCBLNK}}$ *and the last data sample accepted by the gmZ1.*

5.3.2.3.3. Double Pixel Offset Mode.

In this mode, the Horizontal Active Window is programmable in single pixel increments. The sync and control signals are sampled by the gmZ1 every pixel clock, independently of the pixel clock qualifier (VGACREF) state. All pixel clocks are counted.

Pixel data on the VGA bus (24 bit RGB) is transferred into the gmZ1 on each rising edge of pixel clock while VGACREF is active. Pixel data on the VGB (24-bit RGB) is transferred into the gmZ1 on rising edge of the pixel clock while VGACREF is NOT active. The VGACREF active state is programmable to allow the interchanging of A and B Port transfers. The pixel clock qualifier acts as a pixel A/B select for systems providing double width pixel data in a “ping-pong” fashion. Note that the pixel transfer rate is one pixel pair every two pixel clocks and the pixel clock qualifier must be half the pixel clock frequency.

- VGAVS (VGA Port Vertical Sync) and VGAHS are sampled during the selected edge of VGACLK. (Not dependent on the state of VGACREF).

Figure 16: RGB Double Pixel Offset Timing #1

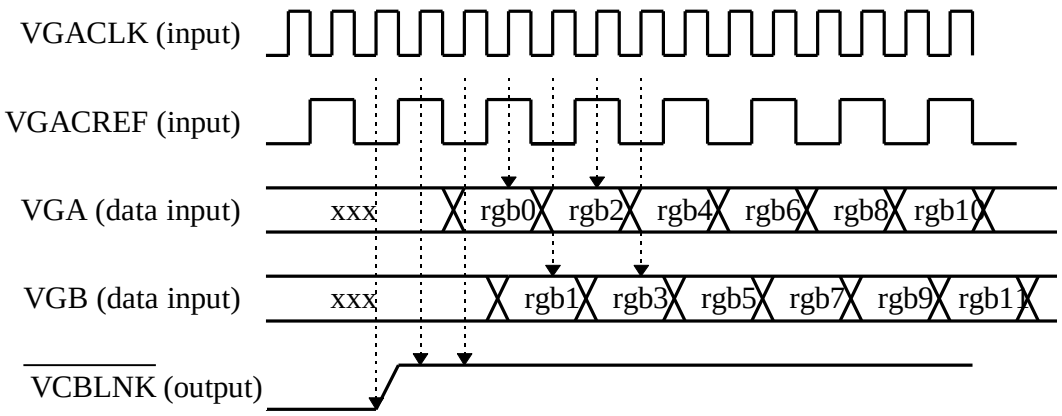
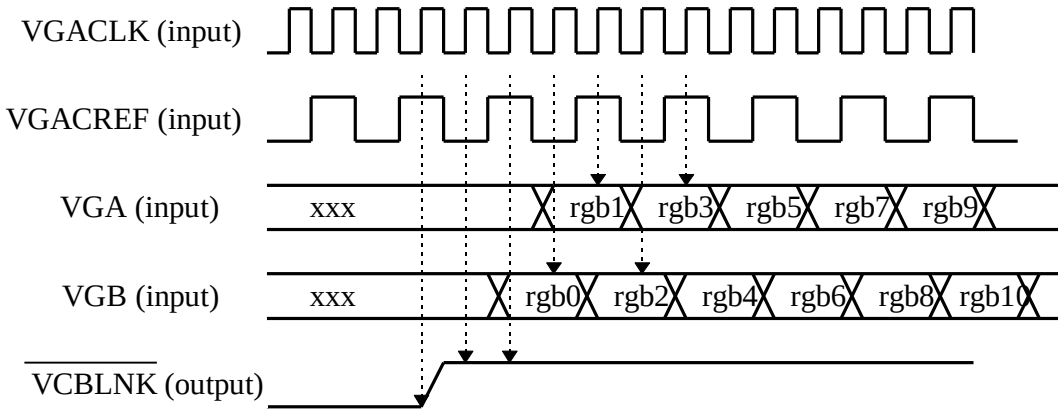


Figure 17: RGB Port Double Pixel Offset Timing #2



Note: In Figure 16 and Figure 17 there is a two clock latency between the de-assertion of $\overline{VCBLNK}$ and the gmZ1 accepting data. This latency also holds true at the end of a line, between the assertion of $\overline{VCBLNK}$ and the last data sampled.

5.3.3. Operating Modes

The gmZ1 operates in several modes: No Zoom, Standard Zoom and De-Interlacing Zoom. These modes will either allow the data to "pass-through" (i.e. the output data will be identical to

the input or the de-interlaced input), data will be zoomed (magnified), or the interlaced data will be de-interlaced and possibly zoomed.

5.3.3.1. No Zoom Mode

In No Zoom mode, the input image data passes through the gmZ1 unchanged. The number of active pixels per line and the number of active lines per frame remains unchanged. However, the data crosses clock boundaries from the input video pixel clock to the display pixel clock.

No Zoom mode is enabled when the input and output active windows are the same size, i.e. register values for the Input Video Register are equal:

IPH_ACTIV_WIDTH = DH_ACTIV_WIDTH

IPV_ACTIV_LNGTH = DV_ACTIV_LNGTH

No Zoom mode also requires the horizontal and vertical scaling values to be set to zero, i.e. Z_HORZ_SV = 0 and Z_VERT_SV = 0.

5.3.3.2. Standard Zoom Mode

This mode is used to magnify non-interlaced data, i.e. graphics. Input image data may be magnified both vertically and horizontally - the vertical and horizontal zoom ratios are independently adjustable. The zoom ratio is set by programming the input active window parameters to the source image size, and by programming the display active window parameters to the required output image size. The Z_HORZ_SV and Z_VERT_SV registers must be programmed for zoom operation.

DH_ACTIV_WIDTH > IPH_ACTIV_WIDTH

DV_ACTIV_LNGTH > IPV_ACTIV_LNGTH

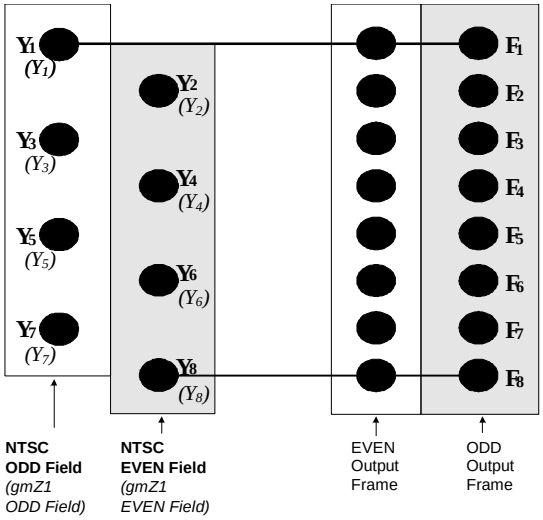
5.3.3.3. De-Interlacing Zoom Mode

This mode is used to spatially de-interlace input data, i.e. video. Every input field is magnified to the output frame resolution, however, the even and odd fields have different fractional vertical offsets applied to properly map the two input fields into the non-interlaced output frame. This ensures the fields are correctly aligned in the output frame and eliminates interlacing artifacts.

5.3.3.3.1. NTSC Video

The spatial de-interlacing process assumes the ODD field is always mapped spatially higher than the EVEN field, which is true for NTSC video sources. No special operations are required by the user to handle NTSC video.

Figure 18: NTSC De-Interlacing Zoom



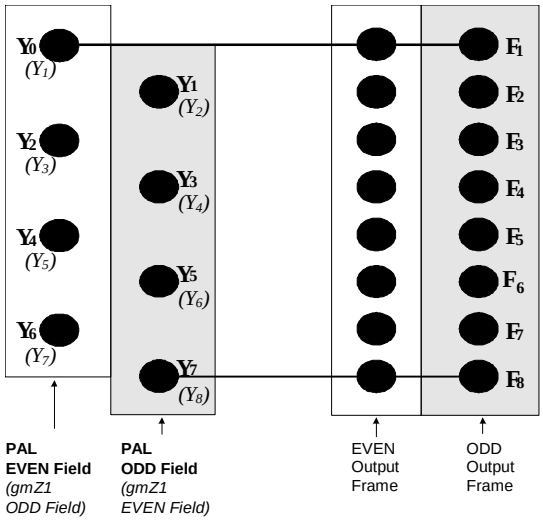
where
IPV_ACTIV_STARTODD = Y_1
IPV_ACTIV_STARTEVN = Y_2

5.3.3.3.2. PAL

For PAL sources, the ODD field is mapped spatially lower than the EVEN field. Since the gmZ1 always maps input fields spatially higher when VCODD is active, the PAL definition of ODD can be accommodated by inverting the VCODD "active" state through the IPCTRL register IPODD_INV control bit.

IPODD_INV should be programmed so that the VCODD active state corresponds with input fields mapped spatially higher in the output frame. Also the IPV_ACTIV_STARTODD control register should be loaded with the vertical start location of the spatially higher input field. The IPV_ACTIV_STARTEVN control register should be loaded with the spatially lower input field.

Figure 19: PAL De-Interlacing Zoom



where
IPV_ACTIV_STARTODD = Y_0
IPV_ACTIV_STARTEVN = Y_1

The EVEN field is mapped spatially higher by inverting the VCODD active state in the IPCTRL register.

5.3.4. Input Active Window Control

The Input Active Window Control provides a means for programming the active window region for the selected input video on either the VGA or VGB Input Port. The horizontal sync and vertical sync controls are used from the selected port to determine the active window region. Only pixels transferred into the device during the Active Window region are used as source data for the scaling process and resulting display output. The Active Window is defined using registers IPV_ACTIV_STARTODD, IPV_ACTIV_STARTEVN, IPV_ACTIV_LNGTH, IPH_ACTIV_START, and IPH_ACTIV_WIDTH.

During single pixel mode, the Horizontal Active Window is programmable in single pixel increments. Note that only qualified pixel clocks (i.e. when VGACREF or VGBCREF is asserted) are counted. When processing YUV inputs, the active region is programmable in single pixel increments, however an even number of active pixels per line should always be used. Note that only pixel clocks where VGBCREF is active are counted.

For interlaced video, VCODD determines which of two possible Vertical Active Region start locations will be used.

Figure 20: YUV Data Start of Active Window

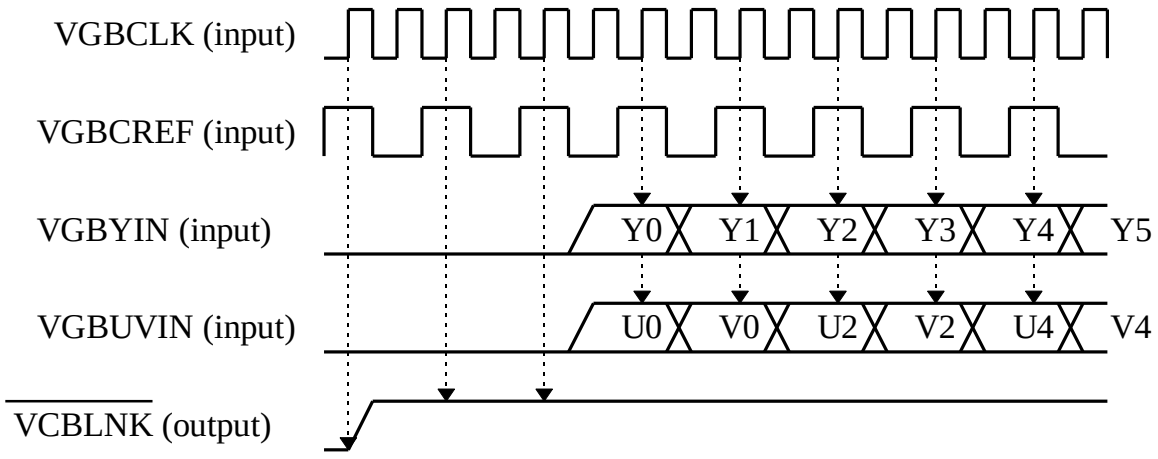
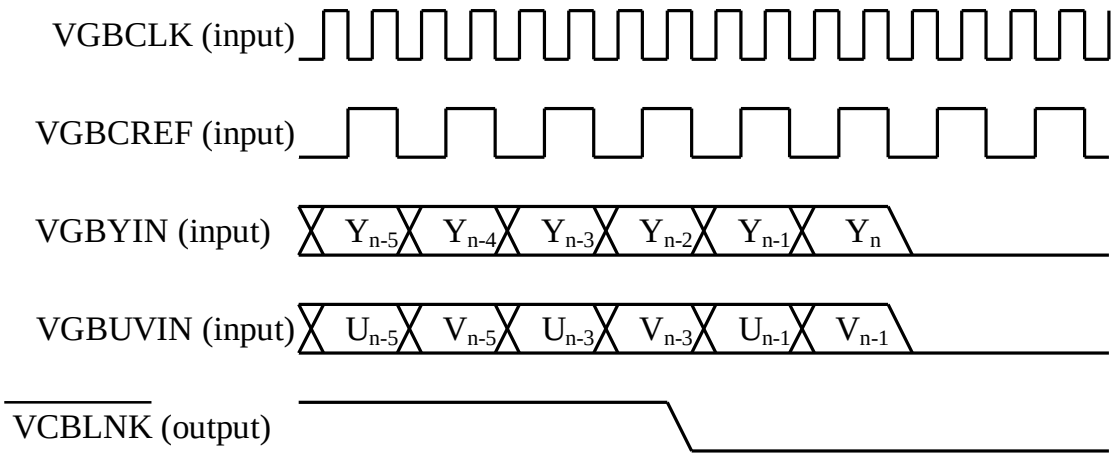


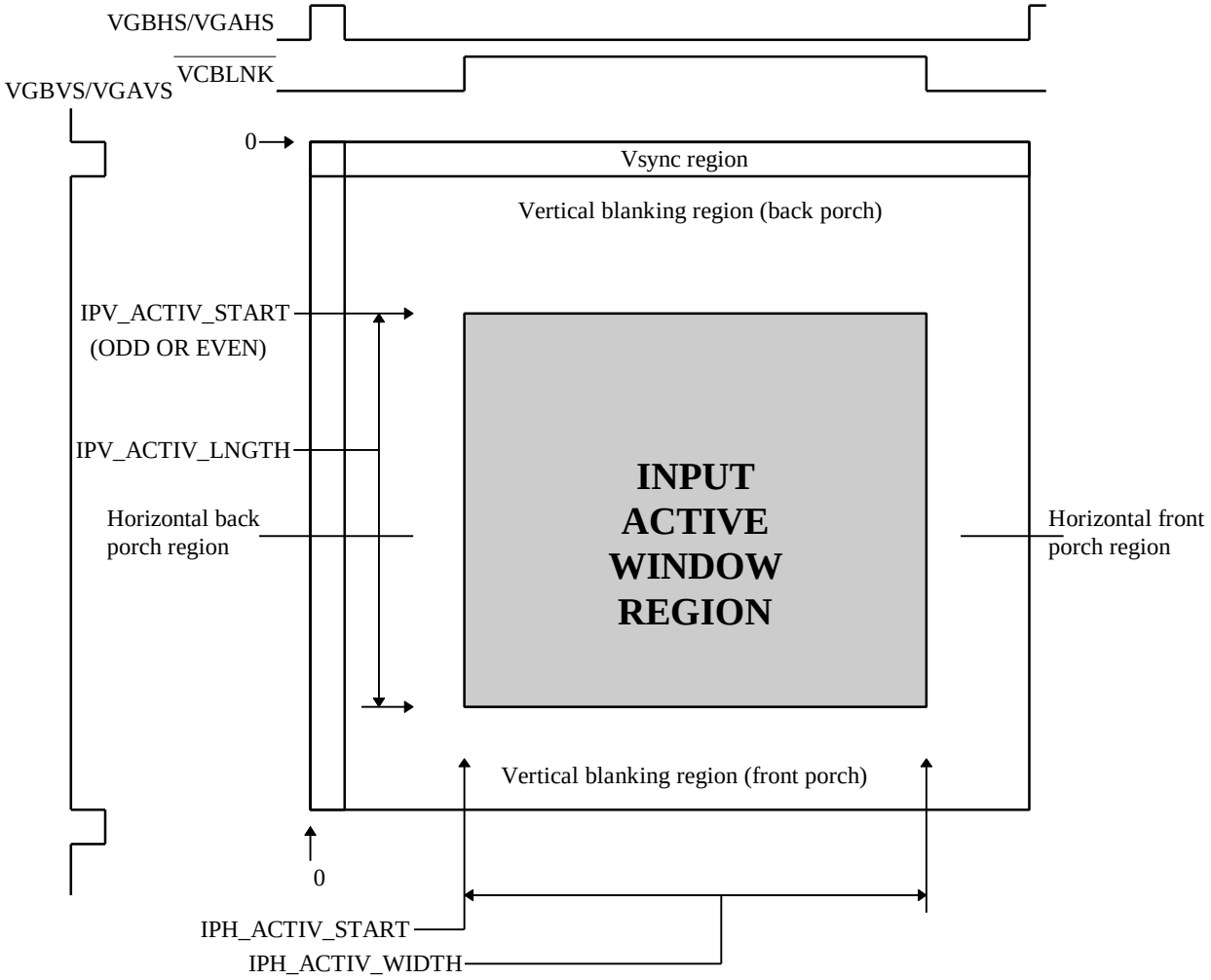
Figure 21: YUV Data End of Active Window



During the double pixel mode, the active region is programmable in double pixel increments. Note that only pixel clocks where VGACREF is active are counted.

During the double pixel offset mode, the active region is programmable in single pixel increments. However, all pixel clocks are counted regardless of the state of VGACREF.

Figure 22: Input Active Window



5.4. RGB Output Port

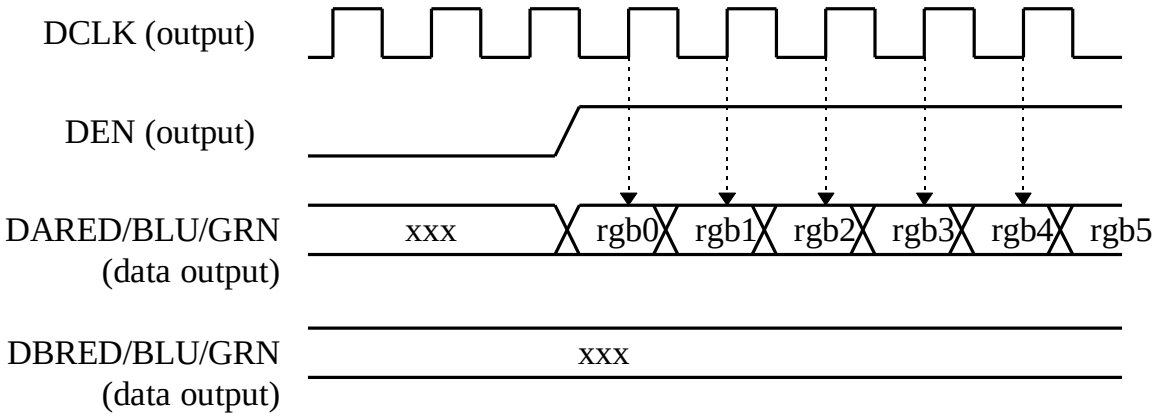
The RGB Output Port sends zoomed video data and control signals to an external display or storage device. This port controls several functions such as data transfer (single/double pixel) and generating the output timing to synchronize the data with the display timing. The RGB Output Port will also support display devices with 6 bits per color, using dithering circuitry which can be enabled by setting the DOUTCNTRL: D_18BIT_EN control bit. Dithering prevents contouring or banding in the display output as a result of the reduced display color resolution. The 6-bit rounding circuitry is optimized to prevent line by line correlation (vertically) and frame by frame correlation (temporally).

5.4.1. Data Transfer Modes

5.4.1.1. Single Pixel Mode

Single pixel data (24-bit RGB) is transferred to display port 'A' (DARED/BLU/GRN) on each active edge of DCLK. Note that the DHCLK signal phase may vary from line to line depending on the line length and Display Synchronization Mode. Normally DHCLK is not used by the external system in this mode. The sync and controls are transferred to display port outputs on each active edge of DCLK. This mode can be selected by programming the DOUTCNTRL register.

Figure 23: Display Data Timing Single Pixel Mode

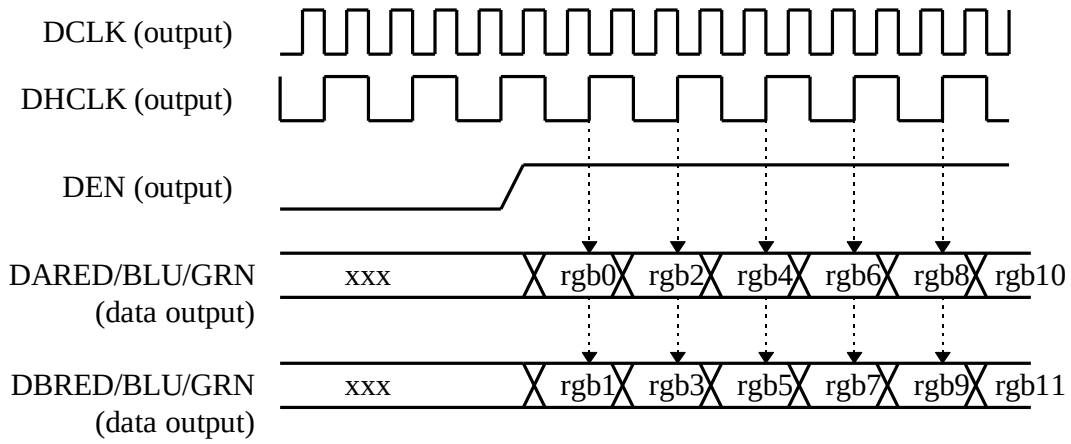


Note: DCLK and DEN polarity are independently programmable within the gmZ1.

5.4.1.2. Double Pixel Mode

Double width pixel data (48-bit RGB), sync, and control information are transferred to the display port outputs on alternate DCLKs. The transfers are synchronized with the half rate clock, DHCLK. DHCLK can be programmed to be rising or falling edge aligned with the data transfers. DHCLK can also be adjusted in ¼ cycle increments relative to data/control transfers. This mode can be selected by programming the DOUTCNTRL register.

Figure 24: Display Data Timing Double Pixel Mode



Note: DCLK, DHCLK, and DEN polarity are all independently programmable.

5.4.2. Programmable Input Lock Event

The Lock Event is a programmable point in time, where the Display Timing Generator synchronizes the input video source and display output frame timing with a programmable amount of phase skew between them. The phase skew between the input and output frame is programmable to optimize the usage of the on chip zoom buffer, i.e. prevent zoom buffer overflow/underflow. The lock event is set through registers IPH_LOCK_EVENT and IPV_LOCK_EVENT. It occurs once per input frame, during any specified pixel location and can be disabled by setting the IPH_LOCK_EVENT and IPV_LOCK_EVENT registers to zero. For Interlaced video sources the LOCK_EVENT occurs during the ODD fields but not during the EVEN fields. Lock Events can also be generated externally by the system using the $\overline{\text{DFSYNC}}$ pin (this requires the DFSYNC_EN control bit to be set).

5.4.3. D_BYPASS Mode

An additional "Bypass" mode is supported within Double Pixel Mode. D_BYPASS Mode transfers the VGA Input Port data and sync inputs directly to the display output port at the input clock rate. There is no processing of the data stream, no zoom operations supported, and the overlay is bypassed (not supported) as well.

5.4.3.1. Mode Selection

D_BYPASS Mode is only supported when the VGA Port is programmed as the input port, interlaced operation is disabled, the input data format is "Double Width Pixel Mode", and No Zoom mode is selected (see Section 5.3.3.1). When all of the above are true, D_BYPASS Mode can be selected by setting the HOSTCTRL register: D_BYPASS_EN control bit to '1'.

5.4.3.2. Output Signals

During D_BYPASS Mode the DCLK output is driven by a buffered version of the VGA Port VGACLK input. The DHCLK output is driven by a pipelined version of the VGACREF signal that aligns with the data output delay. The DCLK and DHCLK signals can still be inverted under software control using the DOUTCNTRL register.

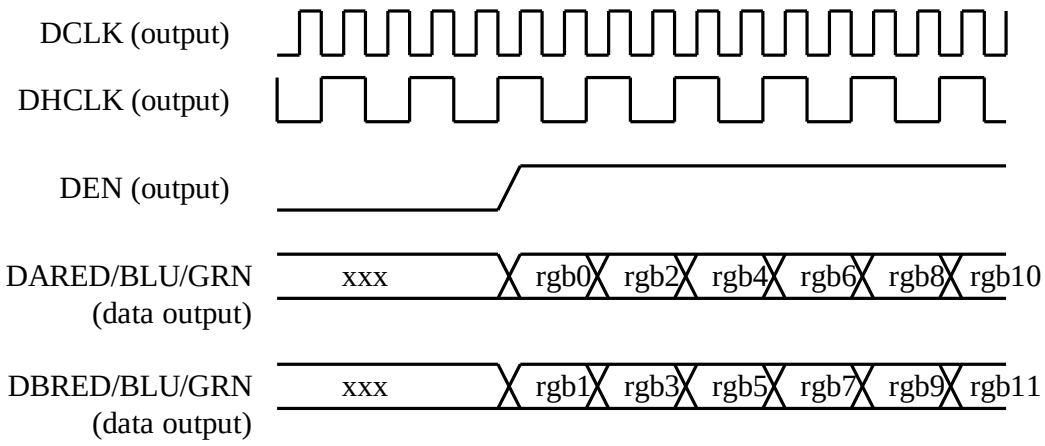
The DEN signal is driven with a pipelined version of the Input Port Composite Blanking Indicator ($\overline{\text{VCBLNK}}$ **)** output signal, compensated with pipeline delays to align with the display output data.

The display output data is driven with a delayed version of the VGA Port input data clocked out of the Display Port as shown in Figure 25. Note the VGARED/BLU/GRN inputs are transferred to the DARED/BLU/GRN outputs. The VGBRED/BLU/GRN inputs are transferred to the DBRED/BLU/GRN outputs.

Table 3: Corresponding Input/Output Signals in D_BYPASS

The input signal ⟶	Becomes the output signal
VGA port input data	DA port display data
VGB port input data	DB port display data
$\overline{\text{VCBLNK}}$	DEN
$\overline{\text{V}}$ $\overline{\text{CRE}}$	DHCLK
VGACLK	DCLK

Figure 25: D_BYPASS Mode Display Timing



Note: DCLK, DHCLK and DEN polarity are independently programmable.

5.4.4. Display Timing Generation

The Display Timing Generator supports four display synchronization modes. The display synchronization mode is selected through the Host Interface DCONTROL register.

Free Run Mode:	supports frame buffers; frame-rate conversion applications
Frame Sync Mode:	forced synchronization of input and output frame periods
Line Sync Mode:	display line rate synthesized from input line rate and the forced synchronization of input and output frame periods
Clock Sync Mode:	system-supplied display clock tracks input clock *- Clock Sync Mode is not recommended since there is no continuous forced synchronization of input and output frame periods.*

Table 4: Display Timing Generation: Synchronization Modes

Register: DCONTROL	Free Run Mode	Frame Sync Mode	Line Sync Mode	Clock Sync Mode
D_LINESYNC_EN	1	0	1	0
D_FRAMELOCK_EN	1	1	0	0

5.4.4.1. Free-Run Mode

This mode is used in systems that can synchronize the source data with free-running display timing. Such systems typically have an external frame buffer containing source data, and can provide data to the selected input port as requested by the $\overline{\text{VCLREQ}}$ and $\overline{\text{VCBLNK}}$ signals.

5.4.4.1.1. Synchronization & Latency

In this mode there is no display start-up synchronization performed by the gmZ1 device. The display timing begins when the DCONTROL: DTG_RUN_EN control bit is set. The external system must determine when to initialize to the start of a new frame. This can be accomplished by monitoring the gmZ1 Display Port DVS (Display VSYNC) or the $\overline{\text{OVSYNC}}$ (Overlay VSYNC) outputs. The external system must provide input data to the gmZ1 as requested by $\overline{\text{VCLREQ}}$ and $\overline{\text{VCBLNK}}$ at sufficient rates to sustain the zoomed video display output.

The $\overline{\text{DFSYNC}}$ input pin and the programmable LOCK_EVENT are ignored, so there is no mechanism within the gmZ1 for synchronizing the DTG (Display Timing Generator) with the input source video.

Any loss of synchronization between the input pixel/line rate and the display zoomed line rate will result in variations between the input active frame period and the display active frame period. This can cause the on-chip zoom buffer to over or under flow.

5.4.4.2. Frame Sync Mode

This mode is used when the system can generate a display pixel clock that is synchronized to the input pixel clock, thereby allowing the display line rate to be synchronized with the input line rate.

Internally the rate that input lines are absorbed for zoom processing, closely matches the input line rate.

The display pixel clock must be generated through an external PLL and the input pixel clock must be an integer multiple of the input line rate (i.e. line-locked).

This mode can also be used with system containing an external Frame Buffer. In this case, the Frame Buffer supplies input lines are requested through the $\overline{\text{VCLREQ}}$ and $\overline{\text{VCBLNK}}$ signals.

The display frame rate is forced to match the input frame rate by means of LOCK_EVENT synchronization. (For interlaced video, the output frame rate matches the input frame rate.)

5.4.4.2.1. Synchronization & Latency

Display start-up synchronization occurs whenever the DCONTROL: DTG_RUN_EN control bit is set, i.e. transitions from a '0' to a '1'. This forces the DTG to wait until either a programmable LOCK_EVENT is detected in the selected input video source timing or the $\overline{\text{DFSYNC}}$ pin is asserted. Either of these events causes the DTG to immediately transition to the display timing state selected by the DH_LOCK_LD and DV_LOCK_LD register values.

The display output line rate is determined from the selected external display reference clock (normally DREFCLK2). If the input data is not provided from an external frame buffer then the display reference clock must track variations in the selected input video pixel clock. The DTG is then also be programmed so that the display output frame is equal to the input video frame period.

Whenever a subsequent LOCK_EVENT occurs in the input video timing sequence or a $\overline{\text{DFSYNC}}$ is detected then the DTG re-synchronizes to the input video frame rate, a transition to the display timing state as selected by the DH_LOCK_LD and DV_LOCK_LD register values.

5.4.4.2.2. Recommended Programming

I. Non-Interlaced Frame Sync

During non-interlaced input video the display output frames are locked with the display input frames.

DH_LOCK_LD	= DH_TOTAL/2
DH_TOTAL	= Correct line period
DV_LOCK_LD	= DV_TOTAL
DV_TOTAL	= A value much greater than the nominal number of lines per frame

II. Interlaced Frame Sync

During interlaced input video the ODD input field forces a LOCK_EVENT to display timing. Display timing must free run through the EVEN field.

DH_LOCK_LD	= DH_TOTAL/2
DH_TOTAL	= Nominal line period
DV_LOCK_LD	= DV_TOTAL
DV_TOTAL	= Number of line per frame

5.4.4.3. Line Sync Mode

This mode allows the use of a free running display reference clock.

5.4.4.3.1. Synchronization & Latency

Display start-up synchronization is identical to "FRAME_SYNC MODE" start up.

Once start-up synchronization has occurred, the DTG always re-synchronizes to the input video frame rate, whenever a Programmable LOCK_EVENT occurs in the input video timing sequence or a falling edge on the $\overline{\text{DFSYNC}}$ input pin is detected. This forces a transition to the display timing state as selected by the DH_LOCK_LD and DV_LOCK_LD register values.

Note that this mode requires that the selected input pixel clock be an integer multiple of the input line rate (i.e. line locked).

The display output line rate is synthesized from the selected input video line rate using "seed" parameters from the DH_RATE_hi, DH_RATE_mid and DH_RATE_lo register values. When using Line Sync Mode the display horizontal total is programmed to be longer than the worst case display line length so that the line is always terminated by the line rate synthesizer and not the regular display horizontal pixel counter.

5.4.4.3.2. Recommended Programming

I. Non-Interlaced Line Sync Mode

DH_LOCK_LD	= DH_TOTAL - 1
DH_TOTAL	= A value much larger than the nominal line period
DV_LOCK_LD	= DV_TOTAL
DV_TOTAL	= A value much larger than the nominal number of lines per display frame

II. Interlaced Line Sync

DH_LOCK_LD	= DH_TOTAL - 1
DH_TOTAL	= A value much larger than the nominal
DV_LOCK_LD	= DV_TOTAL
DV_TOTAL	= Nominal number of lines per frame

5.4.4.4. Clock Sync Mode

5.4.4.4.1. Synchronization & Latency

Display start-up synchronization is identical to Frame Sync Mode start up.

The DTG is free running in this mode. After the initial start-up frame synchronization from the start event (Programmable LOCK_EVENT or $\overline{\text{DFSYNC}}$ input) the external display clock source (normally DREFCLK2) must track the input source video pixel clock or line rate. This maintains frame lock between the input and output video timing. The DTG must also be programmed with appropriate register values so the input and output frame rates match. Any loss of lock between the input pixel/line rate and the display clock source will result in variations between the input active frame period and the display active frame period. This can cause the on-chip zoom buffer to over or under flow.

The Programmable LOCK_EVENT has no effect once the DTG is started and free-running; however, the $\overline{\text{DFSYNC}}$ input pin can still be used to force the DTG to change to the display timing state as selected by the DH_LOCK_LD and DV_LOCK_LD register values.

5.4.5. Output Display Timing Exception Handling

Display timing exceptions occur when a zoom buffer error occurs (overflow/underflow) or the DLOCK input signal is de-asserted, indicating the external system has detected a loss of lock in the DREFCLK2 reference clock input.

5.4.5.1. Zoom Buffer Overflow or Underflow

When a zoom buffer overflow or underflow occurs (regardless of the display synchronization mode) the output data is forced to the background color programmed in the DCONTROL: BKGNDCOL[2:0] control bits. The background color is produced for the remainder of the display frame. The DTG will continue to run and the overlay port retains functionality. At the start of the next frame the display output will again operate normally (assuming another exception condition does not occur during that frame).

5.4.5.2. DLOCK - loss of pixel clock lock

DLOCK conditions only occur when the Display Port pixel clock source is programmed for DREFCLK2. DREFCLK2 is intended for use as a PLL generated clock that is provided by the system. For PLL circuits that can generate clock frequencies outside the valid gmZ1 operating range, the system can drive the gmZ1 DLOCK input to a logic '0' to indicate out of lock conditions.

When gmZ1 detects a de-asserted DLOCK signal, an asynchronous reset of the DCONTROL register will occur, clearing the register's control bits to '0'. Since DTG_RUN_EN and DOUT_RUN_EN are cleared to '0', the DTG halts, the overlay port halts, and the output display interface data and control signals are clamped to GND.

The external host controller must intervene to restart the DTG and enable the display data and control outputs to drive the display interface with display data and timing information.

5.4.6. Display Active Window Control

The complete display window is shown in Figure 26.

Horizontal Period

The display horizontal line period is programmable. Each display line is initiated with a DHS synchronization pulse. The DH_RATE and DH_TOTAL registers determine the display line period for Line Sync Mode. During Frame Sync, Free Run, or Clock Sync Modes the DH_TOTAL register determines the horizontal line period.

HSYNC Width

The DHS (Display Horizontal Sync) pulse width is programmable using the DH_HS_END register. The contents of this register multiplied by four determines the number of DCLK cycles that DHS will be asserted, i.e. for a clock pulse of 136 DCLK cycles, set to 22h.

Horizontal Background

The horizontal background region determines the region that is framed by the Display Port DEN output signal.

The DH_BKGND_START register must contain the number of DCLK cycles from (and including) the start of DHS for a display line to (and including) the location of the first horizontal background pixel. The number of DCLK cycles from (and including) the start of DHS to (and including) the location of the last horizontal background pixel (before blanking) is determined by the value in the DH_BKGND_END register.

Horizontal Active

The horizontal active region determines the active window during which the image is displayed. The display active window is programmable to be the same size or smaller than the horizontal background region.

The number of DCLK cycles from (and including) the start of DHS for a display line to (and including) the location of the first active pixel is determined by the DH_ACTIV_START register. The DH_ACTIV_WIDTH register must contain the number of DCLK cycles for the active portion of a display line.

Horizontal Blanking

The horizontal blanking region is defined as all portions of the display line not part of the Horizontal Background or Horizontal Active Window regions. The HSYNC period is always blanked.

Vertical Period

The display vertical frame period is programmable via the DV_TOTAL register which must contain the total number of display lines (blank + active or background lines) occurring during one display frame.

VSYNC Width

The display vertical sync pulse width is programmable using the DV_VS_END register which determines the number of blank lines that occur during the DVS pulse. This register supports a DVS pulse for 1 to 15 lines in width.

Vertical Background

The vertical background region determines the number of displayed lines that are framed by the Display Port DEN signal.

The DV_BKGND_START register must contain the number of lines from (and including) the start of DVS to (and including) the location of the first background line. The number of lines from (and including) the start of DVS to (and including) the location of the last background line (before vertical blanking) is determined by the value in the DV_BKGND_END register.

Vertical Active

The vertical active region determines the active window during which the scaled image is displayed. The display active window is programmable to be the same size or smaller than the vertical background region.

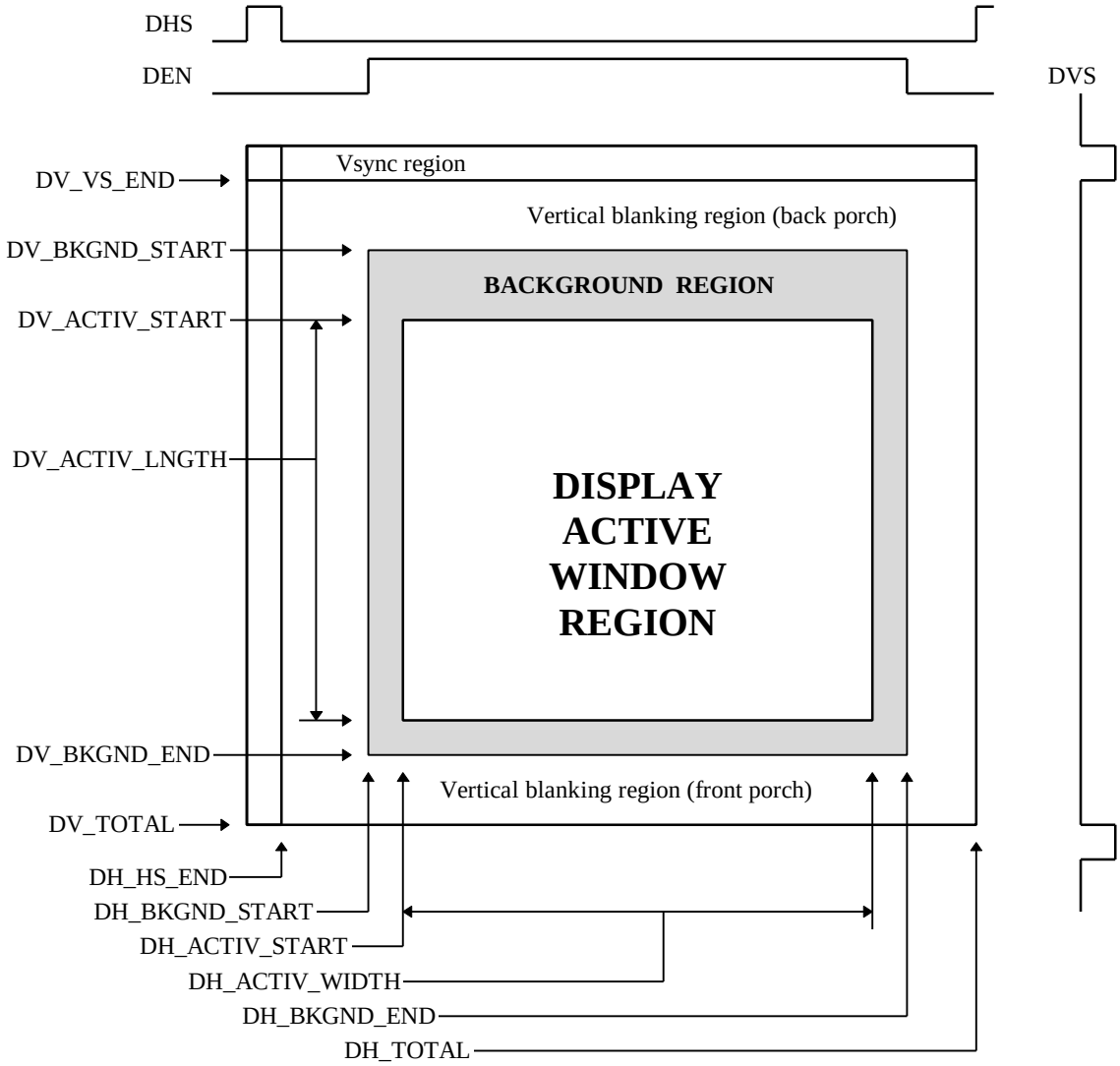
The number of lines from (and including) the start of DVS, to (and including) the location of the first active line is determined by the value written to the DV_ACTIV_START register.

The DV_ACTIV_LNGTH register must contain the number of lines for the active portion of the frame.

Vertical Blanking

The vertical blanking region is defined as all portions of the display frame not part of the Vertical Background or Vertical Active Window regions. The VSYNC period is always blanked.

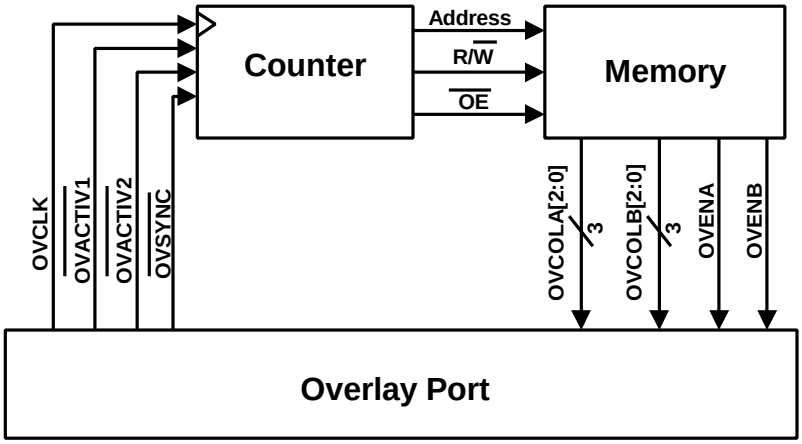
Figure 26: Display Timing Diagram



5.5.Overlay Port

The gmZ1 Overlay Port allows the integration of overlay data with the scaled output pixel stream. The Overlay Port provides a two pixel wide interface for overlay data regardless of the display output configuration (single/double width). This port provides two independently programmable overlay windows that can be positioned within the display active or background regions.

Figure 27: Example of Overlay Implementation



5.5.1. Input Signals

The Overlay Port accepts data for the two programmable overlays (Overlay Active Regions #1 and #2). Each pixel in both overlays is controlled by OVCOLX[2:0] (Overlay Color) and OVENX (Overlay Enable) input signals. Together, these signals produce a 4-bit word to indicate control information for one overlay pixel.

The Overlay Port displays pixels in pairs, “A and B”. The two control words “A and B” are sent to the overlay port at half the display rate so the external overlay circuitry can operate at the slower rate. Since two control words are loaded with each OVCLK, the input rate can control overlay at the full pixel resolution. The “A” control word (signals OVCOLA[2:0] and OVENA) refers to the “left displayed pixel of each overlay pixel pair”. Similarly, the “B” control word (signals OVCOLB[2:0] and OVENB) refers to the “right displayed pixel of each overlay pixel pair”.

OVCOLA[2:0] and OVCOLB[2:0] each select one of 8 colors from the overlay color palette registers, see Table 5.

Table 5: Overlay Color Controls

OVCOL[2:0]	Color Description	Output Red Value DRED[7:0]	Output Green Value DGRN[7:0]	Output Blue Value DBLU[7:0]
000	Black	0	0	0
001	Blue	0	0	OVLY_BLU register contents
010	Green	0	OVLY_GRN register contents	0
011	Cyan	0	OVLY_GRN register contents	OVLY_BLU register contents
100	Red	OVLY_RED register contents	0	0
101	Magenta	OVLY_RED register contents	0	OVLY_BLU register contents
110	Yellow	OVLY_RED register contents	OVLY_GRN register contents	0
111	White	FFh	FFh	FFh

OVENA and OVENB enable the overlay on a pixel by pixel basis within the regions indicated by $\overline{\text{OVACTIV1}}$ or $\overline{\text{OVACTIV2}}$. When OVENA/B is de-asserted (logic low), the overlay is transparent and the scaler output is displayed without any overlay. When OVENA/B is asserted (logic high), the overlay is enabled and the selected overlay color pixel is displayed in place of the scaled output.

Overlay regions #1 and #2 may be allowed to overlap. However, since both regions share the same overlay input port, the external system must determine priority and supply the correct overlay information.

The Overlay Active Window Control provides a means for programming the active window region for the overlay image #1 and overlay image #2. The display timing generator provides programmable outputs ($\overline{\text{OVACTIV1}}$, $\overline{\text{OVACTIV2}}$) to define the start to stop pixel locations on active overlay lines for external overlay control word generation.

Figure 28: Overlay Port - Start of Active Overlay Line

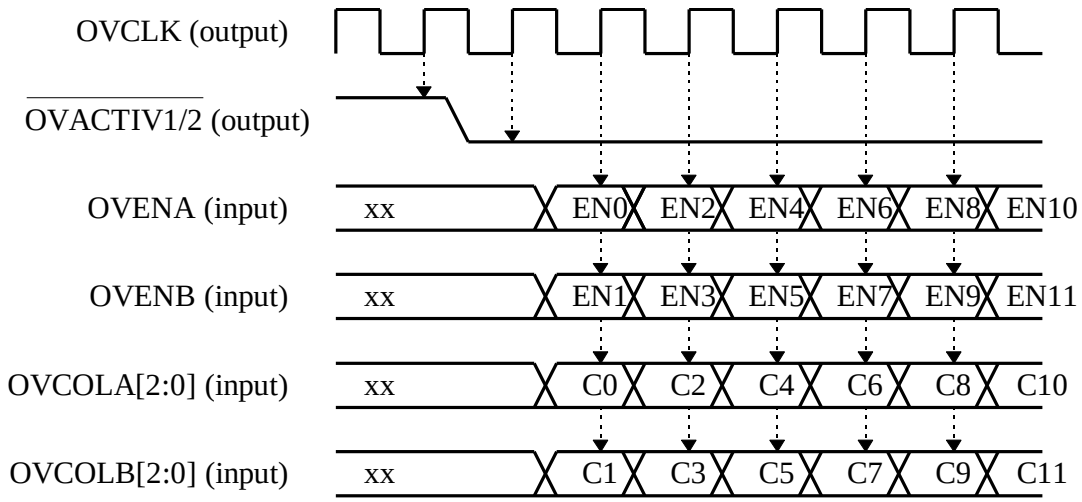


Figure 29: Overlay Port - End of Active Overlay Line

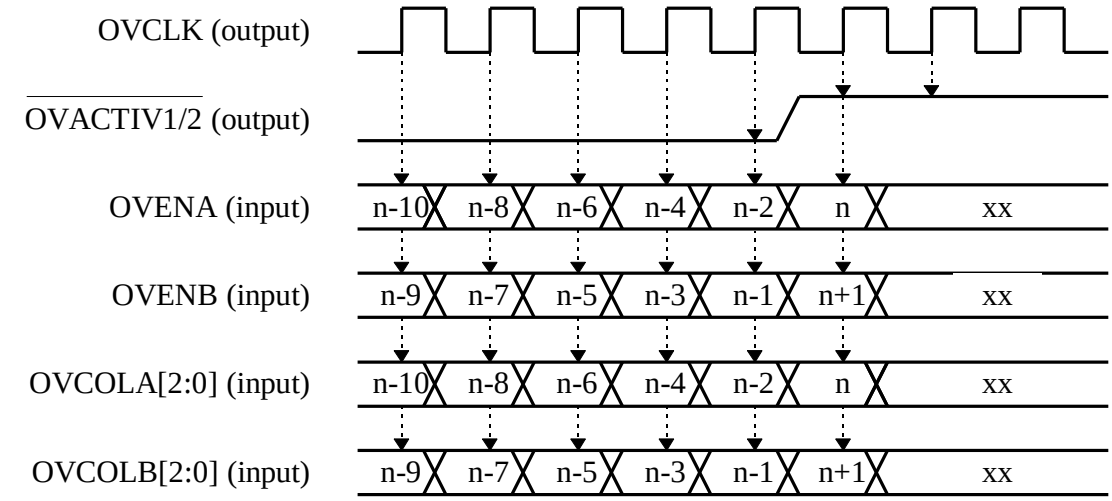
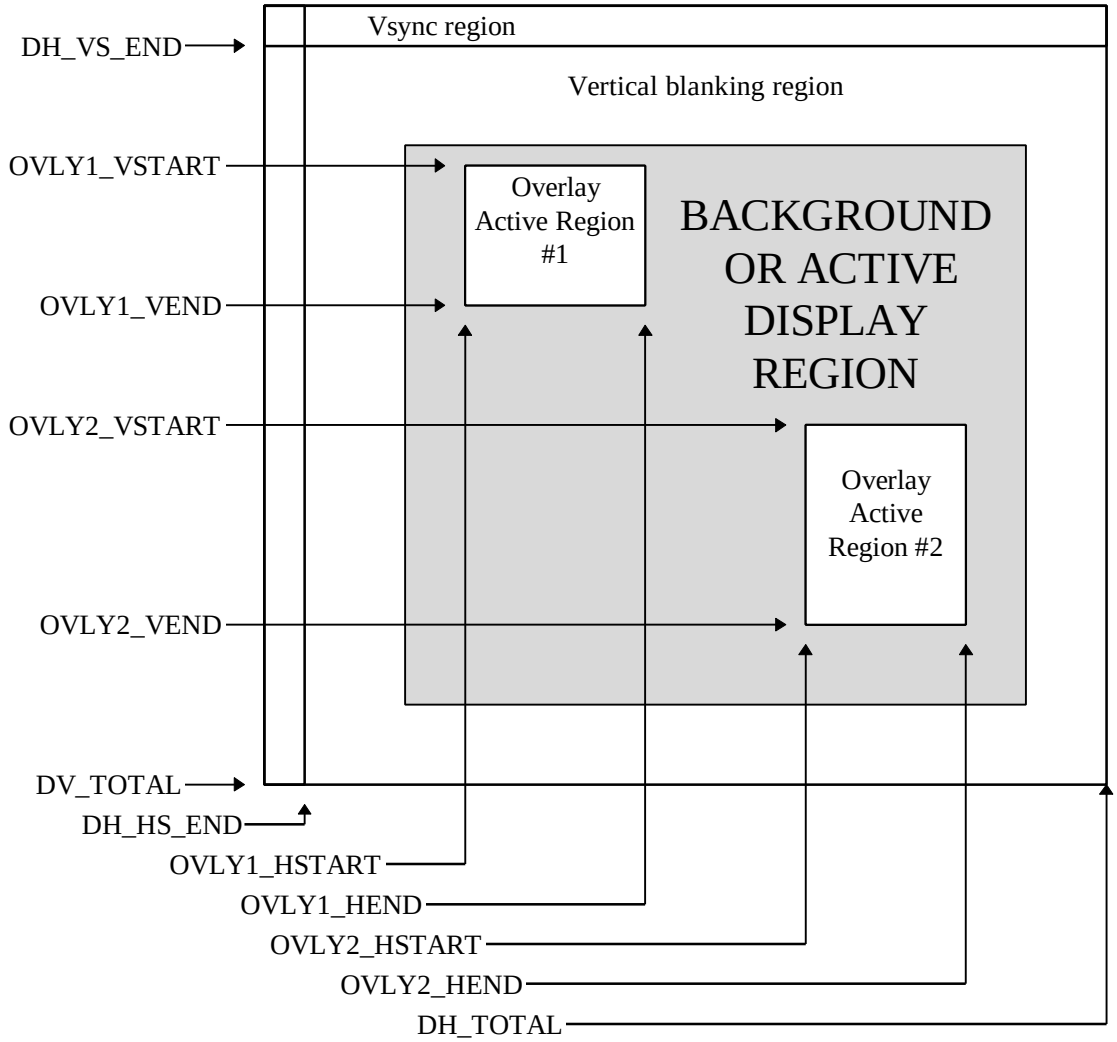


Figure 30: Overlay Active Region Programming



5.5.2. Output Control Signals

The overlay port supports the following four output signals: OVCLK, $\overline{\text{OVACTIV1}}$, $\overline{\text{OVSYNC}}$, and $\overline{\text{OVACTIV2}}$.

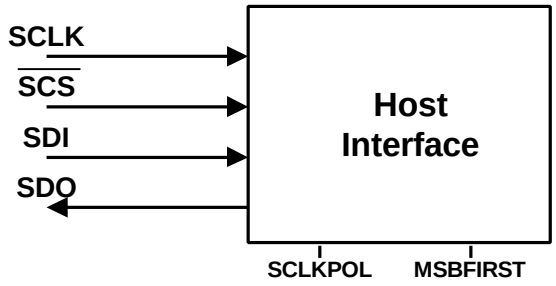
$\overline{\text{OVSYNC}}$ is an active low version of the display VSYNC output (DVS). This signal provides vertical synchronization to initialize any external overlay circuitry at the start of a display frame.

$\overline{\text{OVACTIV1}}$ indicates the active region of a display line for the Overlay #1 image. The external overlay generation circuit provides valid overlay control words synchronous to OVCLK whenever $\overline{\text{OVACTIV1}}$ is detected. When this signal is not asserted, the overlay control inputs have no effect, and the overlay is disabled. $\overline{\text{OVACTIV1}}$ is asserted during the portion of each line that falls within the display region defined by Overlay#1.

$\overline{\text{OVACTIV2}}$ indicates the active region of a display line for the Overlay #2 image. The external overlay generation circuit provides overlay control words whenever $\overline{\text{OVACTIV2}}$ is detected. When de-asserted, the overlay control word inputs have no effect and the overlay is disabled. $\overline{\text{OVACTIV2}}$ is asserted during the portion of each line that falls within the display region defined by Overlay#2.

5.6.Host Interface Port

Figure 31: Host Interface Port



The Host Interface (Host I/F) provides serial access to the gmZ1's control and status registers. The three input signals (SCLK, SDI, and $\overline{SCS}$) and one output signal (SDO) form a four-wire interface that can be controlled by any external microcontroller. Alternatively, SDO may be shorted with SDI to form a three-wire interface. The MSBIRST and SCLKPOL provide static mode control to interface with a wide variety of microcontrollers.

5.6.1. Host Interface Protocol

The Host I/F is enabled by asserting $\overline{SCS}$ (Serial Chip Select). The first transfer to take place following the falling edge of $\overline{SCS}$ should always be an Address Transfer to set internal addressing parameters governing the Host I/F. Any attempted data transfers prior to the detection of the first address transfer would be ignored by gmZ1. Once the initial address transfer has occurred, any number of subsequent data or address transfers can occur during the $\overline{SCS}$ low period. All address and data transfers are 16 SCLK cycles in length. A rising edge on the $\overline{SCS}$ signal (STOP condition) terminates any transfers immediately and disables the gmZ1 Host I/F.

When the Host I/F is not in use ($\overline{SCS}$ is de-asserted), the Serial Data Output (SDO) signal is always driven high in 4-wire mode and passive high in 3-wire mode. Upon $\overline{SCS}$ assertion (transition from logic '1' to logic '0'), the value at the output of SDO is initially "reserved" and will remain this way until bit position two is driven out. This "reserved state" should be treated as a "don't care" by the user and bit position two is always a '1' on SDO as defined in the Host Protocol.

Data is clocked out on SDO on active SCLK edges, based on the value at pin SCLKPOL.

If SCLKPOL = 1 then SDO is clocked out on SCLK rising edge.

If SCLKPOL = 0 then SDO is clocked out on SCLK falling edge.

The Serial Data Input (SDI) should be driven by the external host controller synchronous to SCLK. The SCLK edge (rising or falling) used by the gmZ1 to sample the SDI input is selected with the SCLKPOL pin.

If SCLKPOL = '0' then the rising edge of SCLK is used by the gmZ1 to sample the SDI input.

If SCLKPOL = '1' then the falling edge of SCLK is used by the gmZ1 to sample the SDI input.

The Bit Order (MSBFIRST) pin configures the gmZ1 to accept serial address and data bit fields in the order of MSB-to-LSB (MSBFIRST = 1) or LSB-to-MSB (MSBFIRST = 0).

As noted, the protocol defines the first bit position within the 16 clock cycles of each address or data transfer cycle as a "reserved" bit position on SDO. Therefore the user should treat the first bit as a "don't care". The following three bit positions on SDI are reserved for ARB (Address Read Back), Data/Address and Read/Write indication from the external controller. The gmZ1 leaves these three bit positions passive high on SDO in all cases. Address and data information should be placed on the last 9 or 12 bit positions respectively, depending on the type of transfer.

The Serial Data Output (SDO) is driven by the gmZ1 Host I/F. The SDO output is programmable to operate with two sets of logic levels as follows:

Table 6: Host I/F SDO Mode

Mode	How to enable:	Logic '1' Output	Logic '0' Output
Open Drain Mode (used for 3 wire mode)	Open Drain mode is the default after a reset.	HiZ	GND
Totem Pole Mode (used for 4-wire mode)	Enabled by setting the HI4WIRE_EN in the HOSTCTRL register.	3 V	GND

There are four types of transfer cycles supported; Address Transfer, Address Read-Back Transfer, Write Data Transfer, and Read Data Transfer. Each individual bus transfer consists of 16 SCLK periods with address, data, or control information transferred to/from the gmZ1 Host I/F with each SCLK active edge.

Table 7: Summary of the 3-Wire Host I/F Transfer Modes

Transfer Bits	Host I/F Transfer Modes			
	Address Write	**Address Read-Back**	**Data Write**	**Data Read**
1	Reserved	Reserved	Reserved	Reserved
2	$\overline{ARB}$='1'	$\overline{ARB}$ = '0'	$\overline{ARB}$ = '1'	$\overline{ARB}$ = '1'
3	D/A = '0'	'X'	D/A = '1'	D/A = '1'
4	R/W	'X'	'1'	'1'
5	'1'	'1'	D11	D11[1]
6	'1'	'1'	D10	D10[1]
7	'1'	'1'	D9	D9[1]
8	AUTOINC	AUTOINC[1]	D8	D8[1]
9	A7	A7[1]	D7	D7[1]
10	A6	A6[1]	D6	D6[1]
11	A5	A5[1]	D5	D5[1]
12	A4	A4[1]	D4	D4[1]
13	A3	A3[1]	D3	D3[1]
14	A2	A2[1]	D2	D2[1]
15	A1	A1[1]	D1	D1[1]
16	A0	A0[1]	D0	D0[1]

Note: 1. Address or Data information is driven by the gmZ1 onto the common SDI/SDO data line. The external host driver should be passive high at this point.

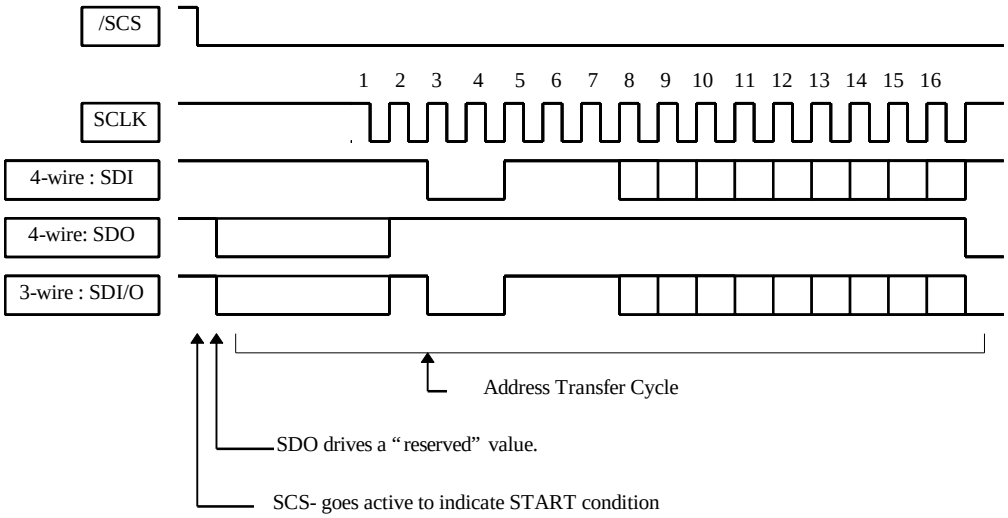
2. This table assumes SCLKPOL = '1' and MSBFIRST = '1'.

Table 8: Summary of the 4-Wire Host I/F Transfer Modes

Transfer Bits	Host I/F Transfer Modes							
	Address Write		Address Readback		Data Write		Data Read	
	SDI	SDO	SDI	SDO	SDI	SDO	SDI	SDO
1	'1'	Reserved	'1'	Reserved	'1'	Reserved	'1'	Reserved
2	$\overline{ARB}$ ='1'	'1'	$\overline{ARB}$ = '0'	'1'	$\overline{ARB}$ = '1'	'1'	$\overline{ARB}$ = '1'	'1'
3	D/A = '0'	'1'	'1'	'1'	D/A = '1'	'1'	D/A = '1'	'1'
4	R/W	'1'	'1'	'1'	'1'	'1'	'1'	'1'
5	'1'	'1'	'1'	'1'	D11	'1'	'1'	D11
6	'1'	'1'	'1'	'1'	D10	'1'	'1'	D10
7	'1'	'1'	'1'	'1'	D9	'1'	'1'	D9
8	AUTOINC	'1'	'1'	AUTOINC	D8	'1'	'1'	D8
9	A7	'1'	'1'	A7	D7	'1'	'1'	D7
10	A6	'1'	'1'	A6	D6	'1'	'1'	D6
11	A5	'1'	'1'	A5	D5	'1'	'1'	D5
12	A4	'1'	'1'	A4	D4	'1'	'1'	D4
13	A3	'1'	'1'	A3	D3	'1'	'1'	D3
14	A2	'1'	'1'	A2	D2	'1'	'1'	D2
15	A1	'1'	'1'	A1	D1	'1'	'1'	D1
16	A0	'1'	'1'	A0	D0	'1'	'1'	D0

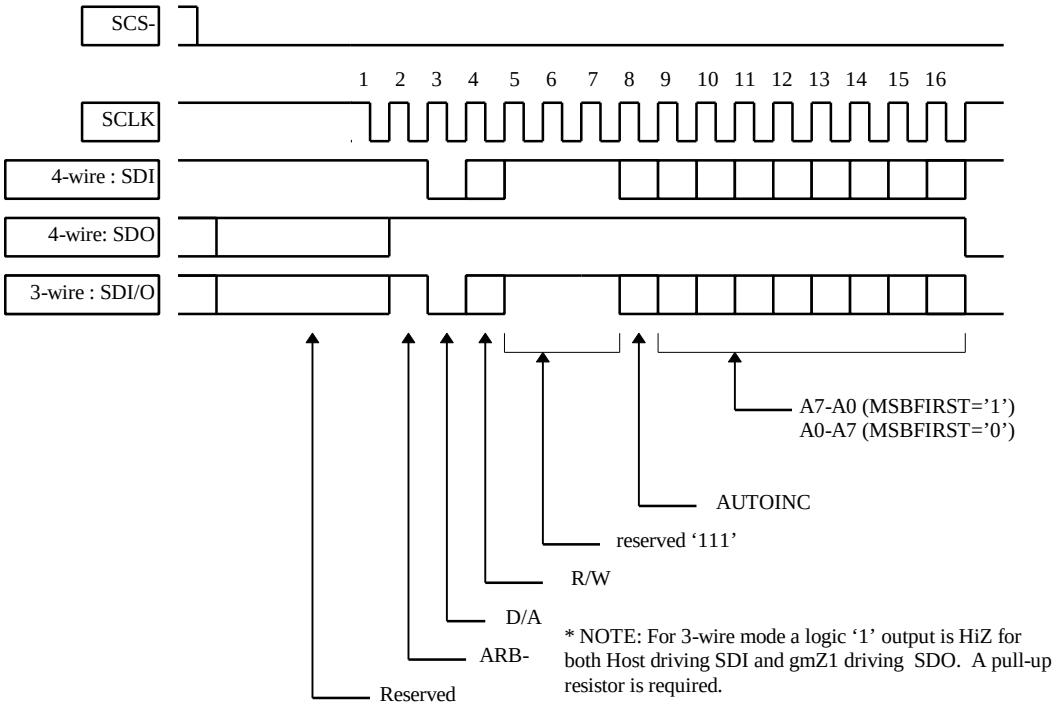
Note: 1. This table assumes SCLKPOL = '1' and MSBFIRST = '1'.

Figure 32: Host I/F START Condition (followed by Address cycle)



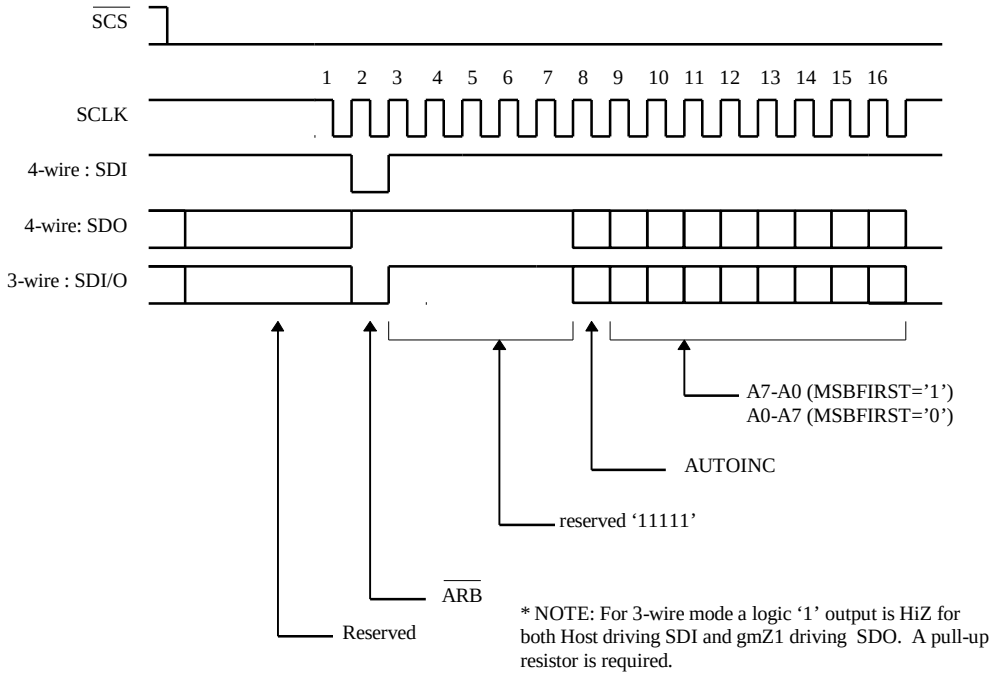
- This diagram assumes SCLKPOL = '1'.
- In 4-wire mode SDO is driven high even when /SCS is de-asserted

Figure 33: Host I/F Address Transfer



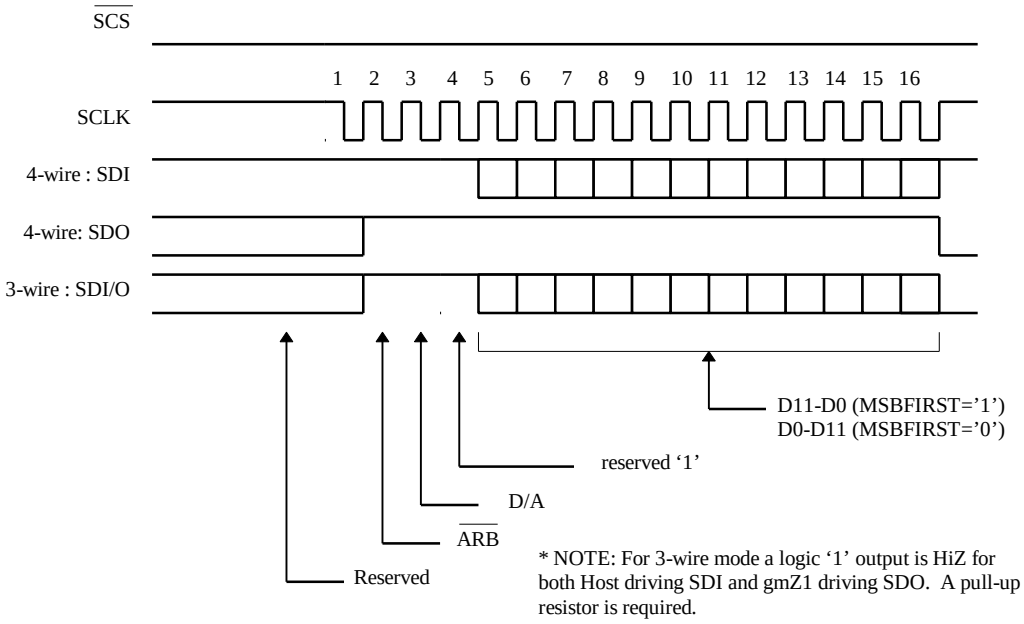
* This diagram assumes SCLKPOL = '1'.

Figure 34: Host I/F Address Read Back (ARB) Transfer



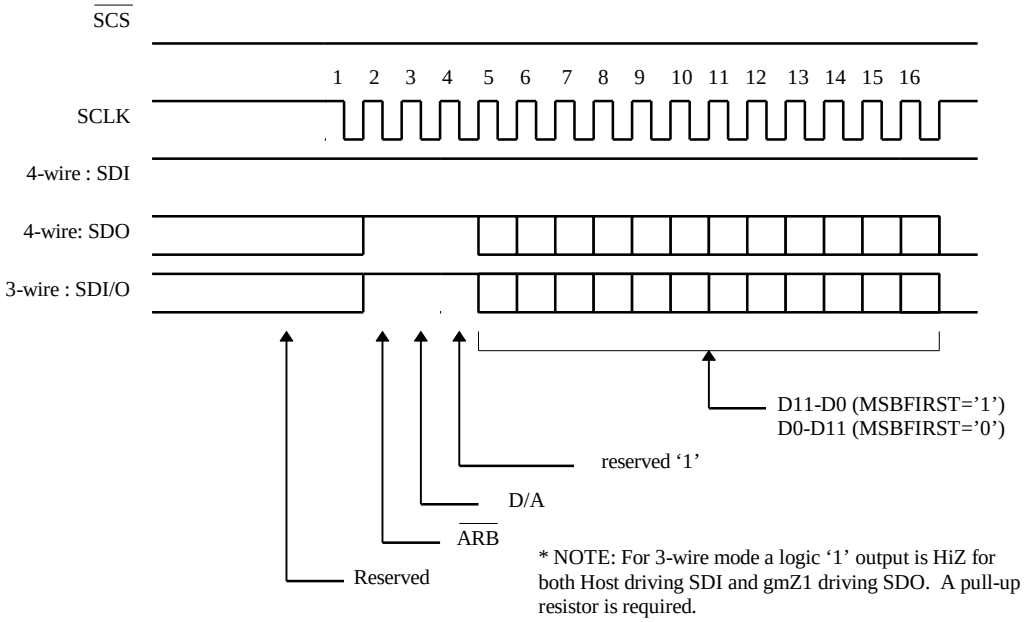
* This diagram assumes SCLKPOL = '1'.

Figure 35: Host I/F Write Data Transfer



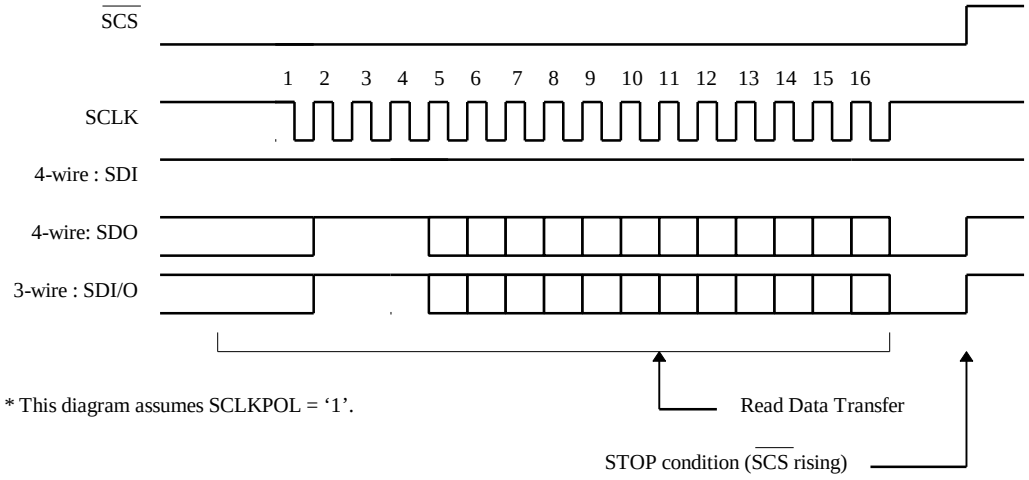
* This diagram assumes SCLKPOL = '1'.

Figure 36: Host I/F Read Data Transfer



* This diagram assumes SCLKPOL = '1'.

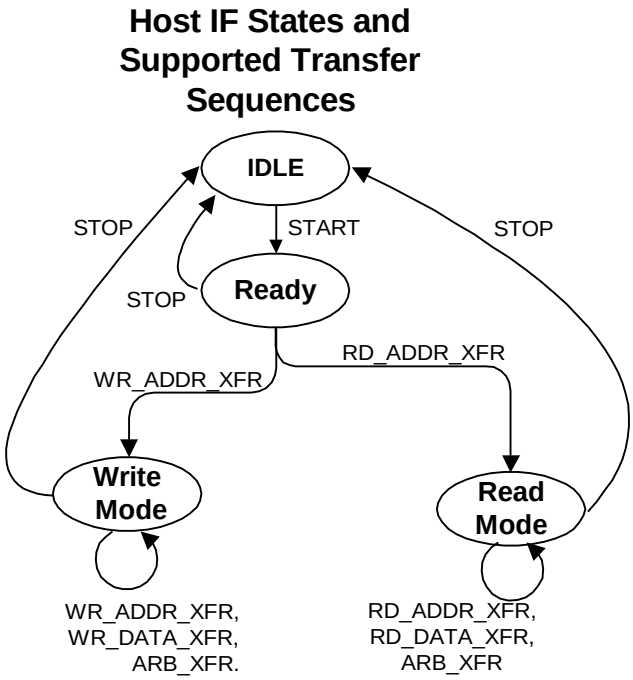
Figure 37: Host I/F Stop Condition (after a Read Data Transfer)



5.6.2. Host Interface State Description

The Host Interface is governed by a 4-state finite state machine. See Figure 38.

Figure 38: Host Interface Operating States and Transfers



5.6.2.1. Idle State

The Host I/F enters the IDLE state after a power-up reset or after the detection of a STOP. Note that the STOP condition always causes a transition to the IDLE state from any other state. From the IDLE state, the Host I/F reverts to the Ready state upon reception of the START condition.

5.6.2.2. Ready State

The Host I/F changes from the IDLE state to the READY state upon reception of the START condition. In the READY state, the Host I/F supports Address Transfers (write or read) only.

Address Transfers with the R/W bit set to logic '1' cause the Host I/F to store the new address and auto increment information, and then change to the READ MODE state.

Address Transfers with the R/W bit set to logic '0' cause the Host I/F to store the new address and auto increment information, and then change to WRITE MODE state.

5.6.2.3. Write Mode State

The Host I/F enters the WRITE MODE state from the READY state when an Address transfer occurs with the R/W bit reset to '0'.

While in the WRITE MODE state the following transfers are supported:

Write Address Transfers, Write Data Transfers, Address Read-Back Transfers.

The Host I/F can only leave this state when a STOP condition occurs.

5.6.2.4. Read Mode State

The Host I/F enters the READ MODE state from the READY state when an Address transfer occurs with the R/W bit reset to '1'.

While in the READ MODE state the following transfers are supported:

Read Address Transfers, Read Data Transfers, Address Read-Back Transfers.

The Host I/F can only leave this state when a STOP condition occurs.

5.6.3. Typical Usage Scenarios

The address and data transfer cycles can then be grouped within one $\overline{SCS}$ active low period to perform different types of Bus Cycles. Typically, most applications would group them to form the following four types of Bus Cycles: Single Write, Single Read, Burst Write, Burst Read

Single read and single write cycles are composed of two 16-clock transfers; Burst cycles involve three or more. The first transfer (address) provides gmZ1 addressing information and the second (and subsequent) transfer involves data transfer.

5.6.3.1. Single Write Transfers

Single Write Transfers can be accomplished by performing the following sequence of events:

1) Force a "START" condition by driving $\overline{SCS}$ low.
2) Execute an ADDRESS TRANSFER to set the register address with the R/W bit reset to '0'.
3) Execute a WRITE DATA TRANSFER to transfer the data to the selected address.
4) Force a "STOP" condition by driving $\overline{SCS}$ high.

5.6.3.2. Burst Write Transfers with Address Auto-increment

Burst Write Transfers can be accomplished by performing the following sequence of events:

1) Force a "START" condition by driving $\overline{SCS}$ low.
2) Execute an ADDRESS TRANSFER (with R/W = '0' and AUTOINC ='1') to set the register address with auto-increment on.
3) Execute a WRITE DATA TRANSFER to transfer the data to the first selected address. (Note that the address will auto increment after the first data transfer is written.)
4) Execute subsequent WRITE DATA TRANSFER cycles to transfer data to the sequentially addressed registers. There is no limit to the number of data transfers that can occur during a burst as long as the addresses remain valid.
5) Force a "STOP" condition by driving $\overline{SCS}$ high.

5.6.3.3. Single Read Transfers

Single Read Transfers can be accomplished by performing the following sequence of events:

1) Force a "START" condition by driving $\overline{SCS}$ low.
2) Execute an ADDRESS TRANSFER with R/W bit = '1' to set the register address.
3) Execute a READ DATA TRANSFER to transfer the data from the selected address to the Host Controller.
4) Force a "STOP" condition by driving $\overline{SCS}$ high.

5.6.3.4. Burst Read Transfers

Burst Read Transfers can be accomplished by performing the following sequence of events:

1) Force a "START" condition by driving $\overline{SCS}$ low.
2) Execute an ADDRESS WRITE TRANSFER (with R/W = '1' and AUTOINC = '1') to set the register address with auto-increment on.
3) Execute a READ DATA TRANSFER to transfer the data to the first selected address. (Note that the address will auto increment after the first data transfer is written.)
4) Execute subsequent READ DATA TRANSFER cycles to transfer data from the sequentially addressed registers to the Host Controller. There is no limit to the number of data transfers that can occur during a burst as long as the addresses remain valid.
5) Force a "STOP" condition by driving $\overline{SCS}$ high.

5.6.3.5. Performing Polling Transfers

Polling operations can be performed without the need for multiple address transfers on the bus as follows:

1) Force a "START" condition by driving $\overline{SCS}$ low.
2) Execute an ADDRESS TRANSFER (with R/W bit = '1' and AUTOINC = '0') to set the register address to an appropriate STATUS register.
3) Execute a READ DATA TRANSFER to transfer the data from the selected address to the Host Controller. Repeat the READ DATA TRANSFER as many times as necessary until the event being polled for occurs.
4) Force a "STOP" condition by driving $\overline{SCS}$ high.

5.6.4. Interrupts

The gmZ1 has two interrupt output signals ($\overline{\text{IRQ1}}$ and $\overline{\text{IRQ2}}$) which can be programmed to provide device status or video timing interrupts to the system. The interrupt is programmable via the Host Interface register set. Each interrupt is independently programmable to select from a number of interrupt sources such as video timing events, zoom buffer status (overflow, underflow), or external display phase lock loop status.

The interrupts support “latched” and “asynchronous flow through” modes. When the interrupt occurs in “latched mode”, the interrupt generation circuitry detects the event and drives the interrupt output to the active state continuously until the external Host Controller reads the gmZ1 Status Register to acknowledge interrupt service.

In the “asynchronous flow through mode” the selected internal interrupt drives the output pin directly. If the event is “TRUE” then the interrupt is driven active. If the event becomes “FALSE”, the interrupt returns to “NOT active”. The “asynchronous flow through mode” is useful during system debug for monitoring internal video or zoom buffer events without the need to clear them each time.

The Interrupt output pins are driven by gmZ1 using open drain logic, i.e. logic ‘1’ output is high impedance, and a logic ‘0’ is driven to GND. Therefore the system must provide an external pull-up resistor (~10kΩ) to detect the logic ‘1’ state and the interrupt outputs can be utilized in an “ACTIVE LOW WIRED OR” configuration with other device interrupts in a system.

5.6.5. Updating Register Contents

Write operations to the Host Interface register set do not have an immediate effect on the gmZ1 operating parameters. The only register that causes an immediate change to the gmZ1 operating configuration is the HOSTCTRL register.

Other registers written by the Host Interface have the data stored in an intermediate bank of latches called the “Pending Register Set”. When the Host Interface performs a read cycle the “Pending Register Set” provides the resultant data. All register updates affect the gmZ1 operating configuration only when the “Pending Register Set” contents are transferred (updated) to the “Active Register Set”.

5.6.5.1. Forcing An Immediate Update

Forced Updates: An immediate update can be achieved by setting the FORC_UPDATE control bit in the HOSTCTRL register. This method is used during device initialization when coming out of a power on or soft reset state and when video timing is not present. Note that for an update to

occur, the selected input clock (VGACLK or VGBCLK) and the selected output clock (DREFCLK1 or DREFCLK2) must be present and toggling.

5.6.5.2. Video Timing Synchronized Updates

Video synchronized updates can be achieved by enabling the UPDATE_EN control bit in the HOSTCTRL register. This method is used for varying any video timing parameters, overlay positioning or state, scaling parameters, or other parameters while processing real-time video. The Host Controller can program new video timing and control parameters into the gmZ1 device while the gmZ1 is operating and processing video.

Since the new parameters are stored in the "Pending Register Set" there is no change to the gmZ1 operating conditions and the device operates normally. When the Host Controller has finished programming the new parameters, the UPDATE_EN control bit can be set.

On the next "LOCK_EVENT", the "Pending Register Set" contents are transferred to the "Active Register Set" synchronous to the video timing, and the new parameters take effect. This technique is useful for changing parameters while video timing is running, without the loss of display synchronization or visual artifacts appearing on the display output.

Note that the "LOCK_EVENT" occurs by programming an input "LOCK_EVENT" based on the selected input video timing or by asserting the $\overline{\text{DFSYNC}}$ input pin.

5.6.6. Host I/F Address Map/Control Bit Map.

Table 10 - Table 23 provide a detailed description of all the on chip registers accessible using the Host I/F. Register addresses are given in Hexadecimal, and any individual control bits are named. Bit '0' is always the LSB of the register.

Reset Conditions

Note: Except for the HOSTCTRL register, all host register contents default to '0' as the result of a soft or hard reset.

The HOSTCTRL register always clears to '0' during a hard reset, and is handled differently for a soft reset. Table 10 provides the soft-reset description.

MON_SEL[2:0]
In the following table, MON_SEL [2:0] selects the video timing event to be monitored as an interrupt source for the IRQ1CNTRL and IRQ2CNTRL registers.

Table 9: MON_SEL[2:0]

MON_SEL Value "binary"	Interrupt Monitor Source:	Description:
000	Disabled	- interrupt monitor source disabled, no interrupt source selected.
001	IP_VS	- interrupt generated on the selected edge of the selected (VGA/VGB) video input port VSYNC.
010	IPV_ACTIV	- interrupt generated on the selected edge of the input vertical active window (internal signal).
011	IP_LOCK_EVENT	- interrupt generated on when the input Lock Event occurs.
100	D_VS	- interrupt generated on the selected edge of display VSYNC.
101	DV_BKGND	- interrupt generated on the selected edge of the display vertical background (internal signal).
110	OVLY_A_VACTIV	- interrupt generated on the selected edge of the display overlay window "A" vertical active region (internal signal).
111	OVLY_B_VACTIV	- interrupt generated on the selected edge of the display overlay window "B" vertical active region (internal signal).

5.7. Host Interface Registers

The following is a summary of fifty programmable control and status registers within the Host Interface.
Host Interface Registers 02-31 are double buffered; write operations to the register set do not have an immediate effect on gmZ1 operating parameters. Setting the FORCE_UPDATE or UPDATE_EN bit in the HOSTCTRL Register enables a transfer of the "Pending Register Set" to the "Active Register Set". See Section 5.6.5 for details.

5.7.1. Host Interface and Main Control Register

This section provides the main control signals to the gmZ1, such as reset and the selection of VGA/VGB input.

Table 10: HOSTCTRL

Address (HEX)	Number of Bits	Mode	Name	Function
00	12	R	ID_REG	MSB 8 bits: 0000 0001 = product code and LSB 4 bits: 0001 = rev code.
01	bit[0]	R/W	SOFT_RESET	This control bit is used to force the gmZ1 device to a $\overline{\text{RESET}}$ condition, clearing all programmable registers to '0', with the exception of: H14WIRE_EN, IP_RGB_EN, IPCLK_INV, D_DREFCLK2_EN, D_BYPASS_EN, PWRDWN, and RGB_B_SEL. This bit will automatically self-clear upon execution of the soft reset. Note that a soft reset has no effect on the Host Interface Controller state machines. 0 = Normal operation. 1 = Forces a device reset. The Host Interface Controller state machines can be reset by driving the $\overline{\text{SCS}}$ input signal to a logic '1' level (high).
	bit[1]		H14WIRE_EN	Host Interface four wire mode enable. This control bit is not affected during a "soft reset". 0 = 3-wire mode. The Host Interface signal: SDO uses HiZ (high impedance) as the logic '1' output state. SDO can be connected to SDI externally for 3 wire operation when this bit is set to '0'. An external pull-up resistor is required for 3-wire mode operation. 1 = 4-wire mode. The SDO output signal outputs a driven 3V output level as the logic '1' output state. SDO cannot be externally connected to SDI for 3-wire operation when this bit is set to '1'. The HI4WIRE_EN control bit state is not affected during a "soft reset".
	bit[2]		UPDATE_EN	This control bit is used to enable a parameter update to the active register set. The parameter update occurs synchronized to the video timing sequence LOCK_EVENT. This parameter update method is intended for updates to video timing parameters while input and output video timing is running. 0 = Parameter update not enabled. 1 = Enable a parameter update when the next LOCK_EVENT occurs.

Address (HEX)	Number of Bits	Mode	Name	Function
				The UPDATE_EN control bit is cleared during a "soft reset" or after a successful video lock event synchronized transfer from the "pending" set to the "active" set of parameter registers.
	bit[3]		FORC_UPDATE	This control bit is used to force a parameter update to the active register set immediately; regardless of the state of the video timing sequence. Updates must be forced when initializing parameters after a reset or when no video source is present or video timing is not running. When coming out of reset or if no video source is present then the input LOCK_EVENT will not be functioning and therefore UPDATE_EN cannot be used for generating updates to the register set. 0 = Parameter update not forced. 1 = Force a parameter update immediately. The FORC_UPDATE control bit is cleared during a "soft reset" or after a successful FORCED UPDATE from the "pending" set to the "active" set of parameter registers.
	bit[4]		IP_RGB_EN	IP_RGB_EN selects between YUV or RGB input modes. 0 = YUV operation is enabled on the VGB port. 1= RGB operation is enabled. (The RGB_B_SEL control bit determines on which port the RGB input is enabled.) The IP_RGB_EN control bit state is not affected during a "soft reset". *Note: IP_RGB_EN affects which input clock is used and therefore any changes to the state of this bit must be followed by a "soft reset".
	bit[5]		IPCLK_INV	Input Video Clock Invert Enable: Controls polarity of selected input clock: VGBCLK or VGACLK 0 = normal clock input polarity. 1 = invert input clock. The IPCLK_INV control bit state is not affected during a "soft reset". Since changes to the state of this bit affect the input pixel clock, any changes must be followed by "soft reset".
	bit[6]		D_DREFCLK2_EN	Display video reference clock #2 enable. Selects between the two possible display clock sources: DREFCLK1 or DREFCLK2. 0 = DREFCLK1 is used as display pixel clock. 1 = DREFCLK2 is used as display pixel clock. WARNING: Switching between display clocks should only occur immediately after a device reset. The switch between clocks is not glitchless and can result in indeterminate operation at the display and overlay interface port outputs. Therefore, any changes to this control bit must always be followed by a "soft reset". The D_DREFCLK2_EN control bit state is not affected during a "soft reset".
	bit[7]		D_BYPASS_EN	Display Bypass Mode Enable. 0 = Normal operation of zoomed input video and overlay output. Timing is generated by the display timing generator. 1 = Bypass mode is active: VGA Port inputs (2 x 24bit RGB pixels) and controls appear at data output port after 2 clock delays. The display clock outputs are no longer sourced by DREF1 or DREF2. The display clock is a delayed version of the

Address (HEX)	Number of Bits	Mode	Name	Function
				VGA port pixel clock (VGACLK). The D_BYPASS_EN control bit state is not affected during a "soft reset". Changes to D_BYPASS_EN must always be followed by a "soft reset" to ensure controller initialization
	bit[8]		RESERVED1	Reserved state; must be set to '0' at all times.
	bit[9]		PWRDWN	This control bit is used to put the device into a low power standby state. When entering the standby state a "soft reset" should be performed first , followed by setting the PWRDWN mode control bit. To leave the low power standby state, set the PWRDWN control bit to '0' and perform a "soft reset", followed by a complete initialization of the device registers. '0' = Normal Operating State. '1' = Low Power Standby - only the Host I/F is functioning. Output signals are at static valid logic levels. The PWRDWN control bit state is not affected during a "soft reset".
	bit[10]		RGB_B_SEL	This control bit is used during RGB mode (IP_RGB_EN = '1') to enable either VGA or VGB port single pixel transfers. '0' = Single Pixel RGB input transfers are active on the VGA port. '1' = Single Pixel RGB input transfers are active on the VGB port. For YUV or double Pixel RGB transfers, clear this bit to '0'. The RGB_B_SEL control bit is not affected during a soft reset.

5.7.2. Input Control Register

Table 11: IPCTRL

Address (HEX)	Number of Bits	Mode	Name	Function
02	bit[0]	R/W	IPRUN_EN	Input Video Run Enable 0 = input active window is held in reset, no data is transferred to scaler, . $\overline{\text{VCPREQ}}$ = '1' and $\overline{\text{VCBLNK}}$ = '0'. 1 =When set input control waits for an input VSYNC which then enables the input video active window to begin sampling input pixels from the selected source for scaling operations.
	bit[1]		IP2PIXWIDE_EN	Input Video Double Pixel Width Enable (applies only to VGA Port). 0 = Single width (24 bit RGB) input pixels enabled. 1 = Double width (2 x 24 bit RGB) input pixels enabled. During YUV mode or IP2PIXOFFSET_EN='1', clear this bit to '0'.

Address (HEX)	Number of Bits	Mode	Name	Function
	bit[2]		IP2PIXOFFSET_EN	Input Video Double Pixel Wide Offset Mode Enable 0 = Standard Single width or Double width pixel transfers. 1 = Enables Double pixel offset transfers, i.e. the first pixel 1 x 24 bit RGB latched on one input clock edge, the second pixel 1 x 24 RGB latched on the next clock edge. During YUV mode or single width RGB mode, clear this bit to '0'.
	bit[3]		IP_INTLC_EN	Input Interlace Mode Enable. 0 = Non-interlace input format. (Note that for non-interlaced input formats, all input frames are handled the same as ODD fields in terms of active window decoding.) 1 = Interlaced input format (YUV or RGB)
	bit[4]		IPCREF_INV	Input Video CREF signal invert enable. (Controls active edge of VGACREF or VGBCREF, whichever has been enabled.) 0 = normal logic polarity. (Clock enable if CREF = 1.) 1 = inverted signal input. (Clock enable if CREF = 0.)
	bit[5]		IPHS_INV	Input Video Hsync signal invert enable. (Controls active state of VGAHS or VGBHS, whichever has been enabled.) 0 = normal logic polarity. (active state = '1', gmZ1 will begin a new line on the rising edge of HSYNC) 1 = inverted signal input. (active state = '0', gmZ1 will begin a new line on the falling edge of HSYNC)
	bit[6]		IPVS_INV	Input Video Vsync signal invert enable. (Controls active state of VGAVS or VGBVS, whichever has been enabled.) 0 = normal logic polarity. (active state = '1' , gmZ1 will begin a new frame on the rising edge of VSYNC) 1 = inverted signal input. (active state = '0' , gmZ1 will begin a new frame on the falling edge of VSYNC)
	bit[7]		IPODD_INV	Input Video ODD signal invert enable. (Controls active state of VCODD input signal.) 0 = normal logic polarity. (active state = '1') 1 = inverted signal input. (active state = '0')

5.7.3. Display Control Register

Table 12: DCONTROL

Address (HEX)	Bits	Mode	Name	Function
03	bit[0]	R/W	DTG_RUN_EN	Display video timing generator run enable. 0 = Display Timing Generator is halted, Zoom Filter halted, all display control and data outputs set to static '0'. 1 = Display Timing Generator and Zoom Filter enabled to run normally as programmed by all other registers.
	bit[1]		DOUT_RUN_EN	Display Output Run Enable. 0 = DHS, DVS, DEN, DCLK, DHCLK and all data lines are clamped to '0'. This overrides any programmable logic polarity controls. 1 = Display output normal operation. DHS, DVS, DEN, DCLK, DHCLK and all data lines are allowed to operate normally.
	bit[2] bit[3]		D_LINESYNC_EN D_FRAMELOCK_EN	Together the Display Line Sync Mode enable and Display Frame Lock Mode Enable registers indicate the synchronization mode of the gmZ1. D_LINESYNC_EN / D_FRAMELOCK_EN **Free Run Mode : 1 / 1** Frame Sync Mode : 0 / 1 **Line Sync Mode : 1 / 0** Clock Sync Mode : 0 / 0
	bit[4]		DFSYNC_EN	Display Frame Sync Input Enable 0 = The $\overline{\text{DFSYNC}}$ input pin does not affect gmZ1 operation. 1 = The $\overline{\text{DFSYNC}}$ input pin operates normally. In Free Run Mode, $\overline{\text{DFSYNC}}$ is ignored regardless of this bit setting.
	bit[5]		OVLY_1_EN	Overlay video port 1 enable. 0 = Overlay region #1 is disabled. $\overline{\text{OVACTIV1}}$ is static and de-asserted. 1 = Overlay region #1 is enabled. $\overline{\text{OVACTIV1}}$ output indicates when overlay pixels are sampled at the overlay port.
	bit[6]		OVLY_2_EN	Overlay video port 2 enable. 0 = Overlay region #2 is disabled. $\overline{\text{OVACTIV2}}$ is static and de-asserted. 1 = Overlay region #2 is enabled. $\overline{\text{OVACTIV2}}$ output indicates when overlay pixels are sampled at overlay port.

Address (HEX)	Bits	Mode	Name	Function
	bit[7]		D_FORC_BKGND	Display Output Force to Background Color. 0 = Display output operates normally 1 = Zoom filter output is forced to the color as selected by the BKGNDCOL[2:0] programmable control bits. Note: The overlay takes precedence over this control bit and will still appear over top of the background color.
	bit[8] bit[9] bit[10]		BKGNDCOL0 BKGNDCOL1 BKGNDCOL2	Display Background Color Select [2:0] These three bits select a display output background color from a palette of 8 colors. The colors available are identical to those available through the Overlay Color Control. See the section on Overlay Color Control. See Table 5.

5.7.4. Display Output Port Control Register

Table 13: DOUTCNTRL

Address (HEX)	Bits	Mode	Name	Function
04	bit[0]	R/W	D_2PIXWIDE_EN	Display Video Output Pixel Double Width Enable. 0 = Single width (24 bit RGB) pixels are output to the display interface with every DCLK cycle. 1 = Double width (2 x 24 bit RGB) pixels are output to the display interface with every second DCLK cycle.
	bit[1]		D_18BIT_EN	Display 18 BIT RGB Mode Enable. 0 = All individual output pixels are full 24 BIT RGB. 1 = All individual output pixels are rounded to 18 BIT RGB (6 bits for each of R,G, and B). Note: In 18 BIT RGB mode the 6 most significant bits for each color are used. The 2 least significant bits are clamped to zero.
	bit[2]		D_CSYNC_EN	0 = Normal sync operation. 1 = The output VSYNC contains composite sync information.
	bit[3]		DCLK_OD	Display Pixel Clock Output Disable. 0 = Display Pixel Clock Outputs (DCLK, DHCLK) are enabled. 1 = Display Pixel Clock Outputs (DCLK, DHCLK) are tri-stated.
	bit[4]		DCTRL_DATA_OD	Display Control and Data Output Disable. 0 = Display DHS, DVS, DEN, DARED, DABLU, DAGRN, DBRED, DBBLU, DBGRN data and control outputs are enabled. 1 = Display DHS, DVS, DEN, DARED, DABLU, DAGRN, DBRED, DBBLU, DBGRN data and control outputs are tri-stated.
	bit[5]		DCLK_INV	Display Clock Invert Enable 0 = Display output clock (DCLK) in normal “rising edge” alignment with data/control outputs. 1 = Display output clock in inverted or “falling edge” alignment with data/control outputs.
	bit[6]		DHCLK_INV	Display Half Rate Clock Invert Enable

Address (HEX)	Bits	Mode	Name	Function
				0 = Display half rate output clock (DHCLK) in normal "rising edge" alignment with data/control outputs. 1 = Display half rate output clock (DHCLK) in inverted or "falling edge" alignment with data/control outputs.
	bit[7]		DDEN_INV	Display data enable (DEN) output signal invert enable. 0 = Display Data Enable output normal active high logic. 1 = Display Data Enable output inverted logic.
	bit[8]		DHS_INV	Display horizontal (DHS) output signal invert enable. 0 = Display Horizontal Sync Output normal active high logic. 1 = Display Horizontal Sync Output inverted logic.
	bit[9]		DVS_INV	Display vertical sync pulse (DVS) output signal invert enable. 0 = Display Vertical Sync Output normal active high logic. 1 = Display Vertical Sync Output inverted logic.

5.7.5. Display Clock Control Register

Table 14: DCLK_CTRL

Address (HEX)	Bits	Mode	Name	Function
05	bit[0]	R/W	DHCLK_PHASE	Display Half Rate Clock phase control. 0 = DHCLK rising edge corresponds with output data and display timing control state changes as selected by the DHCLK_INV control bit. 1 = DHCLK occurs ½ DCLK cycle earlier in phase.
	bit[2:1]		DCLK_PHASE[1:0]	Display clock phase control. "00" = Reference DCLK setting used for display output timing AC characteristics. DCLK "active" edge occurs later (relative to output data/control transitions) than for the DCLK_PHASE[1:0] = "10" "10" = DCLK "active" edge occurs earlier than when DCLK_PHASE[1:0] = "00". "01" = DCLK "active" edge occurs earlier than when DCLK_PHASE[1:0] = "10". "11" = DCLK "active" edge occurs earlier than when DCLK_PHASE[1:0] = "01".

Address (HEX)	Bits	Mode	Name	Function
				*Note: Refer to AC Characteristics for timing data on the amount of phase adjustment possible using DCLK_PHASE[1:0].

5.7.6. Status Register

Table 15: STATUS

Address (HEX)	Bits	Mode	Name	Function
06	bit[0]	R/W	IRQ1	'0' = An IRQ1 interrupt has not occurred since the last status read. '1' = An IRQ1 interrupt has occurred since the last status read. The IRQ1 interrupt is automatically cleared after a status read.
	bit[1]		IRQ2	'0' = An IRQ2 interrupt has not occurred since the last status read. '1' = An IRQ2 interrupt has occurred since the last status read. The IRQ2 interrupt is automatically cleared after a status read.
	bit[2]		ZB_OFLOW	'0' = A zoom buffer overflow has not occurred since the last status read. '1' = A zoom buffer overflow has occurred since the last status read. The ZB_OFLOW status bit is automatically cleared after a status read.
	bit[3]		ZB_UFLOW	'0' = A zoom buffer underflow has not occurred since the last status read. '1' = A zoom buffer underflow has occurred since the last status read. The ZB_UFLOW status bit is automatically cleared after a status read.
	bit[4]		DLOCK	'0' = The DLOCK input signal has not been detected as inactive since the last status read. '1' = The DLOCK input signal has been detected as inactive since the last status read. This is used to detect loss of display clock PLL lock as indicated by the external system. The DLOCK status bit is automatically cleared after a status read.

5.7.7. Interrupt Control Register 1

Table 16: IRQ1CNTRL

Address (HEX)	Bits	Mode	Name	Function
07	bit[0]	R/W	IRQ1_LAT_EN	Interrupt #1 latch enable bit selects if the interrupt event is latched and held, or if asynchronous "flow-through" of interrupt event is enabled. '0' = The monitored video timing event signal selected by MON_SEL (inverted or not inverted under control of the MON_INV control), is then logically OR'd with DLOCK, zoom buffer overflow and zoom buffer underflow flags (when enabled by DLOCK_EN, OFLOW_EN or UFLOW_EN respectively). The result is output to the $\overline{\text{IRQ1}}$ pin as an active low open drain signal. Therefore, MON_SEL $\cup$ DLOCK = $\overline{\text{IRQ1}}$ '1' = The video timing event (inverted under control of MON_INV) is monitored for a rising edge. Once a rising edge is detected the event is latched and held in a flip flop. The flip flop outputs are logically OR'd with DLOCK, zoom buffer overflow and underflow flags (when enabled by DLOCKEN, OFLOW_EN and UFLOW_EN). Once set, IRQ1 remains set (latched) until the STATUS register is read ,which clears the IRQ1. The IRQ1 is output as an active low open drain signal on the $\overline{\text{IRQ1}}$ output pin.
	bit[1]		ZB_OFLOW_EN	'0' = disable the zoom buffer overflow event as an interrupt source. '1' = enable the zoom buffer overflow event as an interrupt source.
	bit[2]		ZB_UFLOW_EN	'0' = disable the zoom buffer underflow event as an interrupt source. '1' = enable the zoom buffer underflow event as an interrupt source.
	bit[3]		DLOCK_EN	'0' = the DLOCK input signal not enabled as an IRQ1 interrupt source. '1' = the DLOCK input signal is enabled as an IRQ1 interrupt source.
	bit[4]		MON_INV_EN	'0' = the monitored event is not inverted. '1' = the monitored event is inverted.
	bit[7:5]		MON_SEL[2:0]	See **Table 9**

5.7.8. Interrupt Control Register 2

Table 17: IRQ2CNTRL

Address (HEX)	Bits	Mode	Name	Function
08	bit[0]	R/W	IRQ2_LAT_EN	The IRQ2CNTRL register controls IRQ2 interrupt sources, whether the interrupt is edge triggered and latched, or not latched. The logic polarity of the interrupt sources is also controllable. IRQ2_LAT_EN Interrupt #2 latch enable bit selects if the interrupt event is latched and held, or if asynchronous "flow-through" of interrupt event is enabled. '0' = The monitored video timing event signal selected by MON_SEL (inverted or not inverted under control of the MON_INV control), is then logically OR'd with DLOCK, zoom buffer overflow and zoom buffer underflow flags (when enabled by DLOCK_EN, OFLOW_EN or UFLOW_EN respectively). The result is output to the $\overline{IRQ2}$ pin as an active low open drain signal. '1' = The video timing event (inverted under control of MON_INV) is monitored for a rising edge. Once a rising edge is detected the event is latched and held in a flip flop. The flip flop outputs are logically OR'd with DLOCK, zoom buffer overflow and underflow flags (when enabled by DLOCKEN, OFLOW_EN and UFLOW_EN). Once set then IRQ2 remains set (latched) until the STATUS register is read, which clears the IRQ2. The IRQ2 is output as an active low open drain signal on the $\overline{IRQ2}$ output pin.
	bit[1]		ZB_OFLOW_EN	'0' = disable the zoom buffer overflow event as an interrupt source. '1' = enable the zoom buffer overflow event as an interrupt source.
	bit[2]		ZB_UFLOW_EN	'0' = disable the zoom buffer underflow event as an interrupt source. '1' = enable the zoom buffer underflow event as an interrupt source.
	bit[3]		DLOCK_EN	'0' = the DLOCK input signal not enabled as an IRQ2 interrupt source. '1' = the DLOCK input signal is enabled as an IRQ2 interrupt source.
	bit[4]		MON_INV_EN	'0' = the monitored event is not inverted. '1' = the monitored event is inverted.
	bit[7:5]		MON_SEL[2:0]	See **Table 9**

5.7.9. Input Video Register

This section contains the registers needed to set the Active Window controls.

Table 18: Input Video

Address (HEX)	Bits	Mode	Name	Function
09	bit[10:0]	R/W	IPH_ACTIV_START	Input Video Horizontal Active Start: This register defines the number of pixel clocks (qualified by VGACREF or VGBCREF) from where the start of the VGAHS or VGBHS pulse is sampled, to the first active pixel sampled by the gmZ1 Active Window Decoder. Therefore in video terms this register defines the input horizontal line period occupied by: Horz Sync Pulse + Horz Back Porch. Input Horizontal Active Start is programmable within the following limits: (Horizontal Active Start + Horizontal Active Period) ≤ 2047. Available range for Horizontal Active Start is: Single Pixel RGB 12 ≤ IPH_ACTIV_START ≤ 2047 Double Pixel Offset RGB 24 ≤ IPH_ACTIV_START ≤ 2046 During Single Pixel RGB or Double Pixel Offset RGB modes, both odd and even numbers are supported. The first active pixel is sampled during the Nth qualified clock, where N = IPH_ACTIV_START. During Double Pixel RGB, only even numbers are supported. Also in Double Pixel RGB mode the register defines the 1st active pixel to be sampled during the Nth qualified clock, where N = IPH_ACTIV_START / 2 Example: For single pixel mode and a combined horizontal sync and horizontal sync back porch interval that totals 226 VGACLK qualified sample edges, and the 227 qualified VGACLK sample edge samples the 1st pixel, program this register with the value (226 + 1) = 0E3h.
0A	bit[10:0]	R/W	IPH_ACTIV_WIDTH	*Input Video Horizontal Active Pixels:* The number of active input pixels sampled (as qualified by VGACREF or VGBCREF) from the start of Horizontal Active Window to the end of the horizontal active period is determined by the value written to the IPH_ACTIV_WIDTH register. (Horizontal Active Start + Horizontal Active Width) ≤ 2047. Available range for Horizontal Active Period is: 16 ≤ IPH_ACTIV_WIDTH ≤ 1024. During Single Width RGB or Double Width Offset RGB modes, both odd and even numbers are supported. During Double Width RGB and YUV Modes, only even numbers are supported. Example: For 1024 active pixels per horizontal line then load this register with the value 400h.
0B	bit[10:0]	R/W	IPV_ACTIV_STARTODD	*Input Video Vertical Active Start - Odd Fields:* The number of lines from the start of the selected input video VSYNC when VCODD = '1', to (and including) the first line of the Vertical Active Window is determined by the value written to the IPV_ACTIV_STARTODD register.

Address (HEX)	Bits	Mode	Name	Function
				(Vertical Active Start + Vertical Active Length) ≤ 2047. When the input video source is not interlaced, VCODD is ignored and all input frames are treated the same as ODD fields. Available range for Vertical Active Start is: 1 ≤ IPV_ACTIV_STARTODD ≤ 2047. Example: For an input video format that has after the start of VGBVS pulse another 18 occurrences of VGBHS pulse before the active region of the first displayed line during the input field when VCODD = '1', program IPV_ACTIV_STARTODD with the value 19 which is 13h.
0C	bit[10:0]	R/W	IPV_ACTIV_STARTEVN	*Input Video Vertical Active Start -Even Fields*: The number of lines from the start of the selected input video VSYNC when input signal VCODD = '0', to the start of the Vertical Active Window, is determined by the value written to the IPV_ACTIV_STARTEVN register. When the input video source is not interlaced video, then VCODD is ignored and all input frames are treated the same as odd fields. (Vertical Active Start + Vertical Active Length) ≤ 2047. Available range for Vertical Active Start is: 1 ≤ IVP_ACTIV_STARTEVN ≤ 2047. Example: For an input video format that has after the start of VGBVS pulse another 17 occurrences of the VGBHS pulse before the active region of the first displayed line during the input field when VCODD = '0', program IV_ACTIV_STARTEVN with the value 12h.
0D	bit[10:0]	R/W	IPV_ACTIV_LNGTH	*Input Video Vertical Active Lines:* The number of active lines from the start of Vertical Active Window to the end of the Vertical Active Window is determined by the value written to the IPV_ACTIV_LNGTH register. It is programmable in terms of single line increments. (Vertical Active Start + Vertical Active Length) ≤ 2047. Available range for Vertical Active Period is: 8 ≤ IPV_ACTIV_LNGTH ≤ 2047. Example: An input video format has 240 active lines per field. Then program IPV_ACTIV_LNGTH with the value F0h.
0E	bit[10:0]	R/W	IPH_LOCK_EVENT	*Input Video Programmable Lock Horizontal Event*: Determines the number of valid input pixel clocks that must occur before the programmable LOCK_EVENT can occur. When the pixel period selected by this register is active and if the IPV_LOCK_EVENT condition is satisfied, then the LOCK_EVENT occurs. 8 ≤ IPH_LOCK_EVENT ≤ 2047. Example: The display timing is to be synchronized to a non-interlaced RGB video source so that the display timing loads to it's predefined state during the 338th pixel location of the 376th vertical line of the input frame. Load

Address (HEX)	Bits	Mode	Name	Function
				IPH_LOCK_EVENT with the value 338 which is 152h.
0F	bit[10:0]	R/W	IPV_LOCK_EVENT	*Input Video Programmable Lock Vertical Event:* Determines the number of lines (input Hsync pulses) that occur before the programmable LOCK_EVENT can occur. When the input line selected by this register is active then the LOCK_EVENT is enabled but the IPH_LOCK_EVENT condition must still be satisfied before the LOCK EVENT occurs. Note that the LOCK_EVENT only occurs once per input frame and therefore occurs once every other field (only on ODD fields) during interlaced input video. $1 \leq$ IPV_LOCK_EVENT ≤ 2047. Example: If the display timing is to be synchronized to a non-interlaced RGB video source so that the display timing loads to its predefined state during the 338th pixel location of the 376th vertical line of the input frame, load IPV_LOCK_EVENT with the value 376, which is 178h. Note: The programmable LOCK_EVENT can be disabled by clearing this register with zeros.

5.7.10. Display Register

Table 19: Display Line Rate

Address (HEX)	Bits	Mode	Name	Function
10	bit[9:0]	R/W	DH_RATE_hi	*Display Line Rate Synth Value MSB:* This register provides the upper portion of the display horizontal rate value used in determining the display line rate during Line_Sync mode.
11	bit[10:0]	R/W	DH_RATE_mid	*Display Line Rate Synth Value Middle Word:* This register provides the middle portion of the display horizontal rate value used in determining the display line rate during Line_Sync mode.
12	bit[10:0]	R/W	DH_RATE_lo	*Display Line Rate Synth Value LSB:* This register provides the lower portion of the display horizontal rate value used in determining the display line rate during Line_Sync mode. The total rate value is 32 bits in length and is segmented between the hi (10-bits), mid (11-bits) and lo (11-bits) registers. The rate value is determined by the off-chip system and written to the DH_RATE

Address (HEX)	Bits	Mode	Name	Function
				DH_RATE = RND [2^{32} x DV_TOTAL/(IPH_TOTAL x IPV_TOTAL)] Where: IPH_TOTAL = the total number of clocks per input line (regardless of the state of VGACREF or VGBCREF) including both active and blanking regions. Note that the pixel clock must be a fixed integer multiple of the input line rate (line-locked). IPV_TOTAL = the total number of lines (VGAHS or VGAHS pulses) in one frame if non-interlaced, or per field if interlaced video. This number includes both vertical active and blanking regions. Example: For NTSC (interlaced) then IPV_TOTAL = 262.5. For VGA (non-interlaced) then IPV_TOTAL = 525.

5.7.11. Zoom Register

This section provides the resizing values of the image.

Table 20: Zoom

Address (HEX)	Bits	Mode	Name	Function
13	bit[8:0]	R/W	Z_HORZ_SV_hi	*Zoom Horizontal Scale Value:* This register provides the upper portion on the horizontal zoom scaling value (Z_HORZ_SV) which can be calculated as described in the following subsections: *Non-interlaced or Interlaced Video Input* Z_HORZ_SV = RND[IPH_ACTIV_WIDTH x 2^{17} / DH_ACTIV_WIDTH] The resulting 17 bit integer value is divided into two words for programming. The most significant word (9 bits) is programmed into Z_HORZ_SV_hi, and the least significant word (8 bits) is programmed into the Z_HORZ_SV_lo register. Example: Zoom 640 pixels per input line to 1024 pixels per output line. Then Z_HORZ_SV = RND[640 x 2^{17} / 1024] = RND[81920] = 81920 This converts to hex as 14000h. The value is split into MSB and LSB which are then programmed as 140h into Z_HORZ_SV_hi and 00h which is programmed into Z_HORZ_SV_lo. *Note: The above method is optimized for graphics type images. As an alternative, the calculation may be done as follows:* Z_HORZ_SV = RND[(IPH_ACTIV_WIDTH -1) x 2^{17} / (DH_ACTIV_WIDTH - 1)] *No Zoom (1:1 Scaling)* No Zoom or 1:1 scaling is a special case that can be enabled by writing the Z_HORZ_SV_hi/lo registers with 0's in all bit

Address (HEX)	Bits	Mode	Name	Function
				positions. Z_HORZ_SV=0
14	bit[7:0]	R/W	Z_HORZ_SV_lo	*Zoom Horizontal Scale Value:* See above section on Z_HORZ_SV_hi.
15	bit[7:0]	R/W	Z_VERT_SV_hi	*Zoom Vertical Scale Value:* This register provides the upper portion on the vertical zoom scaling value (Z_VERT_SV) which can be calculated as described in the following subsections. *Non-interlaced Video Input* Z_VERT_SV = RND[IPV_ACTIV_LNGTH x 2^{16} / DV_ACTIV_LNGTH] The resulting 16 bit integer value is divided into two words for programming. The most significant word (8 bits) is programmed into Z_VERT_SV_hi, and the least significant word (8 bits) into the Z_VERT_SV_lo register. Example: Zoom 480 lines per input frame to 768 lines per output frame. Then, Z_VERT_SV = RND[480 x 2^{16} / 768] = RND[40960] = 40960. This converts to hex as A000h. The value is split into MSB and LSB which are then programmed as A0h into Z_VERT_SV_hi and 00h into Z_VERT_SV_lo *Note: The above method is optimized for graphics type images. As an alternative, the calculation may be done as follows:* Z_VERT_SV = RND[(IPV_ACTIV_LNGTH -1) x 2^{16} / (DV_ACTIV_LNGTH - 1)] *No Zoom (1:1 Scaling)* No Zoom or 1:1 scaling is a special case that can be enabled by writing the Z_VERT_SV_hi/lo registers with 0's in all bit positions. Z_VERT_SV = 0 *Interlaced Video Input* Z_VERT_SV = RND[({2 x IPV_ACTIV_LNGTH} -1) x 2^{16} / (2 x {DV_ACTIV_LNGTH - 1})] The resulting 16 bit integer value is divided into two words for programming. The most significant word (8 bits) is programmed into Z_VERT_SV_hi, and the least significant word (8 bits) is programmed into the Z_VERT_SV_lo register. Example: De-interlace and zoom 240 lines per input field to 768 lines per output frame. Then, Z_VERT_SV = RND[(2 x 240 -1) x 2^{16} / (2 x {768 - 1})] = RND(20463.98) = 20464. This converts to hex as 4FF0h. The value is split into MSB and LSB which are then programmed as 4Fh into Z_VERT_SV_hi and F0h which is programmed into Z_VERT_SV_lo 1:1 zooming is not allowed with interlaced video (i.e. DV_ACTIV_LNGTH must be > than IPV_ACTIV_LNGTH)

Address (HEX)	Bits	Mode	Name	Function
16	bit[7:0]	R/W	Z_VERT_SV_lo	*Zoom Vertical Scale Value:* See above section on Z_VERT_SV_hi.

5.7.12. Filter Horizontal Control Register

Table 21: FHC - Filter Horizontal Control

Address (HEX)	Bits	Mode	Name	Function
17	bit[5:0]	R/W	HFILT_CTRL	This control bit is used in conjunction with the CASC_EN control bit. When CASC_EN is set, this register controls horizontal sub-pixel offset for cascading operations. When CASC_EN = '0' these register control bits must be cleared to '0'.
	bit[6]		RESERVED2	This control bit is reserved for future use. Always program this bit to '0' for normal operation.
	bit[7]		CASC_EN	'0' = NORMAL; Normal Filter operation. '1' = CASC_EN; Enable horizontal cascading.

5.7.13. Display Horizontal Control Register

Table 22: Display Horizontal

Address (HEX)	Bits	Mode	Name	Function
18	bit[10:0]	R/W	DH_LOCK_LD	*Display Horizontal Lock Load*: determines the value to be loaded into the Display Horizontal Counter upon assertion of a LOCK_EVENT. Lock Events can occur as a result of the programmed display synchronization mode controlled by the DCONTROL register. Valid Range: 1 to 2047
19	bit[10:0]	R/W	DH_TOTAL	*Display Horizontal Total Pixel Clocks*: determines the number of DCLK cycles in each display output line (DHS leading edge to DHS leading edge).

Address (HEX)	Bits	Mode	Name	Function
				Valid Range: 1 to 2047. Example: For a display line period of 1344 DCLK cycles, load this register with the value 540h.
1A	bit[7:0]	R/W	DH_VCTEN	*Display Horizontal Vertical Count Enable:* determines (in increments of 8 clocks) the number of DCLK cycles from the start of a display output line (DHS leading edge) to the leading edge of DVS. For values greater than '0' then the skew is DH_VCNTEN x 8 DCLK periods with DHS leading DVS. To make DVS "lead" DHS then program DH_VCNTEN with a value large enough to position DHS near the end of a line, just ahead of DVS. Valid Range: 0 to 255 When cleared to the value "00"h then the DVS and DHS output signals are aligned. When programmed to the value 8h then DVS lags DHS by 64 DCLK cycles.
1B	bit[5:0]	R/W	DH_HS_END	*Display Horizontal Sync End*: this number multiplied by 4 determines the width of DHS pulse in DCLK cycles. Valid Range: 1 to 63 (resulting DHS width of 4 to 256 DCLK cycles) Example: To set the DHS for a pulse width of 136 DCLK cycles, load this register with the value 22h.
1C	bit[10:0]	R/W	DH_BKGND_START	*Display Horizontal Background Start*: this number determines the number of DCLK cycles from start of line to first pixel of the BACKGROUND region. Valid Range: 1 to 2047; DH_HS_END x 4 < DH_BKGND_START <= DH_ACTIV_START < (DH_ACTIV_START+DH_ACTIV_WIDTH) <= (DH_BKGND_END+1) < (DH_TOTAL+1). Single Wide Mode: First produced output background pixel is "N" where "N" is the value in the DH_BKGND_START contents. Double Wide Mode: First produced output background pixel is "N+1" where "N" is the value in the DH_BKGND_START register. Example: In single wide mode for a combined (DHS + horizontal back porch) blanking region of 296 DCLK cycles, (i.e. the 297 pixel period contains the first background pixel), load this register with the value 129h.
1D	bit[10:0]	R/W	DH_ACTIV_START	*Display Horizontal Active Start*: determines the number of DCLK cycles from the start of the line to the start of the ACTIVE region. Valid Range: 1 to 2047; DH_HS_END x 4 < DH_BKGND_START <= DH_ACTIV_START < (DH_ACTIV_START+DH_ACTIV_WIDTH) <= (DH_BKGND_END+1) < (DH_TOTAL+1). Single Wide Mode: First produced output active pixel is "N" where "N" is the value in the DH_ACTIV_START contents. Double Wide Mode: First produced output active pixel is "N+1" where "N" is the value in the DH_ACTIV_START register. Example: For a combined (DHS + horizontal back porch) blanking region of 296 DCLK cycles. (i.e. the 297 pixel period contains the first active pixel), load this register with the value 129h.

Address (HEX)	Bits	Mode	Name	Function
1E	bit[10:0]	R/W	DH_ACTIV_WIDTH	*Display Horizontal Active Width*: determines the number of active pixels (DCLK cycles) per display line. Valid Range: 16 to 2047; DH_HS_END x 4 < DH_BKGND_START <= DH_ACTIV_START < (DH_ACTIV_START+DH_ACTIV_WIDTH) <= (DH_BKGND_END+1) < (DH_TOTAL+1). For both Single Wide and Double Wide modes, the number of "active" (zoomed output) pixels is "N", where "N" is the value in the DH_ACTIV_WIDTH register. Example: For 1024 active display pixels per line, load this value with 400h.
1F	bit[10:0]	R/W	DH_BKGND_END	*Display Horizontal Background End:* determines the number of DCLK cycles from the start of a display line to the start of horizontal blanking. Valid Range: 1 to 2047; DH_HS_END x 4< DH_BKGND_START <= DH_ACTIV_START < (DH_ACTIV_START+DH_ACTIV_WIDTH) <= (DH_BKGND_END+1) < (DH_TOTAL+1). Single Wide Mode: Last produced output background pixel is "N" where "N" is the value in the DH_BKGND_END register. Double Wide Mode: Last produced output background pixel is "N+1" where "N" is the value in the DH_BKGND_END register. Example: If Background and Active regions are equal, DH_BKGRND_END = DH_BKGND_START + DH_ACTIV_WIDTH - 1
20	bit[10:0]	R/W	DV_LOCK_LD	*Display Vertical Lock Load:* determines the line number that the display timing controller jumps to when a LOCK_EVENT occurs and Line_Sync or Frame_Lock modes are enabled. Valid Range: 1 to 2047.
21	bit[10:0]	R/W	DV_TOTAL	*Display Vertical Total:* determines the number of lines per display frame. The number of vertical lines per frame is "N", where "N" is the value in the DV_TOTAL register. Valid Range: 1 to 2047. Example: For a display frame that has 806 lines per frame, load this register with the value 326h.
22	bit[10:0]	R/W	DV_VS_END	Display Vertical Sync End: determines the duration of DVS pulse in lines. The DVS pulse is "N" lines in duration, where "N" is the value in the DV_VS_END register. Valid Range: 1 to 15. Example: For a DVS pulse width of 6 display lines load this register with the value 6.
23	bit[10:0]	R/W	DV_BKGND_START	Display Vertical Background Start: determines the number of lines from start of frame (DVS leading edge) to the first line displayed as Background Color.

Address (HEX)	Bits	Mode	Name	Function
				The first output line that contains background color is line "N", where "N" is the value in the DV_BKGND_START register. Valid Range: 1 to 2047. Example: For a display frame with DVS + vertical back porch = 35 lines, then line 36 is the 1st background line, then load this register with the value 24h.
24	bit[10:0]	R/W	DV_ACTIV_START	*Display Vertical Active Start:* determines the number of lines from the start of the frame to the first line displayed as the Active region. The first output line that contains "active" (zoom output) pixels is line "N", where "N" is the value in the DV_ACTIV_START register. Valid Range: 1 to 2047. Example: For a display frame with DVS + vertical back porch = 35 lines, 36 is the 1st active line. Load this register with the value 24h.
25	bit[10:0]	R/W	DV_ACTIV_LNGTH	*Display Vertical Active Length:* determines the number of lines of Active region during which scaled video output is displayed. The number of active (zoom output) lines is "N", where "N" is the contents of the DV_ACTIV_LNGTH register. Valid Range: 1 to 2047. Example: For a display frame with 768 active lines, load this register with the value 300h.
26	bit[10:0]	R/W	DV_BKGND_END	Display Vertical Background End: determines the number of lines from the start of the display frame to the last line displayed as a Background Color. The last line of background color pixels is "N", where "N" is the contents of the DV_BKGND_END. Valid Range: 1 to 2047. Example: For line number 803 to be the last displayed background line then load this register with the value 323h.

5.7.14. Overlay Register

Table 23: Overlay

Address (HEX)	Bits	Mode	Name	Function
27	bit[7:0]	R/W	OVLY_1_HSTART	*Overlay "1" Region Horizontal Start:* determines the number of clock cycles - from the start of a display line to the start of the horizontal active region for overlay "1" in increments of 8. Therefore, N = (Pixel Location - 9)/8 , where "N" is the value in the OVLY_1_HSTART and Pixel Location is the first produced overlay pixel location. Valid Range: 1 to 255. Effective Range: 8 to 2040. Example: For the 1st overlay pixel to occur during the 257th DCLK cycle from the leading edge of DHS, load this register with the value: (257-9)/8 = 31, which translates to 1Fh.
28	bit[7:0]	R/W	OVLY_1_HEND	*Overlay "1" Region Horizontal End:* determines the number of clock cycles - from the start of a display line to the end of the horizontal active region for overlay "1" in increments of 8. The last produced overlay pixel is at N*8+8, where "N" is the value in the OVLY_1_HEND register. Valid Range: 1 to 255. Effective Range: 8 to 2040. For an overlay that is 64 pixels wide relative to an overlay start at the 256th DCLK cycle from leading edge of DHS, load this register with the value: ({OVLY_1_HSTART + 64}-8)/8 = 39 which translates to 27h.
29	bit[7:0]	R/W	OVLY_1_VSTART	*Overlay "1" Region Vertical Start:* determines the number of display line periods from the start of a display frame (DVS leading edge) to the start of the vertical active region for overlay "1" in increments of 8. The first displayed overlay line is line "N*8", where "N" is the value in the OVLY_1_VSTART register. Valid Range: 1 to 255. Effective Range: 8 to 2040.
2A	bit[7:0]	R/W	OVLY_1_VEND	Overlay "1" Region Vertical End; determines the number of display line periods from the start of a display frame (DVS leading edge) to the end of the vertical active region for overlay "1" in increments of 8. The last displayed overlay line is line "(N*8)-1", where "N" is the value in the OVLY_1_VEND register Valid Range: 1 to 255. Effective Range: 8 to 2040.
2B	bit[7:0]	R/W	OVLY_2_HSTART	*Overlay "2" Region Horizontal Start:* determines the number of clock cycles - from the start of a display line to the start of the horizontal active region for overlay "2" in increments of 8. Valid Range: 1 to 255. Effective Range: 8 to 2040.

Address (HEX)	Bits	Mode	Name	Function
2C	bit[7:0]	R/W	OVLY_2_HEND	*Overlay "2" Region Horizontal End:* determines the number of clock cycles - from the start of a display line to the end of the horizontal active region for overlay "2" in increments of 8. Valid Range: 1 to 255. Effective Range: 8 to 2040.
2D	bit[7:0]	R/W	OVLY_2_VSTART	*Overlay "2" Region Vertical Start:* determines the number of display line periods from the start of a display frame (DVS leading edge) to the start of the vertical active region for overlay "2" in increments of 8. Valid Range: 1 to 255. Effective Range: 8 to 2040.
2E	bit[7:0]	R/W	OVLY_2_VEND	*Overlay "2" Region Vertical End:* determines the number of display line periods from the start of a display frame (DVS leading edge) to the end of the vertical active region for overlay "2" in increments of 8. Valid Range: 1 to 255. Effective Range: 8 to 2040.
2F	bit[7:0]	R/W	OVLY_RED	*Display Overlay Color Red Intensity:* This register determines the Overlay Color Register Palette "RED" intensity. Valid Range: 0 to 255.
30	bit[7:0]	R/W	OVLY_GRN	*Display Overlay Color Green Intensity:* This register determines the Overlay Color Register Palette "GREEN" intensity. Valid Range: 0 to 255.
31	bit[7:0]	R/W	OVLY_BLU	*Display Overlay Color Blue Intensity:* This register determines the Overlay Color Register Palette "BLUE" intensity. Valid Range: 0 to 255.

6. Electrical Specifications

Table 24 Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}	3.00	3.3	3.6	V
Input Levels					
High-Level Input Voltage	V_{IH}	2.0		5.0	V
Low-Level Input Voltage	V_{IL}	GND		0.8	V

.

Table 25: Absolute Maximum Ratings

All voltages are measured with respect to GND

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Supply Voltage (1)	V_{DD}	0		4.2	V
Input Voltage (1)	V_{IN}	-0.6		5.5	V
Electrostatic Discharge	V_{ESD}			±2.0	kV
Latchup	I_{LA}			±100	mA
Storage Temperature	T_{STG}	-40		125	°C
Operating Junction Temp.	T_J	0		125	°C
Operating Junction Temp. (gmZ1EH2)	T_J	-40		125	°C
Thermal Resistance: (Junction to Air)					
Natural Convection					
gmZ1CQ4 (2)	θ_{JA}		29		°C/W
gmZ1CH2 (2)			22		°C/W
0.5 Metres/Sec air flow					
gmZ1CQ4 (2)	θ_{JA}		24		°C/W
gmZ1CH2 (2)			17		°C/W
1.0 Metres/Sec air flow					
gmZ1CQ4 (2)	θ_{JA}		22		°C/W
gmZ1CH2 (2)			15		°C/W
Thermal Resistance: (Junction to Case)					
Convection or air flow					
gmZ1CQ4	θ_{JC}		2		°C/W
gmZ1CH2	θ_{JC}		1		°C/W
Soldering Temperature (30 sec.)	T_{SOL}			220	°C
Vapor Phase Soldering (30 sec.)	T_{VAP}			220	°C

1. Absolute maximum voltage ranges are for transient voltage excursions.
2. Package thermal resistance is based on a PCB with one signal and two power planes. Package θ_{JA} is improved with four or more layer PCB.

Table 26 DC Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Operating Voltage	V_{DD}	3.0	3.3	3.6	V
Supply Current	I_{DD}				
CLK = 65MHz			510 (1)	630 (2)	mA
CLK = 84MHz			670 (1)	810 (2)	mA
Inputs					
High Voltage	V_{IH}	2.0		5	V
Low Voltage	V_{IL}	GND		0.8	V
High Current (V_{IN} = 5.0 V)	I_{IH}	-25		25	µA
Low Current (V_{IN} = 0.8 V)	I_{IL}	-25		25	µA
Capacitance (V_{IN} = 2.4 V)	C_{IN}			8	pF
Outputs					
High Voltage (I_{OH} = 7 mA)	V_{OH}	2.4		VDD	V
Low Voltage (I_{OL} = -7 mA)	V_{OL}	GND		0.5	V
Tri-State Leakage Current	I_{OZ}	-25		25	µA

Notes :

(1) Power Dissipation @ 3.3V, 75% data switching during active region, 25.1% display blanking, worst case process and temperature, 16pF Cload.

(2) Power Dissipation @ 3.6V, 100% data switching during active region, 25.1% display blanking, worst case process and temperature, 16pF Cload.

The gmZ1CH2 device contains a heat slug, and therefore can dissipate more power and operate in higher ambient
temperatures than the gmZ1CQ4 device without exceeding the 125 °C die junction maximum.

gmZ1 POWER DATA

Figure 39 below illustrates the maximum dynamic current I_{DD} for three different voltages and at different DCLK frequencies. This is based on display output formats with indicated data switching, 25.1% display blanking, capacitive loading of 16pF, worst case device/process and worst case temperature.

Figure 39: I_{DD} @ 16pF Output Load

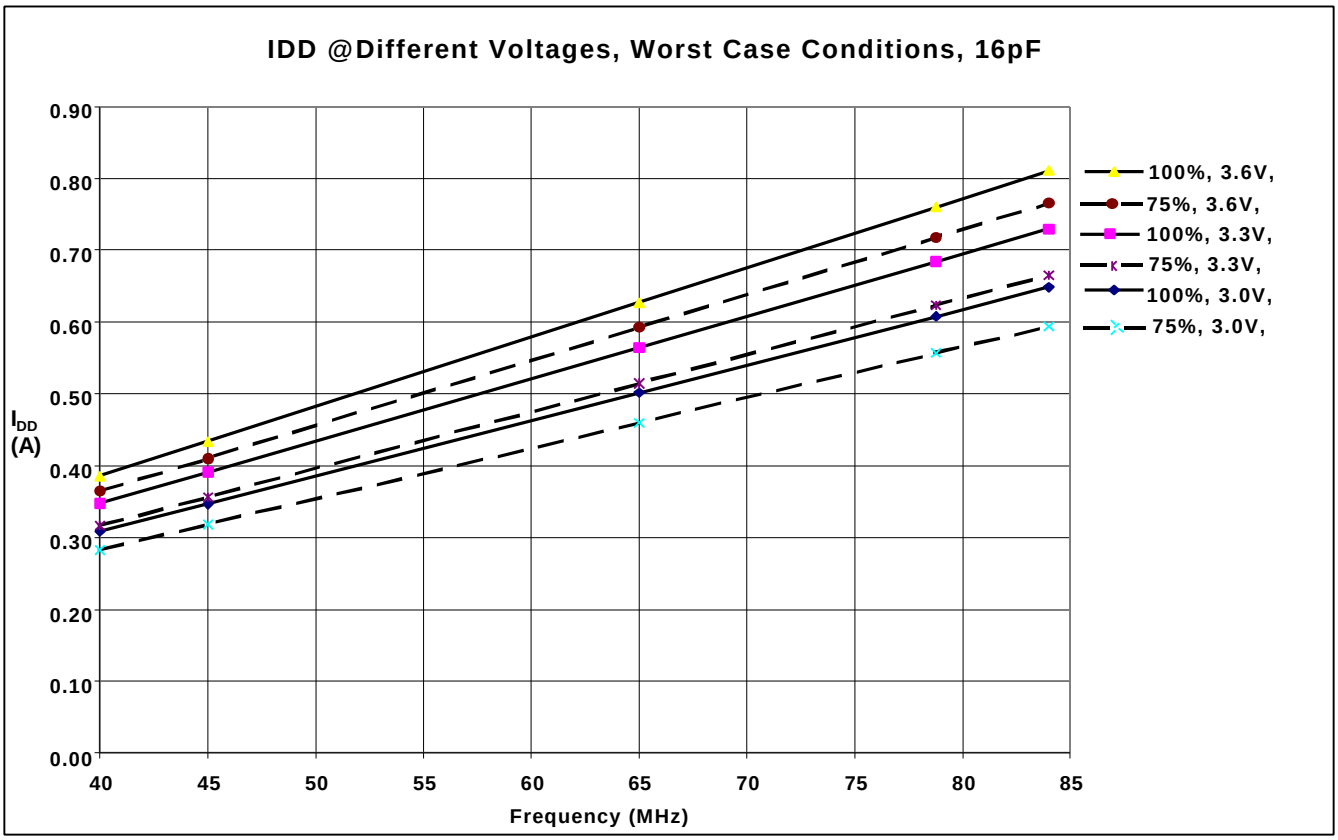


Table 27 : IDD for Different Conditions, 16pF Output Loading

Voltage (V) with Data Switching	I_{DD}, A DCLK = 40MHz, 25.1% display blanking	I_{DD}, A DCLK = 65MHz, XGA, 25.1% display blanking	I_{DD}, A DCLK = 78.75MHz, XGA, 25.1% display blanking	I_{DD}, A DCLK = 84MHz, XGA, 25.1% display blanking
3.0, 100% Data Switching during active region	0.31	0.50	0.61	0.65
3.3, 100% Data Switching during active region	0.35	0.56	0.68	0.78
3.6, 100% Data Switching during active region	0.39	0.63	0.76	0.81
3.0, 75% Data Switching during active region	0.28	0.46	0.56	0.59
3.3, 75% Data Switching during active Region	0.32	0.51	0.62	0.67
3.6, 75% Data Switching during active region	0.36	0.59	0.72	0.77

Calculations :

$$P_{Dissipation} = I_{DD} \times Voltage$$

$$T_{ambient} = T_{MaxJunction} - P_{Dissipation} (\theta_{JA})$$

Table 28 : Power Dissipation = 2.92W @ 3.6V, 84MHz, 100% Data Switching, 25.1% display blanking, C_L=16pF, and 125°C Die Junction Temp

	gmZ1CQ4		gmZ1CH2	
Air Flow in metres/sec	**Thermal Resistance (θ_{JA})**	**Maximum Ambient Temperature**	**Thermal Resistance (θ_{JA})**	**Maximum Ambient Temperature**
0 MPS	29°C/W	40.4°C	22°C/W	60.8°C
0.5 MPS	24°C/W	54.9°C	17°C/W	75.8°C
1.0 MPS	22°C/W	60.8°C	15°C/W	81.2°C

Table 29 : Power Dissipation = 2.26W @ 3.6V, 65MHz, 100% Data Switching, 25.1% display blanking, C_L=16pF, and 125°C Die Junction Temp

	gmZ1CQ4		gmZ1CH2	
Air Flow in metres/sec	**Thermal Resistance (θ_{JA})**	**Maximum Ambient Temperature**	**Thermal Resistance (θ_{JA})**	**Maximum Ambient Temperature**
0 MPS	29°C/W	59.5°C	22°C/W	75.3°C
0.5 MPS	24°C/W	70.8°C	17°C/W	86.6°C
1.0 MPS	22°C/W	75.3°C	15°C/W	91.1°C

Table 30 : Power Dissipation = 2.21W @ 3.3V, 84MHz, 75% Data Switching, 25.1% display blanking, C_L=16pF, and 125°C Die Junction Temp

	gmZ1CQ4		gmZ1CH2	
Air Flow in metres/sec	**Thermal Resistance (θ_{JA})**	**Maximum Ambient Temperature**	**Thermal Resistance (θ_{JA})**	**Maximum Ambient Temperature**
0 MPS	29°C/W	60.9°C	22°C/W	76.4°C
0.5 MPS	24°C/W	72.0°C	17°C/W	87.4°C
1.0 MPS	22°C/W	76.4°C	15°C/W	91.8°C

Table 31 : Power Dissipation = 1.68W @ 3.3V, 65MHz, 75% Data Switching, 25.1% display blanking, C_L=16pF, and 125°C Die Junction Temp

	gmZ1CQ4		gmZ1CH2	
Air Flow in metres/sec	Thermal Resistance (q_{JA})	Maximum Ambient Temperature	Thermal Resistance (q_{JA})	Maximum Ambient Temperature
0 MPS	29°C/W	76.3°C	22°C/W	88.0°C
0.5 MPS	24°C/W	84.7°C	17°C/W	96.4°C
1.0 MPS	22°C/W	88.0°C	15°C/W	99.8°C

Figure 40 below illustrates the maximum dynamic current I_{DD} for three different voltages and at different DCLK frequencies. This is based on a display output formats with indicated data switching during active region, 25.1% display blanking, capacitive loading of 10pF, worst case device/process and worst case temperature.

Figure 40: I_{DD} @ 10pF Output Load

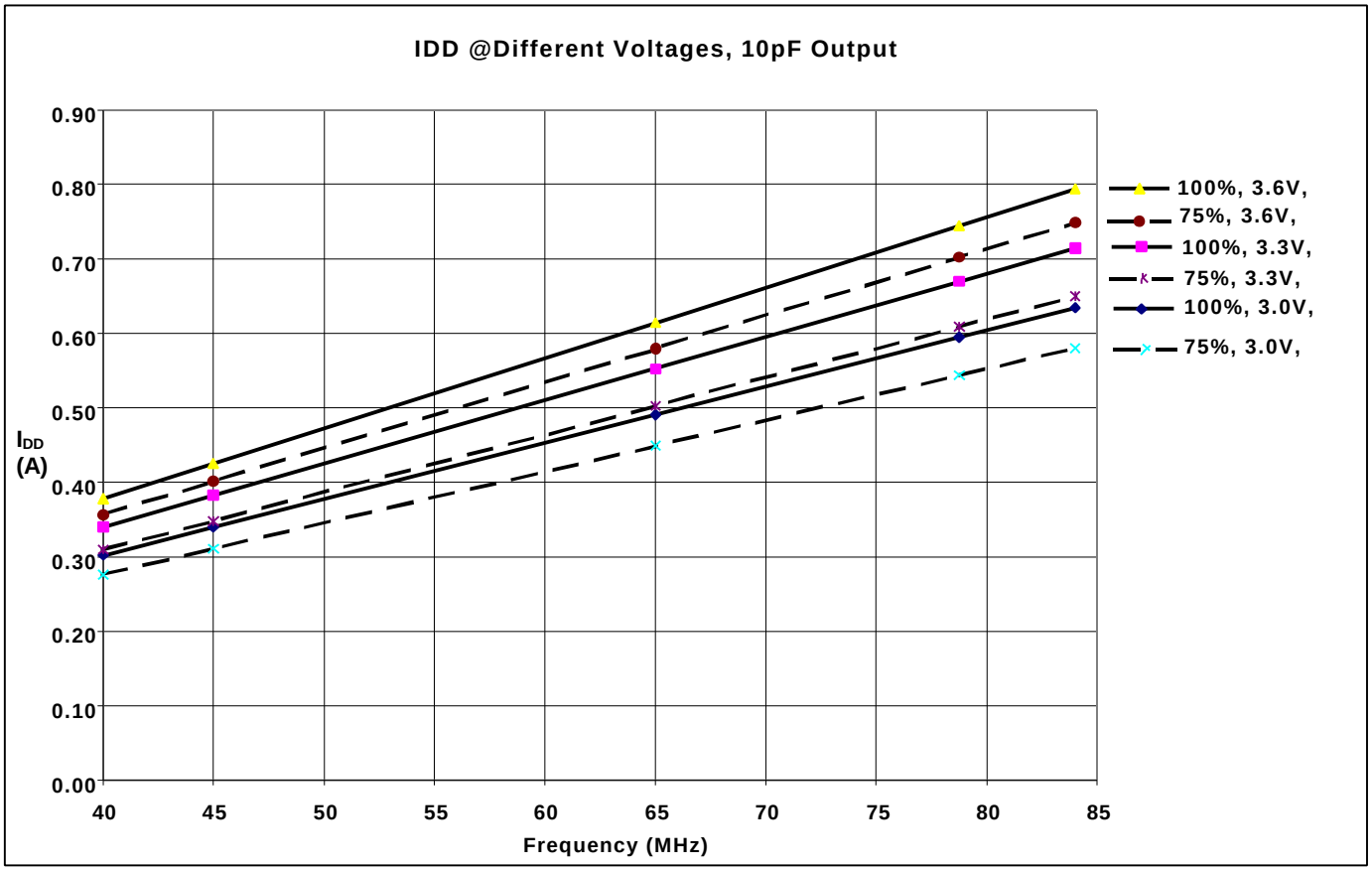


Table 32 : IDD for Different Conditions with 10pF Output Loading

Voltage (V) with Data Switching	I_{DD}, A DCLK = 40MHz, 25.1% display blanking	I_{DD}, A DCLK = 65MHz, XGA, 25.1% display blanking	I_{DD}, A DCLK = 78.75MHz, XGA, 25.1% display blanking	I_{DD}, A DCLK = 84MHz, XGA, 25.1% display blanking
3.0, 100% Data Switching during active region	0.30	0.49	0.59	0.63
3.3, 100% Data Switching during active region	0.34	0.55	0.67	0.71
3.6, 100% Data Switching during active region	0.38	0.61	0.74	0.79
3.0, 75% Data Switching during active region	0.28	0.45	0.54	0.58
3.3, 75% Data Switching during active Region	0.31	0.50	0.61	0.65
3.6, 75% Data Switching during active region	0.36	0.58	0.70	0.75

Table 33 : Power Dissipation = 2.84W @ 3.6V, 84MHz, 100% Data Switching, 25.1% display blanking, C_L=10pF, and 125°C Die Junction Temp

	gmZ1CQ4		gmZ1CH2	
Air Flow in metres/sec	Thermal Resistance (q_{JA})	Maximum Ambient Temperature	Thermal Resistance (q_{JA})	Maximum Ambient Temperature
0 MPS	29°C/W	42.6°C	22°C/W	62.5°C
0.5 MPS	24°C/W	56.8°C	17°C/W	76.7°C
1.0 MPS	22°C/W	62.5°C	15°C/W	82.4°C

Table 34 : Power Dissipation = 2.20W @ 3.6V, 65MHz, 100% Data Switching, 25.1% display blanking, C_L=10pF, and 125°C Die Junction Temp

	gmZ1CQ4		gmZ1CH2	
Air Flow in metres/sec	Thermal Resistance (q_{JA})	Maximum Ambient Temperature	Thermal Resistance (q_{JA})	Maximum Ambient Temperature
0 MPS	29°C/W	63.8°C	22°C/W	76.6°C
0.5 MPS	24°C/W	72.2°C	17°C/W	87.6°C
1.0 MPS	22°C/W	76.6°C	15°C/W	92.0°C

Table 35 : Power Dissipation = 2.14W @ 3.3V, 84MHz, 75% Data Switching, 25.1% display blanking, C_L=10pF, and 125°C Die Junction Temp

	gmZ1CQ4		gmZ1CH2	
Air Flow in metres/sec	**Thermal Resistance (q_{JA})**	**Maximum Ambient Temperature**	**Thermal Resistance (q_{JA})**	**Maximum Ambient Temperature**
0 MPS	29°C/W	62.9°C	22°C/W	77.9°C
0.5 MPS	24°C/W	73.6°C	17°C/W	88.6°C
1.0 MPS	22°C/W	77.9°C	15°C/W	92.9°C

Table 36 : Power Dissipation = 1.65W @ 3.3V, 65MHz, 75% Data Switching, 25.1% display blanking, C_L=10pF, and 125°C Die Junction Temp

	gmZ1CQ4		gmZ1CH2	
Air Flow in metres/sec	**Thermal Resistance (q_{JA})**	**Maximum Ambient Temperature**	**Thermal Resistance (q_{JA})**	**Maximum Ambient Temperature**
0 MPS	29°C/W	77.1°C	22°C/W	88.7°C
0.5 MPS	24°C/W	85.4°C	17°C/W	96.9°C
1.0 MPS	22°C/W	88.7°C	15°C/W	100.2°C

AC CHARACTERISTICS

The minimum and maximum operating conditions used were:

CQ4: T_{DIE} = 0 to 125 °C, EH2: T_{DIE} = -40 to 125 °C
Vdd = 3.0 to 3.6 V
Process = best to worst
C_L = 16 pF for all outputs

All timing measured to 1.5V logic switching threshold.

Table 37: VGA & VGB Port Timing

Parameter	Symbol	MIN	TYP	MAX	Units
VGACLK/VGBCLK RGB mode operating frequency (IP_RGB_EN = '1')	F_{VGXCLK}			84	MHz
VGBCLK/YUV mode operating frequency (IP_RGB_EN = '0')	F_{YUVCLK}			45	MHz
VGACLK/VGBCLK duty cycle	D_{VGXCLK}	40		60	%
Propagation delay from VGACLK/VGBCLK to IPCLKO	T_{IPCLKO}	3.0	-	10	ns
VGACREF/VGBCREF to VGACLK/VGBCLK Setup	T_{CREFS}	4	-	-	ns
VGACREF/VGBCREF from VGACLK/VGBCLK Hold	T_{CREFH}	0.5	-	-	ns
VGAVS/VGAHS to VGACLK Setup	T_{VHAS}	4.4	-	-	ns
VGAVS/VGAHS from VGACLK Hold	T_{VHAH}	0	-	-	ns
VGAVS/VGAHS minimum pulse width, in VGACLKs	T_{VGAXS}	1	-	-	Clocks
VGBVS/VGBHS to VGBCLK Setup	T_{VHBS}	3.0	-	-	ns
VGBVS/VGBHS from VGBCLK Hold	T_{VHBH}	0.5	-	-	ns
VGBVS/VGBHS minimum pulse width, in VGBCLKs	T_{VGBXS}	1	-	-	Clocks
VGAGRN/RED/BLU[7:0]/VGBGRN/RED/BLU[7:0] to VGACLK/VGBCLK Setup	T_{VGXS}	4	-	-	ns
VGAGRN/RED/BLU[7:0]/VGBGRN/RED/BLU[7:0] from VGACLK/VGBCLK Hold	T_{VGXH}	0	-	-	ns
VCODD to VGACLK/VGBCLK Setup	T_{ODDS}	4	-	-	ns
VCODD from VGACLK/VGBCLK Hold	T_{ODDH}	0	-	-	ns
$\overline{\text{DFSYNC}}$ to VGACLK/VGBCLK Setup	$T_{DFSYNCS}$	4	-	-	ns
$\overline{\text{DFSYNC}}$ from VGBCLK/VGACLK Hold	$T_{DFSYNCH}$	0	-	-	ns
Propagation delay from VGACLK/VGBCLK to $\overline{\text{VCLREQ}}$	T_{LREQ}	2.5	-	9	ns
Propagation delay from VGACLK/VGBCLK to $\overline{\text{VCBLNK}}$	T_{BLNK}	2.5	-	9	ns

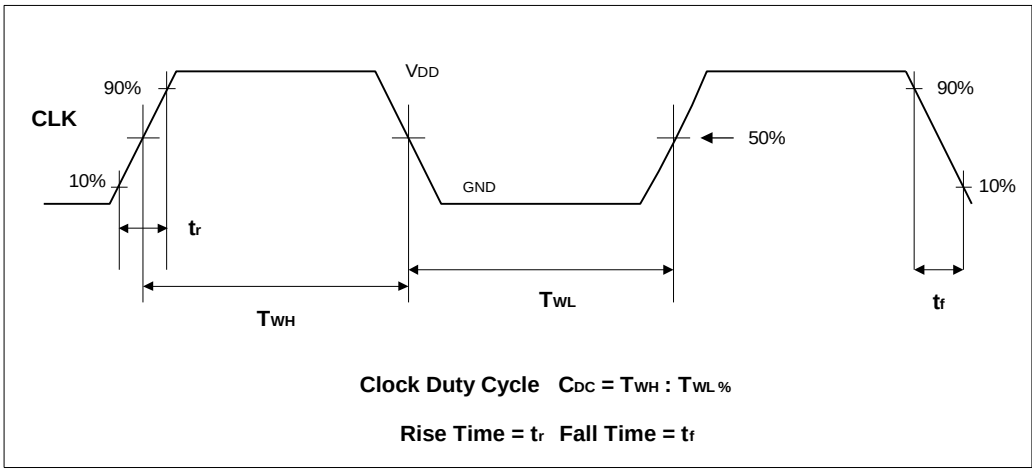


Figure 41: Clock Reference Levels

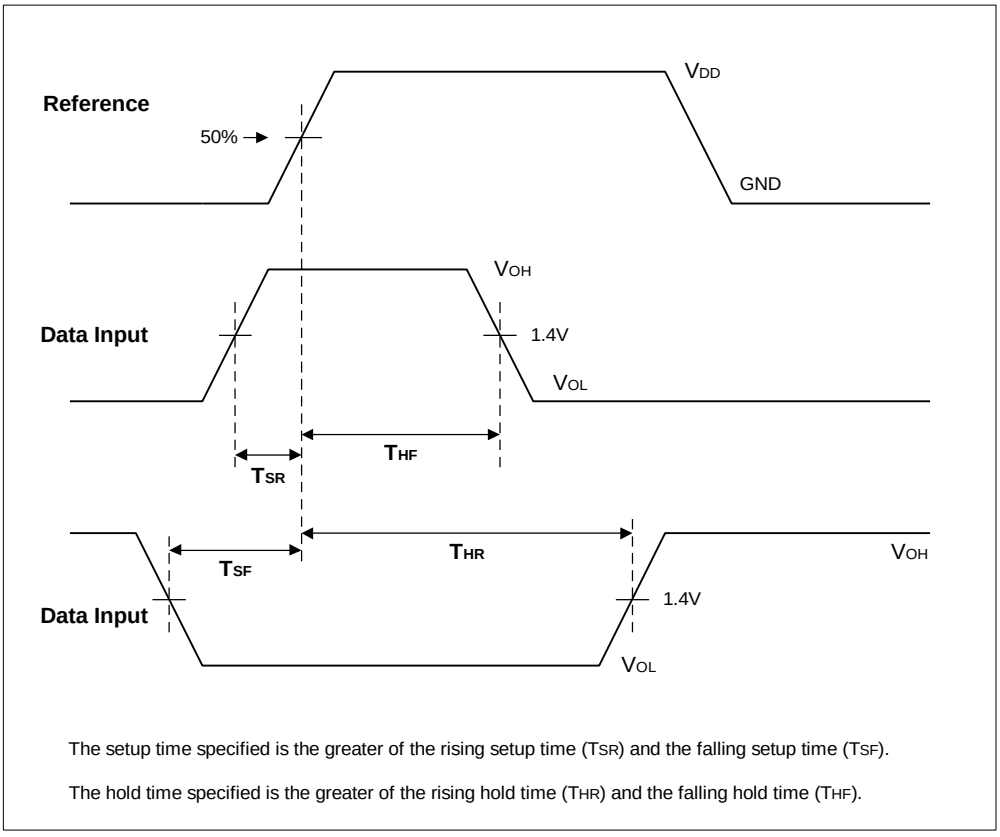


Figure 42: Setup and Hold Reference Levels

Figure 43: VGA & VGB Port Timing

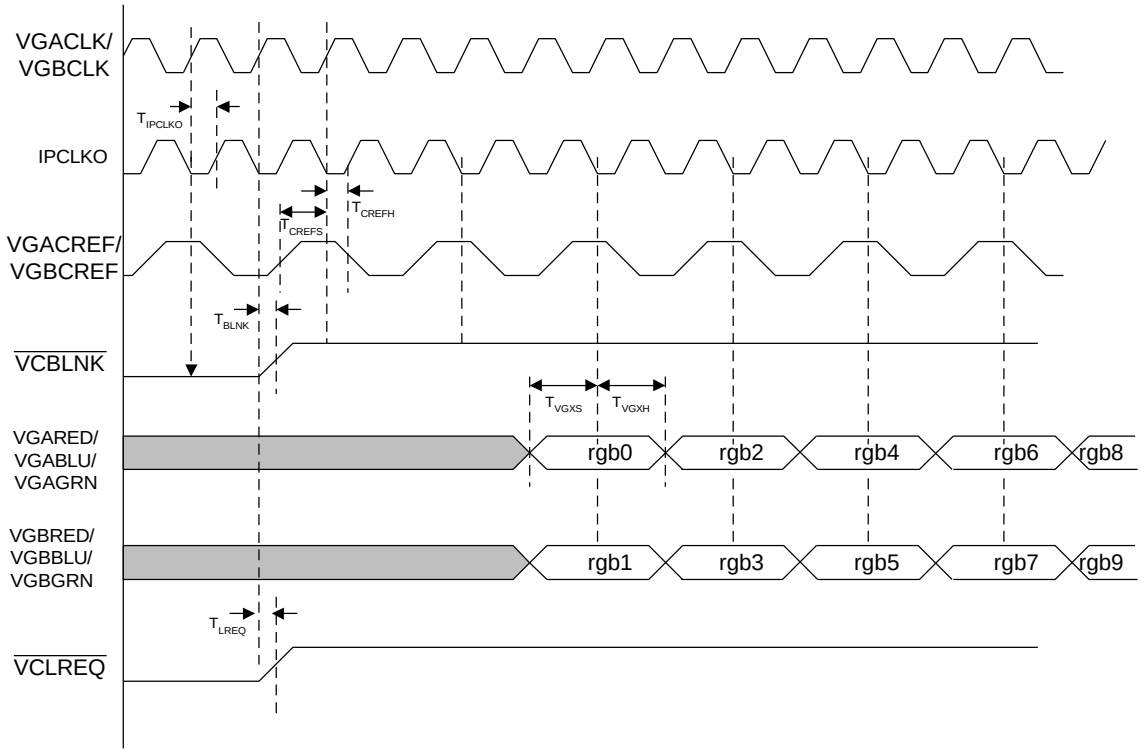
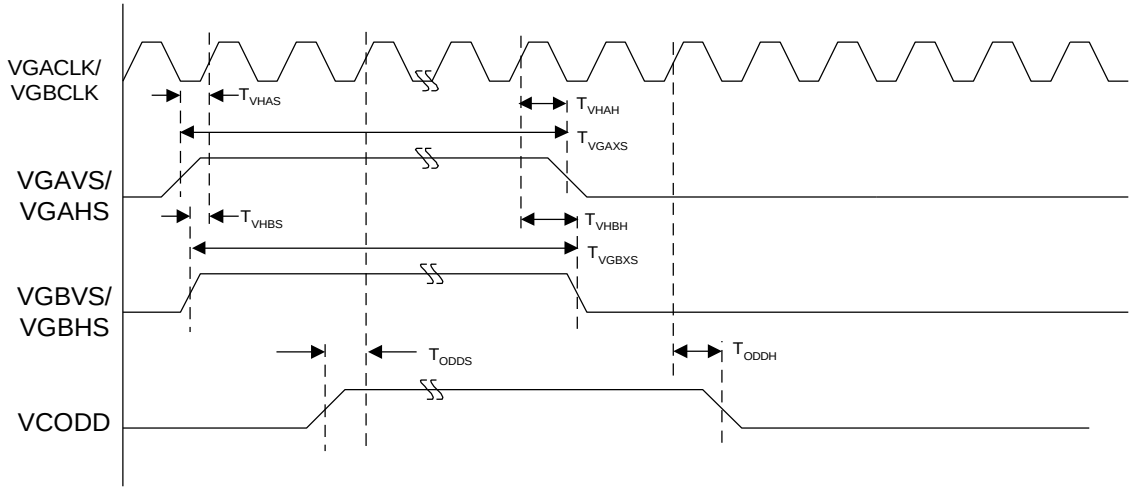


Figure 44: VGA & VGB Port Timing

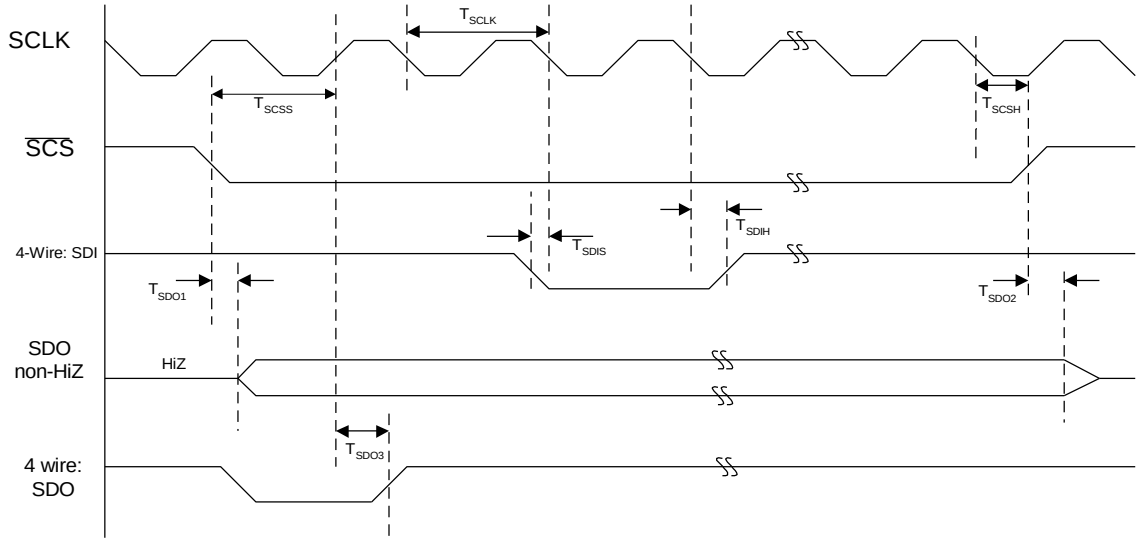


(VGACREF/ VGBCREF signals are active)

Table 38: Host I/F Port Timing

Parameter	Symbol	MIN	TYP	MAX	Units
SCLK Period	T_{SCLK}	50	-	-	ns
SCLK Duty Cycle	D_{SCLK}	40	-	60	%
$\overline{SCS}$ to SCLK Setup	T_{SCSS}	25	-	-	ns
$\overline{SCS}$ from SCLK Hold	T_{SCSH}	25	-	-	ns
SDI to SCLK Setup	T_{SDIS}	10	-	-	ns
SDI from SCLK Hold	T_{SDIH}	1	-	-	ns
Propagation delay from $\overline{SCS}$ to SDO low impedance	T_{SDO1}	1	-	7	ns
Propagation delay from $\overline{SCS}$ to SDO high impedance	T_{SDO2}	1	-	7	ns
Propagation delay from SCLK to SDO (4 wire mode)	T_{SDO3}	3	-	17	ns
Propagation delay from SCLK, to $\overline{IRQ1}$ and $\overline{IRQ2}$	T_{IRQ1}	3	-	23	ns
Propagation delay from VGBCLK, VGACLK to $\overline{IRQ1}$ and $\overline{IRQ2}$	T_{IRQ2}	3	-	23	ns
Propagation delay from DCLK to $\overline{IRQ1}$ and $\overline{IRQ2}$	T_{IRQ3}	3	-	23	ns
Propagation delay from $\overline{DOE}$ to high impedance on Display Port Outputs	T_{DOE1}	1	-	7	ns
Propagation delay from $\overline{DOE}$ to low impedance on Display Port Outputs	T_{DOE2}	1	-	7	ns
Propagation delay from $\overline{DOE}$ to Valid Data on Display Port Outputs	T_{DOE3}	2.5	-	15	ns

Figure 45: 4-Wire Mode Host I/F Timing



Note: This table assumes SCLKPOL = '1'

Table 39: Overlay Port Timing

Parameter	Symbol	MIN	TYP	MAX	Units
OVENA/OVENB to OVCLK Setup	T_{OVENXS}	5.5	-	-	ns
OVENA/OVENB from OVCLK Hold	T_{OVENXH}	0	-	-	ns
OVCOLA[2:0] to OVCLK Setup	$T_{OVCOLAS}$	5.5	-	-	ns
OVCOLA[2:0] from OVCLK Hold	$T_{OVCOLAH}$	0	-	-	ns
OVCOLB[2:0] to OVCLK Setup	$T_{OVCOLBS}$	5.5	-	-	ns
OVCOLB[2:0] from OVCLK Hold	$T_{OVCOLBH}$	0	-	-	ns
Propagation delay from DREFCLK1 or DREFCLK2 to OVCLK	T_{OVCLK}	2.5	-	8.5	ns
Propagation delay from OVCLK to $\overline{\text{OVSYNC}}$	T_{OVSYNC}	3	-	12	ns
Propagation delay from OVCLK to $\overline{\text{OVACTIV1/2}}$	$T_{OVACTIV1/2}$	3	-	12	ns

Figure 46: Overlay Port Timing

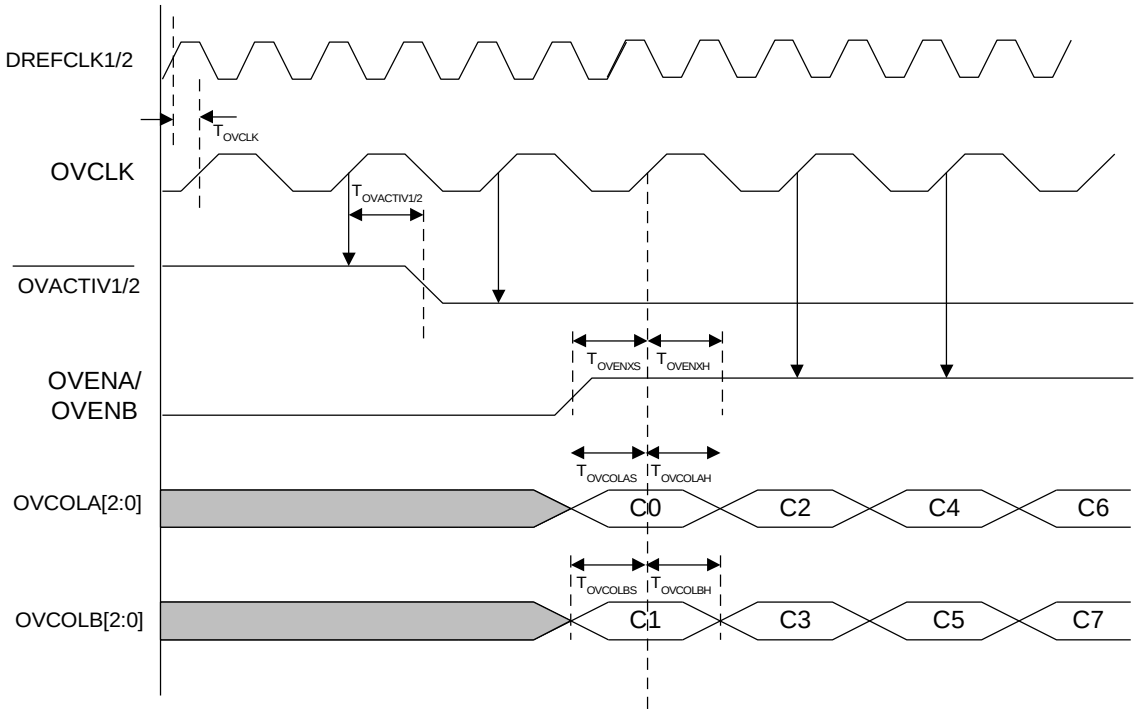


Table 40: Miscellaneous Inputs Timing

Parameter	Symbol	MIN	TYP	MAX	Units
Input Frequency DREFCLK1 and DREFCLK2	f_{CLK}	0		84	MHz
Input Rise Time (All Inputs)	t_r			3.0	ns
Duty Cycle DREFCLK1 and DREFCLK2	t_{DUTY}	40	50	60	%
DLOCK - min low pulse width		10	-	-	ns

Table 41: Single Pixel Mode Display Port Timing

Parameter	Symbol	MIN	TYP	MAX	Units
Propagation delay from DREFCLK1 or DREFCLK2 to DCLK(1)	T_{DCLK1}	4.5	-	14.5	ns
Propagation delay from DCLK to DHCLK (1)	T_{DHCLK1}	0.3	-	3.0	ns
Propagation delay from DCLK to DVS (1)	T_{DDVS1}	1.0	-	6.5	ns
Propagation delay from DCLK to DHS (1)	T_{DDHS1}	1.0	-	6.5	ns
Propagation delay from DCLK to DEN (1)	T_{DDEN1}	1.0	-	6.5	ns

Parameter	Symbol	MIN	TYP	MAX	Units
Propagation delay from DCLK to DARED/DAGRN/DABLU[7:0](1)	T_{DDA1}	0.8	-	6.5	ns
Propagation delay from DCLK to DBRED/DBGRN/DBBLU[7:0](3)	T_{DDB1}	-	-	-	ns

Note:

1. *DHCLK_PHASE = 0; DCLK_PHASE[1:0] = 00; DHCLK_INV = 0; DCLK_INV = 0*
2. *DCLK phase can be adjusted relative to data and control outputs using the DCLK_INV and DCLK_PHASE[1:0] programmable controls.*
3. *DBRED/DBGRN/DBBLU[7:0] are static at logic "0" during single wide display output.*

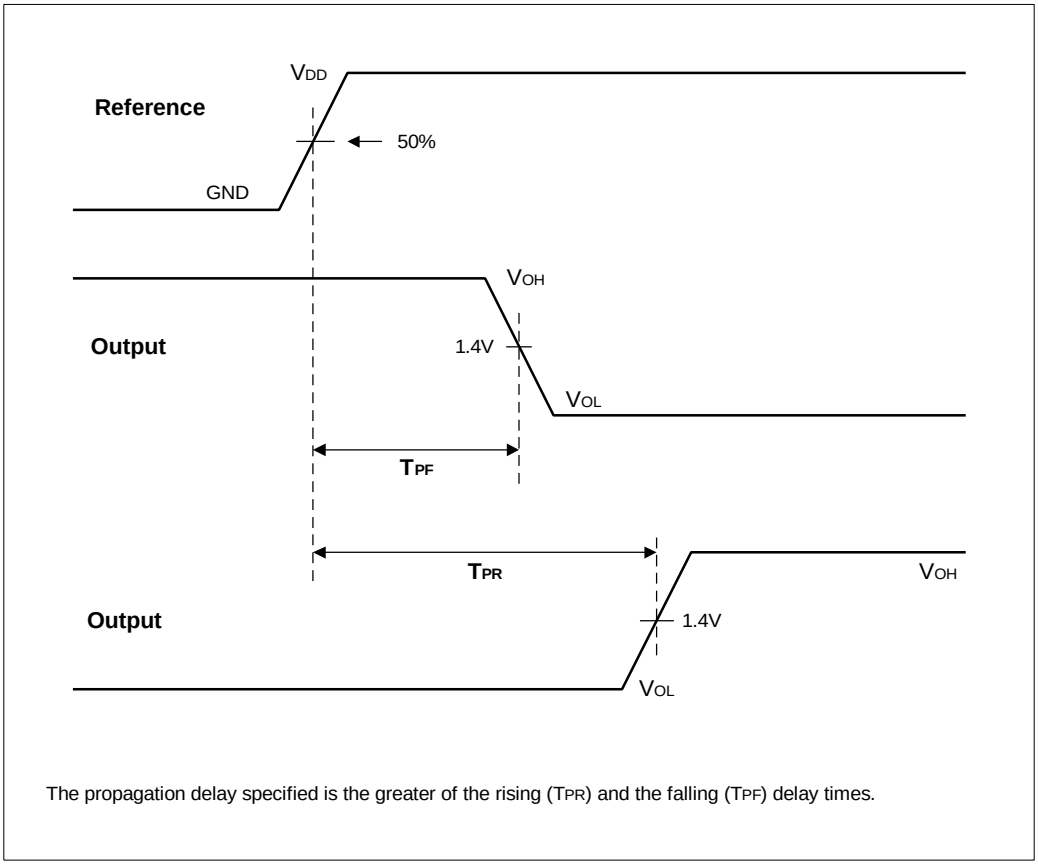


Figure 47: Propagation Delay Reference Levels

Figure 48: Single Pixel Display Port Timing

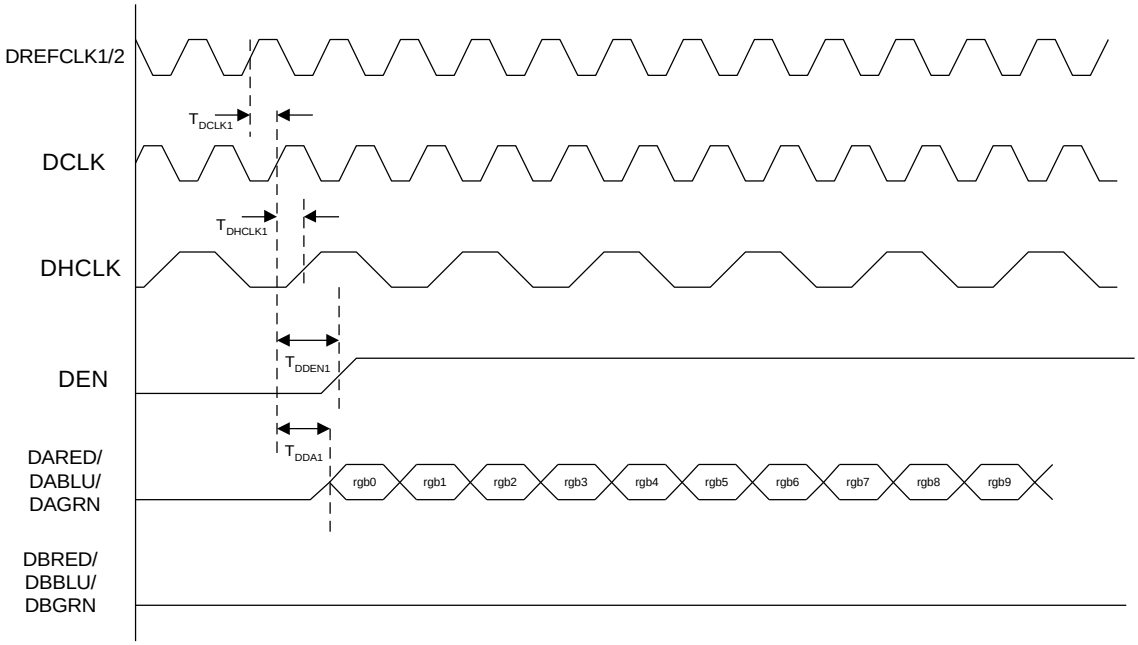


Figure 49: Display Port Timing

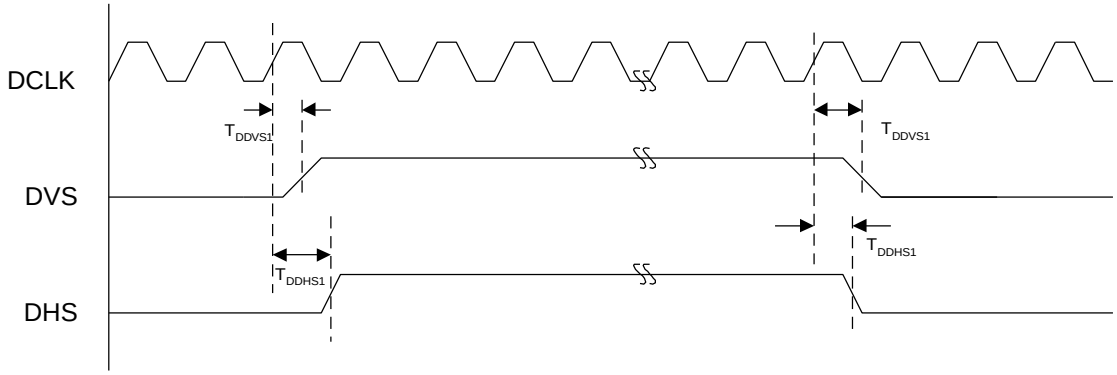


Table 42: Display Port Timing - DCLK_PHASE[1:0]

PIN NAME	Symbol	PARAMETER	MIN	TYP	MAX	Units
DCLK	$T_{PHASE00}$	DCLK_PHASE[1:0] = 00 DCLK reference clock	-		-	ns
DCLK	$T_{PHASE10}$	Incremental DCLK phase advance for DCLK_PHASE = 10 relative to DCLK_PHASE = 00	0.6	-	1.9	ns
DCLK	$T_{PHASE01}$	Incremental DCLK phase advance for DCLK_PHASE = 01 relative to DCLK_PHASE = 00	0.9	-	2.9	ns
DCLK	$T_{PHASE11}$	Incremental DCLK phase advance for DCLK_PHASE = 11 relative to DCLK_PHASE = 00	1.4	-	4.4	ns

Note: When DCLK_PHASE is set to a value other than '00' then DCLK output occurs earlier by the amount shown in the above table. Therefore, all other display port output timing minimum values are increased by the corresponding minimum value of the above table. Also all other display port output timing maximum values are increased by the corresponding maximum value of the above table.

Figure 50: Display Port Timing - DCLK_PHASE[1:0]

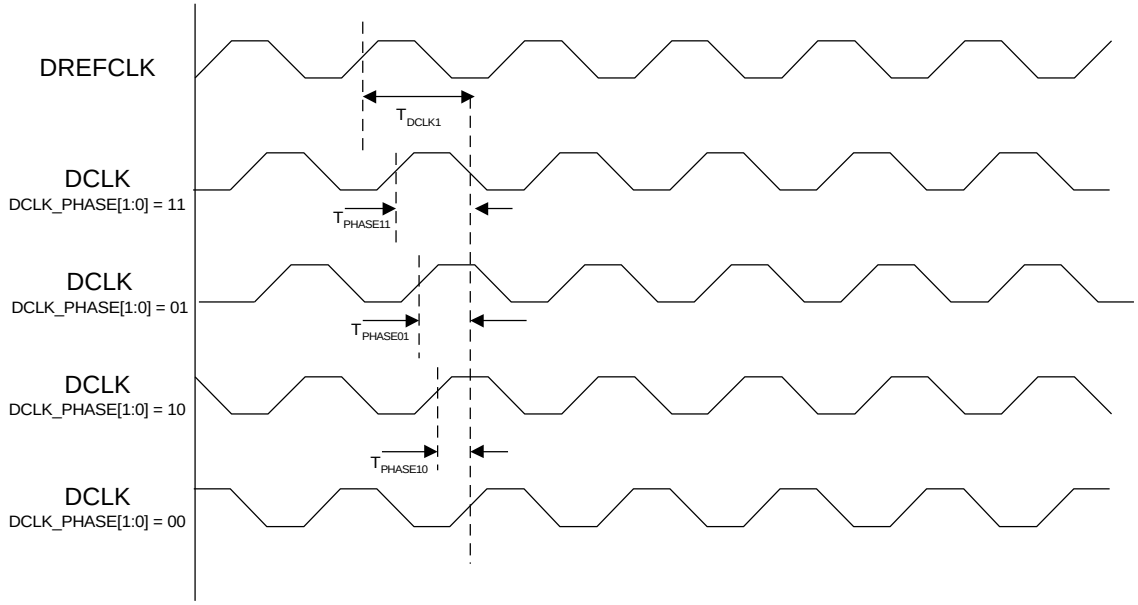


Table 43: Double Pixel Mode Display Port Timing

Parameter	Symbol	MIN	TYP	MAX	Units
Propagation delay from DREFCLK1/DREFCLK2 to DCLK	T_{DCLK1}	4.5	-	14.5	ns
Propagation delay from DCLK to DHCLK (1)	T_{DHCLK1}	0.3	-	3	ns
Propagation delay from DHCLK to DVS (1)	T_{DDVS2}	0.5	-	4.0	ns
Propagation delay from DHCLK to DHS (1)	T_{DDHS2}	0.5	-	4.0	ns
Propagation delay from DHCLK to DEN (1)	T_{DDEN2}	0.5	-	4.0	ns
Propagation delay from DHCLK to DARED/DAGRN/DABLU[7:0](1)	T_{DDA2}	0.3	-	4.0	ns
Propagation delay from DHCLK to DBRED/DBGRN/DBBLU[7:0](1)	T_{DDB2}	1.0	-	5.5	ns

Note:

1. *DHCLK_PHASE = 0; DHCLK_INV = 0; DCLK_PHASE = 00; DCLK_INV = 0*
2. *DHCLK_PHASE can be adjusted relative to data and control outputs using the DHCLK_PHASE and DHCLK_INV programmable control bits. DHCLK phase is programmable in ½ DCLK period increments.*

Figure 51: Double Pixel - Display Port Timing

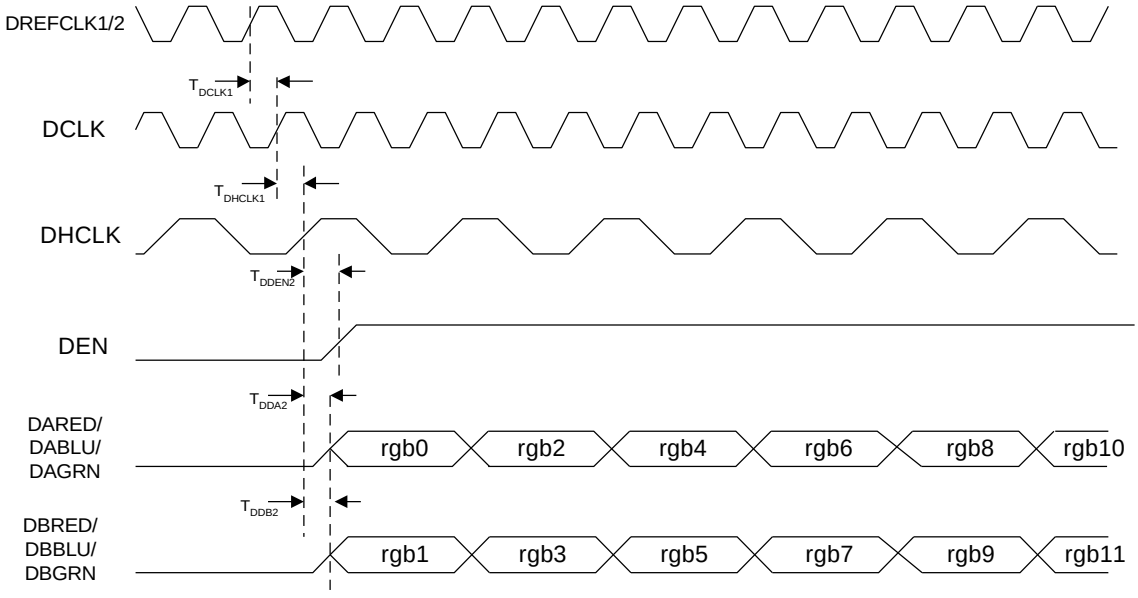
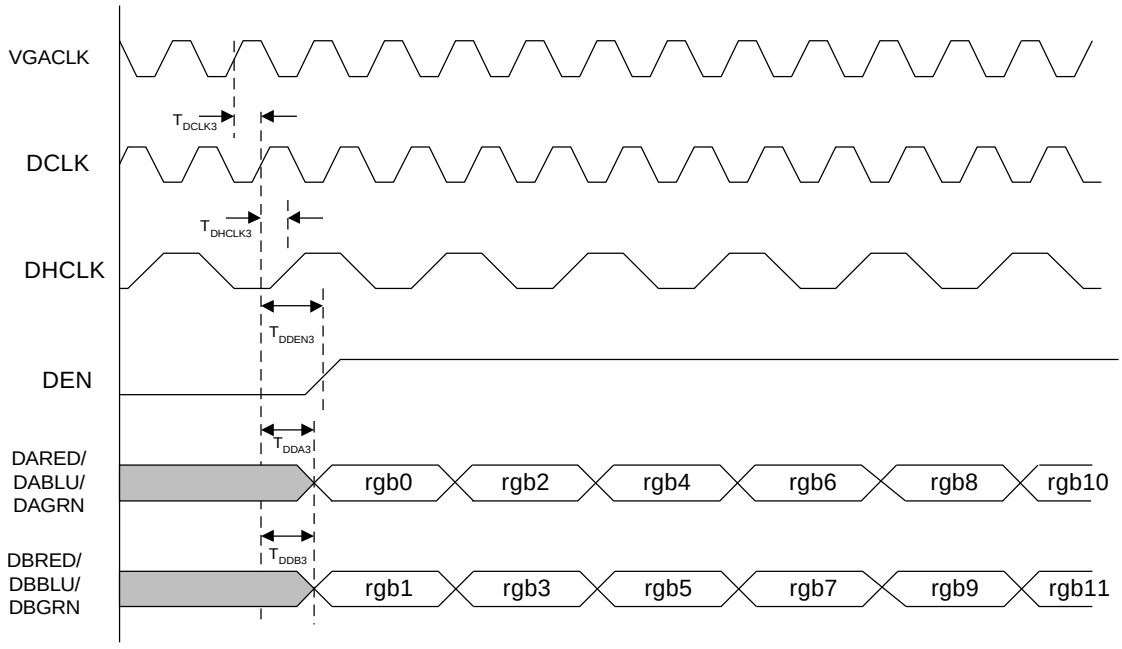


Table 44: Display Port Timing - D_Bypass Mode

PIN NAME	Symbol	MIN	TYP	MAX	Units
Propagation delay from VGACLK to DCLK	T_{DCLK3}	3.5	-	11	ns
Propagation delay from DCLK to DHCLK	T_{DHCLK3}	0.5	-	4.5	ns
Propagation delay from DCLK to DVS	T_{DDVS3}	1.5	-	8.1	ns
Propagation delay from DCLK to DHS	T_{DDHS3}	1.5	-	8.1	ns
Propagation delay from DCLK to DEN	T_{DDEN3}	1.5	-	8.1	ns
Propagation delay from DCLK to DARED/DAGRN/DABLU[7:0]	T_{DDA3}	1.5	-	8	ns
Propagation delay from DCLK to DBRED/DBGRN/DBLU[7:0]	T_{DDB3}	2.0	-	10	ns

Figure 52: By-Pass Mode - Display Port Timing



7. Ordering Information

Order Code [1]	Package	Speed	Package Marking [3] Trace Code
gmZ1 CQ4-65	208-pin PQFP 28 x 28 (mm)	65 MHz	AQ4B
gmZ1 CH2-84	208-pin PQFP with Heat Slug 28 x 28 (mm)	84 MHz	AH2B
gmZ1 EH2 [2]	208-pin PQFP with Heat Slug 28 x 28 (mm)	84MHz	AH2B "-E" also marked

(1) Order code: gmZ1 T PN - nn

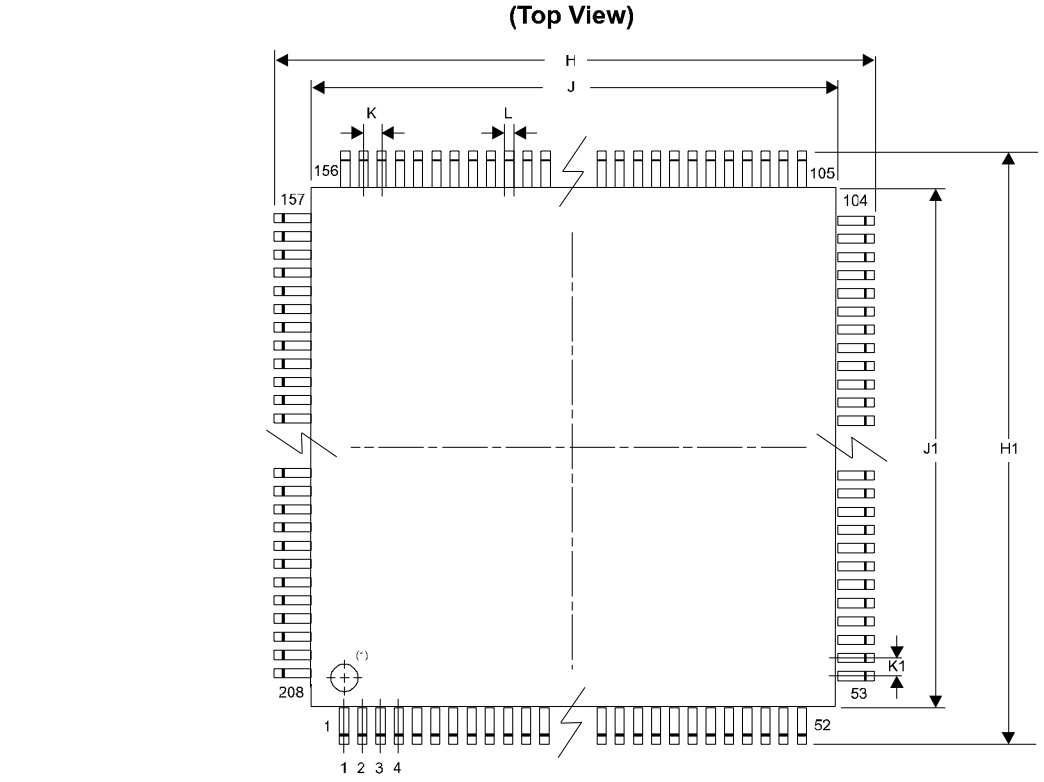
- Speed - 65MHz or 84MHz
- Package code: Q4 = Standard PQFP; H2 = MHS-PQFP (heat slug)
- Genesis device #
- "T" - Temperature Grade:
  - C = Commercial 0 °C - 70°C
  - E = Enhanced -40 °C to 85°C

(2) For enhanced temperature grade parts, the default speed is 84 MHz, provided the die junction operating temperature does not exceed 125 °C.

(3) The four digit Alphanumeric Genesis-assigned trace code (marked on the package) consists of a first letter (die revision, "A" for revision 1) and last letter code which is dependent upon wafer fab and assembly location. The second and third characters are for package type (Q4, H2) as stated in Note 1.

8.Mechanical Specifications

Figure 53: Q4 Package (208-Pin PQFP)

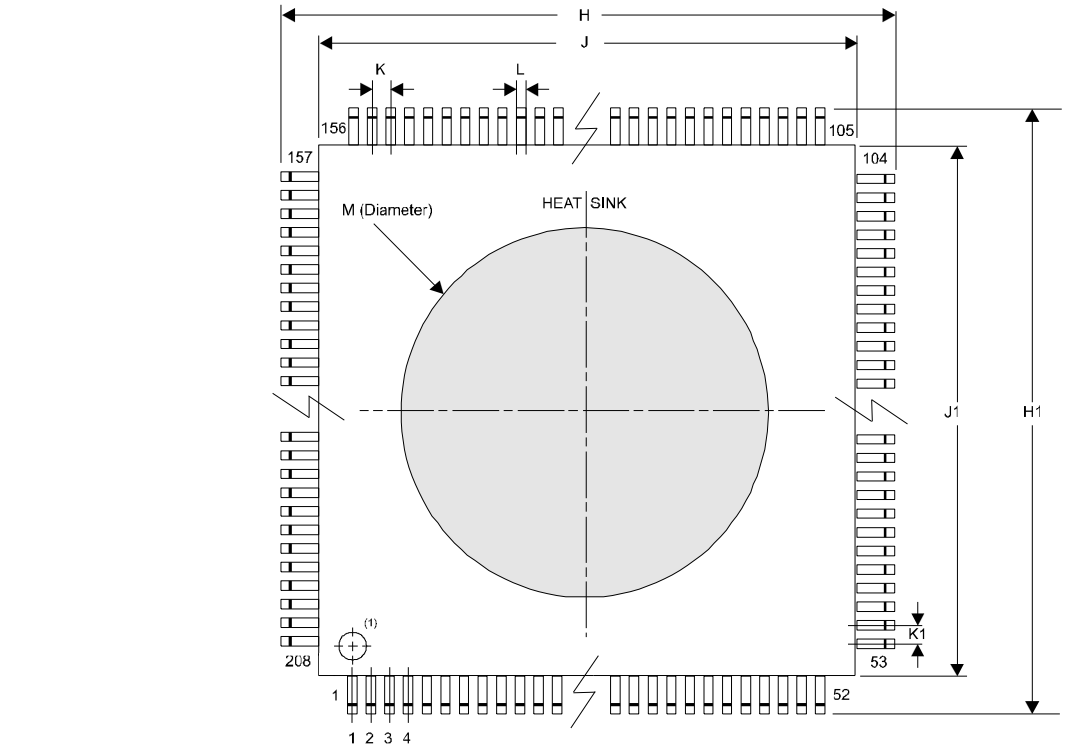


	Milimetres			Inches		
	Min	Nom	Max	Min	Nom	Max
A			4.10			0.1614
B	3.35	3.40	3.45	0.1319	0.1339	0.1358
C	0.25			0.0098		
D	0.090		0.200	0.0035		0.0079
E		1.3Ref			0.0512	
F	0.45		0.75	0.0177		0.0295
G	0°		8°	0°		8°
H	30.40	30.60	30.80	1.1969	1.2047	1.2126
J	27.80	28.00	28.20	1.0945	1.1024	1.1102
H1	30.40	30.60	30.80	1.1969	1.2047	1.2126
J1	27.80	28.00	28.20	1.0945	1.1024	1.1102
K		0.50			0.0197	
K1		0.50			0.0197	
L	0.170		0.270	0.0067		0.0106

(1) Depressed dot indicates Pin 1. One or more package corners may be cut or rounded.

Figure 54: H2 Package (208-Pin PQFP with Heat Slug)

(Top View)



	Milimetres			Inches		
	Min	Nom	Max	Min	Nom	Max
A			4.10			0.1614
B	3.35	3.40	3.45	0.1319	0.1339	0.1358
C	0.25			0.0098		
D	0.090		0.200	0.0035		0.0079
E		1.3Ref			0.0512	
F	0.45		0.75	0.0177		0.0295
G	0°		8°	0°		8°
H	30.40	30.60	30.80	1.1969	1.2047	1.2126
J	27.80	28.00	28.20	1.0945	1.1024	1.1102
H1	30.40	30.60	30.80	1.1969	1.2047	1.2126
J1	27.80	28.00	28.20	1.0945	1.1024	1.1102
K		0.50			0.0197	
K1		0.50			0.0197	
L	0.170		0.270	0.0067		0.0106
M		20.00			0.7874	

(1) Depressed dot indicates Pin 1. One or more package corners may be cut or rounded.