Data Sheet

gmFC1

DAT-0005-D

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gmFC1 Data Sheet

DAT-0005-D

Document	Revision	Incorporated Errata / Details	Release Date
DAT-0005	A	First Release	Nov. 1997
DAT-0005	B	Minor update for CD-ROM	Dec. 1997
DAT-0005	C	MSD-0025-A details major changes	March 1998
DAT-0005	D	1. 64MB memory device interface as in MSD-0038 2. Electrical Specifications finalized 3. Errata E04-0005, E05-0005 incorporated 4. I/O pads incorporate pull-down resistors as in MSD-0028 5. Various corrections and clarifications 6. Order Code changed to BR1C 7. Extended Temp. range part available	Nov. 1998

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1. Overview

The Genesis Microchip gmFC1 functions as a graphics and video frame buffer controller capable of performing frame rate conversion by replicating or dropping incoming data as necessary to maintain a set output frame rate. Frame rate conversion is required in applications where it is necessary to manage high input data rates or accommodate varying video and graphics input frame rates when using display devices operating at a fixed frame rate.

Schematically, the gmFC1 may be thought of as a control device for two circular buffers; the input buffer being write-only, and the output buffer read-only. (See Figure 1 below.) Incoming data is continuously written to the input buffer loop as it arrives. Output data is continuously read from the output buffer loop as required. If the buffers do not overlap, double buffering of data is enabled and frame tear is prevented. Although it is best to prevent frame tear whenever possible, frame tear may not be objectionable in graphics and video applications containing little motion between adjacent frames. As a rule, unless there are noticeable visual differences in successive frames, frame tear is essentially invisible. In the case of motion video, frame tear artifacts may be perceptible along areas of motion. While double buffering, the location of buffers is managed so the output consists of recently acquired input data, and the input does not overwrite output data as it is being displayed. Thus, entire frames may be dropped or replicated at the output, and an individual output frame will consist of data from only a single input frame.

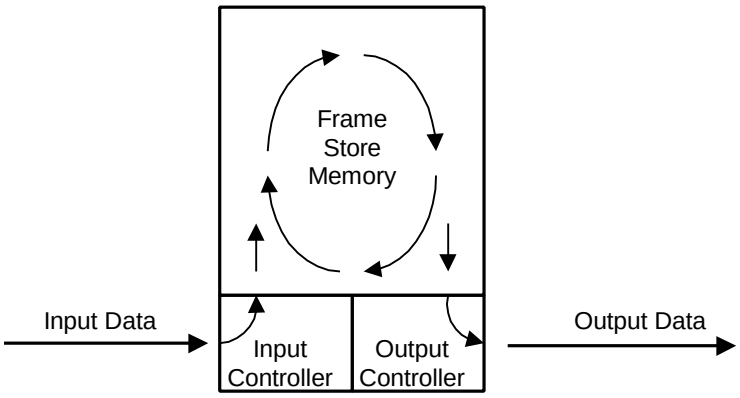


Figure 1. gmFC1 - Overlapping Circular Buffers

Figure 2 below illustrates the gmFC1 internal functional blocks and external interfaces. The data input interface is divided into separate RGB (graphics) and a YUV (video) input ports, further described in the following sections.

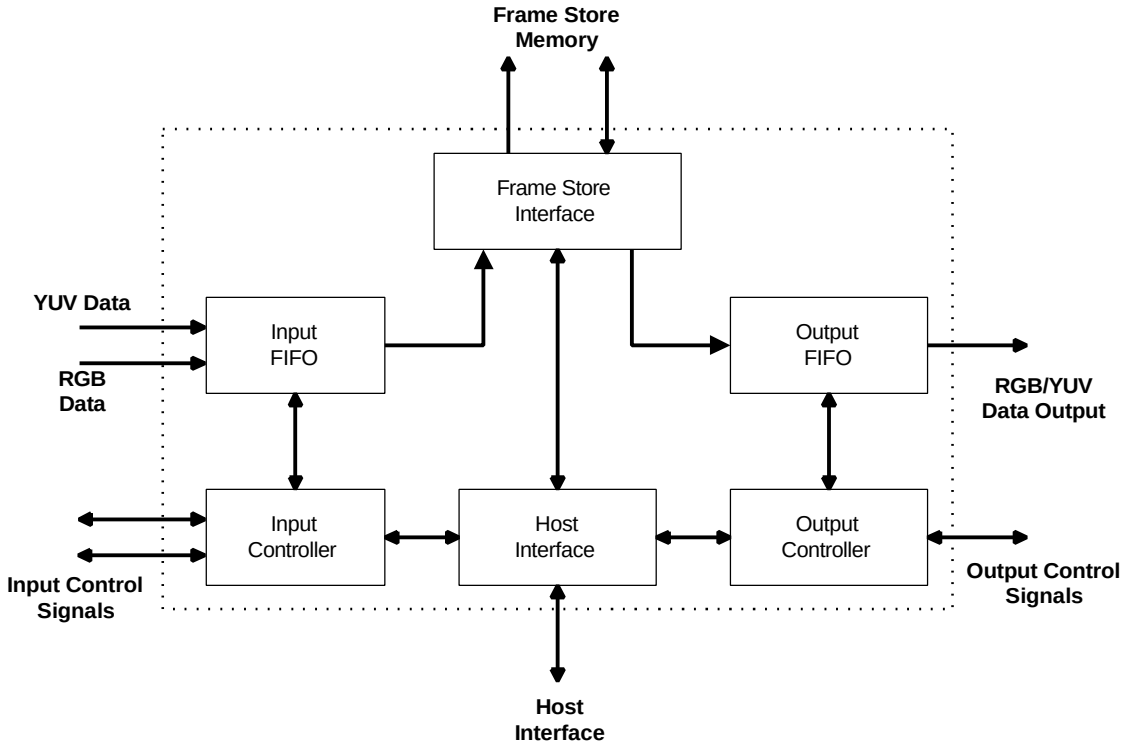


Figure 2: gmFC1 Functional Block Diagram

2. Features and Applications

Features

- 24-bit single pixel wide I/O interfaces
- Independent RGB and YUV input ports
- Supports non-interlaced and vertical / horizontal interlaced formats
- Simplifies input format detection
- Enables constant output frame rate with variable input rates
- Drops or replicates input data to maintain output frame rate
- Seamless interface to the Genesis gmZ1/Z2/Z3 zoom scaler
- Seamless interface to three external frame store 1M x 16-bit SDRAMs
- Eliminates frame tear when double buffering enabled
- Pads or truncate input lines to a programmed output image size
- Seamless interface to common RGB ADCs
- Allows 1:1 windowing of lower resolution inputs on high resolution displays
- 500Mbytes/sec I/O bandwidth
- 3.3 Volt operation, 5 Volt tolerant I/O
- 208 pin PQFP package

Input Format

- Single pixel wide input interface (selectable from independent 24-bit RGB and 16-bit YUV ports)
- Programmable to accept either sequential or interlaced pixels
- Input window cropping
- Flags Input Timing Errors - lines are padded to correct size
- Supports input formats up to 1024 x 768 at 85 Hz (95 MHz pixel clock)
  (dependent on output format - maximum total I/O bandwidth limit of ~ 500 MBytes/s)

Output Format

- Single pixel wide output interface
- Supports output formats up to 1024 x 768 at 85 Hz
  (dependent on input format - maximum total I/O bandwidth limit of ~ 500 MBytes/s)
- 24-bit RGB or 16-bit YUV - dependent on input data format
- Frame Rate Conversion
  - Output faster than input
  - Output slower than input
  - Disabled: frame rate locked to input

Host Interface

- gmZ1/Z2/Z3 compatible three or four wire serial host interface port

Frame Store Interface

- 48-bit wide path to external frame store (3 x16 SDRAM devices)
- 32-bit wide path to external frame store for YUV-only applications (2x16 SDRAM)
- Three 1M x 16-bit devices = 500 Mbytes/sec I/O data rate - 85 Hz XGA in, 60 Hz XGA out. [(85Hz XGA + 60Hz XGA) x 3 bytes/pixel]
- Compatible 1M x 16-bit, 100MHz memory devices include:

IBM	IBM0316169
Hitachi	HM216165
NEC	uPD4516161
Toshiba	TC59S1616AFT
TI	TMS626162
Samsung	KM416S1020B

- Any 4M x 16-bit (64 Mbit) device conforming to SDRAM standards may also interface to the gmFC1. Compatible 4M x 16-bit SDRAM devices include:

Toshiba	TC59S6416BFT-10
Mitsubishi	MB611641642A-100FN
Samsung	KM416S4030BT-GB

Applications

- Accommodates BIOS and various Windows frame rates during Windows boot up sequence:
  BIOS Screen - 720x400 text mode, 70 Hz
  Windows 95 Boot Up Screen Graphics - 640x480 16-color mode, 60 Hz
  Windows Environment - User selectable, VGA, SVGA, XGA, etc.
- Manage high input data rates by reducing frame rates
- Manage various input frame rates to support fixed frame rate O/P such as LCD panels, ex: XGA, PAL, RGB, VESA proposed 85 Hz Standards, older DOS screens @ 70 and 85 Hz, MAC standard formats
- Games preferring low resolutions
- Special effects using frame buffer, ex: cropped zooms, freeze frame, 1:1 windowing
- Simplified FRC designs
- System cost reduction in applications ordinarily requiring expensive variable refresh LCD panels

3. General Operation

The gmFC1 is designed to simplify frame rate conversion of both graphics and digital video (YUV) data, allowing a variety of input formats to be interfaced to a single format display device. Frame rates may be reduced or increased to accommodate the output display. Figure 3 below shows the frame rate reduction and frame replication process, where each horizontal segment represents an entire two dimensional frame. In this example, double buffering is enabled and no frame tearing occurs.

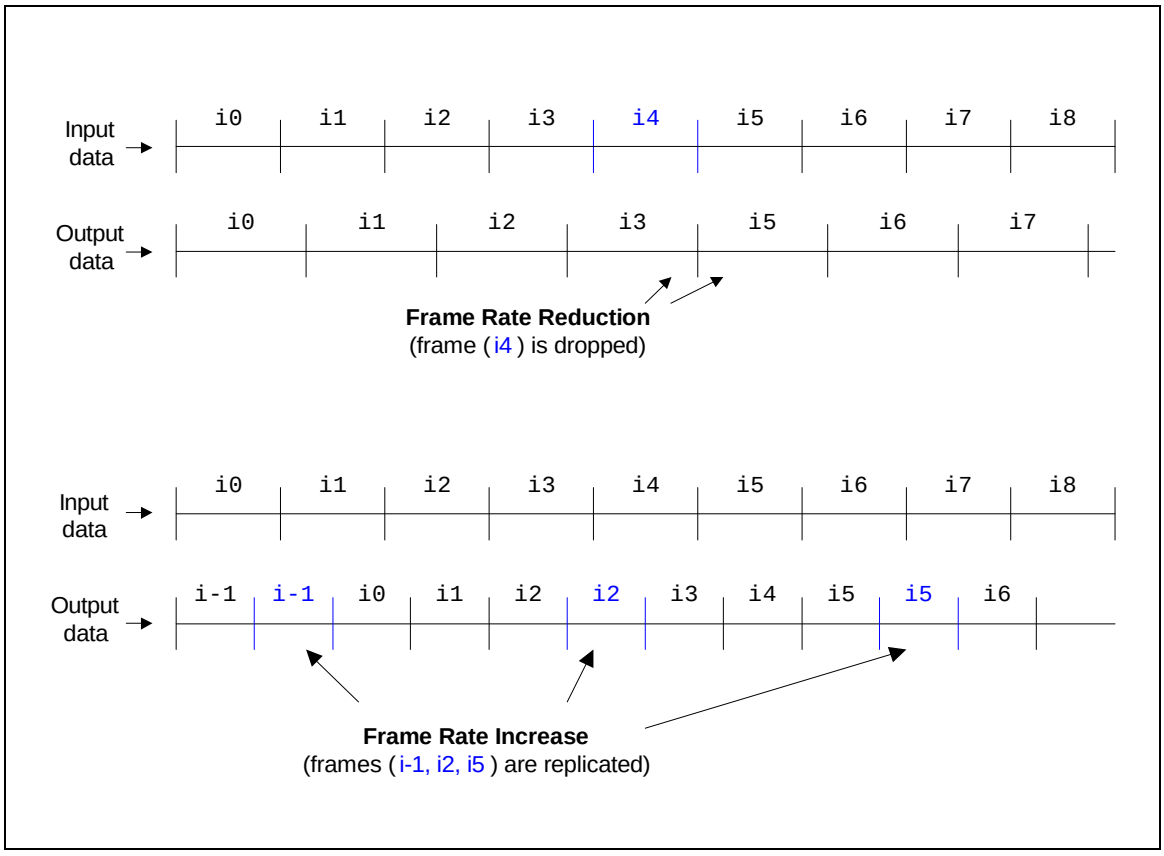


Figure 3. Frame Rate Conversion Process

3.1 Typical Systems

In a typical system, the gmFC1 is seamlessly interfaced to an SDRAM based frame store, input ADC, and the Genesis gmZ1/Z2/Z3 for output to an LCD display panel (see Figure 4 below). The gmFC1 provides data as required by the gmZ1/Z2/Z3 to sustain the programmed display timing. The gmZ1/Z2/Z3 operates in Free Run Mode, with all required display timing programmed into its display register set. (Frame Lock mode is also possible, although it is recommended only for applications where frame dropping/duplication is not desired.) A shared microcontroller oversees all frame rate conversion, image scaling operations and input format detection through a compatible three or four wire serial host interface.

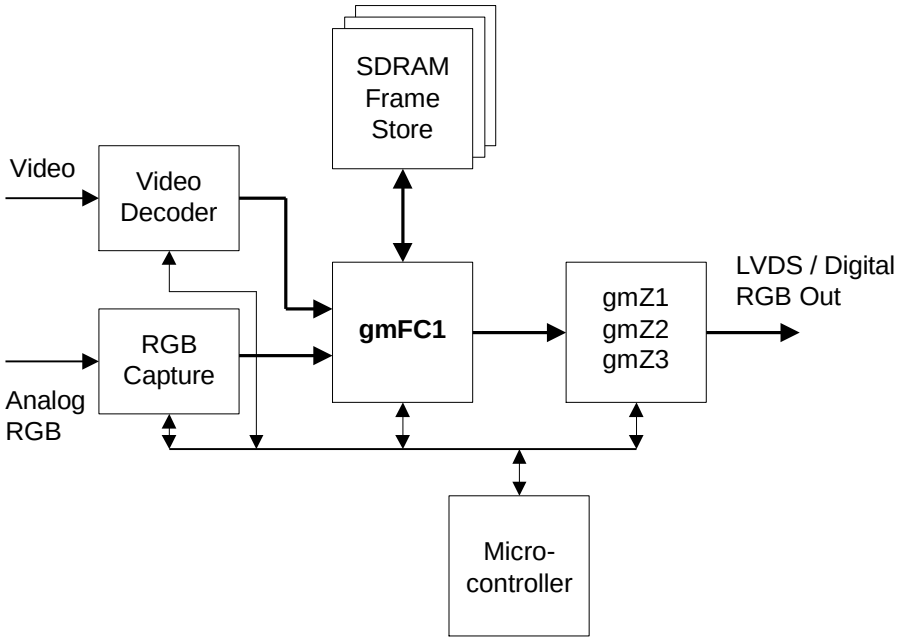


Figure 4: Typical gmFC1 Implementation

4. Pinout

4.1 gmFC1 Pinout- Chip Diagram

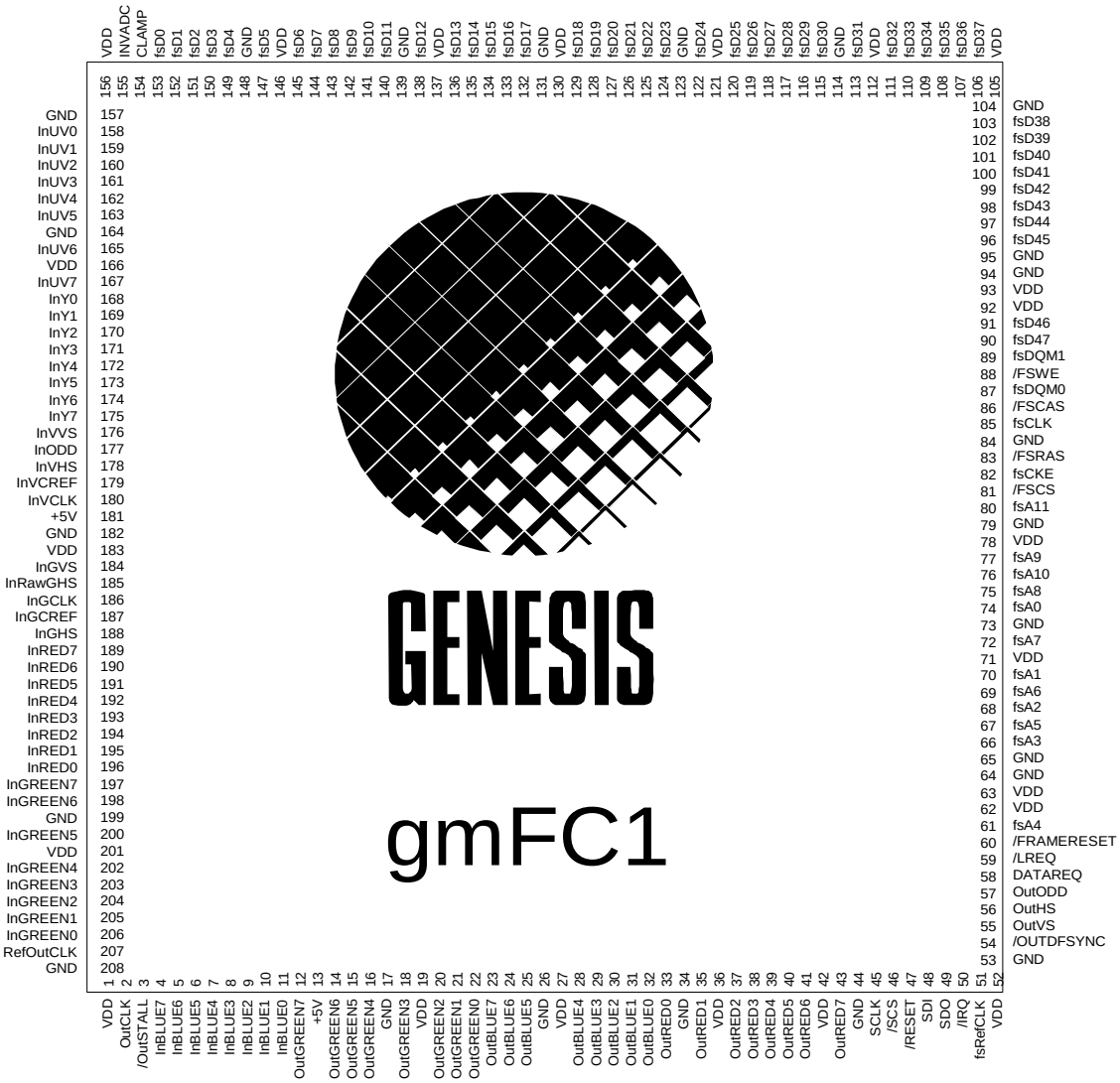


Figure 5: gmFC1 Pinout

4.2 gmFC1 Pinout- Pin List

Table 1 below lists each gmFC1 pin, and provides a concise description of each signal. A detailed signal description may be found on the page listed in the Page column.

Table 1: gmFC1 Pinout Description

Input Interface				
Pin #	**Signal Name**	**I/O**	**Page**	**Brief Description**
4	InBlue7	I (pull-down)	23	Input RGB BLUE data MSB
5	InBlue6	I (pull-down)	23	Input RGB BLUE data
6	InBlue5	I (pull-down)	23	Input RGB BLUE data
7	InBlue4	I (pull-down)	23	Input RGB BLUE data
8	InBlue3	I (pull-down)	23	Input RGB BLUE data
9	InBlue2	I (pull-down)	23	Input RGB BLUE data
10	InBlue1	I (pull-down)	23	Input RGB BLUE data
11	InBlue0	I (pull-down)	23	Input RGB BLUE data LSB
50	**INDATAACTIVE** / $\overline{\text{IRQ}}$	O	25	**Input Data Active** The $\overline{\text{INDATAACTIVE}}$ output signal indicates when the gmFC1 is expecting valid data based on the host programmed active data region registers. Interrupt Request The $\overline{\text{IRQ}}$ interrupt pin of the host interface is physically shared with $\overline{\text{INDATAACTIVE}}$. The IRQ_OUT_EN bit in the IRQMASK register controls the pin function.
154	**CLAMP** / MSBFIRST When $\overline{\text{RESET}}$ = 1, pin 154 = CLAMP When $\overline{\text{RESET}}$ = 0, pin 154 = MSBFIRST	O/I	23	The **CLAMP** output is a pulse with a programmable width and location with respect to InGHS. Can be used to indicate the point for DC restoration in analog RGB signals. The CLAMP pin is shared with: MSBFIRST, Host I/F Mode Select Input. Selects serial data (SDI/SDO) bit ordering. If = '1', the MSB is shifted first. The value is latched on the rising (negating) edge of $\overline{\text{RESET}}$.
155	**INVADC** / SCLKPOL When $\overline{\text{RESET}}$ = 1, pin 155 = INVADC When $\overline{\text{RESET}}$ = 0, pin 155 = SCLKPOL	O/I	23	Invert ADC sampling clock. (Output) **INVADC** is used in horizontal interlace mode to request the ADC to invert its sample clock. It will toggle every graphics frame when in this mode. The INVADC pin is shared with: SCLKPOL, Serial Clock Mode Select. (Input) The value is latched on the rising (negating) edge of $\overline{\text{RESET}}$. This selects the active edge of the host interface shift clock, SCLK. If 0, SDI is sampled on the SCLK rising edge and SDO is shifted out on the SCLK falling edge. Otherwise, SDI is sampled on the SCLK falling edge and

				SDO shifted out on the rising edge.
158	InUV0	I (pull-down)	25	UV Video Data Input LSB
159	InUV1	I (pull-down)	25	UV Video Data Input
160	InUV2	I (pull-down)	25	UV Video Data Input
161	InUV3	I (pull-down)	25	UV Video Data Input
162	InUV4	I (pull-down)	25	UV Video Data Input
163	InUV5	I (pull-down)	25	UV Video Data Input
165	InUV6	I (pull-down)	25	UV Video Data Input
167	InUV7	I (pull-down)	25	UV Video Data Input MSB
168	InY0	I (pull-down)	25	Y Video Data Input LSB
169	InY1	I (pull-down)	25	Y Video Data Input
170	InY2	I (pull-down)	25	Y Video Data Input
171	InY3	I (pull-down)	25	Y Video Data Input
172	InY4	I (pull-down)	25	Y Video Data Input
173	InY5	I (pull-down)	25	Y Video Data Input
174	InY6	I (pull-down)	25	Y Video Data Input
175	InY7	I (pull-down)	25	Y Video Data Input MSB
176	InVVS	I (pull-down)	25	YUV Port Vertical Sync Input
177	InODD	I (pull-down)	26	ODD field indicator in interlaced mode
178	InVHS	I (pull-down)	25	YUV Port Horizontal Sync Input
179	InVCRef	I (pull-down)	24	InVCLK YUV clock qualifier
180	InVClk	I (pull-down)	24	YUV Port Clock
184	InGVS	I (pull-down)	23	RGB Port Vertical Sync Input
185	InRawGHS	I (pull-down)	20	Raw Horizontal Sync source input from ADC
186	InGClk	I (pull-down)	18	RGB Port Clock
187	InGCRef	I (pull-down)	19	InGCLK RGB clock qualifier
188	InGHS	I	19	RGB Port Horizontal Sync Input
189	InRed7	I (pull-down)	23	Input RGB RED data MSB
190	InRed6	I (pull-down)	23	Input RGB RED data
191	InRed5	I (pull-down)	23	Input RGB RED data
192	InRed4	I (pull-down)	23	Input RGB RED data
193	InRed3	I (pull-down)	23	Input RGB RED data
194	InRed2	I (pull-down)	23	Input RGB RED data
195	InRed1	I (pull-down)	23	Input RGB RED data
196	InRed0	I (pull-down)	23	Input RGB RED data LSB
197	InGreen7	I (pull-down)	23	Input RGB GREEN data MSB
198	InGreen6	I (pull-down)	23	Input RGB GREEN data
200	InGreen5	I (pull-down)	23	Input RGB GREEN data
202	InGreen4	I (pull-down)	23	Input RGB GREEN data
203	InGreen3	I (pull-down)	23	Input RGB GREEN data
204	InGreen2	I (pull-down)	23	Input RGB GREEN data
205	InGreen1	I (pull-down)	23	Input RGB GREEN data
206	InGreen0	I (pull-down)	23	Input RGB GREEN data LSB

Note: I (pull-down): Indicates that these gmFC1 inputs are provided with internal pull-down resistors typically valued at 91Kohm.

Output Interface				
Pin #	**Signal Name**	**I/O**	**Page**	**Description**
2	OutClk	O	32	Clock driving gmZ1/2/3. Based on RefOutCLK.
3	$\overline{\text{OUTSTALL}}$	O	33	Stall control to gmZ1 / gmZ2 / gmZ3
12	OutGreen7	O	34	Output RGB GREEN data MSB
14	OutGreen6	O	34	Output RGB GREEN data
15	OutGreen5	O	34	Output RGB GREEN data
16	OutGreen4	O	34	Output RGB GREEN data
18	OutGreen3	O	34	Output RGB GREEN data
20	OutGreen2	O	34	Output RGB GREEN data
21	OutGreen1	O	34	Output RGB GREEN data
22	OutGreen0	O	34	Output RGB GREEN data LSB
23	OutBlue7	O	34	Output RGB BLUE data MSB / Output UV MSB
24	OutBlue6	O	34	Output RGB BLUE data / Output UV
25	OutBlue5	O	34	Output RGB BLUE data / Output UV
28	OutBlue4	O	34	Output RGB BLUE data / Output UV
29	OutBlue3	O	34	Output RGB BLUE data / Output UV
30	OutBlue2	O	34	Output RGB BLUE data / Output UV
31	OutBlue1	O	34	Output RGB BLUE data / Output UV
32	OutBlue0	O	34	Output RGB BLUE data LSB / Output UV LSB
33	OutRed0	O	34	Output RGB RED data LSB / Output Y LSB
35	OutRed1	O	34	Output RGB RED data / Output Y
37	OutRed2	O	34	Output RGB RED data / Output Y
38	OutRed3	O	34	Output RGB RED data / Output Y
39	OutRed4	O	34	Output RGB RED data / Output Y
40	OutRed5	O	34	Output RGB RED data / Output Y
41	OutRed6	O	34	Output RGB RED data / Output Y
43	OutRed7	O	34	Output RGB RED data MSB / Output Y MSB
54	$\overline{\text{OUTDFSYNC}}$	O	34	Forces gmZ1/2/3 frame re-synchronization
55	OutVS	O	33	Output Vertical Sync
56	OutHS	O	33	Output Horizontal Sync
57	OutODD	O	33	Indicates interlaced output field is ODD
58	DATAREQ	I	33	Data Request - the gmFC1 will slave to requests for data at the DATAREQ pin when the OP_HANDSH register bit = 0, providing data three clock cycles after DATAREQ is asserted.
59	$\overline{\text{LREQ}}$	I	33	Line Request Input - accepts gmZ1/2/3 $\overline{\text{VCLREQ}}$
60	$\overline{\text{FRAMERESET}}$	I	32	Forces start of new output frame
207	RefOutCLK	I	32	Clock reference for output interface

Power				
Pin #	**Signal Name**	**I/O**	**Page**	**Description**
1, 19, 27, 36, 42, 52, 62, 63, 71, 78, 92, 93, 105, 112, 121, 130, 137, 146, 156, 166, 183, 201	VDD			3.3VDC
13, 181	+5V			+5VDC *
17, 26, 34, 44, 53, 64, 65, 73, 79, 84, 94, 95, 104, 114, 123, 131, 139, 148, 157, 164, 182, 199, 208	Gnd			Ground

* +5VDC supplies may be wired to 3.3VDC if no 5V tolerance on inputs is required

Host Interface				
Pin #	**Signal Name**	**I/O**	**Page**	**Description**
45	SCLK	I	40	Host Interface Serial Clock
46	$\overline{SCS}$	I	40	Serial Chip Select - Host Interface Enable
47	$\overline{RESET}$	I	40	Reset input to initialize device
48	SDI	I	41	Host Interface Serial Data Input
49	SDO	O	41	Host Interface Serial Data Output
50	**IRQ** / $\overline{INDATAACTIVE}$	O	41	Interrupt Request The **IRQ** interrupt pin of the host interface is physically shared with $\overline{INDATAACTIVE}$. The IRQ_OUT_EN bit in the IRQMASK register controls the pin function. Input Data Active The $\overline{INDATAACTIVE}$ output signal indicates when the gmFC1 is expecting valid data based on the host programmed active data region registers.
154	**MSBFIRST** / CLAMP When $\overline{RESET}$ = 1, pin 154 = CLAMP When $\overline{RESET}$ = 0, pin 154 = MSBFIRST	I/O	40	**MSBFIRST -** Host I/F Mode Select Input. Selects serial data (SDI/SDO) bit ordering. If = '1', the MSB is shifted first. The value is latched on the rising (negating) edge of $\overline{RESET}$. The MSBFIRST pin is shared with CLAMP. The CLAMP output is a pulse with a programmable width and location with respect to InGHS. Can be used to indicate the point for DC restoration in analog RGB signals.
155	**SCLKPOL** / INVADC When $\overline{RESET}$ = 1, pin 155 = INVADC When $\overline{RESET}$ = 0, pin 155 = SCLKPOL	I/O	40	**SCLKPOL -** Serial Clock Mode Select. (Input) The value is latched on the rising (negating) edge of $\overline{RESET}$. This selects the active edge of the host interface shift clock, SCLK. If 0, SDI is sampled on the SCLK rising edge and SDO is shifted out on the SCLK falling edge. Otherwise, SDI is sampled on the SCLK falling edge and SDO shifted out on the rising edge. SCLKPOL is shared with INVADC. INVADC - Invert ADC sampling clock. (Output) Used in horizontal interlace mode to request the ADC to invert its sample clock. It will toggle every InGVS when in this mode.

Frame Store Interface					
Pin #	**Signal Name**	**I/O**	**Page**	**Description**	
74	fsA0	O	38	Frame Store Address Line	
70	fsA1	O	38	Frame Store Address Line	
68	fsA2	O	38	Frame Store Address Line	
66	fsA3	O	38	Frame Store Address Line	
61	fsA4	O	38	Frame Store Address Line	
67	fsA5	O	38	Frame Store Address Line	
69	fsA6	O	38	Frame Store Address Line	
72	fsA7	O	38	Frame Store Address Line	
75	fsA8	O	38	Frame Store Address Line	
77	fsA9	O	38	Frame Store Address Line	
76	fsA10	O	38	Frame Store Address Line	
80	fsA11	O	38	Frame Store Address Line	
153	fsD0	I/O	38	Frame Store Data Line	(BLUE / UV data)
152	fsD1	I/O	38	Frame Store Data Line	(BLUE / UV data)
151	fsD2	I/O	38	Frame Store Data Line	(BLUE / UV data)
150	fsD3	I/O	38	Frame Store Data Line	(BLUE / UV data)
149	fsD4	I/O	38	Frame Store Data Line	(BLUE / UV data)
147	fsD5	I/O	38	Frame Store Data Line	(BLUE / UV data)
145	fsD6	I/O	38	Frame Store Data Line	(BLUE / UV data)
144	fsD7	I/O	38	Frame Store Data Line	(BLUE / UV data)
143	fsD8	I/O	38	Frame Store Data Line	(GREEN data)
142	fsD9	I/O	38	Frame Store Data Line	(GREEN data)
141	fsD10	I/O	38	Frame Store Data Line	(GREEN data)
140	fsD11	I/O	38	Frame Store Data Line	(GREEN data)
138	fsD12	I/O	38	Frame Store Data Line	(GREEN data)
136	fsD13	I/O	38	Frame Store Data Line	(GREEN data)
135	fsD14	I/O	38	Frame Store Data Line	(GREEN data)
134	fsD15	I/O	38	Frame Store Data Line	(GREEN data)
133	fsD16	I/O	38	Frame Store Data Line	(RED / Y data)
132	fsD17	I/O	38	Frame Store Data Line	(RED / Y data)
129	fsD18	I/O	38	Frame Store Data Line	(RED / Y data)
128	fsD19	I/O	38	Frame Store Data Line	(RED / Y data)
127	fsD20	I/O	38	Frame Store Data Line	(RED / Y data)
126	fsD21	I/O	38	Frame Store Data Line	(RED / Y data)
125	fsD22	I/O	38	Frame Store Data Line	(RED / Y data)
124	fsD23	I/O	38	Frame Store Data Line	(RED / Y data)
122	fsD24	I/O	38	Frame Store Data Line	(BLUE / UV data)
120	fsD25	I/O	38	Frame Store Data Line	(BLUE / UV data)
119	fsD26	I/O	38	Frame Store Data Line	(BLUE / UV data)
118	fsD27	I/O	38	Frame Store Data Line	(BLUE / UV data)
117	fsD28	I/O	38	Frame Store Data Line	(BLUE / UV data)
116	fsD29	I/O	38	Frame Store Data Line	(BLUE / UV data)
115	fsD30	I/O	38	Frame Store Data Line	(BLUE / UV data)
113	fsD31	I/O	38	Frame Store Data Line	(BLUE / UV data)

111	fsD32	I/O	38	Frame Store Data Line	(GREEN data)
110	fsD33	I/O	38	Frame Store Data Line	(GREEN data)
109	fsD34	I/O	38	Frame Store Data Line	(GREEN data)
108	fsD35	I/O	38	Frame Store Data Line	(GREEN data)
107	fsD36	I/O	38	Frame Store Data Line	(GREEN data)
106	fsD37	I/O	38	Frame Store Data Line	(GREEN data)
103	fsD38	I/O	38	Frame Store Data Line	(GREEN data)
102	fsD39	I/O	38	Frame Store Data Line	(GREEN data)
101	fsD40	I/O	38	Frame Store Data Line	(RED / Y data)
100	fsD41	I/O	38	Frame Store Data Line	(RED / Y data)
99	fsD42	I/O	38	Frame Store Data Line	(RED / Y data)
98	fsD43	I/O	38	Frame Store Data Line	(RED / Y data)
97	fsD44	I/O	38	Frame Store Data Line	(RED / Y data)
96	fsD45	I/O	38	Frame Store Data Line	(RED / Y data)
91	fsD46	I/O	38	Frame Store Data Line	(RED / Y data)
90	fsD47	I/O	38	Frame Store Data Line	(RED / Y data)
86	$\overline{\text{FSCAS}}$	O	38	Frame Store Column Address Strobe	
82	fsCKE	O	38	Frame Store Clock Enable	
85	fsCLK	O	38	Frame Store Clock - based on fsRefCLK	
81	$\overline{\text{FSCS}}$	O	38	Frame Store Chip Select	
87	fsDQM0	O	38	SDRAM Data Mask. FsDQM0 and fsDQM1 (pin 89) are functionally identical but split to reduce loading. Each SDRAM device has an upper and lower DQM.	
89	fsDQM1	O	38	SDRAM Data Mask. FsDQM0 (pin 87) and fsDQM1 are functionally identical but split to reduce loading. Each SDRAM device has an upper and lower DQM.	
83	$\overline{\text{FSRAS}}$	O	38	Frame Store Row Address Strobe	
51	fsRefCLK	I	38	Frame Store Interface Clock Oscillator Input	
88	$\overline{\text{FSWE}}$	O	38	Frame Store Write Enable	

5. Functional Description

5.1 Power On Reset

A hard reset is required after power-up to ensure proper operation of all gmFC1 functional blocks and guarantee gmFC1 register contents. A hard reset may be performed by asserting $\overline{\text{RESET}}$ for a minimum of 250ns with a stable frame store clock (fsRefCLK) applied to the gmFC1. All host writable register contents default to '0' upon a hard reset, except the SOFT_RESET bit 00 and RESERVED bit 08 in the HOSTCTRL register. See Table 5 for details. After a hard reset, all input clocks must be running and stable before gmFC1 registers may be accessed.

A SOFT_RESET affects all gmFC1 functional blocks except the Host Interface registers, effectively disabling the input, output and frame store interfaces. All Host Interface registers may be loaded in any order while SOFT_RESET =1. To complete the initialization procedure, IN_FORC_UPDATE and OUT_FORC_UPDATE are set to '1', and the SOFT_RESET bit is cleared to '0'.

The gmFC1 frame store SDRAM is unavailable for 200us after a hard or soft reset. The gmFC1 will automatically perform an SDRAM power-on sequence following the negating edge of a $\overline{\text{RESET}}$ to ensure reliable SDRAM access. The SDRAM power-on sequence will also be performed during a host initiated SOFT_RESET. Note that the SDRAM is not cleared on a hard or soft reset. This will result in the first output frame after power up being read as random display data if the output is enabled before the input is enabled.

5.2 Data Input

The gmFC1 provides two separate data input ports: a 24-bit RGB graphics data port, and a 16-bit YUV video data port. Each port provides a complete control interface. The active data source is selected through the IPCTRL host programmable register IP_RGB_nYUV. In this way, the gmFC1 acts as a data stream multiplexer. All Input Port signals except INVADC, InGHS, and CLAMP are provided with internal pull-down resistors.

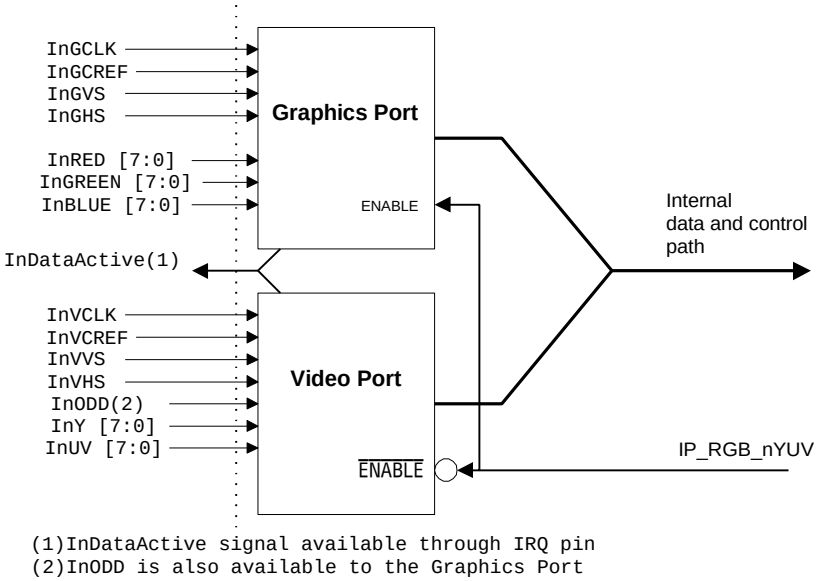


Figure 6. gmFC1 Input Multiplexer

5.2.1 RGB Graphics Input Modes

Data input to the gmFC1 RGB graphics port may be interpreted in one of three ways - Progressive Scan, Vertical Interlace, and Horizontal Interlace. The appropriate mode is selected through the IP_VINTLC_EN and IP_HINTLC_EN register bits, as in Table 2 below. Note that Horizontal and Vertical Interlace modes may not be enabled simultaneously.

Table 2: Graphics Input Modes

Mode	IP_VINTLC_EN	IP_HINTLC_EN
Progressive Scan	0	0
Horizontal Interlace	0	1
Vertical Interlace	1	0
Not Allowed	1	1

In Progressive Scan mode, the input data represents spatially contiguous sample points of the input image.

Vertical interlacing is a common technique in video systems to reduce bandwidth. It is less common in computer graphics. In Vertical Interlace mode, data is input to the gmFC1 in fields containing only odd or even lines of data. Successive alternating odd and

even fields make up the entire image. The gmFC1 automatically determines the state of the current XGA Vertical Interlace Mode field from the timing of InGHS relative to InGVS (see Figure 7 below). If this feature is disabled by setting the IPCTRL register bit EXTGODD_EN=1, the InODD signal is used to determine the current field state.

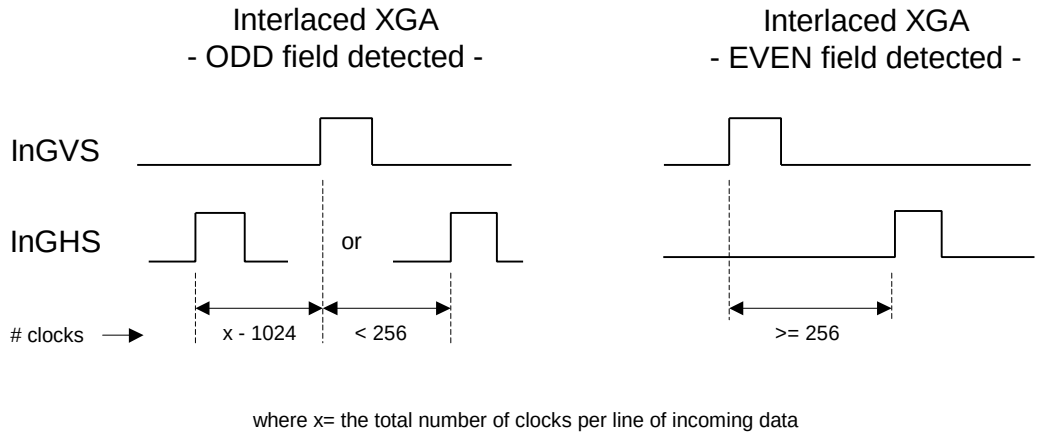


Figure 7: XGA Vertical Interlace Mode Field Detection

In Horizontal Interlace mode, data is input to the gmFC1 in fields containing only odd or only even pixels. The fields alternate between sets of odd and even pixels to make up the entire image. This technique may be useful when sampling computer graphics data. The sample rate, and therefore required bandwidth, is halved. See the INVADC description on page 23 for further details.

5.2.2 YUV Video Input Modes

The gmFC1 supports Progressive Scan and Vertically Interlaced formats as described in Section 5.2.1 above, although automatic determination of odd/even fields is not available in YUV Modes. Horizontal Interlaced YUV data is not supported.

5.2.3 Input Active Window Control

The gmFC1 contains host programmable registers which define the input active data region with respect to input vertical and horizontal sync pulses. Figure 8 below illustrates how these registers control the active input sampling region.

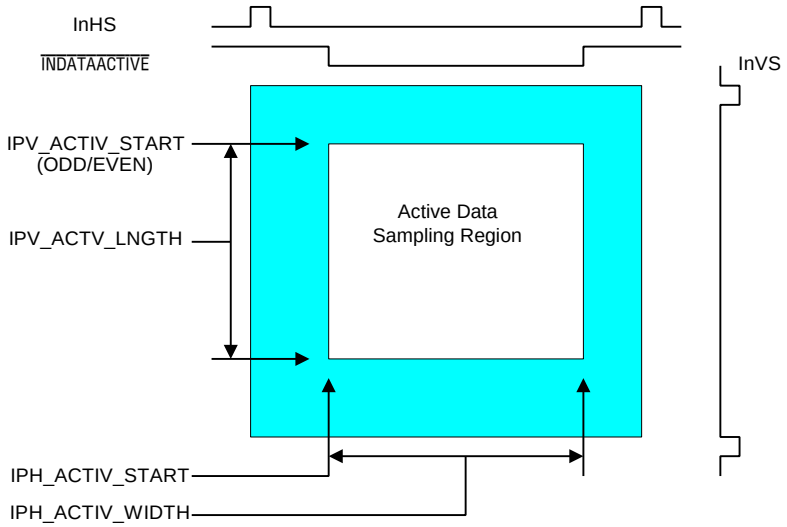


Figure 8: Input Data Sampling Window

5.2.4 Input Synchronization

Modifications to the input data window registers do not take effect immediately. After all desired changes have been made, the external system may set the input update enable bit, IN_UPDATE_EN. This causes the input parameters to become active only at the next input vertical sync. This mechanism ensures input frames are not captured with partially updated parameters. It is also possible for the host to force an immediate update by setting the IN_FORC_UPDATE bit within the HOSTCTRL register, causing modified parameters to become active without waiting for an input VSYNC. See Section 5.8.2 for further details.

5.2.5 Freeze Frame

The input data capture circuitry may be disabled through the host programmed register INP_EN. When disabled, the gmFC1 continues to display previously captured data, providing freeze frame capability.

5.3 Graphics (RGB) Input Port Signals

The Graphics (RGB) Input Port signals are active when the gmFC1 is operating with the RGB port selected, by setting the HOSTCTRL register bit IP_RGB_nYUV=1. Otherwise, this port is ignored. All Graphics Input Port signals except INVADC, InGHS, and CLAMP are provided with internal pull-down resistors.

InGCLK

InGCLK provides the timing reference for the RGB port signals. The active edge is programmable through the IPCLK_INV register.

InGCREF

InGCREF further qualifies InGCLK. InGCREF must be active during an active InGCLK edge to validate the InGCLK cycle, i.e., InGCREF can be considered an InGCLK clock enable. In most designs, the CREF signals may be hard-wired to either VCC or GND to validate all clocks. The active polarity of InGCREF is programmable through the IPCTRL register control bit IPCREF_INV.

If the CREF qualifier signals InVCREF / InGCREF are left floating or not connected, the gmFC1 may operate incorrectly. It is recommended that any unused input clock reference signals (InVCREF or InGCREF) be tied either HIGH or LOW. When the clock reference is tied HIGH, program the gmFC1 IPCTRL register bit IPCREF_INV (Register 05, bit 1) = 1. When the clock reference is tied LOW, program IPCREF_INV = 0.

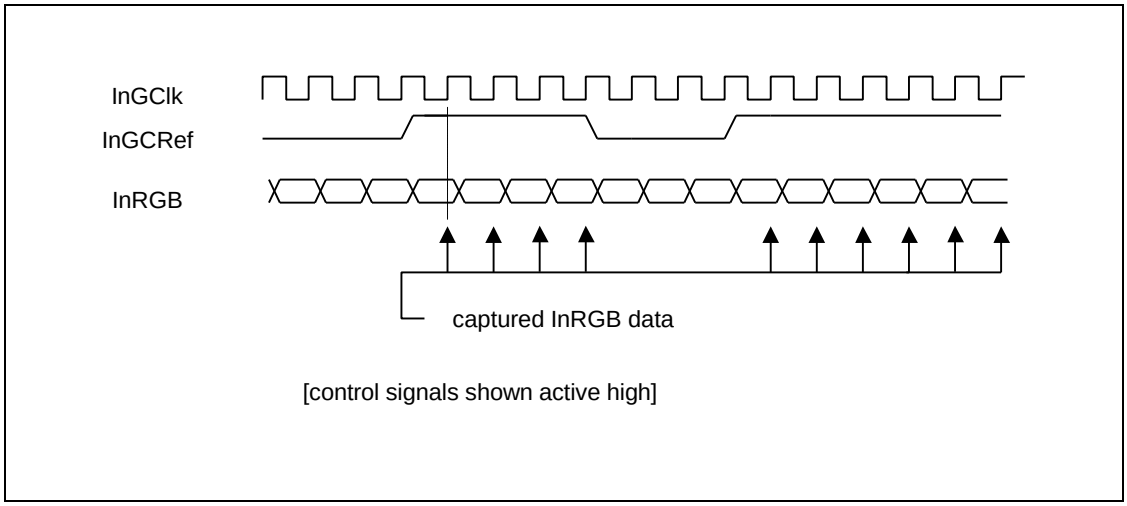


Figure 9: Graphics Input Data Handshaking

InGHS

InGHS is the RGB port horizontal sync input. The active edge of InGHS is sampled synchronously to InGCLK, and resets clock counters used in determining the active data region. The active polarity of InGHS is programmable through the IPCTRL register control bit IPHS_INV. Some amount of skew, approximately 18 InGCLK periods, is accepted between InGHS and InGVS (i.e., if there are less than 18 InGCLK periods between InGVS and InGHS, the internal line counter is not incremented). This is required since the HSYNC is generally synchronized to the reconstructed pixel clock InGCLK, and may have a different path delay from the VSYNC.

InRawGHS

InRawGHS is the 'raw' horizontal sync input for the RGB port. This signal is used as the source for horizontal sync timing measurements when the RGB port is selected. By bypassing the PLL, input mode detection is possible prior to PLL programming.

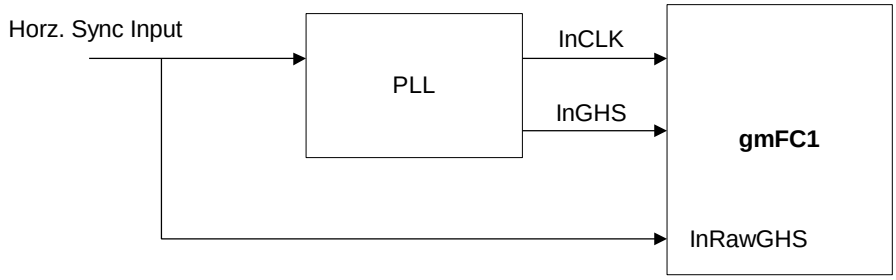


Figure 10: Graphics Horizontal Sync. Inputs

Measurement example:

To measure the active pulse width of the Horizontal Sync Input at InRawGHS:

1. Write register MEAS_VS_nHS = 0 (measure Horizontal Sync)
2. Write register PERIOD_nACTIVE = 0 (measure active 'high' width, not entire period)
3. Read MEAS_VALID, wait until MEAS_VALID =1 (a valid measurement is complete)
4. Read the measured result from MEAS_RESULTL register

Note: The selected measurement is performed continuously once steps 1) and 2) are complete. MEAS_VALID will remain set to '1' while the selected signal is being continuously re-measured. The most recent measurement is always available in the MEAS_RESULTL register. The MEAS_VALID bit will only be cleared to '0' if the MEAS_VS_nHS or PERIOD_nACTIVE bits are re-written.

The following measurements are possible:

Measured Parameter	Units	gmFC1 HOSTCTRL Register settings	
		MEAS_VS_nHS	PERIOD_nACTIVE
H-Sync Period	fsCLK / 2	0	1
H-Sync 'High' Period	fsCLK / 2	0	0
V-Sync Period	H-Sync pulses	1	1
V-Sync 'High' Period	H-Sync pulses	1	0

To determine the period of an input Horizontal or Vertical Sync signal, the gmFC1 register MEAS_RESULTL (Registers 1A) is read by the system microcontroller. The measured value in this register is updated continuously. Erroneous values may be

interpreted from the MEAS_RESULTL register if a read-back is requested during a register update.
For example, if the measured sync value is nominally 0x200, but occasionally varies to 0x1FF, the read-back value may be incorrectly read as 0x2FF if an update occurs between the time the "2" and the next most significant bit are shifted out of the gmFC1. This problem is particularly pronounced during HS measurement read-back, as HS updates occur more frequently than VS updates.
To avoid the possibility of incorrect read-back, it is possible to take advantage of the longer window between VS measurement updates to perform an HS measurement value read-back. The recommended sequence is given below, with the corrective steps highlighted in a box.

1. Program the gmFC1 to measure HS:
WRITE (Register 03 bit 09) MEAS_VS_nHS = 0 (measure HS)
WRITE (Register 03 bit 10) PERIOD_nACTIVE (measure full period =1, measure hi time = 0)

2. Poll (check) gmFC1 to ensure at least one valid measurement has been completed:
READ (Register 01 bit 10) MEAS_VALID = 1

3. Poll gmFC1 for a VS pulse (MEAS_RESULT registers are continuously updated) :
READ (Register 01 bit 08) IPRGB_VS = 1
[or READ (Register 01 bit 07) IPYUV_VS = 1 for YUV inputs]

4. Program gmFC1 to measure VS period (this guarantees no more updates to the MEAS_RESULT registers until the next VS, giving the microcontroller one frame period to read the correct HS measurement results) :
WRITE (Register 03 bit 09) MEAS_VS_nHS = 1 (measure VS)
WRITE (Register 03 bit 10) PERIOD_nACTIVE =1 (measure full VS period)

5. Read the 'captured' HS measurement value (this must be completed prior to next VS) :
READ (Register 1A) MEAS_RESULTL

Similarly, when reading VS measurement values from MEAS_RESULTL register, wait for a VS pulse and read the registers immediately to guarantee the read will not occur during an update.

'C' psuedo-code for the HS measurement and read procedure is given below:

```
/*   HS Period Measurement Procedure
*   MeasureHSPeriod:
*   {
*       SelectMeasurement (HS_Period);
*       WaitForValidMeasurement;
*       WaitForVSYNC;
*       SelectMeasurement (VS_Period);
*       ReadMeasurementResult;
*   }
*/
uint
MeasHSPeriod ()
{
    int hostctrl;
    int status;
    uint result;

    hostctrl = gmFC1_Rd (fc1_HOSTCTRL);  /* read contents of HOSTCTRL register to the hostctrl variable
*/
    hostctrl = hostctrl & (~MEAS_VS_nHS);   /* select HS */
    hostctrl = hostctrl | (PERIOD_nACTIVE); /* period */
    gmFC1_Wr (fc1_HOSTCTRL, hostctrl);  /* write new value of  HOSTCTRL register */
    while (1) {
        /*
        *   wait for measurement to be valid
        */
        status = gmFC1_Rd (fc1_STATUS);
        if ((status & MEAS_VALID) != 0) {
            break;  /* measurement is valid and ready */
        }
    }
    /*
    *   once the horizontal measurement is valid, wait for VSYNC rising edge,
    *   switch to VSYNC measurement, and immediately read the result.
    */
    status = gmFC1_Rd (fc1_STATUS); /* read STATUS register to clear VSYNC bit */
    while (1) {
        /*
        *   wait for VSYNC
        */
        status = gmFC1_Rd (fc1_STATUS);
        if ((status & IPRGB_VS) != 0) {
            break;  /* VSYNC detected */
        }
    }
    /*  switch to VSYNC measurement - prevents updates to the previously measured HSYNC value for 1
frame
    */
    hostctrl = hostctrl | (MEAS_VS_nHS);   /* select VS */
    gmFC1_Wr (fc1_HOSTCTRL, hostctrl); /* read correct value of HSYNC measurement */
    result = (gmFC1_Rd (fc1_MEAS_RESULTL) & 0xFFF);
    return (result);
}
```

InGVS

InGVS is the RGB port vertical sync input. The active edge of InGVS is sampled synchronously to InGCLK, and resets line counters used in determining the active data region. The active polarity of InGVS is programmable through the IPCTRL register control bit IPVS_INV.

InRed [7:0], InGreen [7:0], InBlue [7:0]

These are the 24-bit RGB data inputs.

INVADC

INVADC is an output signal provided by the gmFC1 to support horizontal interlacing. If the data source is an analog to digital converter (ADC), INVADC may be used to invert the ADC sampling clock at the end of every field, effectively shifting the sample points by half a clock period.

When the IPCTRL register bit IP_HINTLC_EN =1, the gmFC1 will change the state of INVADC after the final pixel of a field is captured (before InGVS). INVADC may be tied directly to the ADC clock driver (e.g. the INV pin of the Philips TDA8752 ADC). Inverting the ADC sampling clock using INVADC may cause the sampling clock to momentarily glitch. The gmFC1 InGClk is internally gated to filter these glitches within approximately 16 fsCLK periods prior to and after a toggled INVADC.

CLAMP

CLAMP is a gmFC1 output signal provided to aid the input ADC in DC restoration of the source analog RGB signal. The CLAMP pulse has programmable start and end points referenced from the input InGHS signal. The active polarity is also programmable from the host register bit IP_CLAMP_INV. CLAMP is programmed to frame a short period within the horizontal back porch. The DC restoration circuit in the ADC then modifies the DC offset value to bring the clamping level to the required voltage. The CLAMP pin is shared with the mode select pin MSBFIRST.

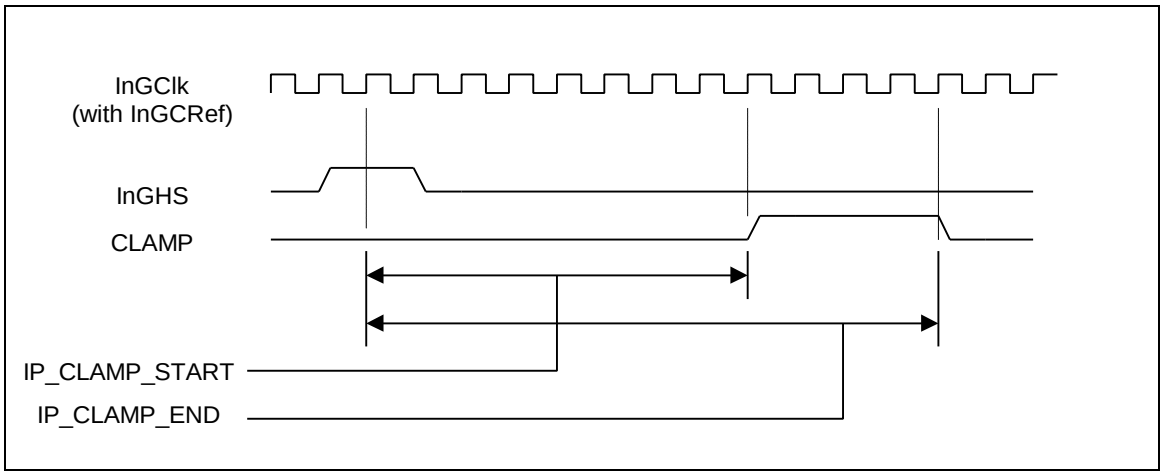


Figure 11. CLAMP Signal

5.4 Video (YUV) Input Port Signals

The Video (YUV) Data Input Port signals are active when the gmFC1 is operating with this port selected by the host programmed register bit IP_RGB_nYUV. Otherwise, this port is ignored. All Video Input Port signals are provided with internal pull-down resistors.

InVCLK

InVCLK provides the timing reference for the YUV port signals. The active edge is programmable though the IPCTRL register control bit IPCLK_INV.

InVCREF

InVCREF further qualifies InVCLK. InVCREF must be asserted during an active InVCLK edge to validate the InVCLK cycle, i.e., InVCREF can be considered an InVCLK clock enable. In most designs, the CREF signals may be hard-wired to either VCC or GND to validate all clocks. The asserting (active) polarity of InVCREF is programmable through the IPCTRL register control bit IPCREF_INV.

If the CREF qualifier signals InVCREF / InGCREF are left floating or not connected, the gmFC1 may operate incorrectly. It is recommended that any unused input clock reference signals (InVCREF or InGCREF) be tied either HIGH or LOW. When the clock reference is tied HIGH, program the gmFC1 IPCTRL register bit IPCREF_INV (Register 05, bit 1) = 1. When the clock reference is tied LOW, program IPCREF_INV = 0.

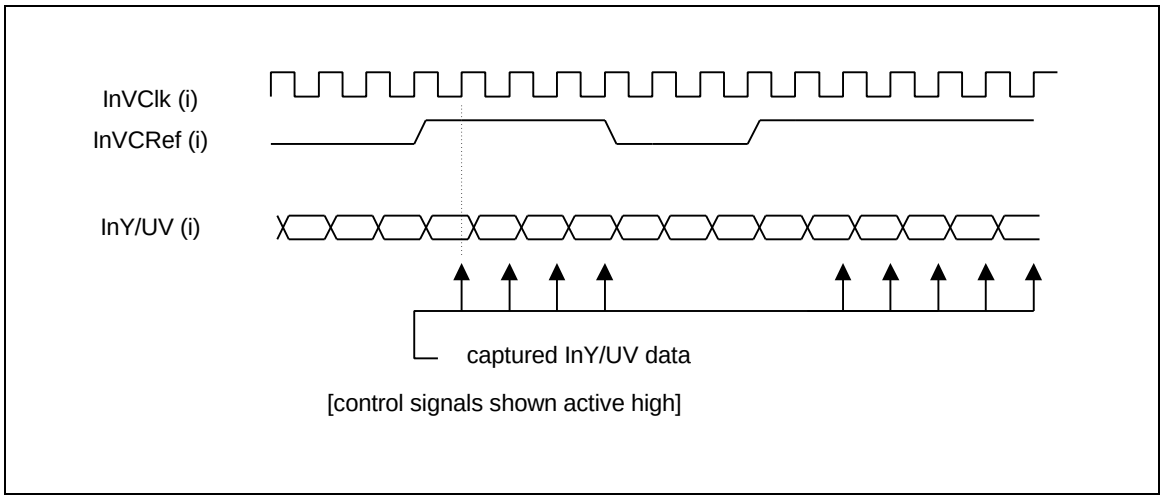


Figure 12. Video Input Data Handshaking

InVHS

InVHS is the YUV port horizontal sync input. The active edge of InVHS resets clock counters used in determining the active data region. The active polarity of InVHS is programmable through the IPCTRL register control bit IPHS_INV.

InVVS

InVVS is the YUV port vertical sync input. The active edge of InVVS resets line counters used in determining the active data region. The active polarity of InVVS is programmable through the IPCTRL register control bit IPVS_INV.

InY [7:0], InUV [7:0]

These are the 16-bit YUV data inputs.

5.5 Graphics / Video Common Port Signals

INDATAACTIVE

$\overline{\text{INDATAACTIVE}}$ is common to both graphics and video ports and is driven based on the active clock input. The $\overline{\text{INDATAACTIVE}}$ output signal indicates when the gmFC1 is expecting valid data based on the host programmed active data region registers.

$\overline{\text{INDATAACTIVE}}$ is not predictive. The $\overline{\text{INDATAACTIVE}}$ pin is physically shared with the $\overline{\text{IRQ}}$ interrupt pin of the host interface; the IRQ_OUT_EN bit in the IRQMASK register controls the function. Note that the output is open-drain, and requires a pull-up resistor.

InODD

InODD is the odd/even field indicator when operating in vertical interlace mode. It must be valid prior to the first line of active input data. When asserted, InODD indicates the current input field contains odd lines. The active polarity of InODD is programmable through the IPCTRL register control bit IPODD_INV.

The gmFC1 has the capability to auto-detect odd/even fields in certain graphics interlaced modes. The gmFC1 distinguishes fields by monitoring InGVS and InGHS. If this feature is disabled by setting the IPCTRL register bit EXTGODD_EN=1, the InODD signal is used to determine the current field state. InODD is provided with an internal pull-down resistor.

5.6 Data Output

5.6.1 Output Formats

The gmFC1 will produce a Progressive Scan output format if the input format is Progressive Scan.

If the input format is vertically interlaced, the gmFC1 may output vertically interlaced data, or it may be configured to perform static mesh de-interlacing and output a Progressive Scan format. Static mesh de-interlacing weaves together alternating odd and even lines of data as illustrated in Figure 13 below.

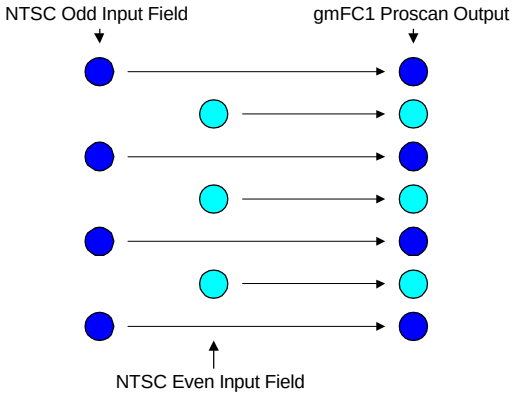


Figure 13: Vertical De-Interlacing

If the input format is horizontally interlaced, the gmFC1 will weave together alternating odd and even pixel data fields, and produce a Progressive Scan output. Horizontal interlacing allows an ADC to effectively sample a signal at twice the maximum ADC clock rate (e.g., a 160 MHz signal may be sampled using a 80 MHz ADC, assuming the full power bandwidth of the ADC is >= 160 MHz). See Figure 14 below.

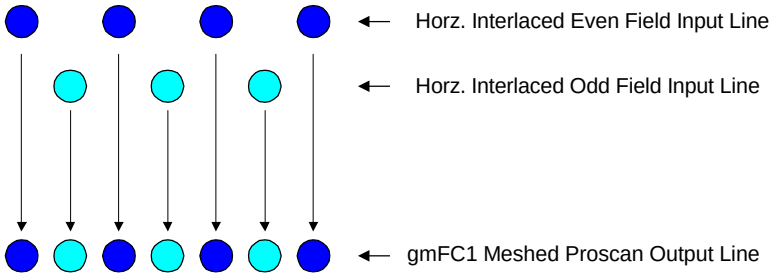


Figure 14: Horizontal De-Interlacing

5.6.2 Output Interface Overview

The operational parameters of both the gmFC1 and the Genesis gmZ1/Z2/Z3 zoom scaler are closely related. In Free Run Mode, the gmFC1 depends on the gmZ1/Z2/Z3 to set the output frame rate, and to request data required to maintain the data rate. (In Frame Sync Mode, the gmFC1 input source sets the frame rate.) Output interface handshaking is shown in Figure 15 below. See Figure 16 for interface details.

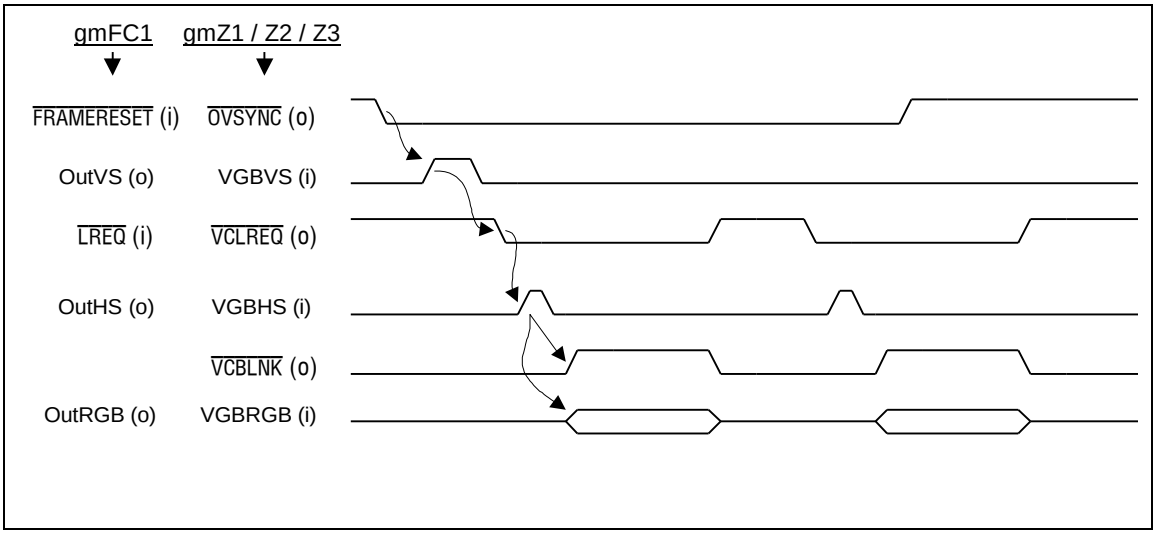


Figure 15: Output Timing (to gmZ1/2/3)

The gmFC1 is programmed to provide active output data a specified number of clock cycles (OPH_ACTIV_START) after the gmFC1 asserts OutHS. The gmZ1/Z2/Z3 is programmed to receive active single pixel RGB input data occupying the same active window as the gmFC1 RGB output data. This is achieved by matching the gmFC1 Active Output Window parameters to the gmZ1/Z2/Z3 Active Input Window parameters.

When the gmZ1/Z2/Z3 has completed displaying an image, the gmFC1 must be signaled to queue up data for the next frame. This is accomplished by tying a gmZ1/Z2/Z3 display-side VSYNC signal (ex: OVSYNC) to the gmFC1 $\overline{\text{FRAMERESET}}$ input. This resets the gmFC1's output circuitry, and produces a pulse on the OutVS signal. In response to this the gmZ1/Z2/Z3 asserts $\overline{\text{VCLREQ}}$, indicating internal line storage is available. $\overline{\text{VCLREQ}}$ is tied to the gmFC1's $\overline{\text{LREQ}}$ pin.

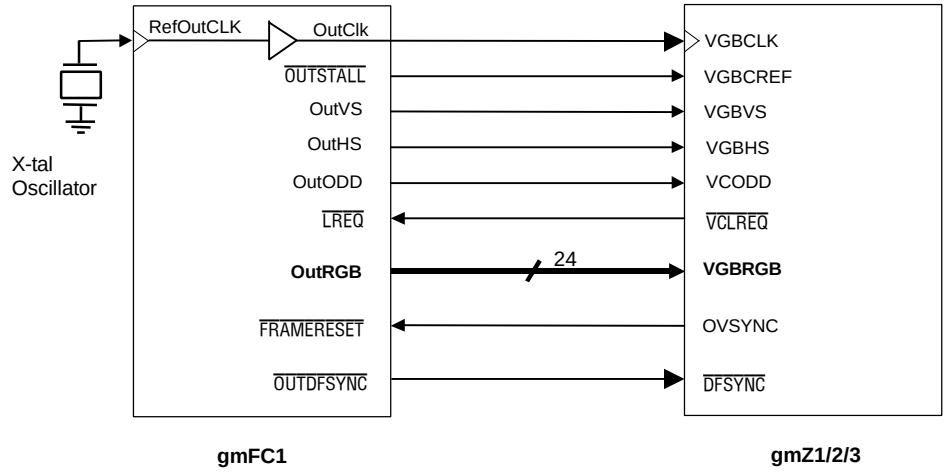


Figure 16: gmFC1 - gmZ1/2/3 Interface

In applications where the gmFC1 must provide data on demand from a source other than the gmZ1 / gmZ2 / gmZ3, the DATAREQ signal may be used. By programming the MISC register control bit OP_HANDSH = 0, the gmFC1 will slave to requests for data at the DATAREQ input pin and provide data three clock cycles after DATAREQ is asserted. In this mode, the latency to data from DATAREQ (three clock cycles) differs from the gmZ1 / gmZ2 / gmZ3's $\overline{\text{VCBLNK}}$ data latency requirement (two clock cycles). Therefore, in applications where the gmFC1 is interfacing to the gmZ1 / gmZ2 / gmZ3, the gmFC1 control bit OP_HANDSH must be programmed to '1'. This enables the gmFC1 to provide data a fixed number of clock cycles after asserting OutHS. The gmZ1/Z2/Z3 must be programmed to expect data at the same point.

$\overline{\text{OUTSTALL}}$ is used by the gmFC1 to indicate it does not have the requested data available. Because of internal buffering within the gmZ1 / gmZ2 / gmZ3, momentary data transfer stalls are acceptable. If prolonged data transfer stalls occur (ex: because the I/O data rates through the gmFC1 exceed its frame store capabilities) the gmZ1/Z2/Z3 will underflow.

5.6.3 Output Active Size

The gmFC1 may be programmed to output a region of data smaller than the active sampled input region. The parameters of the output region are set through host programmed registers. This feature allows zooming of a captured freeze frame input image. The location of the output region within the input data is restricted to multiples of two pixels. To position the output image an offset Y_OFFSET lines from the captured input start, and an offset X_OFFSET pixels from the captured image left edge:

Progressive Scan Images:
OP_MEM_START= IPH_MEM_WIDTH * Y_OFFSET + *int* (X_OFFSET / 2)
Vertical Interlaced Images:

OP_MEM_START= IPH_MEM_WIDTH * *int* (Y_OFFSET/2) + *int* (X_OFFSET / 2)
Horizontal Interlaced Images:
OP_MEM_START= IPH_MEM_WIDTH * Y_OFFSET + *int* (X_OFFSET / 4)

where the function *int (x)* returns the nearest integer not greater than *(x).*

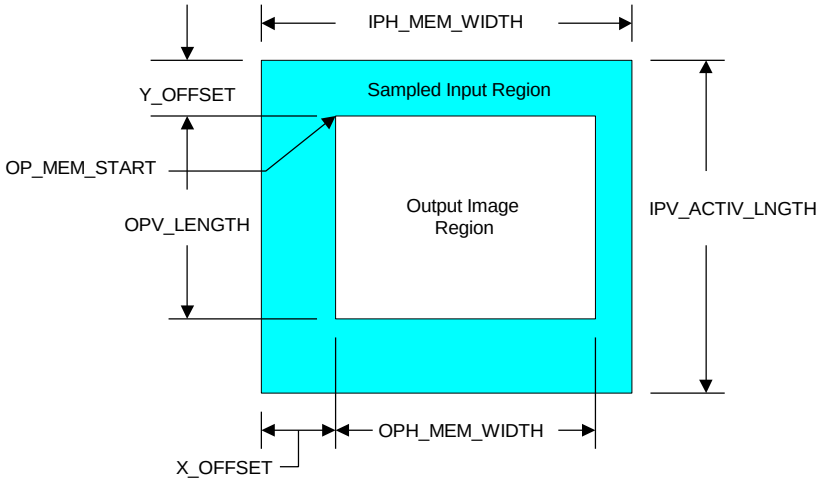


Figure 17: Output Sub-Region of Captured Input Image

5.6.4 Output Synchronization

Because of the close relationship between gmFC1 output and gmZ1/Z2/Z3 input sections, care must be taken to ensure they remain synchronized. This is particularly true in applications where the operational parameters are modified dynamically.

The gmFC1 host programmed registers associated with the output interface incorporate an Active and a Pending Register Set. When modified by the host, only the Pending Register Set is affected. The Active Register Set is the set actually used by the output circuitry. The Pending Register contents are copied to the Active Set only after the OUT_UPDATE_EN register bit is set, and the $\overline{\text{FRAMERESET}}$ signal becomes asserted. This is at a point where no active data is being transferred to the gmZ1 / gmZ2 / gmZ3.

The gmZ1/Z2/Z3 has a similar scheme, with Pending and Active Register sets. For the gmZ1 / gmZ2 / gmZ3, the transfer to the Active Register Set also occurs at approximately this same point. For a more detailed description of gmFC1 - gmZ1/Z2/Z3 interfacing, see the Genesis Application Note MSD-0016, 'Interfacing the Genesis gmFC1 and gmZ1, gmZ2 and gmZ3', included with this data sheet.

When parameters are modified dynamically (i.e., while active data is flowing), the host microcontroller is responsible to ensure gmFC1 and gmZ1/Z2/Z3 Active Register sets are synchronized. This may be achieved by enabling the Pending to Active set transfers for both the gmFC1 and the gmZ1/Z2/Z3 within a short period after the $\overline{\text{FRAMERESET}}$ has

occurred. This ensures the transfer for one device will not happen while the host is enabling the transfer for the other device.

5.6.5 Reverse Scanning

The image may be scanned out of memory from bottom to top, effectively flipping the output image. To enable this feature, OP_MEM_START must be set to the bottom of the image, using one of the following basic formulas:

For Progressive Scan and Horizontal Interlaced images:

OP_MEM_START = (IPV_ACTIV_LNGTH-1)* IPH_MEM_WIDTH

For Vertical Interlaced images:

OP_MEM_START = int((IPV_ACTIV_LNGTH-1)/2) * IPH_MEM_WIDTH

Note that the above formulas assume that no image cropping is taking place.

With the REV_SCAN bit enabled, IPH_MEM_WIDTH is subtracted from OP_MEM_START when addressing the SDRAM. Therefore, the image is read out from bottom to top. Note that correct Double Buffering is not guaranteed when reverse scanning, and frame tear may result.

5.6.6 Bypass Mode

To aid in system development, the gmFC1 provides a Bypass Mode. In Bypass Mode, the selected input port signals are routed unmodified to the corresponding output signals, although there is a two-clock pipeline delay. The programmable polarity functions are still available. The following table illustrates the mapping of gmFC1 input to output signals.

Table 3: Corresponding Input/Output Signals in Bypass Mode

gmFC1 Input Signal ⟶	Corresponding Output Signal
In[GV]CLK	OutCLK
In[GV]CRef	$\overline{\text{OUTSTALL}}$
InODD	OutODD
In[GV]VS	OutVS
In[GV]HS	OutHS
InRED [7:0] / InY [7:0]	OutRED [7:0] / OutY [7:0]
InGREEN [7:0]	OutGREEN [7:0]
InBLUE [7:0] / InUV [7:0]	OutBLUE [7:0] / OutUV [7:0]

5.6.7 Frame Lock Mode

In normal operation, the input frame rate is set by the input data source, and the output frame rate is set by the gmZ1 / gmZ2 / gmZ3. In many applications, these rates differ, and frame rate conversion is required. However, there are instances where the input and output rates are *nominally* the same. In such cases, it may be desirable to ensure that frame rates remain locked to avoid motion glitches in video. The gmFC1 output signal $\overline{\text{OUTDFSYNC}}$ may be used to force the gmZ1/Z2/Z3 display timing generator to reset. A gmZ1/Z2/Z3 display vertical sync signal then asserts $\overline{\text{FRAMERESET}}$, which in turn causes the gmFC1 to reset its output circuitry. In Frame Lock Mode, the gmFC1 will assert $\overline{\text{OUTDFSYNC}}$ based on the selected input VS.
When frame rate converting an interlaced video input to an interlaced video output, back to back odd and even fields will occur, the frequency of which will depend on the ratio of the input to output frame rate. Slight image jitter may result, the measure of which is dependent on the frame rate conversion factor employed. If this is objectionable, the gmFC1 system should be run in Frame Locked Mode when working with interlaced video.

5.6.8 Output Signals

RefOutCLK

The RefOutCLK input provides the crystal clock reference for the output interface. (The exception is Bypass Mode, in which the selected input port clock provides the output interface timing reference.)

OutCLK

The OutCLK clock drives the gmZ1/Z2/Z3 input interface. OutCLK is a buffered version of RefOutCLK (except in Bypass Mode).

FRAMERESET

The $\overline{\text{FRAMERESET}}$ input forces a re-synchronization of the gmFC1 output circuitry. $\overline{\text{FRAMERESET}}$ must be asserted to initialize the next output frame. This pin may be driven asynchronously to OutCLK. Generally, $\overline{\text{FRAMERESET}}$ is tied to one of the gmZ1/Z2/Z3 display vertical sync signals such as $\overline{\text{OVSYNC}}$.

OutVS

OutVS is asserted by the gmFC1 in response to $\overline{\text{FRAMERESET}}$. It is used to initiate the gmZ1/Z2/Z3 input circuitry to the start of a new frame.

OutHS

OutHS is asserted by the gmFC1 in response to an $\overline{\text{LREQ}}$ line request input, i.e., in response to a gmZ1/Z2/Z3 $\overline{\text{VCLREQ}}$ request for input lines. OutHS begins a new line and increments the gmZ1/Z2/Z3 line counter.

OutODD

OutODD is used in the Vertical Interlace output format. When asserted, OutODD indicates that the current output field contains odd lines of data.

OUTSTALL

$\overline{\text{OUTSTALL}}$ is asserted by the gmFC1 when it is unable to provide the requested pixel data to the gmZ1 / gmZ2 / gmZ3. This may occur if the I/O bandwidth requirement is close to the bandwidth provided by the frame store interface. If the gmFC1 is unable to provide data for a sustained period of time, the gmZ1/Z2/Z3 will receive an underflow error. If this occurs, the combined gmFC1 input and output data rates will be too high to be supported by the frame store interface.

In applications where the gmFC1 is *not* interfacing to the gmZ1 / gmZ2 / gmZ3, FIFO's may be required at the gmFC1 output to maintain consistent data output.

LREQ

The $\overline{\text{LREQ}}$ Line Request input is connected to the gmZ1/Z2/Z3 $\overline{\text{VCLREQ}}$. $\overline{\text{VCLREQ}}$ indicates a request for an input line by the gmZ1 / gmZ2 / gmZ3. The gmFC1 uses $\overline{\text{LREQ}}$ to trigger an OutHS pulse.

DATAREQ

The DATAREQ signal may be used in applications where the gmFC1 must provide data on demand from a source other than the gmZ1 / gmZ2 / gmZ3. When the MISC register control bit OP_HANDSH is programmed to '0', the gmFC1 will slave to requests for data at the DATAREQ input pin and provide data three clock cycles after DATAREQ is asserted.

In this mode the latency to data from DATAREQ (three clock cycles) is different than the gmZ1 / gmZ2 / gmZ3's $\overline{\text{VCBLNK}}$ data latency requirement (two clock cycles). Therefore, when interfacing to the gmZ1 / gmZ2 / gmZ3, OP_HANDSH is programmed to '1', enabling the gmFC1 to output data a programmed number of clocks after asserting OutHS.

OutRed [7:0] OutGreen [7:0], OutBlue [7:0]

These are the 24-bit RGB data outputs. If the YUV input port is used to acquire data, OutRed [7:0] corresponds to the YUV input port Y [7:0], and OutBlue [7:0] corresponds to the YUV input port UV [7:0].

OUTDFSYNC

$\overline{\text{OUTDFSYNC}}$ is used by the gmFC1 in Frame Lock mode to force the gmZ1/Z2/Z3 to re-synchronize to a new frame. It is tied to the gmZ1/Z2/Z3 $\overline{\text{DFSYNC}}$ pin.

5.7 Frame Store Requirements

5.7.1 Interface Overview

An external frame buffer provides storage required for the frame rate conversion process. The gmFC1 is intended to operate with three 16-Mbit Synchronous DRAM (SDRAM) devices, organized as 1 M x 16-bits.

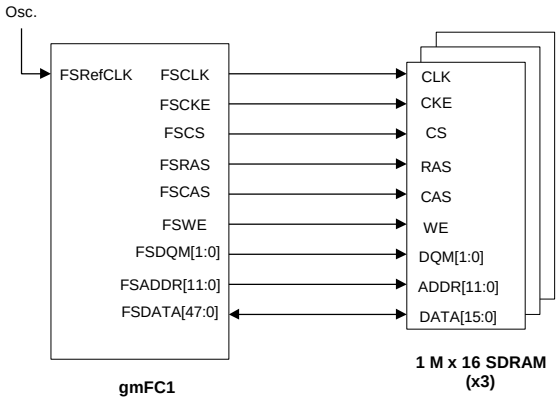


Figure 18. Frame Store Interface to SDRAM

Internally, the total frame store memory is divided in two, each half representing a single buffer. The gmFC1 memory controller attempts to read the most recently written data available within a buffer wherein there is no danger of overlapping the read and write pointers (which would result in frame tear). Any data read from a buffer is then free to be overwritten by new incoming data. Each memory location holds two pixels, and the image is mapped to memory as follows: for any pixel (X) on line (Y) in a Proscan image, the corresponding memory address is given as [(Y*IPH_MEM_WIDTH) + int(X/2)]. For

Vertical Interlaced images, the address is given as [(Y*IPH_MEM_WIDTH / 2) + int(X/2)]. For Horizontal Interlaced images, the address is given as [(Y*IPH_MEM_WIDTH) + int(X/4)].

5.7.2 Constraints on I/O Data Rates

Except within Bypass Mode, all data flowing into and out of the gmFC1 must pass through the frame store interface. Therefore, the interface must provide enough bandwidth to support the combined demands of the input and output ports.

The bandwidth required from a port, measured in bytes/second, is three times the pixel clock frequency (each RGB pixel consists of three bytes of information). The minimum bandwidth provided by the frame store interface must then be:

Minimum Frame Store Bandwidth = 3(InCLK + OutCLK) [Equation (1)]

For example, an input format of 85 Hz SVGA has a pixel clock of 56.25 MHz. This requires 3 x 56.25 MB/s bandwidth. Frame rate converting this to 60 Hz drops the pixel rate to 40.00 MHz. This requires 3 x 40.00 MB/s. The frame store interface must provide the sum of these, 288.75 MB/s.

In order to provide this bandwidth, a fast and wide path to the frame store is necessary. The gmFC1 uses synchronous DRAM devices clocked at up to 95 MHz.

With three devices in parallel providing a 48-bit (6 Byte) wide bus, the peak bandwidth available is 95 MHz x 6 bytes, or 570 MB/second. Because of transfer setup overhead, the sustained bandwidth from the SDRAM may be approximately 90% of peak, or approximately 513 MB/s.

The available frame store bandwidth must be greater than the combined I/O pixel bandwidth. From Equation 1:

Frame Store bandwidth >= 3(InCLK + OutCLK) [Equation (2)]

Although the frame store interface is designed to operate at 95 MHz, it may be desirable to operate at the lowest possible frequency which will support the application to facilitate less critical PCB layout, lower power consumption and EMI emissions, etc. The frame store bandwidth may also be related to its frequency of operation. Sustained transfers rate are assumed to be 90% of the peak transfer rate. The sustained bandwidth is 6 bytes x fsCLK x 0.9. Tying this in with Equation (2) gives:

fsCLK x 6 x 0.9 >= 3(InCLK + OutCLK) or

fsCLK >= (InCLK + OutCLK) / 1.8

e.g., for an 85Hz XGA input and 60Hz XGA output:

InCLK = 95MHz OutCLK = 65MHz

Therefore fsCLK >= (95 + 65) / 1.8 = 89MHz

Note: for YUV-only applications, only two SDRAM devices are required (the GREEN channel is unused) . See the Frame Store Interface Pinout in Table 1 re: correct SDRAM Data Bus mapping.

5.7.3 Frame Store Clock Frequency and Various Data Formats

The following table details the minimum frame store clock frequencies required to support frame rate conversion of various formats, based on the equations in Section 5.7.2.

Note: In all cases, the output is assumed to be 60 Hz. The 60Hz output is arbitrary, and is not a limitation imposed by the gmFC1. The Maximum Frame Store Clock : Output Pixel Freq. ratio is 4:1.

Table 4: Frame Store Clock Requirements

Input Format	Input Pixel Freq.	Output Pixel Freq. (at 60Hz)	Minimum Frame Store Clock Required (2)
640x480 @ 75Hz	31.5 MHz	25.175 MHz	31.5 MHz
800x600 @ 72 Hz	50.0 MHz	40 MHz	49.7 MHz
1024x768 @ 85 Hz	94.5 MHz	65 MHz	88.6 MHz
NTSC @ 60 Hz (interlaced) (1)	13.25 MHz	13.25 MHz (3)	14.7 MHz

(1) Frame rate 'conversion' from 60 Hz to 60 Hz is unnecessary, but may be useful where the input is *nominally* NTSC, such as the output from a VCR.

(2) Due to minimum SDRAM refresh cycle requirements, the actual minimum fsCLK = 62MHz

(3) The actual minimum Output Pixel Frequency = Minimum fsCLK/4, = 62MHz/4 = 15.5MHz.

Table 4 shows that in order to support a frame rate conversion from XGA 85 Hz to 60 Hz, the frame store interface must be clocked at a minimum of 88.6 MHz. (The frame store interface may be clocked at a higher frequency than is strictly necessary.) If the application is required to support various input formats, the frame store must be clocked at the highest frequency required.

5.7.4 SDRAM Power On

SDRAMs have a power-on sequence which must be performed before they may be reliably accessed. The gmFC1 will automatically perform an SDRAM power-on sequence following the negating edge of a $\overline{\text{RESET}}$. The SDRAM power-on sequence will also be performed during a host initiated SOFT_RESET. The gmFC1 frame store SDRAM is unavailable for 200us after a hard or soft reset.

5.7.5 Clearing SDRAM

SDRAM is not cleared after a power on reset. The gmFC1 will output one frame of random data prior to reading out the first valid frame after a power up. If it is not desirable to display this initial frame of random data, the gmFC1 output may be disabled or the gmZ1/Z2/Z3 may be programmed to output a background color.

5.7.6 SDRAM Power Down

SDRAM devices typically have a low power, non-operational mode. The gmFC1 will support this feature. Low power mode is enabled by the programmed register PWRDWN. A Soft Reset will be required after bringing the SDRAMs up from power down mode.

5.7.7 Supported SDRAM Devices

5.7.7.1 1M x 16-bit SDRAM

The gmFC1 will function correctly using any 100 MHz speed grade 16-Mbit SDRAM, organized as 1 M x 16-bits. The following are confirmed supported SDRAM devices:

IBM	IBM0316169
Hitachi	HM216165
NEC	uPD4516161
Toshiba	TC59S1616AFT
TI	TMS626162
Samsung	KM416S1020B

5.7.7.2 4M x 16-bit SDRAM

Any 4M x 16-bit (64 Mbit) device conforming to SDRAM standards may interface to the gmFC1 if certain hardware modifications are observed. The following 4M x 16-bit SDRAM devices have been tested by Genesis Microchip:

Toshiba	TC59S6416BFT-10
Mitsubishi	MB611641642A-100FN
Samsung	KM416S4030BT-GB

To interface 4M x 16 SDRAM devices to the gmFC1, the additional SDRAM address lines A13 and A12 are tied to ground, limiting SDRAM addressing to 1M x 16-bits. This modification is illustrated on the following page.

Note: RESERVED pins on the SDRAM devices are not connected.

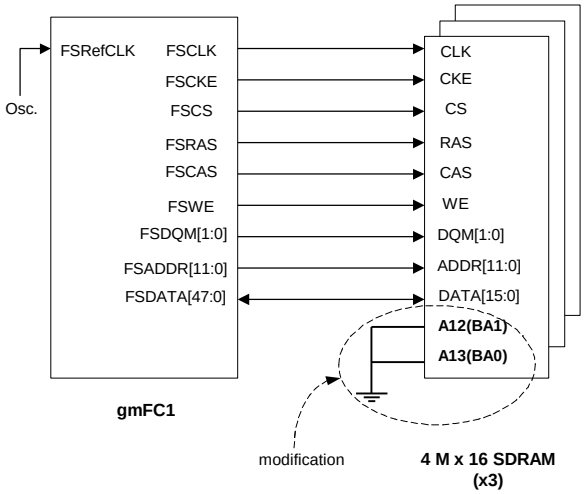


Figure 19: 4M x 16-bit Frame Store Interface

5.7.8 Frame Store Signals

fsRefCLK

The fsRefCLK input provides the timing reference for the frame store interface.

fsCLK

fsCLK provides the clock to the external SDRAM devices. It is based on fsRefCLK.

fsCKE

fsCKE is the fsCLK (SDRAM Clock) Enable signal.

FSCS

$\overline{\text{FSCS}}$ is the SDRAM Chip Select, common to all SDRAM devices.

FSRAS

$\overline{\text{FSRAS}}$ is the SDRAM Row Address Strobe, common to all SDRAM devices.

FSCAS

$\overline{\text{FSCAS}}$ is the SDRAM Column Address Strobe, common to all SDRAM devices.

FSWE

$\overline{\text{FSWE}}$ is the SDRAM Write Enable, common to all SDRAM devices.

fsDQM [1:0]

fsDQM is the SDRAM Data Mask. These signals are functionally identical but are split into two signals in order to reduce loading (each SDRAM device has an upper and lower DQM).

FSADDR [11:0]

This is the SDRAM multiplexed address. Bit 11 is the MSB and corresponds to the Bank Select address bit.

FSDATA [47:0]

This is the SDRAM data bus.

5.8 Host Interface Requirements

5.8.1 Interface Overview

The gmFC1 provides a host interface to support device configuration and provide the following capabilities:

- SPI protocol through the Host Interface Port. (gmZ1/Z2/Z3 compatible)
- Reading of registers for ease of microcontroller programming and system testing.
- Burst mode, where only one address transfer is required for multiple data transfers.

5.8.2 Updating Register Contents

Write operations to many Host Interface registers do not have an immediate effect on gmFC1 operating parameters. In these cases, any data written by the Host Interface is placed into an intermediate bank of latches called the Pending Register Set. Any Host Interface read cycles access the Pending Register Set for read back data. For the write data to take effect on the gmFC1 operating configuration, the Pending Register Set contents must be transferred (updated) to the Active Register Set.

The gmFC1 has host registers associated with input data parameters, and registers associated with output data parameters. These may be transferred independently to the corresponding Active Register Sets.

5.8.2.1 Forcing An Immediate Update

An immediate update of input parameters may be achieved by setting the IN_FORC_UPDATE bit within the HOSTCTRL register. An immediate update of output parameters may be achieved by setting the OUT_FORC_UPDATE bit within the same register. Forced updates are used during device initialization when coming out of a power-on or Soft Reset state, and no video timing is operating.

5.8.2.2 Video Timing Synchronized Updates

Input and/or output synchronized updates may be achieved by setting the IN_UPDATE_EN or OUT_UPDATE_EN bit within the HOSTCTRL register. Update Enable is used for varying any video active region parameters during real time video. The Host Controller can program new parameters into the device while the gmFC1 is operating and processing video. Since the new parameters are stored in the Pending Register Set, there are no immediate changes made to gmFC1 operating conditions, and the device operates normally.

When the external host controller has finished programming the new parameters, it may set the IN_UPDATE_EN or OUT_UPDATE_EN bits. Once enabled by IN_UPDATE_EN, the input related parameters are transferred from the Pending Register Set to the Active Register Set on the next input vertical sync pulse. Output related parameters are transferred to the Active set when enabled using OUT_UPDATE_EN, on an active transition of $\overline{\text{FRAMERESET}}$. This technique is useful for changing parameters while video timing is running without loss of display synchronization or visual artifacts appearing on the display output.

5.9 SPI Host Interface Protocol Requirements

5.9.1 SPI Interface Control Signals

RESET

The $\overline{\text{RESET}}$ signal initializes the gmFC1 by resetting all gmFC1 registers to '0', except the SOFT_RESET bit (disabling the gmFC1 input and output interfaces) and the RESERVED bit 08 in the HOSTCTRL register. All Host Interface registers may then be loaded in any order, and an IN_FORC_UPDATE and OUT_FORC_UPDATE performed. The SOFT_RESET bit in the HOSTCRTL register is then cleared to '0', completing the initialization procedure. See Section 5.1 for more details.

SCS

The Serial Chip Select ($\overline{\text{SCS}}$) signal is a master enable for the Host Interface. If $\overline{\text{SCS}}$ is de-asserted, all activity on other Host Interface signals is ignored. If $\overline{\text{SCS}}$ is asserted, the Host Interface will listen to bus activity. The assertion of $\overline{\text{SCS}}$ initializes the Host Interface, and the de-assertion of $\overline{\text{SCS}}$ terminates the current transfer.

SCLK

The Serial Clock (SCLK) signal is the clock by which data is loaded into or read from the Host Interface.

SCLKPOL

Serial Clock Mode Select Input. SCLKPOL selects the active edge of the host interface shift clock, SCLK. If SCLKPOL=0, SDI is sampled on the SCLK rising edge and SDO is shifted out on the SCLK falling edge. If SCLKPOL=1, SDI is sampled on the SCLK falling edge and SDO shifted out on the rising edge. The value of SCLKPOL is latched on the rising (negating) edge of $\overline{\text{RESET}}$. The SCLKPOL input is shared with the INVADC output. Figure 20 below.

MSBFIRST

Host Interface Mode Select Input. MSBFIRST selects serial data (SDI/SDO) bit ordering. If MSBFIRST=1, the MSB is shifted first. If MSBFIRST=0, the LSB is shifted first. The value of MSBFIRST is latched on the rising (negating) edge of $\overline{\text{RESET}}$. The MSBFIRST input is shared with the CLAMP output. See Figure 20 below.

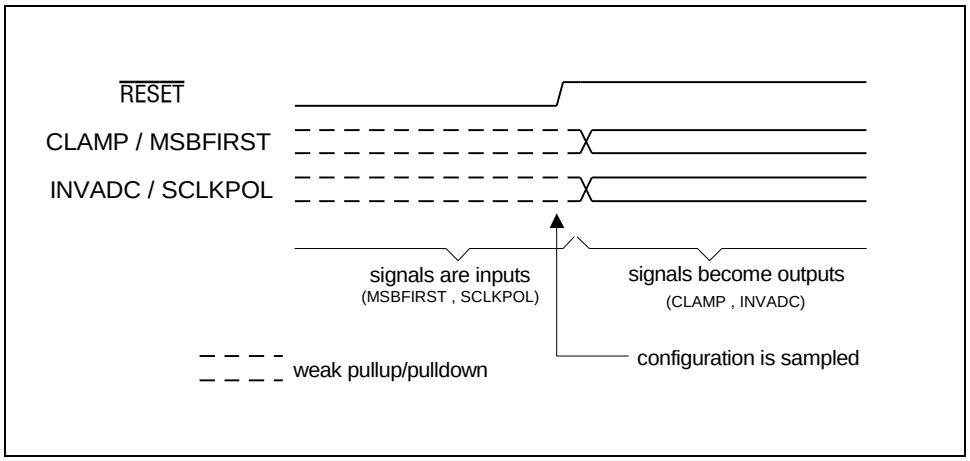


Figure 20: SCLKPOL and MSBFIRST Configuration

SDI

The Serial Data Input (SDI) signal contains the data which is loaded into the Host Interface.

SDO

The Serial Data Output (SDO) signal contains the data which is read from the Host Interface. The SDO signal is an open-drain output. It may be connected to SDI in a 3-wire configuration or used by itself in a 4-wire configuration. The selection of 3-wire or 4-wire configurations is controlled by the HI4WIRE_EN bit in the HOSTCTRL register.

IRQ

The gmFC1 has one interrupt output signal, $\overline{IRQ}$, which may be programmed to provide device status or video timing interrupts to the system. The interrupt is programmable via the Host Interface IRQMASK register to select from a number of interrupt sources such as video timing events or input buffer overflow.

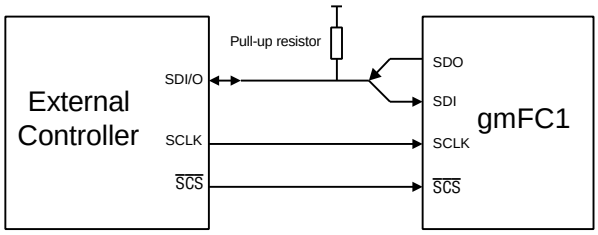
The $\overline{IRQ}$ interrupt operates in “latched” mode. When the interrupt occurs, the interrupt generation circuitry detects the event and drives the interrupt output to the active state continuously until the external Host Controller reads the STATUS register to acknowledge interrupt service.

The $\overline{IRQ}$ interrupt output pin is driven by the gmFC1 using open drain logic, i.e. logic ‘1’ output is high impedance, and a logic ‘0’ is driven to GND. Therefore the system must provide an external pull-up resistor (~10kΩ) to detect the logic ‘1’ state. The interrupt output may be utilized in an “ACTIVE LOW WIRED OR” configuration with other device interrupts in a system.

The $\overline{\text{INDATAACTIVE}}$ pin is physically shared with the $\overline{\text{IRQ}}$ interrupt pin. The IRQ_OUT_EN bit in the IRQMASK register controls the pin function.

5.9.2 3-Wire Configuration

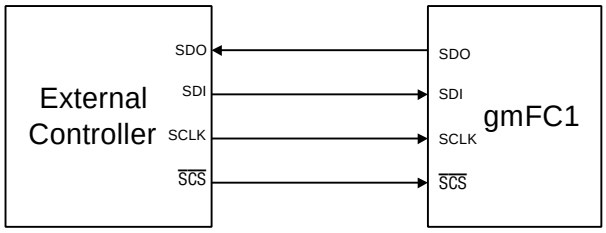
The 3-wire Host configuration is shown below:



In 3-wire configuration, SDI and SDO signals are tied together and connected to a pull-up resistor.

5.9.3 4-Wire Configuration

The 4-wire Host configuration is shown below:



5.9.4 SPI Host Interface State Description

The Host Interface is governed by a 4-state finite state machine as shown in Figure 21:

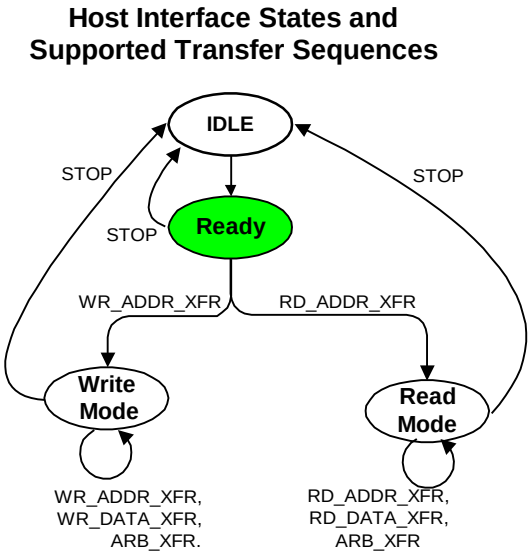


Figure 21: Host Interface Operating States

5.9.4.1 Idle State

The Host Interface enters the IDLE state after a power-on reset or after the detection of a STOP condition (see section 5.9.5.7). Note the STOP condition will always cause a transition to the IDLE state from any other state. Upon reception of the START condition (see section 5.9.5.2) within the IDLE state, the Host Interface moves to the READY state.

5.9.4.2 Ready State

Upon reception of the START condition (see section 5.9.5.2) within the IDLE state, the Host Interface moves to the READY state. In the READY state, the Host Interface supports only Address Transfers (write or read).

Address Transfers initiated with the R/W bit = '1' cause the Host Interface to store the new address and auto-increment information, then transition to READ MODE state.

Address Transfers initiated with the R/W bit = '0' cause the Host Interface to store the new address and auto-increment information, then transition to WRITE MODE state.

5.9.4.3 Write Mode State

The Host Interface enters the WRITE MODE state from the READY state when an Address transfer occurs with the R/W bit = '0'.

While in the WRITE MODE state the following transfers are supported:

Write Address Transfers (see section 5.9.5.3)

Write Data Transfers (see section 5.9.5.5)

Address Read-Back Transfers. (see section 5.9.5.4)

The Host Interface leaves Write Mode only when a STOP condition occurs. (See section 5.9.5.7).

5.9.4.4 Read Mode State

The Host Interface enters the READ MODE state from the READY state when an Address transfer occurs with the R/W = '1'.

While in the READ MODE state the following transfers are supported:

Read Address Transfers (see section 5.9.5.3)

Read Data Transfers (see section 5.9.5.6)

Address Read-Back Transfers. (see section 5.9.5.4)

The Host Interface leaves Read Mode only when a STOP condition occurs. (see section 5.9.5.7).

5.9.5 Host Interface Protocol

The Host Interface uses a 16-bit protocol to transfer data. The protocol is detailed below in Figure 22:

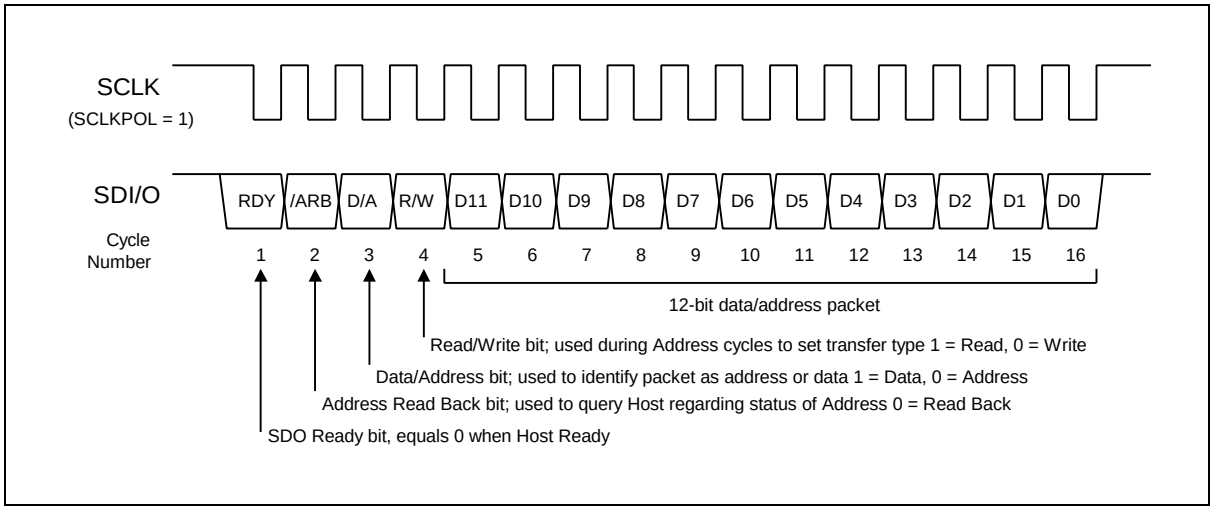


Figure 22: Host Interface Protocol

Note that Figure 22 represents the general case. In various transfer modes, some of the control bits or data bits may not be used. The specific pattern is detailed below for each transfer mode.

5.9.5.1 Bus Transfer Cycles

Four types of transfer cycles are supported, as well as START and STOP conditions. The transfer cycles supported are:

1) Address Transfer
2) Address Read Back (ARB) Transfer
3) Write Data Transfer
4) Read Data Transfer

Each individual bus transfer consists of 16 SCLK periods with address, data, or control information transferred to/from the gmFC1 Host Interface with each rising SCLK.

5.9.5.2 START Condition

A START condition is initiated by the external Host Controller asserting $\overline{SCS}$. This indicates to the Host Interface that serial transfers are about to take place, and forces initialization of the Host Interface bit counters and transfer state machines. The internal address pointer and stored AUTOINC bit are not affected.

The first transfer to take place following the falling edge of $\overline{SCS}$ should typically be an address transfer to set the Host Interface to read or write mode, initialize the internal address pointer and set the address increment mode governing the Host Interface until the next address cycle.

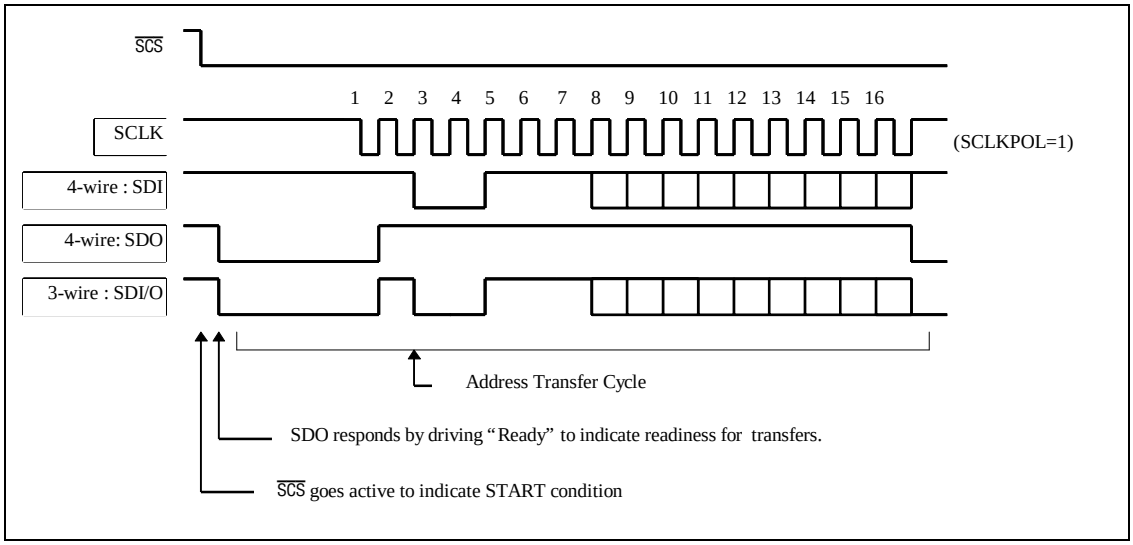


Figure 23: Host Interface START cycle (followed by Address)

5.9.5.3 Address Transfers

Address transfers are used to transfer the following information to the gmFC1 Host Interface:

1) Set the Host Interface to Read or Write Mode.
2) Set the selected device internal register address.
3) Configure the device for static or auto-increment address operation.

An address transfer is always indicated during the second and third bit periods of the transfer with $\overline{ARB}$ bit = '1' and D/A = '0'. The gmFC1 Host Interface responds to an address transfer by sampling and storing the AUTOINC bit and current address from the SDI input. If the Host Interface was previously in the READY state, it moves to either the Write Mode state or Read Mode state, depending on the value of the R/W bit. If the Host Interface is already in one of the two latter states, the R/W bit is ignored.

The AUTOINC bit provides the following addressing information to the Host Interface:

AUTOINC = 0: Addressing mode is "Static". The address written during this cycle remains constant for all subsequent Write Data Transfer, Read Data Transfer and ARB operations. This mode is used to perform individual write or read cycles to the Host Interface. This mode is also intended for polling applications where a single status register is read repeatedly over an extended period of time with no need for repeated address transfers.

AUTOINC = 1: Addressing mode is "Auto-increment". The address written during this cycle provides the initial address pointer value until the first Read Data Transfer or Write Data Transfer cycle occurs. The address increments at the completion of every Read Data or Write Data Transfer cycle. This mode is used for burst loading or reading a contiguous set of registers within the device.

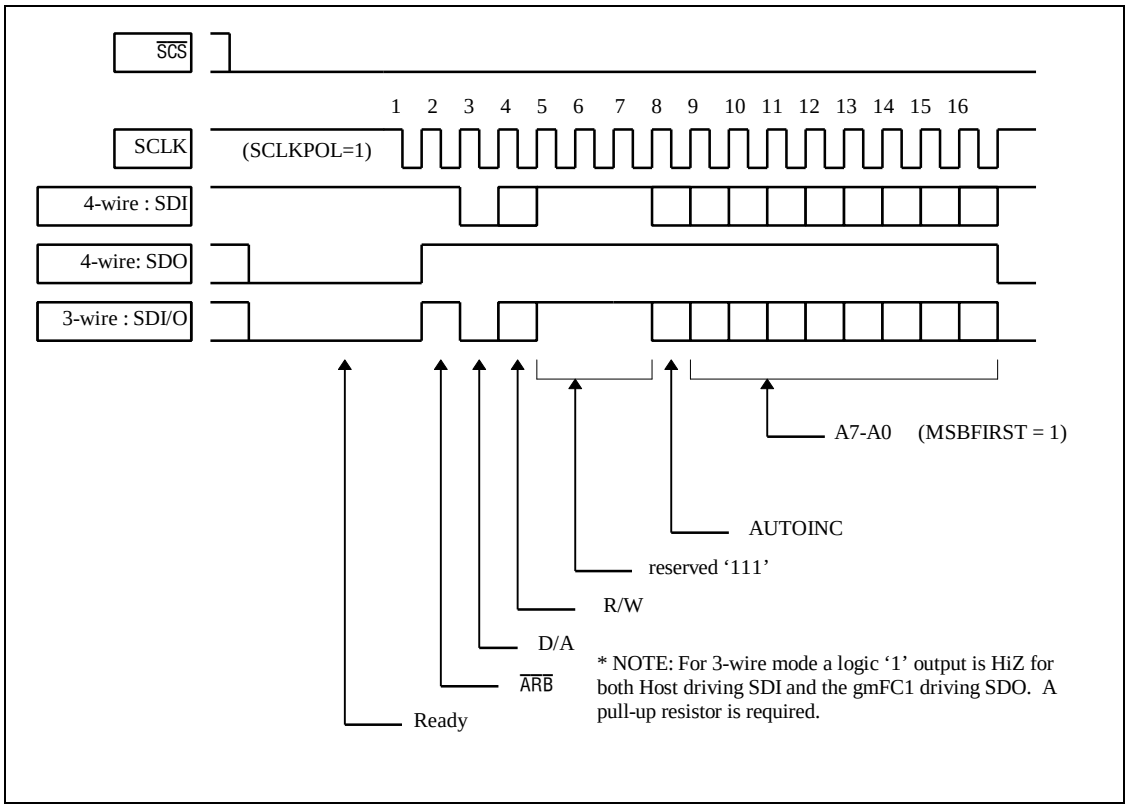


Figure 24: Host Interface Address Transfer

5.9.5.4 Address Read Back Transfers

Address read back (ARB) transfers are used to transfer the gmFC1 Host Interface register address value and auto-increment control bit to the external host. This transfer cycle is typically used to verify Host Interface operation. A complete read back operation is performed in a single 16-clock transfer cycle.

The address read back cycle is invoked through the external controller by setting the $\overline{\text{ARB}}$ bit (second bit) = '0'. The AUTOINC bit and present address pointer value are driven by the gmFC1 on SDO during the last nine bit periods. This special read back cycle is non-intrusive, and will not change the value of the present address counter, or AUTOINC bit, or the state of the Host Interface.

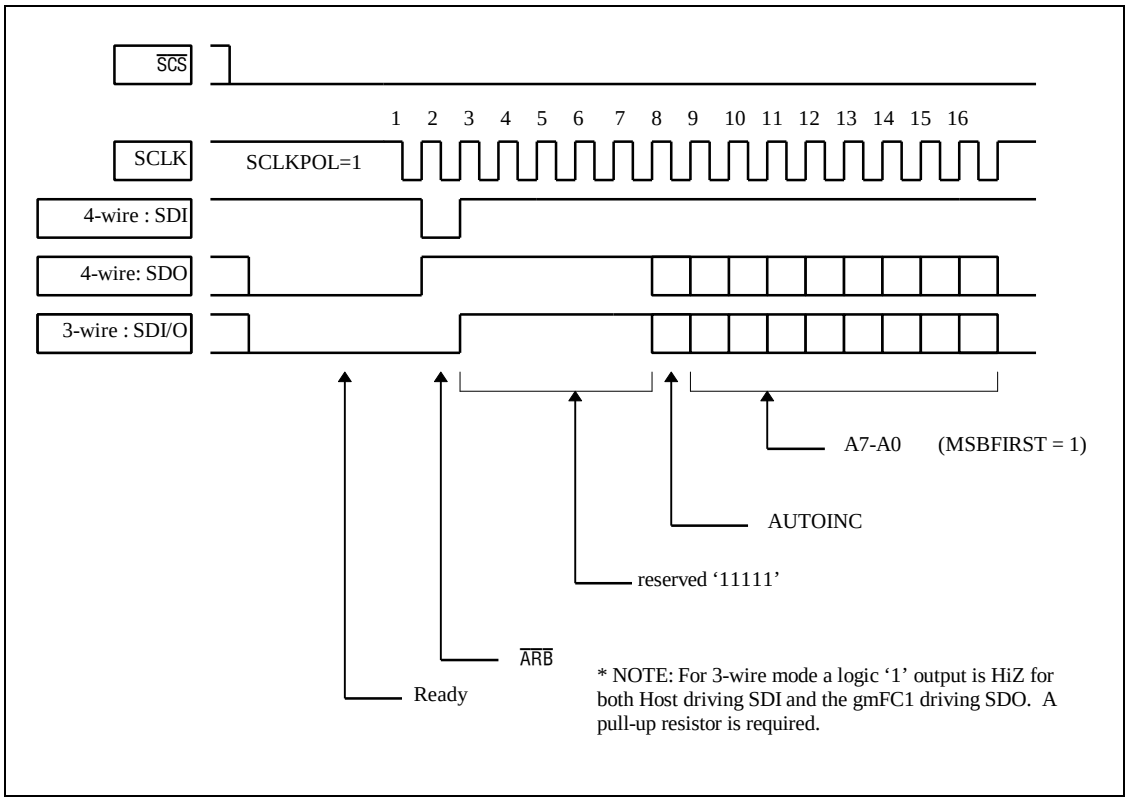


Figure 25: Host Interface Address Read Back (ARB) Transfer

5.9.5.5 Write Data Transfers

Write Data Transfers are used to transfer data from the Host Controller to the gmFC1 via the Host Interface. The data is written to the register referenced by the current address pointer. An Address Transfer must have been executed prior to this operation to determine the register address.

Write Data Transfers may occur in groups or between other Address, or ARB transfers. If the AUTOINC bit is set during the most recent Address Transfer, the address increments upon completion of the Write Data Transfer.

A Write Data Transfer only occurs when the Host Interface is in the Write Mode state and is indicated by $\overline{ARB}$ = '1' and D/A = '1' during the third and fourth bit periods of the transfer cycle. The Host Interface responds to a Write Data Transfer by driving a '0' (ready indication) followed by 15 '1's onto SDO as shown in Figure 26. Data is strobed in on the falling edge of SCLK.

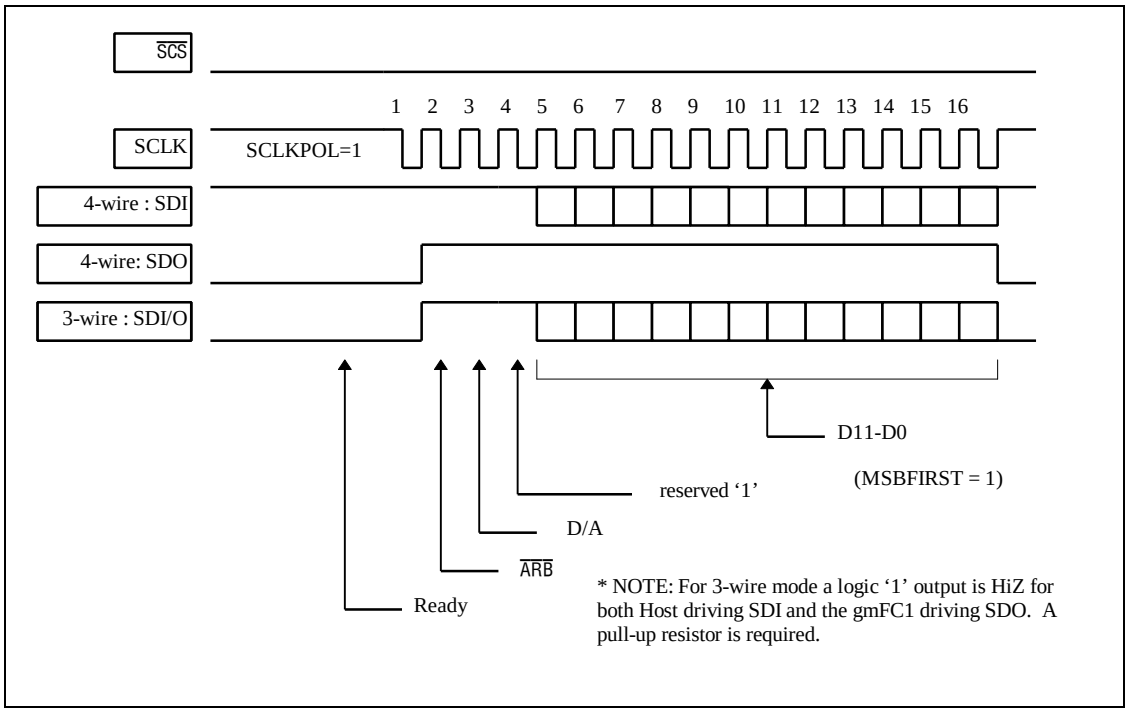


Figure 26: Host Interface Write Data Transfer

5.9.5.6 Read Data Transfers

Read Data Transfers are used to transfer data from the gmFC1 Host Interface to the Host Controller. The data source is a readable register whose address matches the current address. An Address Transfer must have been executed prior to this operation to determine the address.

Read Data Transfers may occur in groups, between other Address transfers, or between ARB transfers.

If the AUTOINC bit were set during the most recent Address Transfer, the address increments upon completion of the Read Data Transfer.

A Read Data Transfer only occurs when the Host Interface is in Read Mode state, and is indicated by $\overline{ARB}$ ='1' and D/A = '1' during the second and third bit periods of the transfer. The Host Interface responds to a Read Data Transfer by driving the addressed register data onto the SDO output as shown below in Figure 27.

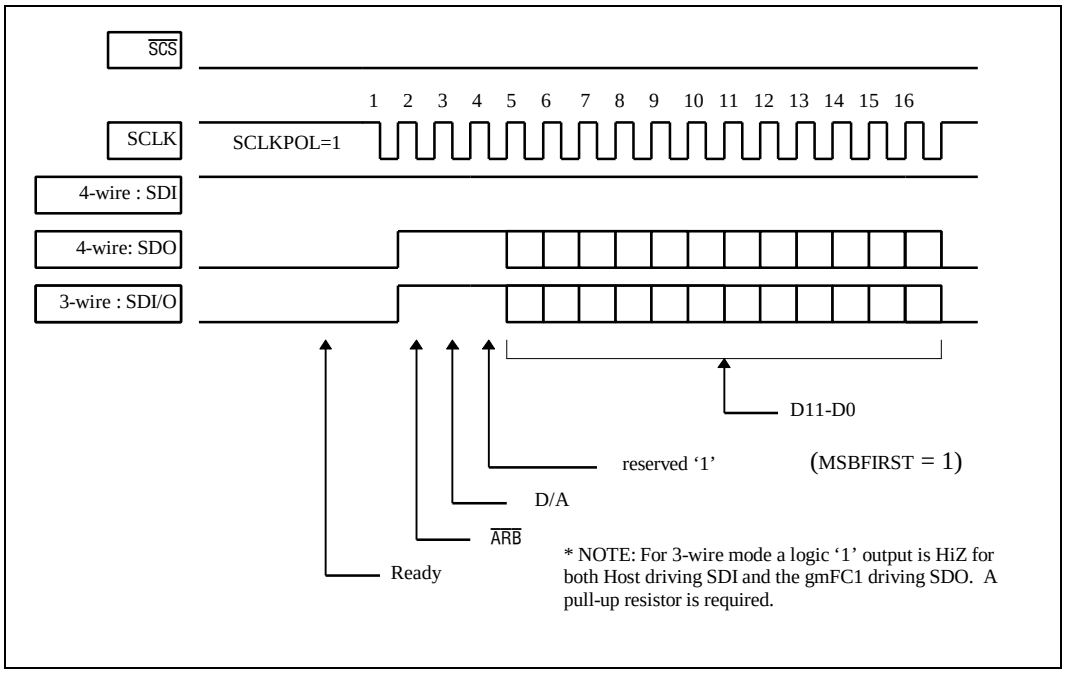


Figure 27: Host Interface Read Data Transfer

5.9.5.7 STOP Condition

The STOP event is used to indicate to the Host Interface that serial transfers are terminated. The external controller imposes a STOP event by de-asserting $\overline{SCS}$. The gmFC1 leaves SDO in a passive '1' state.

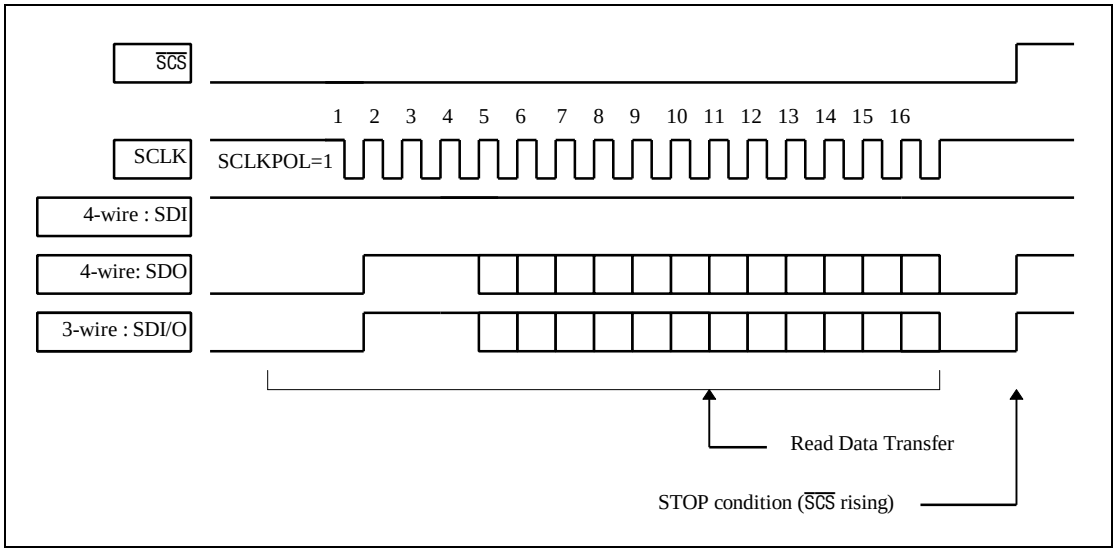


Figure 28: Host Interface STOP condition

5.9.6 Typical Usage Scenarios

The above cycles may be grouped within one $\overline{SCS}$ active low period to perform different types of Bus Cycles. Typically, most applications group them to form the following four types of Bus Cycles:

1) Single Write
2) Single Read
3) Burst Write
4) Burst Read

Single read and single write cycles are composed of two 16-clock transfers while burst cycles involve three or more transfers. The first transfer (address) provides the gmFC1 addressing information, the second (and subsequent) transfers provide data.

5.9.6.1 Single Write Transfers

Single Write Transfers are accomplished by performing the following sequence:

1) Force a START condition by asserting $\overline{SCS}$.
2) Execute an ADDRESS TRANSFER to set the register address with R/W = '0'.
3) Execute a WRITE DATA TRANSFER to transfer data to the selected address.
4) Force a STOP condition by de-asserting $\overline{SCS}$.

5.9.6.2 Burst Write Transfers with Address Auto-increment

Burst Write Transfers are accomplished by performing the following sequence of events:

1) Force a START condition by asserting $\overline{SCS}$.
2) Execute an ADDRESS TRANSFER with R/W = '0' and AUTOINC ='1' to set the register address with auto-increment on.
3) Execute a WRITE DATA TRANSFER to transfer the data to the first selected address. (Note that the address will auto-increment after the first data transfer is written.)
4) Execute subsequent WRITE DATA TRANSFER cycles to transfer data to sequentially addressed registers. There is no limit to the number of data transfers that may occur during a burst, as long as addresses remain valid.
5) Force a STOP condition by de-asserting $\overline{SCS}$.

5.9.6.3 Single Read Transfers

Single Read Transfers may be accomplished by performing the following sequence of events:

1) Force a START condition by asserting $\overline{SCS}$.

2) Execute an ADDRESS TRANSFER with R/W = '1' to set the register address.

3) Execute a READ DATA TRANSFER to transfer data from the selected address to the Host Controller.

4) Force a STOP condition by de-asserting $\overline{SCS}$.

5.9.6.4 Burst Read Transfers

Burst Read Transfers may be accomplished by performing the following sequence of events:

1) Force a START condition by asserting $\overline{SCS}$.

2) Execute an ADDRESS WRITE TRANSFER with R/W = '1' and AUTOINC = '1' to set the register address with auto-increment on.

3) Execute a READ DATA TRANSFER to transfer data to the first selected address. (Note that the address will auto-increment after the first data transfer is written.)

4) Execute subsequent READ DATA TRANSFER cycles to transfer data from the sequentially addressed registers to the Host Controller. There is no limit to the number of data transfers that may occur during a burst, as long as addresses remain valid.

5) Force a STOP condition by de-asserting $\overline{SCS}$.

5.9.6.5 Frame Store Read Transfers

The procedure for reading the frame store from the host microcontroller is as follows:

1. The input and output must be disabled and a Force Update performed in order for the host to properly read the frame store. This may be accomplished by setting the MISC register bit OUTP_EN = 0, the IPCTRL register bit INP_EN = 0, and performing a Force Update.
2. Write the desired initial host frame store read address into OP_MEM_STARTL and OP_MEM_STARTH, and perform a Force Update.
3. Strobe the SOFT_RESET bit in the HOSTCTRL register.
4. Read the frame store contents out from HOST_MEMDATA. Each read will return, in order, Blue, Green, then Red data, then automatically advance to the next pixel. Note that $\overline{SCS}$ must remain asserted during data reads.

Performing reads will automatically advance the HOST_MEMDATA data to the next pixel according to the frame store related parameters. For example, after OPH_MEM_WIDTH number of frame store reads, the frame store address will increment to the start of the next line.

5.9.6.6 Frame Store Write Transfers

The procedure for writing to the frame store from the host microcontroller is as follows:

1. The input must be disabled and a Force Update performed in order for the host to properly read the frame store. This may be accomplished by setting the IPCTRL register bit INP_EN = 0, and performing a Force Update.
2. Write the desired initial host frame store write address into HOST_WRADDRL and HOST_WRADDRH, and perform a Force Update.
3. Write the contents of HOST_MEMDATA to the frame store in the order Red, Green, Blue data. Each complete pixel write will automatically increment the frame store write address to the next pixel location.
4. When writing the final pixel, set the MISC register bit HWR_FLUSH=1. Write the final pixel, and reset HWR_FLUSH=0.

5.9.6.7 Performing Polling Transfers

Polling operations may be performed without the need for multiple address transfers on the bus as follows:

1) Force a START condition by asserting $\overline{SCS}$.
2) Execute an ADDRESS TRANSFER with R/W bit = '1' and AUTOINC = '0' to set the register address to an appropriate STATUS register.
3) Execute a READ DATA TRANSFER to transfer data from the selected address to the Host Controller. Repeat the READ DATA TRANSFER as many times as necessary until the event being polled for occurs.
4) Force a STOP condition by de-asserting $\overline{SCS}$.

5.9.7 Host Interface Registers

5.9.7.1 Host Interface Register Space

Table 5 details the on-chip registers accessible through the gmFC1 Host Interface. Register addresses are given in hexadecimal, and any individual control bits are named. Bit '0' is always the LSB of a register.

5.9.7.2 Reset Conditions

All registers are addressable from bit 0 to bit 11. Bits not defined in Table 5 below should be programmed to '0'.

All host writable register contents default to '0' as the result of a hard reset, except the SOFT_RESET bit 00 and RESERVED bit 08 in the HOSTCTRL register. Writable register contents are not affected by a SOFT_RESET.

Table 5: Host Interface Registers

Identification Register

Address (Hex) : 00	Register : ID_REG	Mode : R
CONTROL BIT	**CONTROL BIT NAME**	**FUNCTION**
bits [0-3]	---	Revision Code = 0010 (2^{nd} rev)
bits [4-11]	---	Product Code = 00111100

Status Register

Address (Hex) : 01	Register : STATUS	Mode : R
STATUS is a read-only register, providing information about the state of gmFC1 operation		
CONTROL BIT	**CONTROL BIT NAME**	**FUNCTION**
0	MEMRDY	Memory Ready After a hard or soft reset, the frame store controller will automatically initialize the SDRAM memory devices. During this time, the memory cannot be accessed. This bit is set to '1' when the memory is available for access.
1	IP_ODD	Input ODD State. This bit represents the current state of the InODD signal (or the internally decoded ODD state, if applying an RGB Vertical Interlaced input with the IPCTRL register EXTGODD_EN set to 0) .
2	IP_OVFLOW	Input Overflow. Input data captured by the gmFC1 is internally buffered until the frame store interface is available (the frame store is also being used for the output data stream, and for periodic refresh). If data is input at a rate greater than the gmFC1 can handle, the internal buffer may overflow, setting this bit to '1'. Remains set until the STATUS register is read.
3	IP_ODDERR	Input ODD Error. In interlaced modes, the input ODD signal should toggle every VSYNC period. If it does not toggle, this bit is set to '1'. Remains set until the STATUS register is read.
4	IP_VSERR	Input Vertical Sync Time-out Error. If the input VSYNC signal does not occur within (2^{22} x fsCLK period) this bit will be set to '1'. This bit may be used to detect loss of the input signal. Remains set until the STATUS register is read.
5	IP_MIDHSYNC	If an input active HSYNC edge occurs within the programmed active period, this bit is set to '1', indicating a format error and incorrect input capture. This condition must be corrected by reducing IPH_ACTIV_START or IPH_ACTIV_WIDTH. Remains set until the STATUS register is read.
6	IP_MIDVSYNC	If an input active VSYNC edge occurs within the programmed active period, this bit is set to '1', indicating a format error and incorrect input capture. This condition must be corrected by reducing IPV_ACTIV_START or IPV_ACTIV_WIDTH. Remains set until the STATUS register is read. Note: for correct input capture, (IPV_ACTIV_START + IPV_ACTIV_LNGTH + 1) <= total vertical # of lines
7	IPYUV_VS	When an active InVVS edge occurs, this bit is set to '1'. Remains set until the STATUS register is read. IPYUV_VS remains available even when the gmFC1 is in Low Power Mode.
8	IPRGB_VS	When an active InGVS edge occurs, this bit is set to '1'. Remains set until the STATUS register is read IPRGB_VS remains available even when the gmFC1 is in Low Power Mode.
9	OP_VS	When OutVS is asserted, this bit is set to '1'. Remains set until the STATUS register is read
10	MEAS_VALID	If an HSYNC or VSYNC measurement has been completed, this bit is set to '1'. If a change occurs in MEAS_VS_nHS or PERIOD_nACTIVE registers, this bit is cleared to '0'

Miscellaneous Control Register

Address (Hex) : 02	Register : MISC	Mode : R/W

Note: Writing to the MISC register has an immediate effect on the gmFC1 operation (there is no Pending Register).

CONTROL BIT	CONTROL BIT NAME	FUNCTION
0	OP_VINTLC_EN	Output Vertical Interlace Enable If '1', and if IP_VINTLC_EN is '1', the output data stream will be vertically interlaced. Otherwise, the output will be progressive scan. If '0' and if IP_VINTLC_EN = '1', de-interlacing is performed by 'static mesh' merging of odd / even input fields.
1	OP_GTR_IN	Output Greater than Input (used with Progressive Scan inputs only) This bit is used to indicate the relative frame rates of input and output data streams. If '1', the output data frame rate is greater than the input rate. If '0', the input data frame rate is greater than the output rate. This information is used by the gmFC1 when double buffering to decide when to swap buffers.
2	FS_PWRDWN	Frame Store Power Down Enable If set to '1', will request the frame store controller put the external SDRAM devices into a low-power, non-operational mode. After bringing the devices out of this mode, a soft reset is required.
3	REVSCAN	Reverse Scanning Enable If '1', the output image is scanned out from bottom to top (i.e., the image is flipped) If '0', the output image is scanned out top to bottom (i.e., the image is normal)
4	FSDB_EN	Frame Store Double Buffering Enable (used with Progressive Scan inputs only) If set to '1', will enable the non-frame tearing, double buffered mode of frame rate conversion.
5	HWR_FLUSH	Used during host write access to the frame store. Must be set to '1' while the final pixel is written. See Register Address (Hex) 17, HOST_MEMDATA below.
6	OUTP_EN	Output Enable If set to '1', enables the output circuitry. If set to '0', the gmFC1 will ignore all control signals on the output (gmZ1/2/3) interface, and will not transfer data. The output must be disabled for the host to read the frame store.
7	BYPASS_EN	Bypass Mode Enable If set to '1', the gmFC1 will operate in Bypass Mode, effectively transferring input data and control information to corresponding pins on the output (gmZ1/2/3) interface.
8	OP_HANDSH	Output Handshake Control Selects between two modes of output interface handshake control. If '0', the output interface will slave to data requests from the DATAREQ pin. (not used for gmZ1/2/3 interface) If '1', the output will begin to output data OPH_ACTIV_START clocks after OutHS is asserted.
9	IP_FLOCK_EN	Input Frame Lock Enable If '1', enables input-output frame lock.
10	IP_HSPHASE	Input Horizontal Sync Phase Selects the default phase relationship between input HSYNC and the input clock. Selects the active clock edge for HSYNC sampling independent of the programmed input clock polarity.
11	TRISTATE	Tristate Outputs If '1', places all gmFC1 outputs except SDO and $\overline{IRQ}$ in hi-z mode. (tri-stated)

Host Interface and Main Control Register

Address (Hex) : 03	Register : HOSTCTRL	Mode : R/W

Note: Writing to the HOSTCTRL register has an immediate effect on the gmFC1 operation (there is no Pending Register).

CONTROL BIT	CONTROL BIT NAME	FUNCTION
0	SOFT_RESET	Setting this bit to '1' forces the gmFC1 into a reset state, in which the input, output, and frame store interfaces are halted. All non-user-accessible internal registers are brought to a default state. The host interface registers are not affected by a SOFT_RESET. Host Interface registers may be accessed and modified while the gmFC1 is in a soft reset condition. This bit is forced to '1' by a hard reset, i.e., the gmFC1 will 'power-up' in a soft reset state.
1	HI4WIRE_EN	Host Interface Four Wire Mode Enable This bit determines the mode of the host electrical interface. If '1', the host interface operates in 4-wire mode. If '0', the host interface operates in 3-wire mode.
2	IN_UPDATE_EN	Input Parameters Update Enable If set to '1', allows registers associated with the gmFC1 input parameters to become active at the next input vertical sync leading edge (of the selected port). This allows parameters to be modified while the input interface is operational, and ensures they all take effect at the same point in time. The bit is automatically reset to '0' after the update occurs.
3	OUT_UPDATE_EN	Output Parameters Update Enable If set to '1', allows registers associated with the gmFC1 output parameters to become active at the next output frame reset. This allows parameters to be modified while the output interface is operational, and ensures they all take effect at the same point in time. The bit is automatically reset to '0' after the update occurs.
4	IN_FORC_UPDATE	Input Parameters Force Update Setting this bit to '1' forces the gmFC1 input parameters to become active immediately. Used when no video timing is present, and prior to coming out of a soft reset. The bit is automatically cleared to '0'.
5	OUT_FORC_UPDATE	Output Parameter Force Update Setting this bit to '1' forces the gmFC1 output parameters to become active immediately. Used when no video timing is present, and prior to coming out of a soft reset. The bit is automatically cleared to '0'.
6	PWRDWN	Power Down If '1', the gmFC1 will enter a low power, non-functional mode of operation.
7	IP_RGB_nYUV	Input RGB or YUV This bit selects the source of input information. If '1', the gmFC1 uses the 24-bit RGB port. If '0', the gmFC1 will use the 16-bit YUV port.
8	RESERVED	Program this bit to '1'
9	MEAS_VS_nHS	If '1', the vertical sync of the selected input port will be measured. If '0', the horizontal sync of the selected input port is measured. If the selected input is the RGB port, the horizontal sync measurement is made from the InRawGHS. Measurement result is placed in the MEAS_RESULTL register.
10	PERIOD_nACTIVE	If '1', the full period of the selected sync signal is measured (rising edge to next rising edge). If '0', the signal 'high' time duration only is measured (rising edge to falling edge). (See MEAS_VS_nHS above for further information)

Interrupt Control Register

Address (Hex) : 04	Register : IRQMASK	Mode : R/W

IRQMASK bits provide control of the external interrupt request ($\overline{IRQ}$) output pin. By setting the desired interrupt bits below, any combination of interrupt sources may be programmed to cause $\overline{IRQ}$ to become asserted. A single bit (IRQ_OUT_EN) is provided as a master interrupt enable. Reading the STATUS register will clear all sources of interrupts.

Note: Writing to the IRQMASK register has an immediate effect on the gmFC1 operation (there is no Pending Register).

CONTROL BIT	CONTROL BIT NAME	FUNCTION
0	RESERVED	Program this bit to '0'
1	OP_VS	Output Vertical Sync Interrupt If '1', the output vertical sync is programmed to cause an interrupt.
2	IP_OVFLOW	Input Buffer Overflow Interrupt If '1', an overflow condition on the internal input buffer is programmed to cause an interrupt.
3	IP_ODDERR	Input ODD Error Interrupt If '1', and if the input ODD signal does not toggle every VSYNC in interlaced modes, an interrupt is generated.
4	IP_VSERR	Input Vertical Sync Time-out Error Interrupt If '1', loss of input VSYNC is programmed to cause an interrupt.
5	IP_FERR	Input Format Error Interrupt If '1', an input format error (mid-line HSYNC, mid-field VSYNC) is programmed to cause an interrupt.
6	RESERVED	Program this bit to '0'
7	IPYUV_VS_EN	Input YUV Vertical Sync Interrupt If '1', InVVS input vertical sync is programmed to cause an interrupt.
8	IPRGB_VS_EN	Input RGB Vertical Sync Interrupt If '1', InGVS input vertical sync is programmed to cause an interrupt.
9	RESERVED	Program this bit to '0'
10	IRQ_OUT_EN	Interrupt Request Output Enable Controls the use of the $\overline{IRQ}$ pin. If '0', the $\overline{IRQ}$ pin is used to indicate the active input sampling region $\overline{INDATAACTIVE}$. If '1', the $\overline{IRQ}$ pin is used to interrupt the microcontroller based on the IRQMASK conditions. Default value = '0'

Input Port Control Register

Address (Hex) : 05	Register : IPCTRL	Mode : R/W

This register provides a programmable polarity on many of the input port control signals. A bit position set to '1', will cause the corresponding signal of the selected input port to become active low. By default, all signals are active high. This register has an input related active/pending register pairing.

CONTROL BIT	CONTROL BIT NAME	FUNCTION
0	IPCLK_INV	Input Clock Invert Enable If set to '1', will cause falling edge of CLK to become the active edge.
1	IPCREF_INV	Input CREF Invert Enable. If set to '1', will cause CREF on the selected input port to become active low.
2	IPVS_INV	Input Vertical Sync Invert Enable. If set to '1', will cause VS on the selected input port to become active low.
3	IPHS_INV	Input Horizontal Sync Invert Enable. If set to '1', will cause HS on the selected input port to become active low.
4	EXTGODD_EN	External ODD Signal Enable (Graphics) By default, odd and even field detection of vertically interlaced graphics (RGB) data is performed automatically, based on the VSYNC and HSYNC relationship. Setting this bit to '1', forces the gmFC1 to use the external InODD signal to determine the odd and even fields. When the video (YUV) port is selected as the data source, the external InODD signal is always used.
5	IPODD_INV	Invert InODD If set to '1', will invert the InODD input signal
6	IPCLAMP_INV	Input CLAMP Invert Enable If set to '1', will invert the CLAMP input signal
7	INP_EN	Input Data Sampling Enable. If set to '1', enables the input circuitry. If '0', the gmFC1 will not capture and store input data, allowing a 'freeze-frame' mode. The input must be disabled for the host to write to the frame store memory.
8	IP_VINTLC_EN	Input Vertical Interlace Enable If '1', the input is interpreted as vertically interlaced data. This bit must not be enabled at the same time as IP_HINTLC_EN.
9	IP_HINTLC_EN	Input Horizontal Interlace Enable If '1', the input is interpreted as horizontally interlaced data, and the INVADC output will toggle on every frame, inverting the ADC sampling clock. This bit must not be enabled at the same time as IP_VINTLC_EN.
10	IP_INV_INV	Invert INVADC If '1', inverts the default polarity of the INVADC (the ADC sample clock invert) pin.
11	HSPHASE_TGL	Horizontal Sync Phase Toggle If '1', the InGCLK edge used to sample InGHS is automatically toggled after every InGVS. Used with horizontal interlaced inputs (IP_HINTLC_EN=1). Some PLL/ADC devices supporting horizontal interlacing (e.g., Philips TDA8752) keep HSYNC fixed to an internal clock reference, but shift the output clock (i.e., gmFC1's InGCLK) 180 degrees based on the field. Relative to InGCLK, the InGHS switches between being driven on rising and falling edges. In this case, HSPHASE_TGL= 1. In other systems, InGHS is always driven on the same InGCLK phase, and HSPHASE_TGL= 0.

Input Control Registers

Address (Hex) : 06	Register : IPH_ACTIV_STARTODD	Mode : R/W
CONTROL BIT	**RANGE**	**FUNCTION**
bits [0-10]	9 - 2047 (decimal)	Input Horizontal Active Start Odd / Non Interlaced Active Start (11 bits) This register is used to indicate the left edge of the input active region. The number of input clocks are counted from the active edge of the input HSYNC before data is sampled. Used in all modes except for even fields of horizontal interlaced input.

Address (Hex) : 07	Register : IPH_ACTIV_STARTEVEN	Mode : R/W
CONTROL BIT	**RANGE**	**FUNCTION**
bits [0-10]	9 - 2047 (decimal)	Input Horizontal Active Start Even (11 bits) This register is used to indicate the left edge of the input active region. The number of input clocks are counted from the active edge of the input HSYNC before data is sampled. Used only on even fields of horizontal interlaced input.

Address (Hex) : 08	Register : IPH_ACTIV_WIDTH	Mode : R/W
CONTROL BIT	**RANGE**	**FUNCTION**
bits [0-10]	2 - 2047 (decimal)	Input Horizontal Active Width (11 bits) This register indicates the number of active pixels within a line of input data.

Address (Hex) : 09	Register : IPV_ACTIV_STARTODD	Mode : R/W
CONTROL BIT	**RANGE**	**FUNCTION**
bits [0-10]	1 - 2047 (decimal)	Input Vertical Active Start - Odd Field / Non-interlaced Active Start (11 bits) This register indicates the number of lines from the start of the input VSYNC before active lines are sampled. This value is used in non-vertical interlace modes, and in the ODD field of Vertical Interlace mode.

Address (Hex) : 0A	Register : IPV_ACTIV_STARTEVEN	Mode : R/W
CONTROL BIT	**RANGE**	**FUNCTION**
bits [0-10]	1 - 2047 (decimal)	Input Vertical Active Start - Even Field (11 bits) This register indicates the number of lines from the start of the input VSYNC before active lines are sampled. This value is used only in Vertical Interlace mode on EVEN fields.

Address (Hex) : 0B	Register : IPV_ACTIV_LNGTH	Mode : R/W
CONTROL BIT	**RANGE**	**FUNCTION**
bits [0-10]	1 - 2047 (decimal)	Input Vertical Active Length (11 bits) This value indicates the number of lines within the active input region.

Clamp Signal Control Registers

Address (Hex) : 0C	Register : IP_CLAMP_START	Mode : R/W
CONTROL BIT	**RANGE**	**FUNCTION**
bits [0-10]	9 - 2047 (decimal)	Start of Input Clamp Signal Pulse (11 bits) This value represents the number of input clocks between the active edge of the input HSYNC and the start of the gmFC1 output signal CLAMP. If programmed = '0', no CLAMP signal occurs.

Address (Hex) : OD	Register : IP_CLAMP_END	Mode : R/W
CONTROL BIT	**RANGE**	**FUNCTION**
bits [0-10]	min. IP_CLAMP_START+1 max. 2047 (decimal)	End of Input Clamp Signal Pulse (11 bits) This value represents the number of input clocks between the active edge of the input HSYNC and the end of the gmFC1 output signal CLAMP.

Address (Hex) : OE	Register : IPH_MEM_WIDTH	Mode : R/W
CONTROL BIT	**RANGE**	**FUNCTION**
bits [0-10]	1 - 2047 (decimal)	Input Frame Store Image Width (11 bits) This value represents the active input image width in terms of frame store addresses. Set IPH_MEM_WIDTH >= *ceil* (IPH_ACTIV_WIDTH / 2) where the function *ceil (x)* returns the nearest integer not less than *(x)*.

Output Control Registers

Address (Hex) : OF	Register : OPH_MEM_WIDTH	Mode : R/W
CONTROL BIT	**RANGE**	**FUNCTION**
bits [0-10]	>= 1 <= IPH_MEM_WIDTH	Output Frame Store Image Width (11 bits) This value represents the active output image width in terms of frame store addresses. The value is dependent on OPH_ACTIV_WIDTH. OPH_MEM_WIDTH should be set according to the following equations: If IP_HINTLC_EN == 0: OPH_MEM_WIDTH = (OPH_ACTIV_WIDTH / 2) If IP_HINTLC_EN == 1: OPH_MEM_WIDTH = (OPH_ACTIV_WIDTH / 4)

Address (Hex) : 10	Register : OP_MEM_STARTL	Mode : R/W
CONTROL BIT		**FUNCTION**
bits [0-11]		Output Frame Store Image Start (low 12 bits) This register combined with OP_MEM_STARTH makes up the OP_MEM_START value. This is programmed with the starting position (upper left), in the frame store, where the output image will be read from. This value allows positioning of a smaller output image within a captured input image. To position the output image an offset Y_OFFSET lines from the captured input start, and an offset X_OFFSET pixels from the captured image left edge: Proscan: OP_MEM_START= IPH_MEM_WIDTH * Y_OFFSET + *int* (X_OFFSET / 2) V. Interlaced: OP_MEM_START= IPH_MEM_WIDTH * *int* (Y_OFFSET/2) + *int* (X_OFFSET / 2) H. Interlaced: OP_MEM_START= IPH_MEM_WIDTH * Y_OFFSET + *int* (X_OFFSET / 4) where the function *int (x)* returns the nearest integer not greater than *(x).*

Address (Hex) : 11	Register : OP_MEM_STARTH	Mode : R/W
CONTROL BIT		**FUNCTION**
bits [0-6]		Output Frame Store Image Start (high 7 bits) This register combined with OP_MEM_STARTL makes up the OP_MEM_START value. See OP_MEM_STARTL.

Address (Hex) : 12	Register : OPV_LENGTH	Mode : R/W
CONTROL BIT	**RANGE**	**FUNCTION**
bits [0-10]	6 - 2047 (decimal)	Output Vertical Image Length (11 bits) This register is programmed with the number of lines in the output image. In horizontal interlaced mode this register is programmed to a value double the number of desired output lines.

Address (Hex) : 13	Register : OPH_ACTIV_START	Mode : R/W
CONTROL BIT	**RANGE**	**FUNCTION**
bits [0-10]	8 - 2047 (decimal)	Output Horizontal Active Start The gmFC1 will count OPH_ACTIV_START output clocks from the leading edge of OutHS before providing output data when the OP_HANDSH bit = '1'

Address (Hex) : 14	Register : OPH_ACTIV_WIDTH	Mode : R/W
CONTROL BIT		**FUNCTION**
bits [0-10]		Output Horizontal Active Width (11 bits) This register is programmed with the number of pixels of the output image width. i.e.: OPH_MEM_WIDTH *2 for Progressive Scan signals OPH_MEM_WIDTH *4 for Horizontal Interlaced signals

Address (Hex) : 15	Register : HOST_WRADDRL	Mode : W
Note: Writing to the HOST_WRADDRL register has an immediate effect on the gmFC1 operation (there is no Pending Register).		
CONTROL BIT		**FUNCTION**
bits [0-9]		Host Frame Store Write Address (low 10 bits) This register, combined with HOST_WRADDRH, makes up the host to frame store write address. The host can initialize these registers to point anywhere into the frame store. Subsequent writes to the HOST_MEMDATA register cause data to be transferred into the frame store starting from this address. The input must be disabled (INP_EN = '0') for the host to properly write to the frame store.

Address (Hex) : 16	Register : HOST_WRADDRH	Mode : W
Note: Writing to the HOST_WRADDRH register has an immediate effect on the gmFC1 operation (there is no Pending Register).		
CONTROL BIT		**FUNCTION**
bits [0-9]		Host Frame Store Write Address (high 10 bits) This register, combined with HOST_WRADDRL, makes up the host to frame store write address. The host can initialize these registers to point anywhere into the frame store. Subsequent writes to the HOST_MEMDATA register cause data to be transferred into the frame store starting from this address. The input must be disabled (INP_EN = '0') for the host to properly write to the frame store.

Frame Store Control Registers

Address (Hex) : 17	Register : HOST_MEMDATA	Mode : R/W
Note: Writing to the HOST_MEMDATA register has an immediate effect on the gmFC1 operation (there is no Pending Register).		
CONTROL BIT		**FUNCTION**
bits [0-7]		Host Frame Store Read/Write Data (8 bits) This register is used during host microcontroller external frame store memory read and write operations. The 8-bit HOST_MEMDATA register location is used to write a full 24-bit RGB pixel value. Internally, a state machine advances from Red to Green to Blue after each write. The state machine is reset after the third write (Blue value). (The state machine is also reset after accessing any other register). The transfer to the frame store takes place only after the three values have been written. The frame store address will automatically advance after enough data has been written to fill a frame store word. In order to ensure that all data is transferred to the frame store, the final data value should be written with the HWR_FLUSH bit of the MISC register set. This register is also used to read 24-bit RGB values from the frame store. An internal state machine advances from Blue to Green to Red after each read access. After a full pixel read, the next pixel is available. $\overline{SCS}$ must remain asserted from the first to the final pixel read.

SYNC Status Registers

Address (Hex) : 1A	Register : MEAS_RESULTL	Mode : R
CONTROL BIT		**FUNCTION**
bits [0-11]		Input VSYNC / HSYNC Measurement Results (12 bits) This register returns the active duration or the period of the most recent input VSYNC or HSYNC. The parameter measured is controlled by the HOSTCTRL register bits MEAS_VS_nHS and PERIOD_nACTIVE. HS results are expressed in terms of frame store interface clocks divided by 2. (fsCLK / 2) VS results are expressed in terms of lines (i.e., HSYNC pulses)

Clock Phase Adjust Register

Address (Hex) : 23	Register : CLK_PHASE	Mode : R/W
CONTROL BIT	**CONTROL BIT NAME**	**FUNCTION**
bits [0-1]	RESERVED	Program to '0'
2	FS_CLK_PHASE	Frame Store Clock Phase Adjust If `1', the fsCLK is delayed relative to frame store data and control signals. Table 11 and Table 15 specify the relevant setup/hold and propagation times for the two possible states of FS_CLK_PHASE. This bit allows the circuit designer to address, for example, specific PCB effects.
bits [3-11]	RESERVED	Program to '0'

6. Electrical Specifications

The gmFC1 operates under commercial conditions; 0 °C to 70 °C ambient temperature and 3.0 to 3.6 V supply voltage. The gmFC1 provides 5V-tolerant input pads to allow connection to devices using 5V power supplies. All preliminary specifications are derived from simulations.

Table 6: Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
5VDC Supply Voltage(1)	V_{DD}	-0.5		5.5	V
3.3VDC Supply Voltage(1)	V_{DD}	-0.5		3.6	V
5VDC Tolerant Input Voltage(1)	V_{IN}	-0.5		5.5	V
3.3VDC Input Voltage(1)	V_{IN}	-0.5		3.6	V
Electrostatic Discharge(2)	V_{ESD}			±2.0	kV
Latchup(3)	I_{LA}			±100	mA
Ambient Operating Temperature	T_A	0		70	°C
Storage Temperature	T_{STG}	-65		125	°C
Operating Junction Temperature	T_J	0		125	°C
Thermal Resistance	θ_{JA}			25.3	°C/W
Soldering Temperature (30 sec.)	T_{SOL}			210	°C
Vapor Phase Soldering (30 sec.)	T_{VAP}			215	°C

Notes:

(1) Absolute maximum voltage ranges are for transient voltage excursions.
(2) Electrostatic discharge evaluation performed in accordance with Mil-Std-883 method 3015.7.
(3) Latchup testing is done according to JEDEC Standard 17.

All voltages are measured with respect to GND.

6.1 Preliminary DC Characteristics

Table 7: DC Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Operating Voltage	V_{DD}	3.0	3.3	3.6	V
Power Consumption	PD			1.7	W
Supply Current	IDD			470	mA
Input Capacitance	CIN			8	pF
Inputs					
Logic High Voltage - 5V Tolerant	V_{IH5}	2.0		5.0	V
Logic Low Voltage - 5V Tolerant	V_{IL5}	(GND)		0.8	V
Logic High Voltage - 3.3 V Only	V_{IH3}	2.0		VDD	V
Logic Low Voltage - 3.3 V Only	V_{IL3}	(GND)		0.8	V
Clock Logic High Input Voltage	V_{IH}	2.4		5.0	V
Clock Logic Low Input Voltage	V_{IL}	(GND)		0.4	V
Leakage Current	IL	-0.1		1.5	mA
Outputs					
Logic High Voltage (1)	VOH	VDD-1.0			V
Logic Low Voltage (1)	VOL			GND+0.4	V

(1) with current source/sink as specified for driver

Table 8: Output Drive Capability / Input Tolerance

Signal	I/O	Drive	Input Tolerance *
InGCLK	I		5V
InGCREF	I		5V
InGVS	I		5V
InGHS	I		5V
InRawGHS	I		5V
InRED [7:0]	I		5V
InGREEN [7:0]	I		5V
InBLUE [7:0]	I		5V
INVADC / SCLKPOL	I/ O	6 mA	3.3 V
CLAMP / MSBFIRST	I / O	6 mA	3.3 V
InVCLK	I		5V
InVCREF	I		5V
InODD	I		5V
InVVS	I		5V
InVHS	I		5V
InY [7:0]	I		5V
InUV [7:0]	I		5V
RefOutCLK	I		5 V
OutCLK	O	12 mA	
OutVS	O	6 mA	
OutHS	O	6 mA	
OutODD	O	6 mA	
$\overline{\text{OUTSTALL}}$	O	6 mA	
$\overline{\text{LREQ}}$	I		3.3 V
DATAREQ	I		3.3 V
OutRED [7:0]	O	6 mA	
OutGREEN [7:0]	O	6 mA	
OutBLUE [7:0]	O	6 mA	
$\overline{\text{FRAMERESET}}$	I		3.3 V
$\overline{\text{OUTDFSYNC}}$	O	6 mA	
$\overline{\text{RESET}}$	I		5 V
$\overline{\text{SCS}}$	I		5 V
SCLK	I		5 V
SDI	I		5 V
SDO	O	6 mA	
$\overline{\text{IRQ}}$ / $\overline{\text{INDATAACTIVE}}$	O	6 mA	
FSDATA [47:0]	I / O	6 mA	3.3 V
FSADDR [11:0]	O	6 mA	
$\overline{\text{FSRAS}}$	O	8 mA	
$\overline{\text{FSCAS}}$	O	8 mA	
$\overline{\text{FSWE}}$	O	8 mA	
fsCKE	O	6 mA	
$\overline{\text{FSCS}}$	O	6 mA	
fsDQM [1:0]	O	8 mA	
fsRefCLK	I		5 V
fsCLK	O	12 mA	

* 5VDC Input Tolerance is obtained only if the gmFC1 is supplied with 5VDC at pin 13 and 181

6.2 Preliminary AC Characteristics

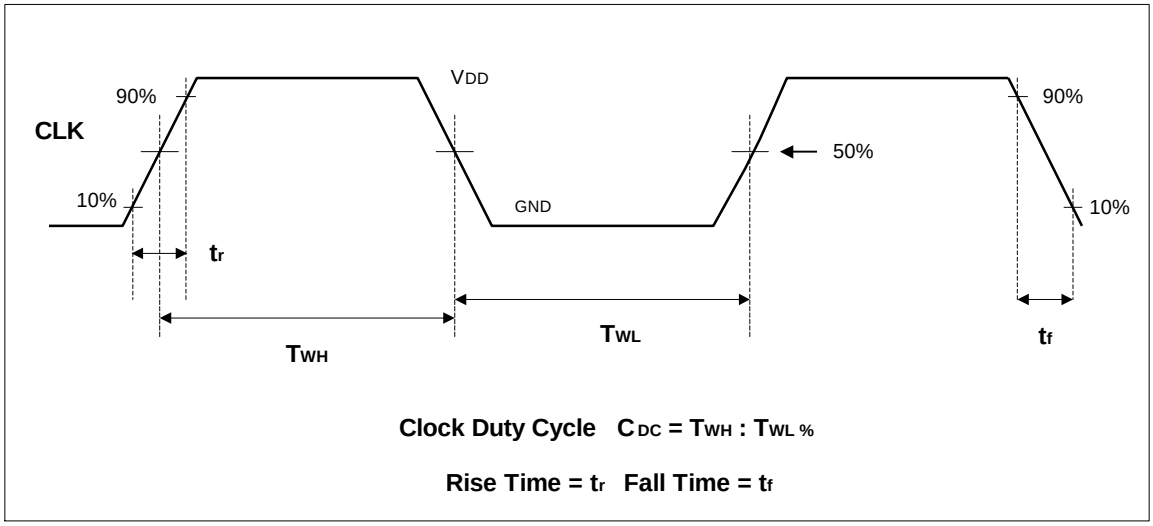


Figure 29 Clock Timing Measurement

T_{WH} >= 4.2ns
T_{WL} >= 4.2ns
t_r = 3ns
t_f = 3ns

6.2.1 Input Port Timing

Maximum input clock frequency (InVCLK/InGCLK) - 95 MHz.

6.2.2 Output Port Timing

Maximum output clock frequency (OutCLK) - 84 MHz.

6.2.3 Frame Store Interface Timing

Minimum frame store clock frequency (fsCLK) - 62 MHz.

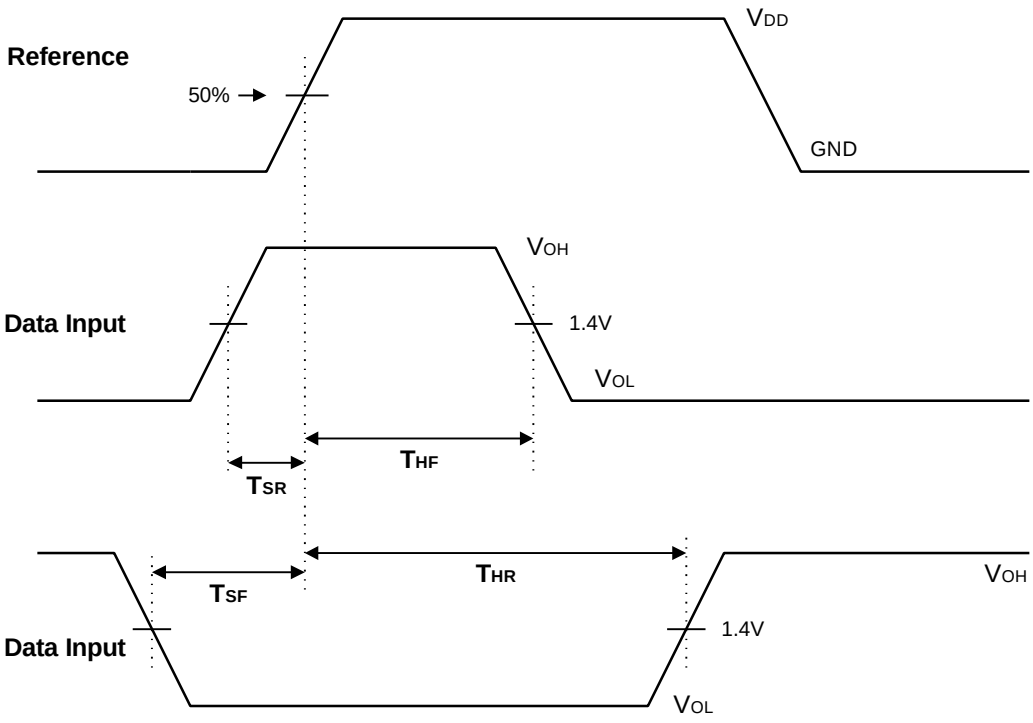
Maximum frame store clock frequency (fsCLK) - 95 MHz.

6.2.4 Host Interface Timing

Maximum Host Interface clock frequency (SCLK) in SPI mode is the lower of 5MHz or fsCLK / 16.

6.3 Preliminary Input Setup and Hold Times

The worst-case setup and hold time requirements on input pins are defined as follows:



The setup time specified (T S) is the greater of the rising setup time (T SR) and the falling setup time (T SF).

The hold time specified (T H) is the greater of the rising hold time (T HR) and the falling hold time (T HF).

Figure 30: Input Setup and Hold Time Measurement

6.3.1 YUV Video Input Interface

All setup and hold times are specified with respect to InVCLK (required only when selected as active data source).

Table 9: YUV Input Interface Setup/Hold Times

PIN	T_H HOLD TIME (ns)	T_S SETUP TIME (ns)
InVCREF	1.0	5.5
InODD	1.0	4.0
InVVS	1.0	5.0
InVHS	1.0	5.0
InY [7:0]	1.0	4.0
InUV [7:0]	1.0	4.0

6.3.2 RGB Graphics Input Interface

All setup and hold times are specified with respect to InGCLK (required only when selected as active data source).

Table 10: RGB Input Interface Setup/Hold Times

PIN	T_H HOLD TIME (ns)	T_S SETUP TIME (ns)
InGCREF	1.0	4.0
InGVS (1)	1.0	2.0
InGHS (2)	2.0	3.0
InRED [7:0]	2.0	2.0
InGREEN [7:0]	2.0	2.0
InBLUE [7:0]	2.0	2.0

(1) InGVS is considered an asynchronous input, and does not require setup/hold for correct operation.

(2) Applies to either the rising or falling edge of InGCLK, depending on the selected sampling edge

6.3.3 Frame Store Interface

All setup and hold times are specified with respect to fsCLK (the frame store interface output clock)

Table 11: Frame Store Interface Setup/Hold Times

PIN	T_H HOLD TIME (ns)		T_S SETUP TIME (ns)	
	FS_CLK_PHASE = 0	FS_CLK_PHASE = 1	FS_CLK_PHASE = 0	FS_CLK_PHASE = 1
FSDATA [47:0]	2.0	1.0	1.5	2.5

6.3.4 Output (gmZ1/2/3) Interface

All setup and hold times are specified with respect to OutCLK (the output interface *output* clock).

Table 12: Output Interface Setup/Hold Times

PIN	T_H HOLD TIME (ns)	T_S SETUP TIME (ns)
$\overline{\text{LREQ}}$ (1)	0	8.0
DATAREQ	0	10.5
$\overline{\text{FRAMERESET}}$ (1)	0	7.5

(1) Considered an asynchronous input. Does not require setup/hold for correct operation.

6.3.5 Host Interface

All setup and hold times are specified with respect to SCLK.

Table 13: Host Interface Setup/Hold Times

PIN	T_H HOLD TIME (ns)	T_P SETUP TIME (ns)
$\overline{\text{SCS}}$	100	100
SDI	100	100

6.4 Preliminary Output Propagation Delays

The worst-case propagation delay requirements on outputs are specified as follows:

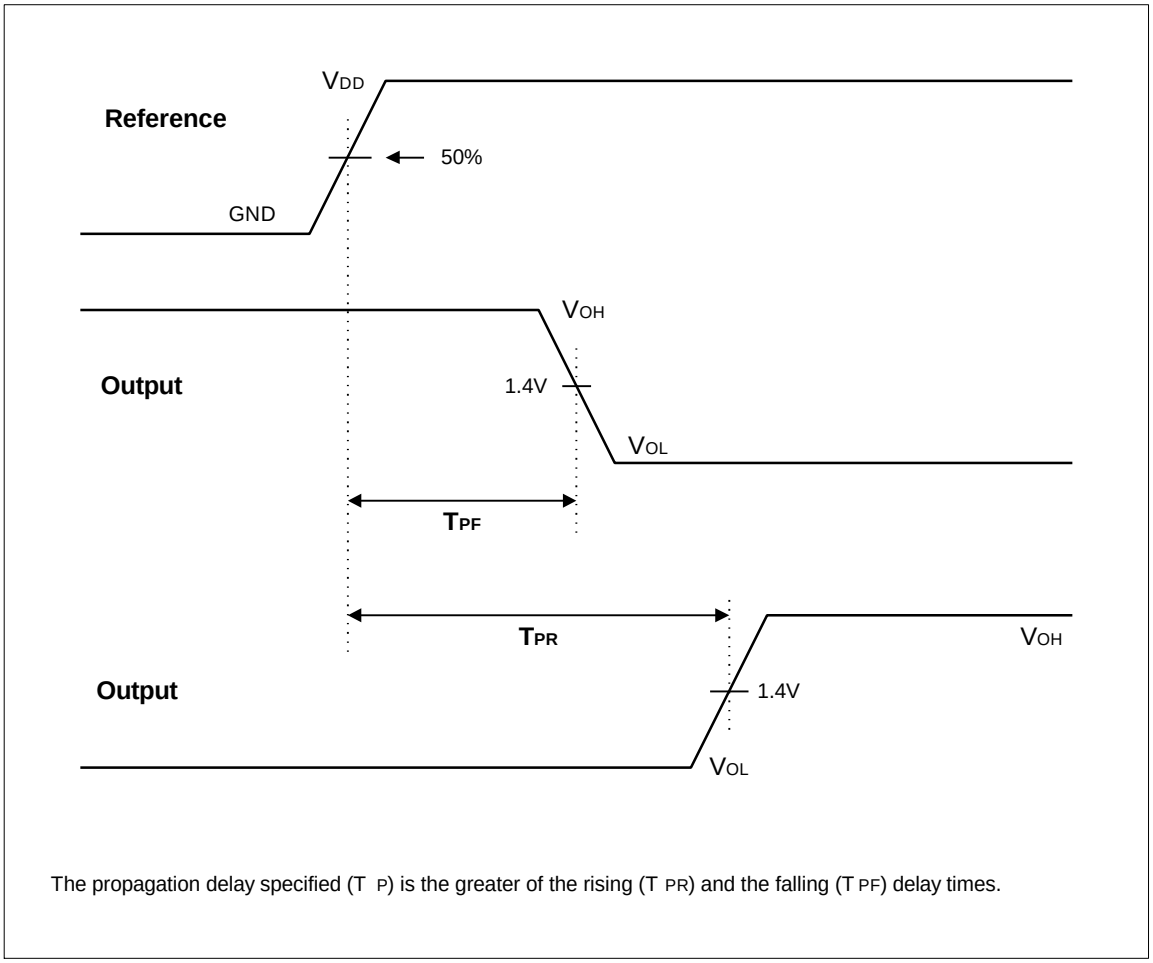


Figure 31: Output Propagation Delay Measurement

6.4.1 RGB Graphics Input Interface

All propagation delay times are specified with respect to the selected input clock (InGCLK / InVCLK).

Table 14: RGB Input Interface Data Propagation Times

PIN (C_{LOAD} = 15pf)	T_P PROPAGATION DELAY (ns)	
	MAXIMUM	MINIMUM
CLAMP	19.0	2.0
INVADC	22.0	2.0
$\overline{\text{OUTDFSYNC}}$	19.0	2.0

6.4.2 Frame Store Interface

All propagation delay times are specified with respect to fsCLK (the frame store interface clock output).

Table 15: Frame Store Interface Data Propagation Times

PIN	T_p PROPOGATION DELAY			
	MAXIMUM		MINIMUM	
(C_{LOAD} = 12pf) ⇓	FS_CLK_PHASE =0	FS_CLK_PHASE =1	FS_CLK_PHASE =0	FS_CLK_PHASE =1
FSDATA [47:0]	8.5	7.5	1.3	1.0
(C_{LOAD} = 25pf) ⇓				
FSADDR [11:0] (1)	8.5	7.5	1.5	1.0
$\overline{\text{FSRAS}}$	8.0	7.0	1.5	1.0
$\overline{\text{FSCAS}}$	8.0	7.0	1.5	1.0
$\overline{\text{FSWE}}$	8.0	7.0	1.5	1.0
fsCKE	8.0	7.0	1.5	1.0
$\overline{\text{FSCS}}$	8.0	7.0	1.5	1.0
fsDQM [1:0]	8.0	7.0	1.5	1.0

(1) FSADDR is always driven a minimum of one cycle earlier than required by SDRAM devices.

6.4.3 Output (gmZ1/2/3) Interface

All propagation delay times are specified with respect to OutCLK (the output interface clock output).

Table 16: Output (gmZ1/2/3) Interface Data Propagation Times

PIN (C_{LOAD} = 15pf)	T_P PROPAGATION DELAY (ns)	
	MAXIMUM	MINIMUM
OutVS	8.0	1.5
OutHS	8.0	1.5
OutODD	8.5	1.5
$\overline{\text{OUTSTALL}}$	7.5	1.5
OutRED [7:0]	8.0	1.5
OutGREEN [7:0]	8.0	1.5
OutBLUE [7:0]	8.0	1.5

6.4.4 Host Interface

All propagation delay times are specified with respect to SCLK.

Table 17: Host Interface Data Propagation Times

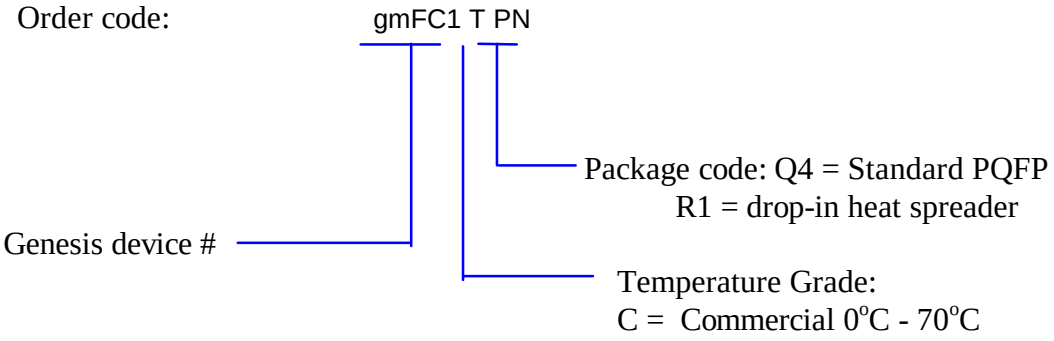
PIN	T_P PROPAGATION DELAY (ns)	
	MAXIMUM	MINIMUM
SDO	200	100

7. Ordering Information

The following order codes are preliminary:

Order Code[1]	Temperature	Package	Speed [2]	Package Marking[3]
gmFC1 CR1	Commercial 0-70^{0}C	208-pin PQFP with drop-in heat spreader	95MHz	BR1C
gmFC1 ER1	- 40 to +85 ^{0}C	See Genesis document E06-0005-A for specifications.		

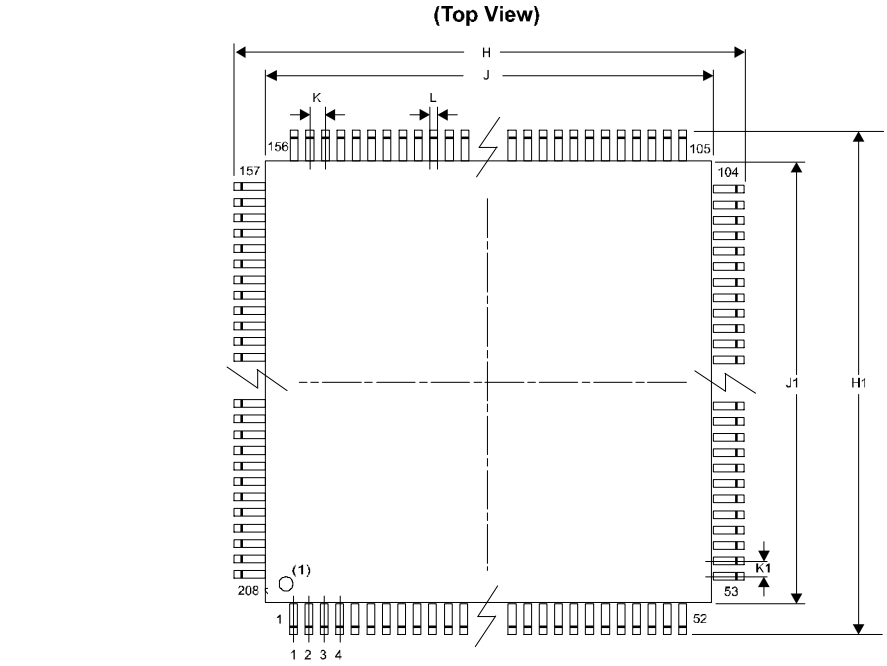
(1) Order code:



(2) The speed rating is not marked on the gmFC1 package

(3) The four digit Alphanumeric Genesis-assigned trace code marked on the package consists of a first letter (die revision, "B" for revision 1) and a last letter code dependent upon wafer fabrication and assembly location. The second and third characters define the package type (R1) as stated in Note (1).

8. Mechanical Specifications



	Milimetres			Inches		
	Min	Nom	Max	Min	Nom	Max
A	3.17		3.47	0.1248		0.1366
C	0.25			0.0098		
D		0.15			0.0039	
E		1.30			0.0512	
F	0.35		0.65	0.0138		0.0256
G	0°		10°	0°		10°
H	30.35	30.60	30.85	1.1949	1.2047	1.2146
J	27.90	28.00	28.10	1.0984	1.1024	1.1063
H1	30.35	30.60	30.85	1.1949	1.2047	1.2146
J1	27.90	28.00	28.10	1.0984	1.1024	1.1063
K		0.50			0.0197	
K1		0.50			0.0197	
L	0.10		0.30	0.0039		0.0118

Figure 32: R1 - 208 pin Plastic Quad Flat Pack (PQFP)

(1) Depressed dot indicates Pin 1. One or more corners may be rounded.

9. Interfacing the gmZ1 and gmFC1

Genesis application note MSD-0016 follows

Interfacing the Genesis gmFC1 Frame Rate Converter and gmZ1/2/3 Zoom Scaler

GENESIS

Application Note

Interfacing the

gmFC1 Frame Rate Converter

and

gmZ1 / gmZ2 / gmZ3 Zoom Scalers

MSD-0016-D

November 1998

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Interfacing the Genesis gmFC1 Frame Rate Converter and gmZ1 Zoom Scaler

MSD-0016-D

November 1998

Document	Changes	Date
MSD-0016-D	Includes gmZ2, gmZ3 information. GmZ3 interface to dual gmFC1's.	November 1998

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1. Introduction

The Genesis Microchip gmFC1 functions as a graphics and video frame buffer controller capable of performing frame rate conversion by replicating or dropping incoming frames as necessary to maintain a set output frame rate. Frame rate conversion (FRC) is required in applications where it is necessary to manage high input data rates or accommodate varying video and graphics input frame rates while using display devices operating at a fixed frame rate.

The gmZ1/Z2/Z3 family of chips are highly integrated IC's producing scaled digital video or computer graphics images. The gmZ1/Z2/Z3 uses an Advanced Image Magnification algorithm to create images of the highest image quality at 1x or larger magnifications. Additionally, features such as a built-in fully programmable display timing generator, graphics overlay support, multiple input and output data formats and on-board memory make the gmZ1/Z2/Z3 a preferred solution for LCD projectors and displays.

Some benefits to interfacing the gmFC1 and gmZ1/Z2/Z3 include simplified FRC designs, supporting many different input frame rates, and system cost reduction in applications ordinarily requiring expensive variable refresh LCD panels.

In a typical application, the gmFC1 is seamlessly interfaced to an SDRAM based frame store, input ADC, and the Genesis gmZ1/Z2/Z3 for output to an LCD display panel (see Figure 1 below). The gmFC1 provides data as required by the gmZ1/Z2/Z3 to sustain the programmed display timing. The gmZ1/Z2/Z3 operates in Free Run Mode, with all required display timing programmed into its display register set. (Frame Sync Mode is also possible, although it is recommended only for applications where frame dropping/duplication is not desired.) A shared microcontroller oversees all frame rate conversion, image scaling operations and input format detection through a compatible three or four wire serial host interface.

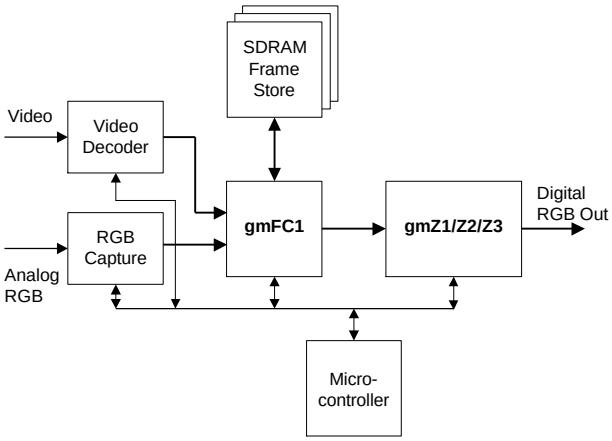


Figure 1: gmFC1 - gmZ1/Z2/Z3 System Block Diagram

2. Single gmFC1 - gmZ1/Z2/Z3 Interface

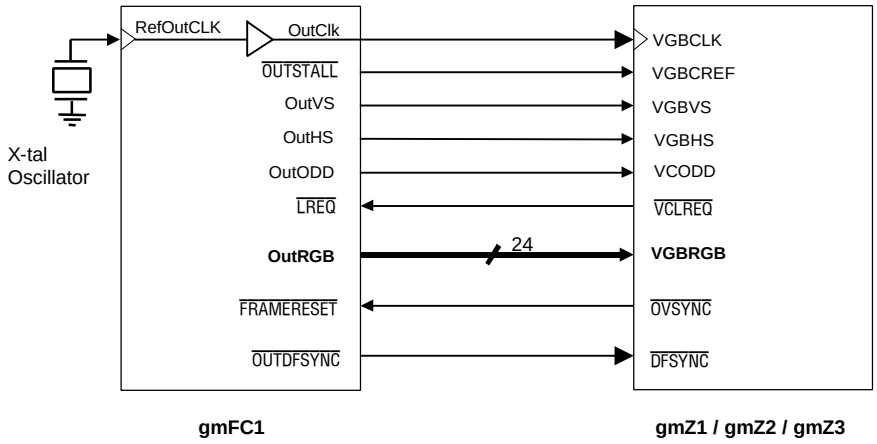


Figure 2: gmFC1 - gmZ1/Z2/Z3 Interface

2.1 Interface Overview

The hardware interface for RGB signals is illustrated in Figure 2 above. A detailed explanation of the input and output interface signals may be found in the following sections.

In this application, the gmFC1 is programmed to provide active output data a specified number of clock cycles (OPH_ACTIV_START) after the gmFC1 asserts OutHS. The gmFC1 output controls FSDB_EN, OUTP_EN, BYPASS_EN, OP_HANDSH and IP_FLOCK_EN are programmed as in Table 1.

The gmZ1/Z2/Z3 is programmed to receive active single pixel RGB input data occupying the same active window as the gmFC1 RGB output data. This is achieved by matching the gmFC1 Active Output Window parameters to the gmZ1/Z2/Z3 Active Input Window parameters, as described in Section 2.3. The gmZ1/Z2/Z3 input controls IP_RGB_EN, RGB_B_SEL, IP2PIXWIDE_EN, IP2PIXOFFSET_EN, IP_CREF_INV, IPHS_INV, IPODD_INV, D_LINESYNC_EN, D_FRAMELOCK_EN, DFSYNC_EN and DVS_INV are programmed as in Table 2.

The operational parameters of both the gmFC1 and the gmZ1/Z2/Z3 are closely related. In Free Run Mode, the gmFC1 depends on the gmZ1/Z2/Z3 to set the output frame rate, and to request data required to maintain the data rate. The gmFC1 output interface

handshaking is shown in Figure 5 below. (In the optional Frame Sync Mode, the gmZ1/Z2/Z3 output frame rate is locked to the gmFC1 input source.)

When the gmZ1/Z2/Z3 has completed displaying an image, the gmFC1 is signaled to queue up data for the next frame. This is accomplished by tying a gmZ1/Z2/Z3 display-side VSYNC signal (ex: $\overline{\text{OVSYNC}}$) to the gmFC1 $\overline{\text{FRAMERESET}}$ input. $\overline{\text{FRAMERESET}}$ resets the gmFC1's output circuitry and produces an OutVS pulse. In response, the gmZ1/Z2/Z3 asserts $\overline{\text{VCLREQ}}$, indicating internal line storage is available. ($\overline{\text{VCLREQ}}$ is tied to the gmFC1's $\overline{\text{LREQ}}$ pin.)

2.2 Interface Signals

The gmFC1 is designed to interface seamlessly to the gmZ1. All control signals specific to this application are described in detail below. Additional information regarding gmFC1 SDRAM, ADC and microcontroller interfacing is available in the gmFC1 Data Sheet. Additional information regarding gmZ1/Z2/Z3 input, display, and microcontroller interfacing is available in the gmZ1, gmZ2 and gmZ3 Data Sheets.

2.2.1 gmFC1 Output Interface Signals

Signal Name	I/O	Description
OutClk	O	Output Clock driving the gmZ1. Based on the gmFC1 RefOutCLK.
$\overline{\text{OUTSTALL}}$	O	Stall control to gmZ1. (1)
OutVS	O	Output Vertical Sync. Asserted by the gmFC1 in response to $\overline{\text{FRAMERESET}}$. Used to reset internal gmZ1/Z2/Z3 counters to the start of a new frame. Active high.
OutHS	O	Output Horizontal Sync. Asserted by the gmFC1 in response to the $\overline{\text{LREQ}}$ signal from the gmZ1/Z2/Z3 (i.e., gmZ1's $\overline{\text{VCLREQ}}$). Active high.
OutOdd	O	Indicates the interlaced output field to the gmZ1/Z2/Z3 is ODD during Vertical Interlace output format. High = odd fields.
$\overline{\text{LREQ}}$	I	Line Request - the gmZ1/Z2/Z3 indicates it is ready to receive a new line by driving this input with $\overline{\text{VCLREQ}}$.

		The gmFC1 monitors $\overline{\text{LREQ}}$ to trigger an OutHS pulse. Active low.
$\overline{\text{FRAMERESET}}$	I	Forces the gmFC1 to begin the next output frame. May be driven asynchronously to OutCLK. Active low.
RefOutCLK	I	Clock reference for the gmZ1/Z2/Z3 interface.
OutRGB [23:0]	O	24 bit RGB data output. If the YUV input port is used to acquire data, OutRGB [23:16] correspond to YUV [15:8], and OutRGB [7:0] correspond to YUV [7:0].
$\overline{\text{OUTDFSYNC}}$	O	$\overline{\text{OUTDFSYNC}}$ is used by the gmFC1 only in Frame Sync Mode to force the gmZ1/Z2/Z3 to re-synchronize to a new frame. Tied to the gmZ1/Z2/Z3 $\overline{\text{DFSYNC}}$ pin. See Section 2.4.2. Active low.
DATAREQ	I	For gmFC1 - gmZ1/Z2/Z3 interface, wire to ground.

(1) $\overline{\text{OUTSTALL}}$ is asserted by the gmFC1 when it is unable to provide requested pixel data to the gmZ1. This may be due to arbitration in the frame store interface. Because of internal buffering within the gmZ1, momentary data transfer stalls are acceptable. If the gmFC1 is unable to provide data for a sustained period of time, the gmZ1/Z2/Z3 will produce an underflow error. If this occurs, the combined gmFC1 input and output data rates are too high to be supported by the frame store interface. This may be overcome by adjusting the gmFC1 input clock/memory clock frequencies, and/or the gmZ1/Z2/Z3 display timing.

2.2.2 gmZ1/Z2/Z3 Input Interface Signals

Signal Name	I/O	Description
$\overline{\text{OVSYNC}}$	O	Overlay Vertical Sync. Indicates start of a new frame of overlay data. Active low.
$\overline{\text{VCLREQ}}$	O	Line request. Indicates the gmZ1/Z2/Z3 is ready to accept input lines. Active low.
VGBCLK	I	Video graphics VGB port system clock.
VGBCREF	I	Video graphics input system clock enable. Qualifies VGBCLK. Programmed active high for this application.

VGBVS	I	Vertical Sync Input. Programmed active high.
VGBHS	I	Horizontal Sync Input. Programmed active high.
VCODD	I	Interlace Mode Field status, programmed active high: 1=odd field, 0=even field.
VGBRGB [23:0]	I	24 bit RGB data input. If input data is YUV, VGBRGB [23:16] correspond to YUV [15:8] and VGBRGB [7:0] correspond to YUV [7:0].

2.3 Active Window Parameters

The gmFC1 and gmZ1/Z2/Z3 Active Window parameters determine the start and end positions of the active RGB data. These parameters are programmed into internal registers via the respective Host Interfaces. The gmFC1 input parameters are programmed such that only active data is captured.

2.3.1 gmFC1 Output Parameters

The gmFC1 may be programmed to output a region of data smaller than the active sampled input region. The parameters of the output region are set through host programmed registers. This feature allows cropping, dynamic re-sizing, or zooming of a captured freeze frame input image to be performed. The location of the output region within the input data can be varied in two pixel increments. See the gmFC1 Data Sheet for more detailed information on programming gmFC1 registers.

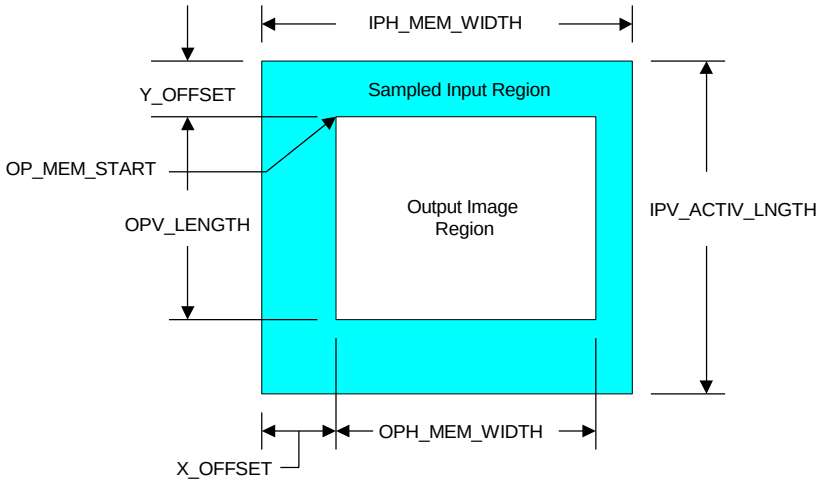


Figure 3: gmFC1 Output Active Window Parameters

Table 1: gmFC1 Output Video Registers

Address (HEX)	Bit	Mode	Name	Description	Programmed Value (decimal)
02	01	R/W	OP_GTR_IN	*Output Greater Than Input*	Application Specific
02	04	R/W	FSDB_EN	*Frame Store Double Buffering Enable* (1)	1
02	06	R/W	OUTP_EN	*Output Enable*	1
02	07	R/W	BYPASS_EN	*Bypass Mode Enable*	0
02	08	R/W	OP_HANDSH	*Output Handshake Control*	1
02	09	R/W	IP_FLOCK_EN	*Input-Output Frame Lock Enable* (2)	0
0F	bit[10:0]	R/W	OPH_MEM_WIDTH	*Output Frame Store Image Width* (OPH_ACTIV_WIDTH / 2 rounded up to the nearest decimal)	Application Specific
10	bit[11:0]	R/W	OPH_MEM_STARTL	*Output Frame Store Image Start (low 12 bits)* Frame Store start address	Application Specific
11	bit[6:0]	R/W	OP_MEM_STARTH	*Output Frame Store Image Start (high 7 bits)* Frame Store start address	Application Specific
12	bit[10:0]	R/W	OPV_LENGTH	*Output Vertical Image Length* Number of lines in the active image	See Table 3
13	bit[10:0]	R/W	OPH_ACTIV_START	*Output Horizontal Active Start* The gmFC1 will count this number of output clocks from the leading edge of OutHS before providing output data when OP_HANDSH=1	See Table 3
14	bit[10:0]	R/W	OPH_ACTIV_WIDTH	*Output Horizontal Active Width* Active Image Width in pixels	See Table 3

(1) Double Buffering eliminates the possibility of frame tear artifacts. This parameter should be programmed to '1' at all times.
(2) For Frame Sync applications, program IP_FLOCK_EN=1. The state of OP_GTR_IN is ignored.

2.3.2 gmZ1/Z2/Z3 Input Parameters

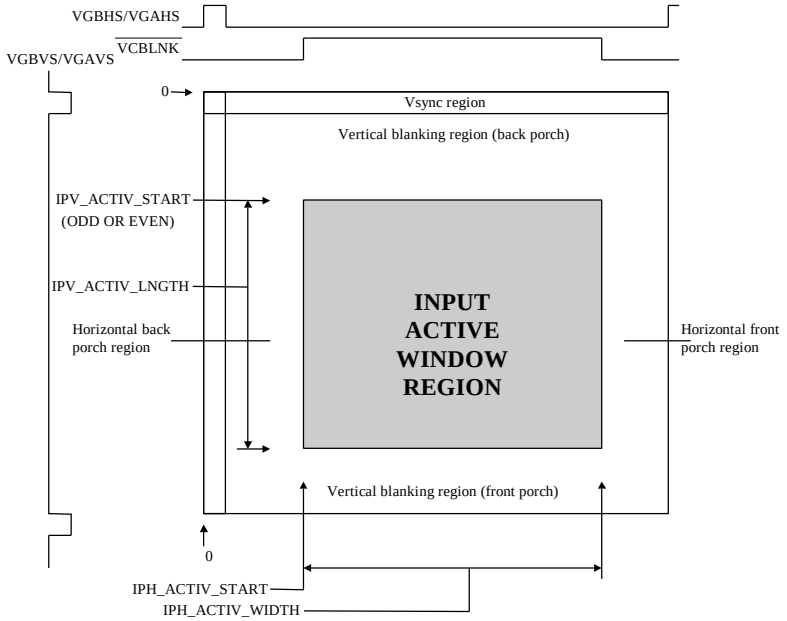


Figure 4: gmZ1/Z2/Z3 Input Actve Window Parameters

The gmZ1/Z2/Z3 Input Active Window Control provides a means of programming the active window region for the selected input video. The horizontal sync and vertical sync controls from the selected port are used to determine the active window region. Only pixels transferred to the device during the Active Window region are used as source data for the scaling process and resulting display output. The Active Window is defined using the registers IPV_ACTIV_STARTODD, IPV_ACTIV_STARTEVN, IPV_ACTIV_LNGTH, IPH_ACTIV_START, and IPH_ACTIV_WIDTH.

Table 2: gmZ1/Z2/Z3 Input Video Registers

Address (HEX)	Bit	Mode	Name	Description	Programmed Value (decimal)
01	04	R/W	IP_RGB_EN	*Input RGB Enable* [(1)]	1
01	10	R/W	RGB_B_SEL	*RGB 'B' Port Select*	1
02	01	R/W	IP2PIXWIDE_EN	*Double Pixel Wide Input Enable*	0
02	02	R/W	IP2PIXOFFSET_EN	*Double Pixel Offset Input Enable*	0
02	04	R/W	IP_CREF_INV	*Invert CREF Input*	0
02	05	R/W	IPHS_INV	*Invert Horizontal Sync Input*	0
02	06	R/W	IPVS_INV	*Invert Vertical Sync Input*	0
02	07	R/W	IPODD_INV	*Invert ODD Input*	0
03	02	R/W	D_LINESYNC_EN	*Display Line Sync Mode Enable*	1
03	03	R/W	D_FRAMELOCK_EN	*Display Frame Lock Mode Enable*	1
03	04	R/W	DFSYNC_EN	*Display Frame Sync Input* ($\overline{\text{DFSYNC}}$) *Enable*	0
09	bit[10:0]	R/W	IPH_ACTIV_START	*Input Video Horizontal Active Start:* Defines the number of pixel clocks (qualified by VGACREF or VGBCREF) from where the start of the VGAHS or VGBHS pulse is sampled, to the first active pixel sampled by the gmZ1/Z2/Z3	See

Address (HEX)	Bit	Mode	Name	Description	Programmed Value (decimal)
				Active Window Decoder. Available range for Horizontal Active Start is: Single Pixel RGB 12 ≤ IPH_ACTIV_START ≤ 2047	Table 3
0A	bit[10:0]	R/W	IPH_ACTIV_WIDTH	*Input Video Horizontal Active Pixels:* The number of active input pixels sampled (as qualified by VGACREF or VGBCREF) from the start of Horizontal Active Window to the end of the horizontal active period. (Horizontal Active Start + Horizontal Active Width) ≤ 2047. 16 ≤ IPH_ACTIV_WIDTH ≤ 1024.	See Table 3
0B	bit[10:0]	R/W	IPV_ACTIV_STARTODD	*Input Video Vertical Active Start - Odd Fields:* The number of lines from the start of the selected input video VSYNC when VCODD = '1', to (and including) the first line of the Vertical Active Window. When the input video source is not interlace video, then VCODD is ignored and all input frames are treated the same as ODD fields.	2
0C	bit[10:0]	R/W	IPV_ACTIV_STARTEVN	*Input Video Vertical Active Start -Even Fields:* The number of lines from the start of the selected input video VSYNC when input signal VCODD = '0', to the start of the Vertical Active Window. When the input video source is not interlaced video, then VCODD is ignored and all input frames are treated the same as odd fields.	2
0D	bit[10:0]	R/W	IPV_ACTIV_LNGTH	*Input Video Vertical Active Lines:* The number of active lines from the start of Vertical Active Window to the end of the Vertical Active Window. Programmable in single line increments. (Vertical Active Start + Vertical Active Length) ≤ 2047. 8 ≤ IPV_ACTIV_LNGTH ≤ 2047.	See Table 3

(1) Program IP_RGB_EN=0 if the input is YUV format.

In this application, the gmZ1/Z2/Z3 is programmed in Single Pixel Mode, and the Horizontal Active Window is programmable in single pixel increments. Note that only qualified pixel clocks (i.e. when VGBCREF is asserted) are counted. When processing YUV inputs, the active region is programmable in single pixel increments; however, an even number of active pixels per line should always be used. Note that only pixel clocks where VGBCREF is active are counted.

For interlaced video, VCODD determines which of two possible Vertical Active Region start locations will be used. See the Genesis gmZ1, gmZ2, or gmZ3 Data Sheet for a detailed description of all registers.

2.3.3 Matching gmFC1 and gmZ1/Z2/Z3 Parameters

In order for active data to be correctly transferred from the gmFC1 to the gmZ1, all gmFC1 output active window parameters must be programmed to coincide with gmZ1/Z2/Z3 input active window parameters, as described in Table 3 below.

Table 3: Active Window Parameter Equivalents

gmFC1 Output Register		gmZ1/Z2/Z3 Input Register
OPH_ACTIV_START - 1	=	IPH_ACTIV_START [(1)]
OPH_ACTIV_WIDTH	=	IPH_ACTIV_WIDTH
*	=	IPV_ACTIVE_STARTODD = 2
*	=	IPV_ACTIV_STARTEVN = 2
OPV_LENGTH	=	IPV_ACTIV_LENGTH

(1) gmZ1/Z2/Z3 IPH_ACTIVE_START should be set to the minimum value of 0x0C, therefore gmFC1 OPH_ACTIV_START would programmed to 0x0D.

* There are no corresponding gmFC1 registers. These parameters are internally locked to a value of 2 within the gmFC1. The gmZ1/Z2/Z3 IPV_ACTIV_START_ODD and IPV_ACTIV_START_EVEN parameters must therefore be set to a value of 2.

2.4 Synchronization

In this application, the gmZ1/Z2/Z3 operates in Free Run Mode. All required display timing is programmed into its display register set. The input frame rate is captured by the gmFC1, and the output frame rate is determined by the gmZ1. Because of the close relationship between gmFC1 output and gmZ1/Z2/Z3 input sections, care must be taken to ensure they remain synchronized. This is particularly true in applications where the operational parameters are modified dynamically.

2.4.1 Register Sets

The gmFC1 host interface output parameters incorporate an Active and a Pending Register Set. When modified by the host, only the Pending Register Set is affected. The Active Register Set remains utilized by the output circuitry. The Pending Register contents are copied to the Active Set only after the OUT_UPDATE_EN register bit is set, and the $\overline{\text{FRAMERESET}}$ signal is asserted. This occurs at a point when active data is not being transferred to the gmZ1. The gmZ1/Z2/Z3 has a similar architecture, with Pending and Active Register sets. The transfer to the Active Register Set also occurs at approximately this same point.

When parameters are modified dynamically (i.e., while active data is flowing), the host microcontroller is responsible for ensuring gmFC1 and gmZ1/Z2/Z3 Active Register sets are synchronized. This may be achieved by transferring both gmZ1/Z2/Z3 and gmFC1 Pending sets to the Active sets within a short period after a $\overline{\text{FRAMERESET}}$ has occurred.

This ensures the transfer for one device will not happen while the host is enabling the transfer for the other device.

2.4.2 Locking Output and Input Frame Rates

For applications in which the input and output frame rates are *nominally* the same, and frame dropping/duplication is not desired, it may be advantageous to operate the gmZ1/Z2/Z3 in Frame Sync Mode and lock the gmZ1/Z2/Z3 output frame rate to the gmFC1 input frame rate. In such an application, the gmFC1 output signal $\overline{\text{OUTDFSYNC}}$ is connected to the gmZ1/Z2/Z3 input $\overline{\text{DFSYNC}}$ to force the gmZ1/Z2/Z3 display timer to reset. The gmFC1 will assert $\overline{\text{OUTDFSYNC}}$ based on the selected input VS. This causes the gmZ1/Z2/Z3 to assert $\overline{\text{OVSYNC}}$ (connected to gmFC1 $\overline{\text{FRAMERESET}}$), which resets the gmFC1 output circuitry.

Note: DFSYNC has no effect during Free Run Mode operation, therefore it is possible to connect gmFC1's OUTDFSYNC pin to gmZ1's DFSYNC pin for all synchronization modes.

For Frame Sync Mode, the gmFC1 output control parameter IP_FLOCK_EN = 1, and the OP_GTR_IN state is ignored. The gmZ1/Z2/Z3 input control parameters are modified as follows: D_LINESYNC_EN = 0, D_FRAMELOCK_EN=1, DFSYNC_EN=1.

2.5 gmFC1 Output Timing

The following diagrams illustrate gmFC1 - gmZ1/Z2/Z3 handshaking. The gmFC1 timing parameters are detailed in the gmFC1 Data Sheet (DAT-0005).

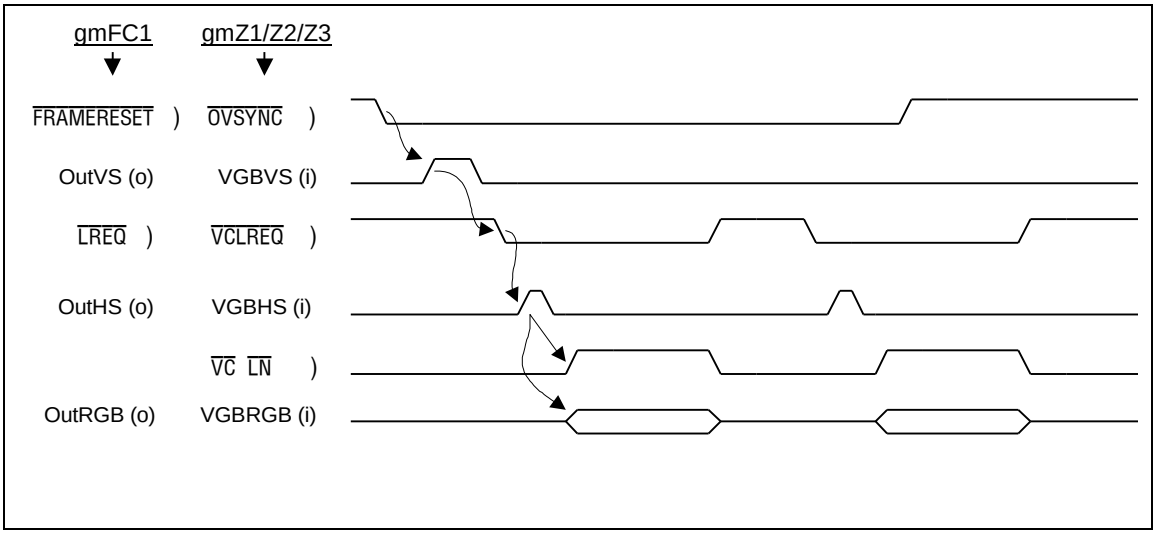


Figure 5: gmFC1 Output Timing

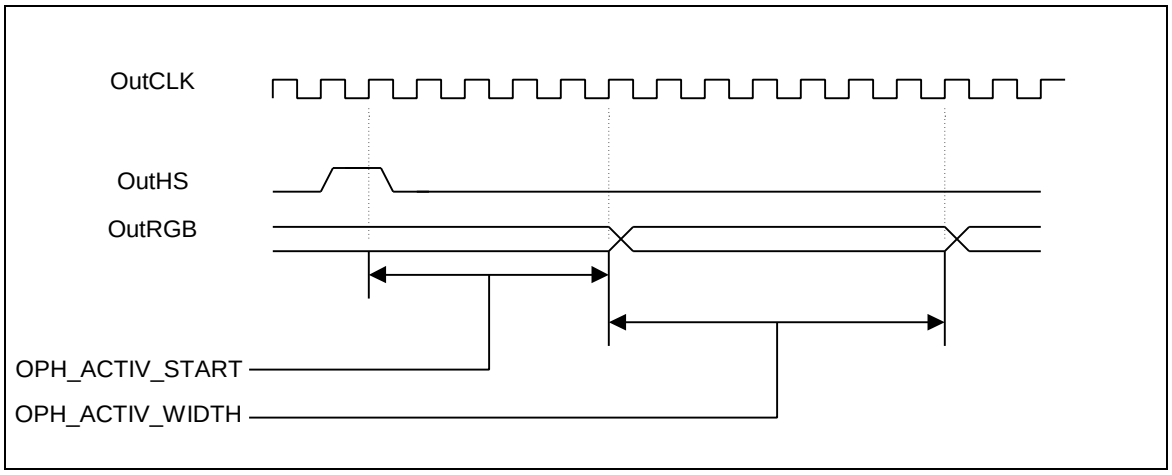


Figure 6: gmFC1 Output Active Start and Width

2.6 Host Interface

When operating the gmZ1 and gmFC1 host interfaces in 4-wire mode, it is necessary to program the gmZ1 for 3-wire mode operation while retaining the 4-wire hardware configuration, and pulling up the common SDO signal line using a 1K resistor. (See Figure 7 below.) This will cause the gmZ1 SDO output to operate open-drain, and thus prevent the gmZ1 from driving the SDO signal line to an active '1' state when the gmZ1 chip select (/CS1) is de-asserted. Without these modifications, it is not possible for the microcontroller to correctly interpret SDO signaling from the gmFC1.

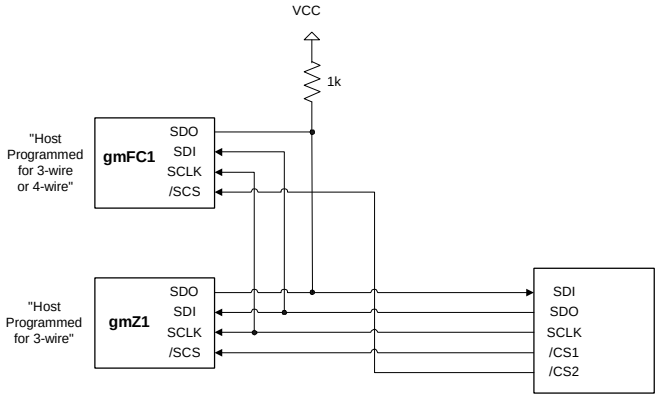


Figure 7: Recommended 4-Wire Host Interface to gmZ1

There are no modifications required when interfacing to the gmZ2 or gmZ3 in any mode, or when operating the gmZ1 and gmFC1 in a 3-wire host interface hardware configuration. In a 3-wire hardware configuration, the SDO and SDI lines are tied together, to a 1K pull-up resistor. See Figure 8 below for the standard 3-wire setup.

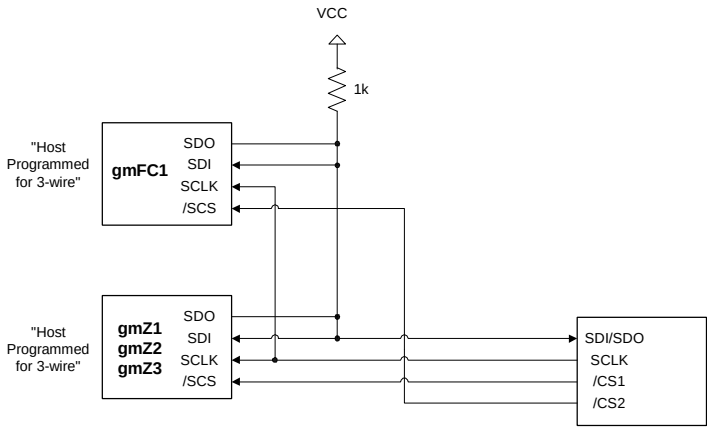


Figure 8: 3-Wire Host Interface

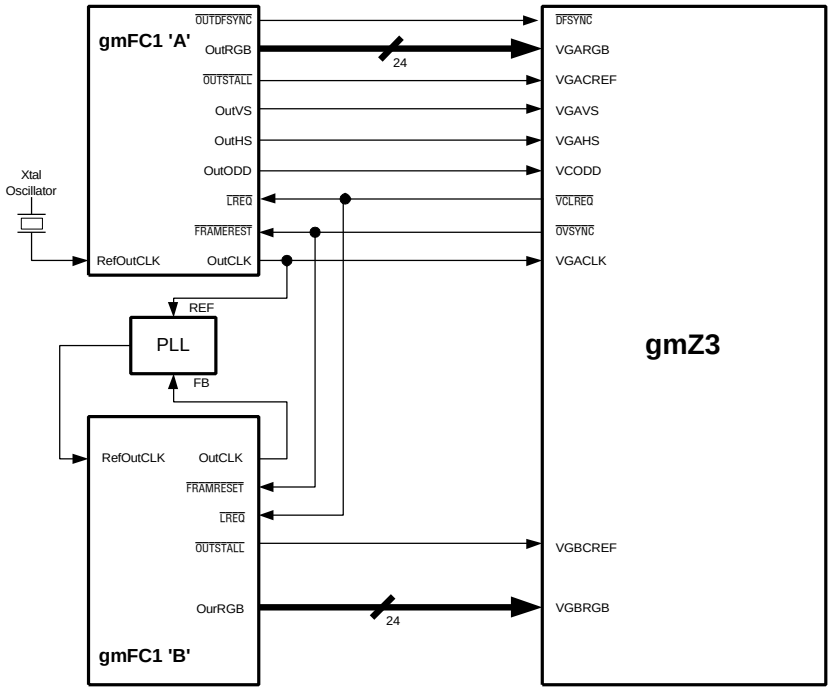
3. Dual gmFC1 – gmZ3 Interface

When running in Half Rate Mode, the gmZ3 allows the two halves of the double wide pixel input path to be independently stalled, using VGACREF and VGBCREF. When interfacing the gmZ3 to two gmFC1's, this allows the Frame Buffer Controller output data to remain aligned.

The gmZ3 maintains two internal line request ($\overline{\text{VCLREQ}}$) and blanking ($\overline{\text{VC}}$ $\overline{\text{LN}}$) signals, one pair for each half of the data pair. The actual gmZ3 output signals $\overline{\text{VCLREQ}}$ and $\overline{\text{VC}}$ $\overline{\text{LN}}$ are generated by an internal OR-ing of these internal signal pairs. That is, if either data path is actively capturing data, $\overline{\text{VC}}$ $\overline{\text{LN}}$ is de-asserted, and $\overline{\text{VCLREQ}}$ is asserted. This feature is intended for frame buffer applications where input Lock Events are not required (other than possibly those generated by $\overline{\text{DFSYNC}}$). If the clock qualifier (CREF) is used with real time input data, the horizontal input Lock Event is based on the VGACREF qualified VGACLK.

If the gmZ3 is run in Half-Rate Mode in a system where independent stalling of the data pairs is not required, VGACREF and VGBCREF must be tied together.

Figure 9: Dual gmFC1 Interface



4. Example Register Sets

4.1 Example - 72Hz VGA Input, 60Hz XGA Output

In this example, the video source is VGA (72Hz). A single gmFC1 reduces the 72Hz frame rate to 60Hz. The gmZ1/Z2/Z3 then scales the output from VGA (60Hz) to XGA (60Hz). See Table 4 below for the video standard specifications. The system is operating in Free Run Mode, using the gmZ1's $\overline{\text{OVSYNC}}$ sync output.

Table 4: VGA (72Hz) and XGA (60Hz) VESA Specifications

Specification	VGA (72Hz)	XGA (60Hz)
Horizontal Frequency	37.86 kHz	48.36 kHz
Vertical Frequency	72.8 Hz	60 Hz
Pixel Clock	31.5 MHz	65 MHz
Horizontal Active Pixels	640	1024
Horizontal Front Porch	24	24
Horizontal Sync Width	40	136
Horizontal Back Porch	128	160
Horizontal Total Pixels	832	1344
Vertical Active Lines	480	768
Vertical Front Porch	9	3
Vertical Sync Width	3	6
Vertical Back Porch	28	29
Vertical Total Lines	520	806

4.2 Example gmZ1/Z2/Z3 Registers

The gmZ1/Z2/Z3 Output Display Registers are programmed to produce VESA 60Hz XGA timing, and the input registers are programmed to accept 60Hz VGA from the gmFC1. Table 5 below lists the gmZ1/Z2/Z3 interface control registers and their required values for VGA (60Hz) input and XGA (60Hz) output. Note that Table 5 lists only the registers relevant to this general example. The complete gmZ1/Z2/Z3 register set must be programmed with application specific values for correct gmZ1/Z2/Z3 operation. See the applicable Data Sheet.

Table 5: gmZ1/Z2/Z3 Register Set

Address (HEX)	Bit	Mode	Name	Description	Programmed Value (decimal)
01	04	R/W	IP_RGB_EN	*Input RGB Enable*	1
01	10	R/W	RGB_B_SEL	*RGB 'B' Port Select*	1
02	01	R/W	IP2PIXWIDE_EN	*Double Pixel Wide Input Enable*	0
02	02	R/W	IP2PIXOFFSET_EN	*Double Pixel Offset Input Enable*	0
02	03	R/W	IP_INTLC_EN	*Interlaced Input Enable*	0
02	04	R/W	IP_CREF_INV	*Invert CREF Input*	0
02	05	R/W	IPHS_INV	*Invert Horizontal Sync Input*	0
02	06	R/W	IPVS_INV	*Invert Vertical Sync Input*	0
02	07	R/W	IPODD_INV	*Invert ODD Input*	0
03	02	R/W	D_LINESYNC_EN	*Display Line Sync Mode Enable*	1
03	03	R/W	D_FRAMELOCK_EN	*Display Frame Lock Mode Enable*	1
03	04	R/W	DFSYNC_EN	*Display Frame Sync Input (* $\overline{\text{DFSYNC}}$ *) Enable*	0
04	08	R/W	DHS_INV	*Invert Display Horizontal Sync Out*	0
04	09	R/W	DVS_INV	*Invert Display Vertical Sync Out*	1
09	bit[10:0]	R/W	IPH_ACTIV_START	*Input Video Horizontal Active Start*	12
0A	bit[10:0]	R/W	IPH_ACTIV_WIDTH	*Input Video Horizontal Active Pixels*	640
0B	bit[10:0]	R/W	IPV_ACTIV_STARTODD	*Input Video Vertical Active Start - Odd Fields*	2
0C	bit[10:0]	R/W	IPV_ACTIV_STARTEVN	*Input Video Vertical Active Start -Even Fields*	2
0D	bit[10:0]	R/W	IPV_ACTIV_LNGTH	*Input Video Vertical Active Lines:*	480
0E	bit[10:0]	R/W	IPH_LOCK_EVENT	*Input Horizontal Programmable Lock Event* (1)	8
0F	bit[10:0]	R/W	IPV_LOCK_EVENT	*Input Vertical Programmable Lock Event* (1)	2
13	bit[8:0]	R/W	Z_HORZ_SV_hi	*Zoom Horizontal Scale Value (high 9 bits)*	13F (hex)
14	bit[7:0]	R/W	Z_HORZ_SV_lo	*Zoom Horizontal Scale Value (low 8 bits)*	D0 (hex)
15	bit[7:0]	R/W	Z_VERT_SV_hi	*Zoom Vertical Scale Value (high 8 bits)*	9F (hex)
16	bit[7:0]	R/W	Z_VERT_SV_lo	*Zoom Vertical Scale Value (low 8 bits)*	E0 (hex)
19	bit[10:0]	R/W	DH_TOTAL	*Display Horizontal Total Pixel Clocks*	1344
1A	bit[7:0]	R/W	DH_VCTEN	*Display Horizontal Vertical Count*	0
1B	bit[5:0]	R/W	DH_HS_END	*Display Horizontal Sync End*	34
1C	bit[10:0]	R/W	DH_BKGND_START	*Display Horizontal Background Start*	297
1D	bit[10:0]	R/W	DH_ACTIV_START	*Display Horizontal Active Start*	297
1E	bit[10:0]	R/W	DH_ACTIV_WIDTH	*Display Horizontal Active Width*	1024
1F	bit[10:0]	R/W	DH_BKGND_END	*Display Horizontal Background End*	1320
21	bit[10:0]	R/W	DV_TOTAL	*Display Vertical Total*	806
22	bit[10:0]	R/W	DV_VS_END	*Display Vertical Sync End*	6
23	bit[10:0]	R/W	DV_BKGND_START	*Display Vertical Background Start*	36
24	bit[10:0]	R/W	DV_ACTIV_START	*Display Vertical Active Start*	36
25	bit[10:0]	R/W	DV_ACTIV_LNGTH	*Display Vertical Active Length*	768
26	bit[10:0]	R/W	DV_BKGND_END	*Display Vertical Background End*	803

(1) A Programmable Lock Event is set prior to active data to initiate an update of the gmZ1/Z2/Z3 active register set.

4.3 Example gmFC1 Registers

Table 6 below lists the relevant gmFC1 interface control registers and their required values for capturing a VESA VGA (72Hz) input. The gmZ1/Z2/Z3 determines the output frame rate (60Hz). Note that Table 6 lists only the registers relevant to this general example. The complete gmFC1 register set must be programmed with application specific parameter values for correct gmFC1 operation. Note that all registers are addressable from bit 0 to bit 11, and any bits not defined in the gmFC1 Data Sheet DAT-0005 must be programmed to '0' for gmZ1/Z2/Z3 interface applications.

All host writable register contents default to '0' as the result of a hard reset, except the SOFT_RESET bit 00 and RESERVED bit 08 in the HOSTCTRL register. Writable register contents are not affected by a SOFT_RESET.

Table 6: gmFC1 Register Set

Register Address (HEX)	Bit	Mode	Name	Description	Programmed Value (decimal)
02	00	R/W	OP_VINTLC_EN	*Output Vertical Interlace Enable*	0
02	01	R/W	OP_GTR_IN	*Output Data Rate Greater Than Input*	0
02	04	R/W	FSDB_EN	*Frame Store Double Buffering Enable*	1
02	06	R/W	OUTP_EN	*Output Enable*	1
02	07	R/W	BYPASS_EN	*Bypass Mode Enable*	0
02	08	R/W	OP_HANDSH	*Output Handshake Control*	1
02	09	R/W	IP_FLOCK	*Input-Output Frame Lock Enable*	0
03	08	R/W	(reserved)	*(program to 1)*	1
05	02	R/W	IPVS_INV	*Input Vertical Sync Invert*	1
05	03	R/W	IPHS_INV	*Input Horizontal Sync Invert*	1
05	08	R/W	IP_VINTLC_EN	*Input Vertical Interlace Enable*	0
05	09	R/W	IP_HINTLC_EN	*Input Horizontal Interlace Enable*	0
06	bit[10:0]	R/W	IPH_ACTIV_STARTODD	*Input Horizontal Active Start - Odd Pixel*	131
07	bit[10:0]	R/W	IPH_ACTIV_STARTEVEN	*Input Horizontal Active Start - Even Pixel*	131
08	bit[10:0]	R/W	IPH_ACTIV_WIDTH	*Input Active Width*	640
09	bit[10:0]	R/W	IPV_ACTIV_STARTODD	*Input Vertical Active Start - Odd Field*	32
0A	bit[10:0]	R/W	IPV_ACTIV_STARTEVEN	*Input Vertical Active Start - Even Field*	32
0B	bit[10:0]	R/W	IPV_ACTIV_LNGTH	*Input Vertical Active Length*	480
0E	bit[10:0]	R/W	IPH_MEM_WIDTH	*Input Horizontal Active Width*	320
0F	bit[10:0]	R/W	OPH_MEM_WIDTH	*Output Frame Store Image Width*	320
10	bit[11:0]	R/W	OPH_MEM_STARTL	*Output Frame Store Image Start (low 12 bits)*	0
11	bit[6:0]	R/W	OP_MEM_STARTH	*Output Frame Store Image Start (high 7 bits)*	0
12	bit[10:0]	R/W	OPV_LENGTH	*Output Vertical Image Length*	480
13	bit[10:0]	R/W	OPH_ACTIV_START	*Output Horizontal Active Start*	13
14	bit[10:0]	R/W	OPH_ACTIV_WIDTH	*Output Horizontal Active Width*	640