Ordering number : ENN7217

N-Channel and P-Channel Silicon MOSFET

FW352

Ultrahigh-Speed Switching Applications

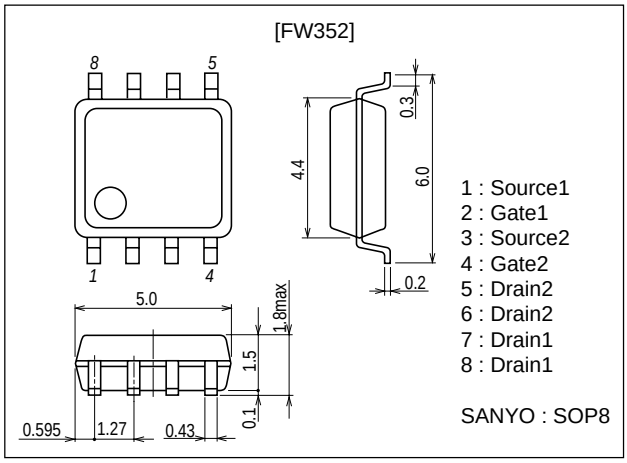
Features

- Low ON-resistance.
- Ultrahigh-speed switching.
- Dual chip device with both a p-channel and an n-channel MOSFETs encapsulated in one package for high-density mounting.
- High-density mounting.
- Excellent ON-resistance characteristic.

Package Dimensions

unit : mm

2129



Specifications

Absolute Maximum Ratings at Ta=25°C

Parameter	Symbol	Conditions	Ratings		Unit
			N-channel	P-channel	
Drain-to-Source Voltage	V_{DSS}		60	−60	V
Gate-to-Source Voltage	V_{GSS}		±20	±20	V
Drain Current (DC)	I_D		4	−2.4	A
Drain Current (Pulse)	I_{DP}	PW≤10μs, duty cycle≤1%	48	−32	A
Allowable Power Dissipation	P_D	Mounted on a ceramic board (1200mm²×0.8mm)1unit	1.7		W
Total Dissipation	P_T	Mounted on a ceramic board (1200mm²×0.8mm)	2.0		W
Channel Temperature	Tch		150		°C
Storage Temperature	Tstg		−55 to +150		°C

Electrical Characteristics at Ta=25°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[N-channel]						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=1mA, V_{GS}=0	60			V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=60V, V_{GS}=0			10	μA
Gate-to-Source Leakage Current	I_{GSS}	V_{GS}=±16V, V_{DS}=0			±10	μA
Cutoff Voltage	$V_{GS}(off)$	V_{DS}=10V, I_D=1mA	1.0		2.4	V
Forward Transfer Admittance	$\|yfs\|$	V_{DS}=10V, I_D=4A	5	7		S

Marking : W352

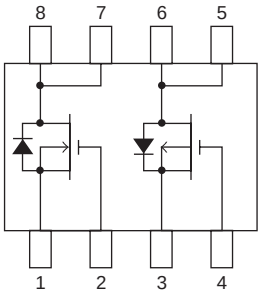
Continued on next page.

SANYO Electric Co.,Ltd. Semiconductor Company
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

Continued from preceding page.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Static Drain-to-Source On-State Resistance	$R_{DS}(on)1$	I_D=4A, V_{GS}=10V		70	90	mΩ
	$R_{DS}(on)2$	I_D=2A, V_{GS}=4V		90	125	mΩ
Input Capacitance	Ciss	V_{DS}=20V, f=1MHz		350		pF
Output Capacitance	Coss	V_{DS}=20V, f=1MHz		110		pF
Reverse Transfer Capacitance	Crss	V_{DS}=20V, f=1MHz		35		pF
Turn-ON Delay Time	$t_d(on)$	See specified Test Circuit.		9		ns
Rise Time	t_r	See specified Test Circuit.		40		ns
Turn-OFF Delay Time	$t_d(off)$	See specified Test Circuit.		40		ns
Fall Time	t_f	See specified Test Circuit.		55		ns
Total Gate Charge	Qg	V_{DS}=10V, V_{GS}=10V, I_D=4A		12		nC
Gate-to-Source Charge	Qgs	V_{DS}=10V, V_{GS}=10V, I_D=4A		2		nC
Gate-to-Drain “Miller” Charge	Qgd	V_{DS}=10V, V_{GS}=10V, I_D=4A		3		nC
Diode Forward Voltage	V_{SD}	I_S=4A, V_{GS}=0		0.81	1.2	V
[P-channel]						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=−1mA, V_{GS}=0	−60			V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=−60V, V_{GS}=0			−10	μA
Gate-to-Source Leakage Current	I_{GSS}	V_{GS}=±16V, V_{DS}=0			±10	μA
Cutoff Voltage	$V_{GS}(off)$	V_{DS}=−10V, I_D=−1mA	−1.0		−2.4	V
Forward Transfer Admittance	|yfs|	V_{DS}=−10V, I_D=−2.4A	3.2	4.6		S
Static Drain-to-Source On-State Resistance	$R_{DS}(on)1$	I_D=−2.4A, V_{GS}=−10V		165	215	mΩ
	$R_{DS}(on)2$	I_D=−1.2A, V_{GS}=−4V		230	320	mΩ
Input Capacitance	Ciss	V_{DS}=−20V, f=1MHz		440		pF
Output Capacitance	Coss	V_{DS}=−20V, f=1MHz		110		pF
Reverse Transfer Capacitance	Crss	V_{DS}=−20V, f=1MHz		33		pF
Turn-ON Delay Time	$t_d(on)$	See specified Test Circuit.		10		ns
Rise Time	t_r	See specified Test Circuit.		24		ns
Turn-OFF Delay Time	$t_d(off)$	See specified Test Circuit.		50		ns
Fall Time	t_f	See specified Test Circuit.		40		ns
Total Gate Charge	Qg	V_{DS}=−10V, V_{GS}=−10V, I_D=−2.4A		14		nC
Gate-to-Source Charge	Qgs	V_{DS}=−10V, V_{GS}=−10V, I_D=−2.4A		2		nC
Gate-to-Drain “Miller” Charge	Qgd	V_{DS}=−10V, V_{GS}=−10V, I_D=−2.4A		3.7		nC
Diode Forward Voltage	V_{SD}	I_S=−2.4A, V_{GS}=0		−0.81	−1.2	V

Electrical Connection

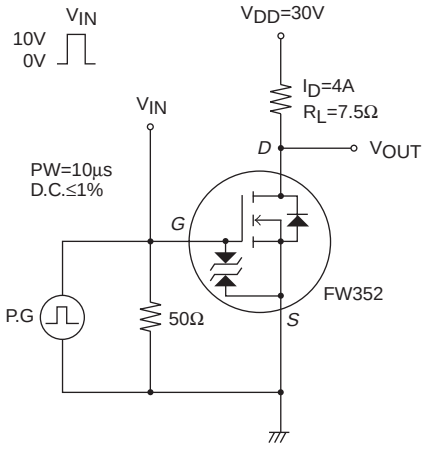


1 : Source1
2 : Gate1
3 : Source2
4 : Gate2
5 : Drain2
6 : Drain2
7 : Drain1
8 : Drain1

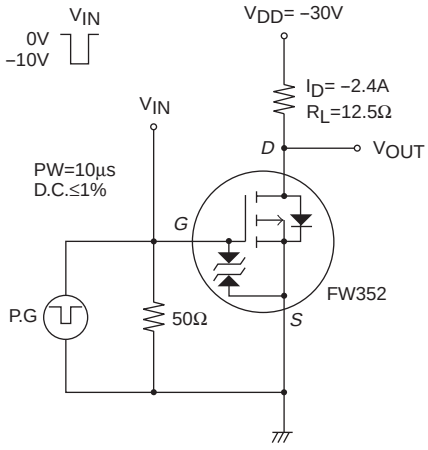
(Top view)

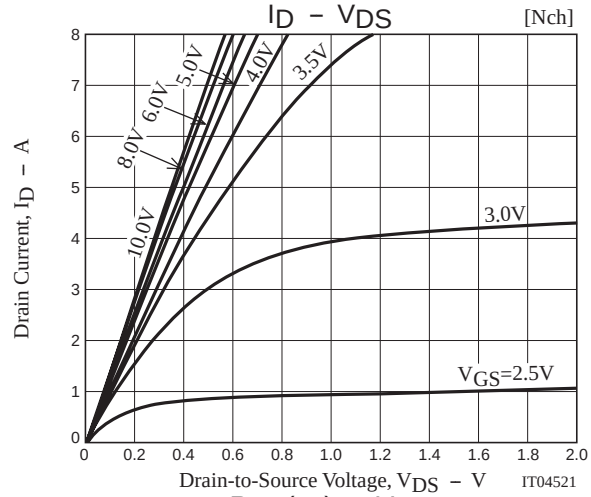
Switching Time Test Circuit

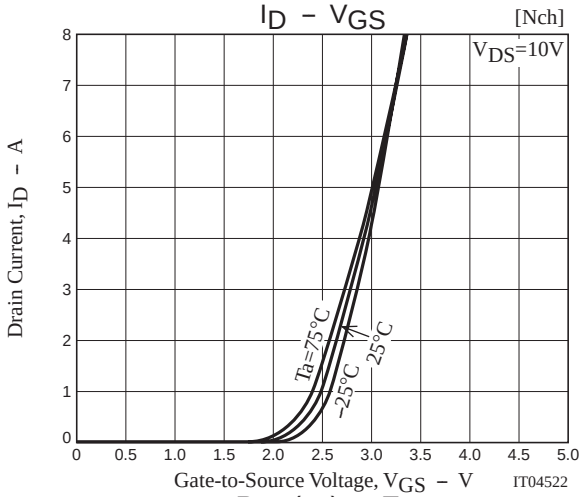
[N-channel]

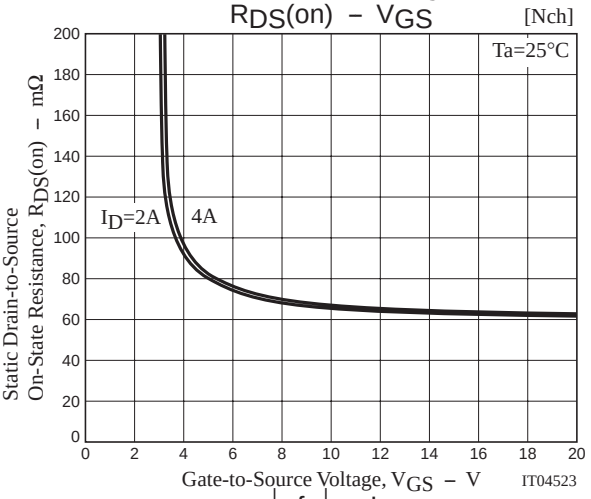


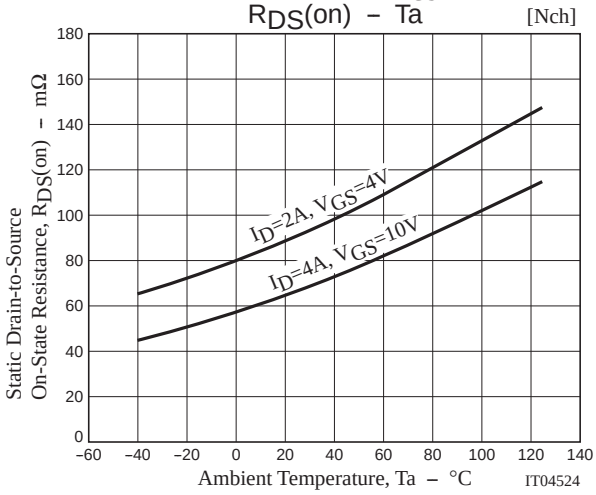
[P-channel]

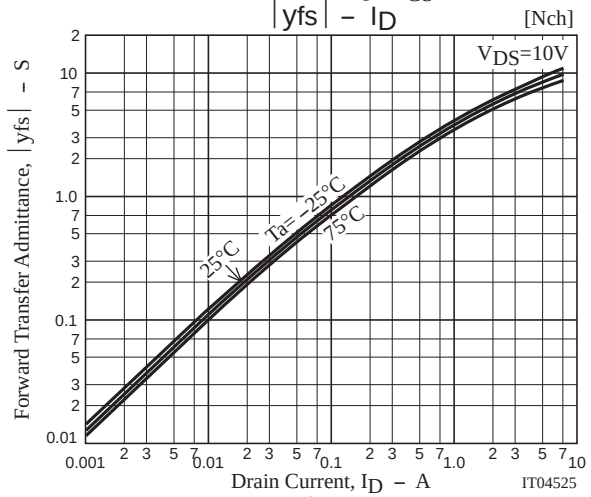


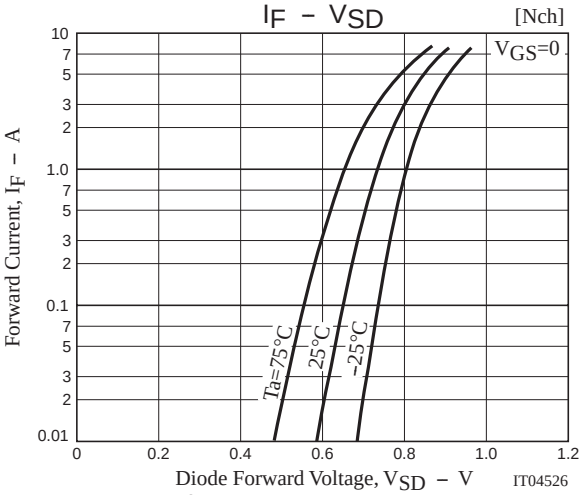

ID – VDS
[Nch]
Drain Current, ID – A
8.0V
6.0V
5.0V
4.0V
3.5V
10.0V
3.0V
VGS=2.5V
Drain-to-Source Voltage, VDS – V
IT04521

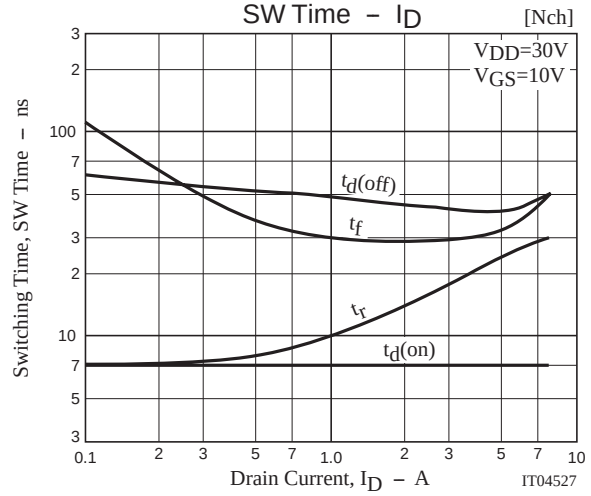

ID – VGS
[Nch]
VDS=10V
Drain Current, ID – A
Ta=75°C
25°C
–25°C
Gate-to-Source Voltage, VGS – V
IT04522

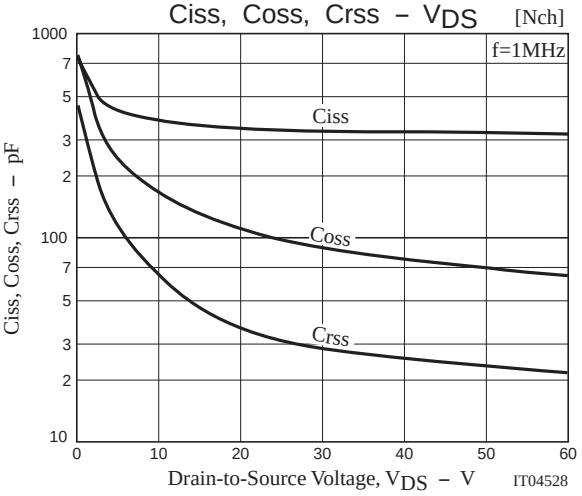

RDS(on) – VGS
[Nch]
Ta=25°C
Static Drain-to-Source On-State Resistance, RDS(on) – mΩ
ID=2A
4A
Gate-to-Source Voltage, VGS – V
IT04523

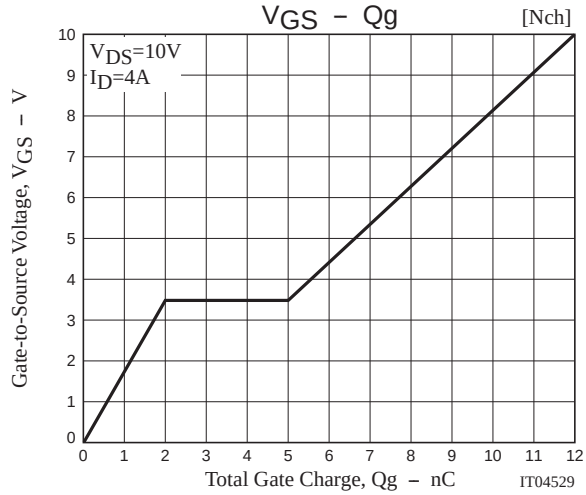

RDS(on) – Ta
[Nch]
Static Drain-to-Source On-State Resistance, RDS(on) – mΩ
ID=2A, VGS=4V
ID=4A, VGS=10V
Ambient Temperature, Ta – °C
IT04524

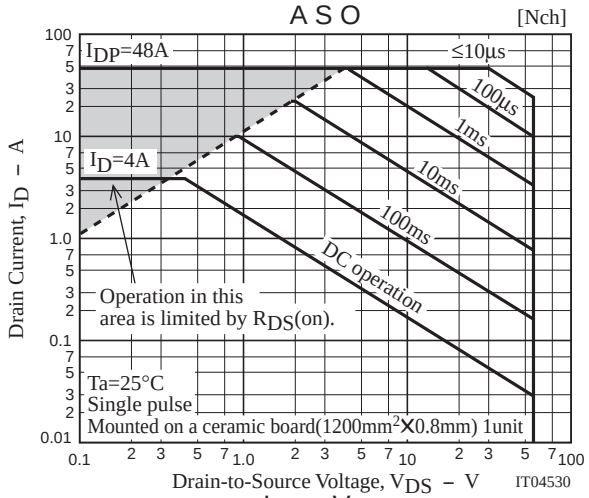

|yfs| – ID
[Nch]
VDS=10V
Forward Transfer Admittance, |yfs| – S
25°C
Ta=–25°C
75°C
Drain Current, ID – A
IT04525

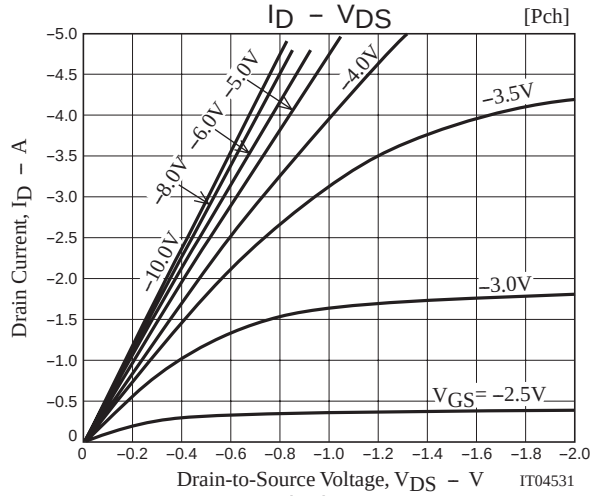

IF – VSD
[Nch]
VGS=0
Forward Current, IF – A
Ta=75°C
25°C
–25°C
Diode Forward Voltage, VSD – V
IT04526

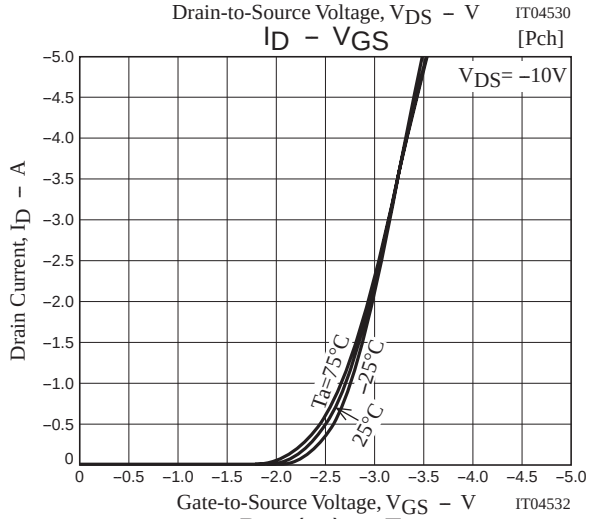

SW Time – ID
[Nch]
VDD=30V
VGS=10V
Switching Time, SW Time – ns
td(off)
tf
tr
td(on)
Drain Current, ID – A
IT04527

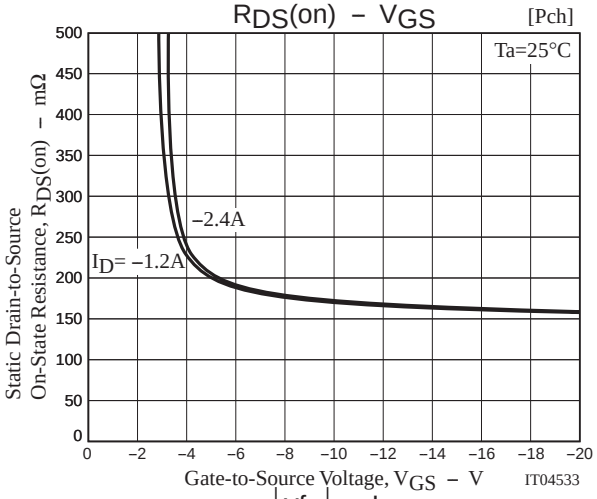

Ciss, Coss, Crss – VDS
[Nch]
f=1MHz
Ciss, Coss, Crss – pF
Ciss
Coss
Crss
Drain-to-Source Voltage, VDS – V
IT04528

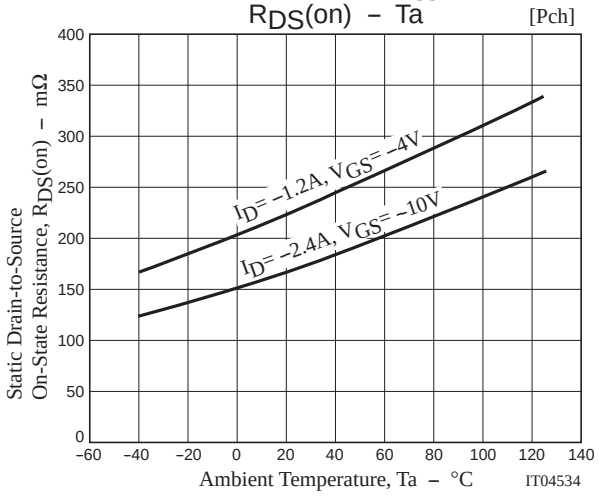

VGS – Qg
[Nch]
VDS=10V
ID=4A
Gate-to-Source Voltage, VGS – V
Total Gate Charge, Qg – nC
IT04529

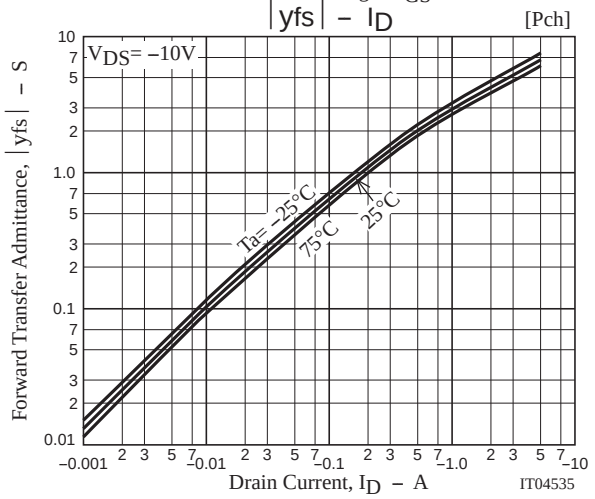

A S O
[Nch]
IDP=48A
≤10μs
100μs
1ms
10ms
100ms
DC operation
ID=4A
Operation in this area is limited by RDS(on).
Ta=25°C
Single pulse
Mounted on a ceramic board(1200mm2×0.8mm) 1unit
Drain Current, ID – A
Drain-to-Source Voltage, VDS – V
IT04530

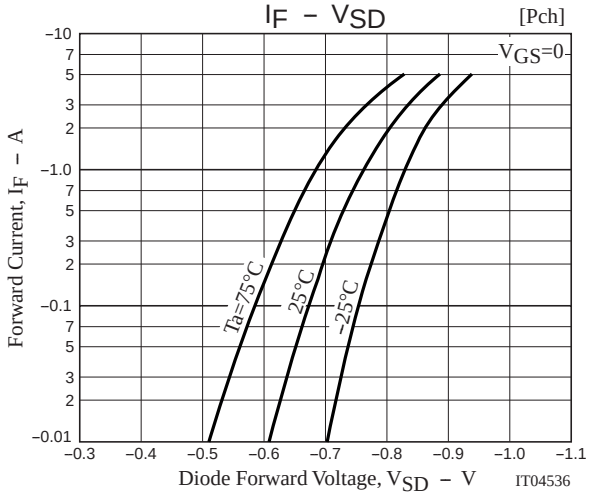

ID – VDS
[Pch]
–4.0V
–5.0V
–6.0V
–8.0V
–10.0V
–3.5V
–3.0V
VGS= –2.5V
Drain Current, ID – A
Drain-to-Source Voltage, VDS – V
IT04531


ID – VGS
[Pch]
VDS= –10V
Ta=75°C
–25°C
25°C
Drain Current, ID – A
Gate-to-Source Voltage, VGS – V
IT04532

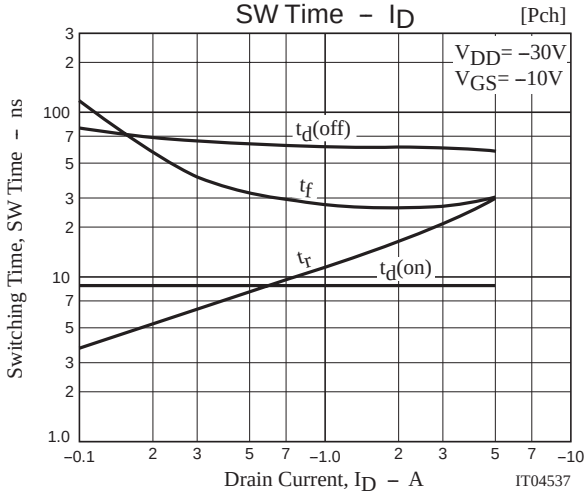

RDS(on) – VGS
[Pch]
Ta=25°C
–2.4A
ID= –1.2A
Static Drain-to-Source On-State Resistance, RDS(on) – mΩ
Gate-to-Source Voltage, VGS – V
IT04533


RDS(on) – Ta
[Pch]
ID= –1.2A, VGS= –4V
ID= –2.4A, VGS= –10V
Static Drain-to-Source On-State Resistance, RDS(on) – mΩ
Ambient Temperature, Ta – °C
IT04534

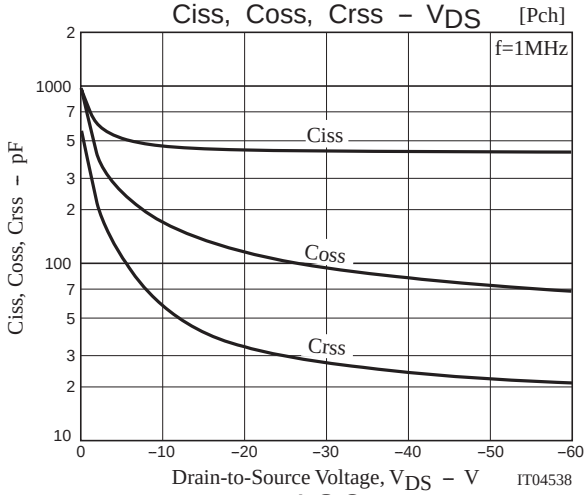

|yfs| – ID
[Pch]
VDS= –10V
Ta= –25°C
75°C
25°C
Forward Transfer Admittance, |yfs| – S
Drain Current, ID – A
IT04535


IF – VSD
[Pch]
VGS=0
Ta=75°C
25°C
–25°C
Forward Current, IF – A
Diode Forward Voltage, VSD – V
IT04536

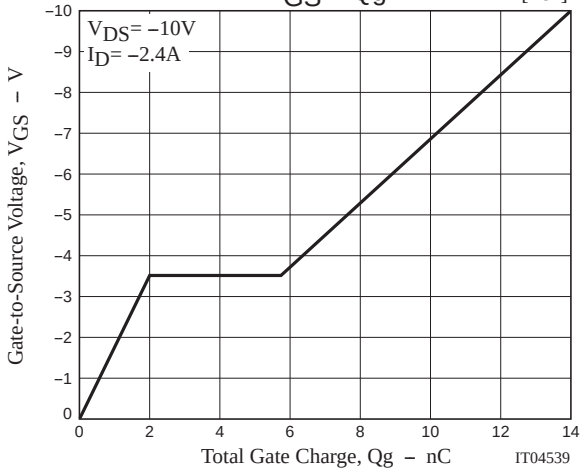
SW Time – I_D [Pch]



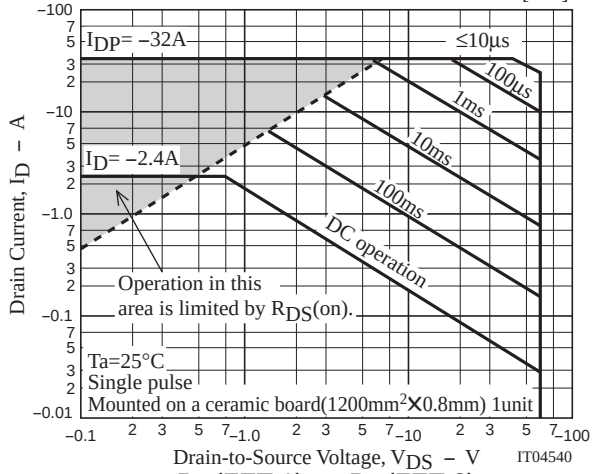
Ciss, Coss, Crss – V_{DS} [Pch]



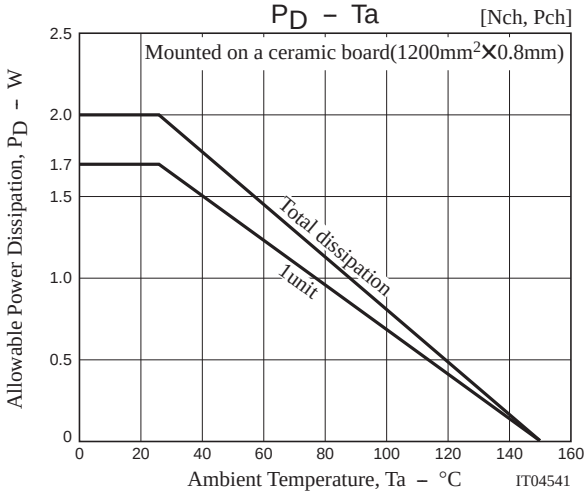
V_{GS} – Qg [Pch]



A S O [Pch]



P_D – Ta [Nch, Pch]



P_D(FET 1) – P_D(FET 2) [Nch, Pch]