Ordering number:ENN6389

N-Channel and P-Channel Silicon MOSFETs

FW313

Ultrahigh-Speed Switching Applications

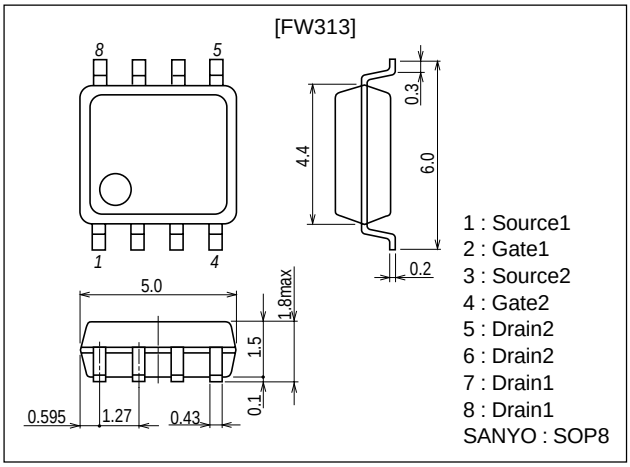
Features

- Low ON resistance.
- Ultrahigh-speed switching.
- Composite type with a N-channel MOSFET and a P-channel MOSFET driving from a 4V supply voltage contained in a single package.
- High-density mounting.

Package Dimensions

unit:mm

2129



Specifications

Absolute Maximum Ratings at Ta = 25˚C

Parameter	Symbol	Conditions	Ratings		Unit
			N-channel	P-channel	
Drain-to-Source Voltage	V_{DSS}		30	–30	V
Gate-to-Source Voltage	V_{GSS}		±20	±20	V
Drain Current (DC)	I_D		7	–5	A
Drain Current (pulse)	I_{DP}	PW≤10μs, duty cycle≤1%	28	–20	A
Allowable Power Dissipation	P_D	Mounted on a ceramic board (1000mm²×0.8mm) 1unit	1.7		W
Total Dissipation	P_T	Mounted on a ceramic board (1000mm²×0.8mm)	2.0		W
Channel Temperature	Tch		150		˚C
Storage Temperature	Tstg		–55 to +150		˚C

Electrical Characteristics at Ta = 25˚C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[N-channel]						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=1mA, V_{GS}=0	30			V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=30V, V_{GS}=0			10	μA
Gate-to-Source Leakage Current	I_{GSS}	V_{GS}=±16V, V_{DS}=0			±10	μA
Cutoff Voltage	$V_{GS}(off)$	V_{DS}=10V, I_D=1mA	1.0		2.4	V
Forward Transfer Admittance	| yfs |	V_{DS}=10V, I_D=7A	9	13		S
Static Drain-to-Source On-State Resistance	$R_{DS}(on)1$	I_D=7A, V_{GS}=10V		25	32	mΩ
	$R_{DS}(on)2$	I_D=4A, V_{GS}=4V		37	50	mΩ

Continued on next page.

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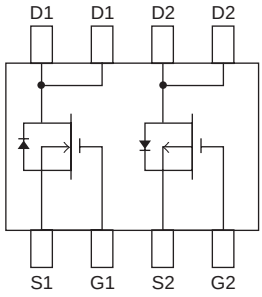
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

Continued from preceding page.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input Capacitance	Ciss	V_{DS}=10V, f=1MHz		700		pF
Output Capacitance	Coss	V_{DS}=10V, f=1MHz		380		pF
Reverse Transfer Capacitance	Crss	V_{DS}=10V, f=1MHz		180		pF
Turn-ON Delay Time	$t_{d(on)}$	See specified Test Circuit		15		ns
Rise Time	t_r	See specified Test Circuit		180		ns
Turn-OFF Delay Time	$t_{d(off)}$	See specified Test Circuit		90		ns
Fall Time	t_f	See specified Test Circuit		80		ns
Total Gate Charge	Qg	V_{DS}=10V, V_{GS}=10V, I_D=7A		22		nC
Gate-to-Source Charge	Qgs	V_{DS}=10V, V_{GS}=10V, I_D=7A		5		nC
Gate-to-Drain "Miller" Charge	Qgd	V_{DS}=10V, V_{GS}=10V, I_D=7A		6		nC
Diode Forward Voltage	V_{SD}	I_S=7A, V_{GS}=0		0.85	1.2	V
[P-channel]						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=–1mA, V_{GS}=0	–30			V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=–30V, V_{GS}=0			–10	μA
Gate-to-Source Leakage Current	I_{GSS}	V_{GS}=±16V, V_{DS}=0			±10	μA
Cutoff Voltage	V_{GS}(off)	V_{DS}=–10V, I_D=–1mA	–1.0		–2.5	V
Forward Transfer Admittance	| yfs |	V_{DS}=–10V, I_D=–5A	5	8		S
Static Drain-to-Source On-State Resistance	R_{DS}(on)1	I_D=–5A, V_{GS}=–10V		42	53	mΩ
	R_{DS}(on)2	I_D=–2A, V_{GS}=–4V		85	120	mΩ
Input Capacitance	Ciss	V_{DS}=–10V, f=1MHz		820		pF
Output Capacitance	Coss	V_{DS}=–10V, f=1MHz		470		pF
Reverse Transfer Capacitance	Crss	V_{DS}=–10V, f=1MHz		230		pF
Turn-ON Delay Time	$t_{d(on)}$	See specified Test Circuit		15		ns
Rise Time	t_r	See specified Test Circuit		150		ns
Turn-OFF Delay Time	$t_{d(off)}$	See specified Test Circuit		85		ns
Fall Time	t_f	See specified Test Circuit		90		ns
Total Gate Charge	Qg	V_{DS}=–10V, V_{GS}=–10V, I_D=–5A		25		nC
Gate-to-Source Charge	Qgs	V_{DS}=–10V, V_{GS}=–10V, I_D=–5A		5		nC
Gate-to-Drain "Miller" Charge	Qgd	V_{DS}=–10V, V_{GS}=–10V, I_D=–5A		7		nC
Diode Forward Voltage	V_{SD}	I_S=–5A, V_{GS}=0		–1.0	–1.5	V

Marking : W313

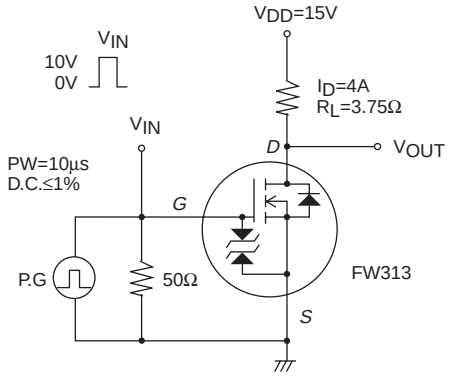
Electrical Connection



(Top view)

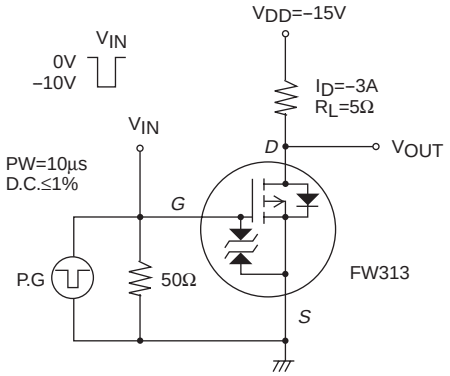
Switching Time Test Circuit

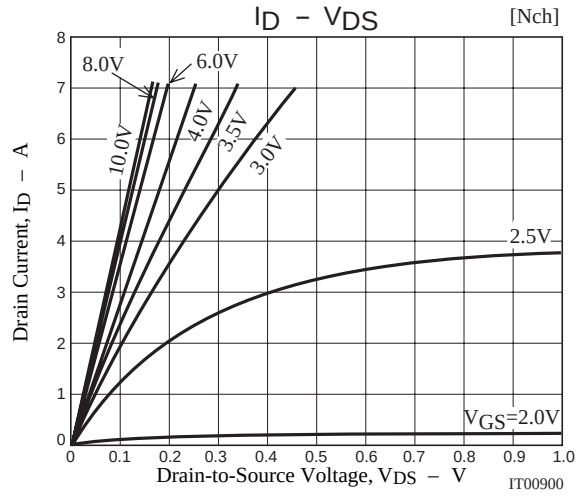
[N-channel]

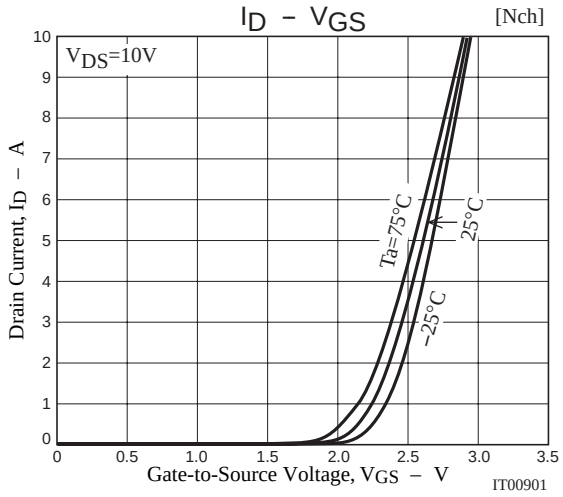


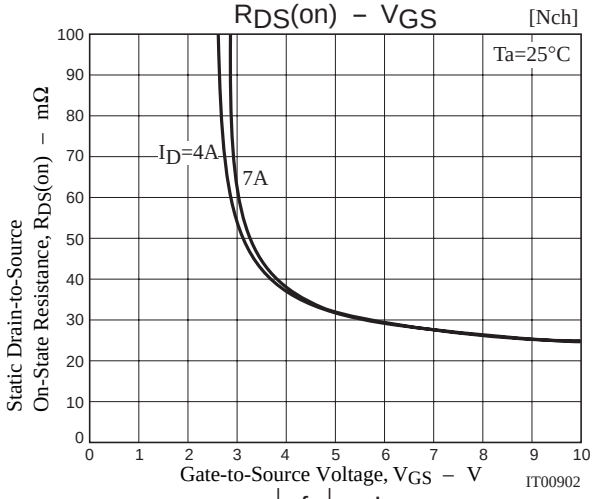
Switching Time Test Circuit

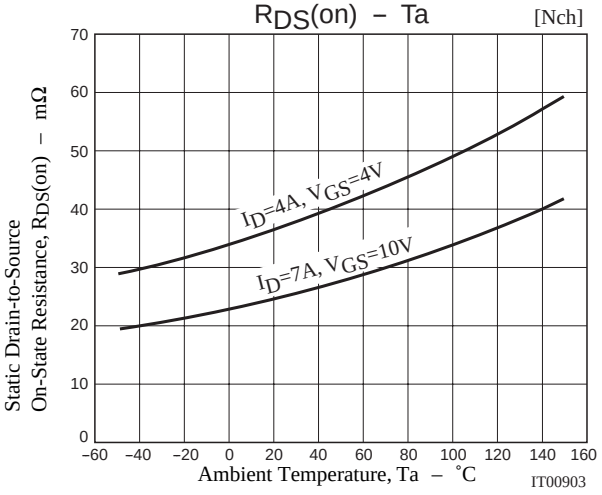
[P-channel]

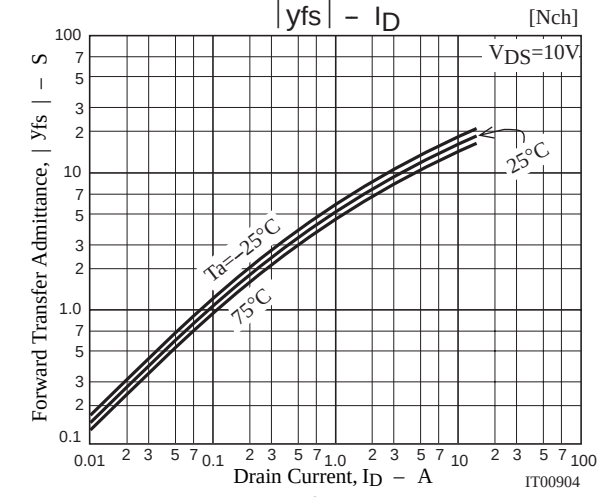


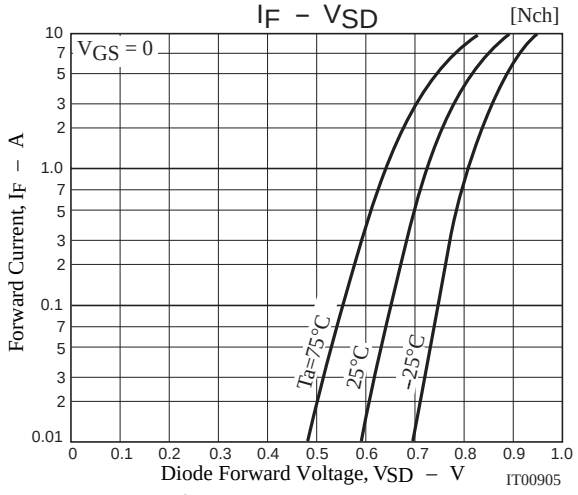

ID – VDS [Nch]
8.0V
6.0V
10.0V
4.0V
3.5V
3.0V
2.5V
VGS=2.0V
Drain Current, ID – A
Drain-to-Source Voltage, VDS – V
IT00900

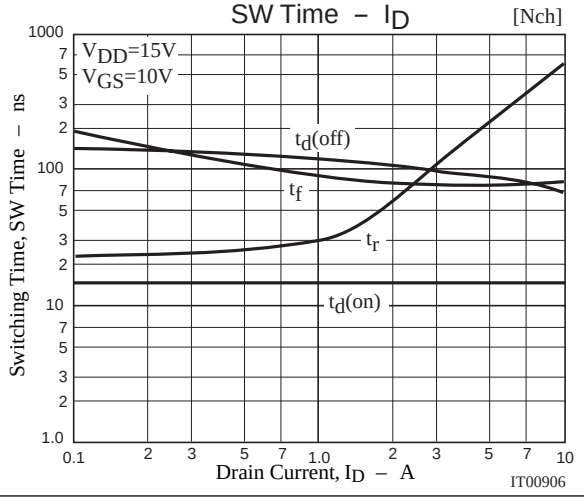

ID – VGS [Nch]
VDS=10V
Ta=75°C
25°C
–25°C
Drain Current, ID – A
Gate-to-Source Voltage, VGS – V
IT00901

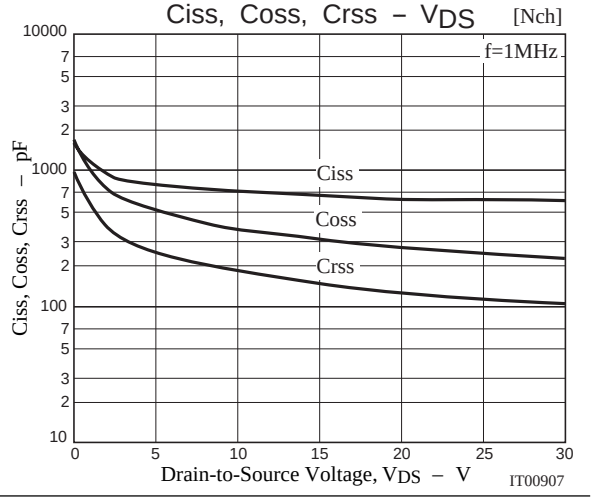

RDS(on) – VGS [Nch]
Ta=25°C
ID=4A
7A
Static Drain-to-Source On-State Resistance, RDS(on) – mΩ
Gate-to-Source Voltage, VGS – V
IT00902

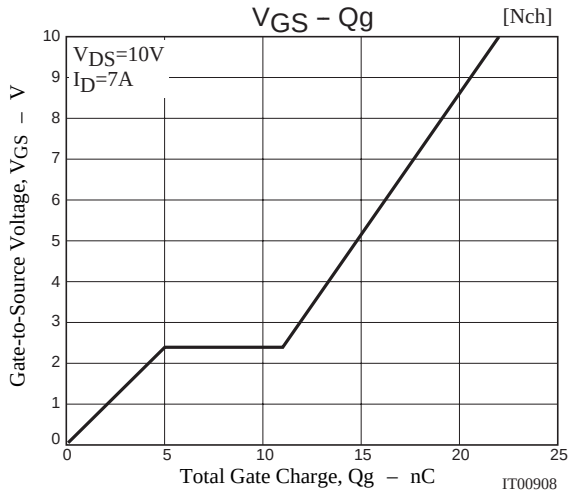

RDS(on) – Ta [Nch]
ID=4A, VGS=4V
ID=7A, VGS=10V
Static Drain-to-Source On-State Resistance, RDS(on) – mΩ
Ambient Temperature, Ta – °C
IT00903

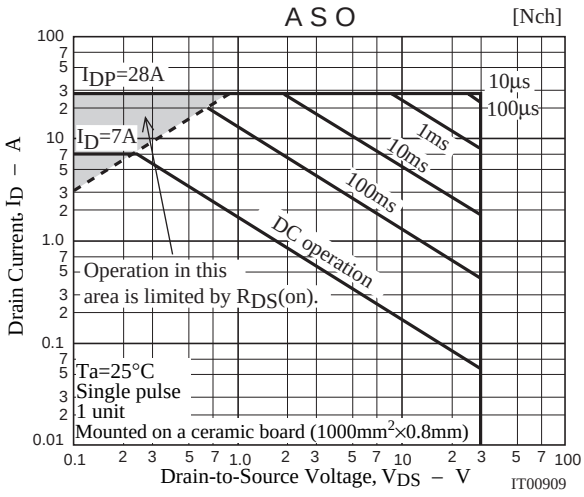

|yfs| – ID [Nch]
VDS=10V
25°C
Ta=–25°C
75°C
Forward Transfer Admittance, | yfs | – S
Drain Current, ID – A
IT00904

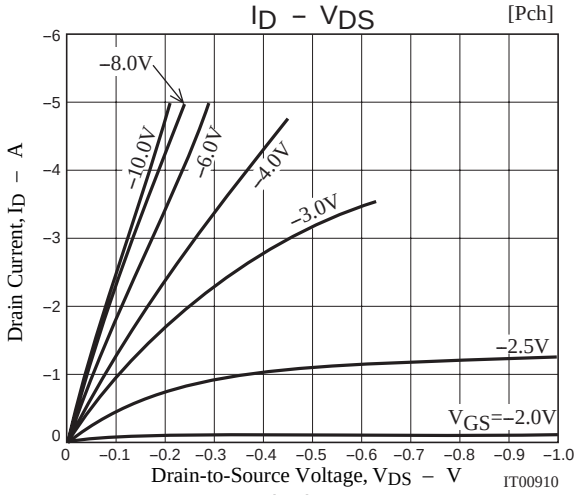

IF – VSD [Nch]
VGS = 0
Ta=75°C
25°C
–25°C
Forward Current, IF – A
Diode Forward Voltage, VSD – V
IT00905

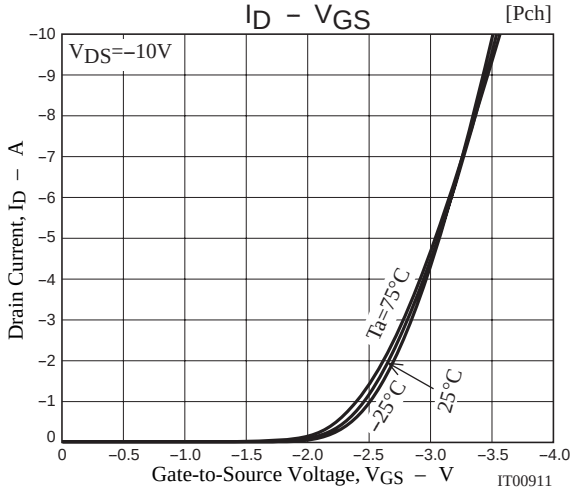

SW Time – ID [Nch]
VDD=15V
VGS=10V
td(off)
tf
tr
td(on)
Switching Time, SW Time – ns
Drain Current, ID – A
IT00906

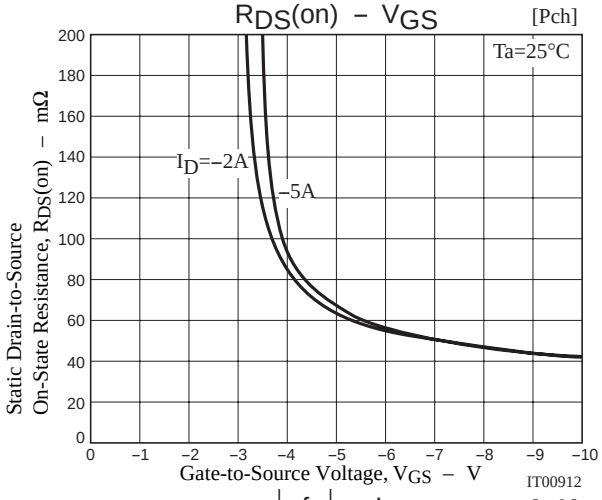

Ciss, Coss, Crss – VDS [Nch]
f=1MHz
Ciss
Coss
Crss
Ciss, Coss, Crss – pF
Drain-to-Source Voltage, VDS – V
IT00907

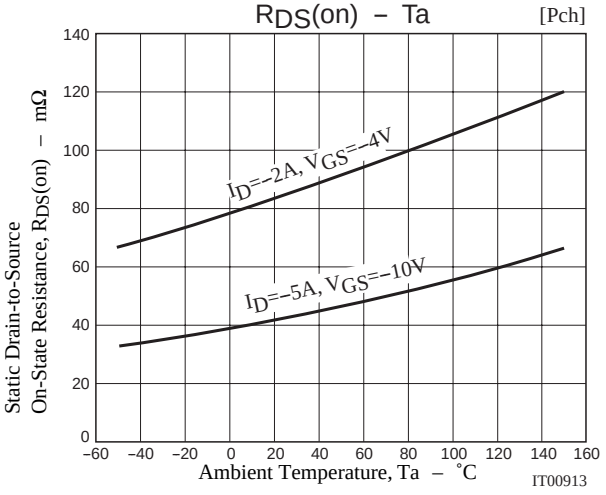

VGS – Qg
[Nch]
VDS=10V
ID=7A
Gate-to-Source Voltage, VGS – V
Total Gate Charge, Qg – nC
IT00908

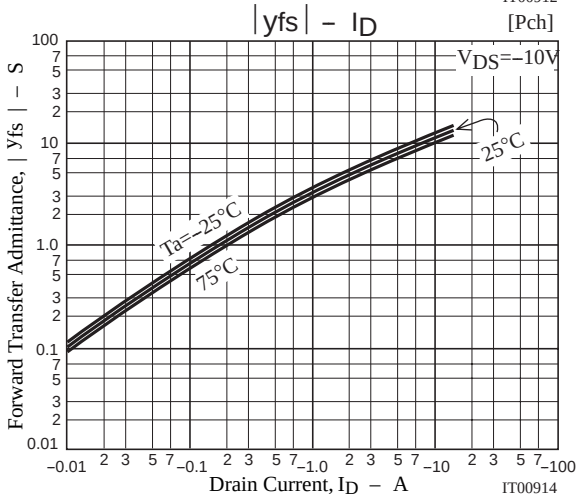

A S O
[Nch]
IDP=28A
ID=7A
10μs
100μs
1ms
10ms
100ms
DC operation
Operation in this
area is limited by RDS(on).
Ta=25°C
Single pulse
1 unit
Mounted on a ceramic board (1000mm2×0.8mm)
Drain Current, ID – A
Drain-to-Source Voltage, VDS – V
IT00909

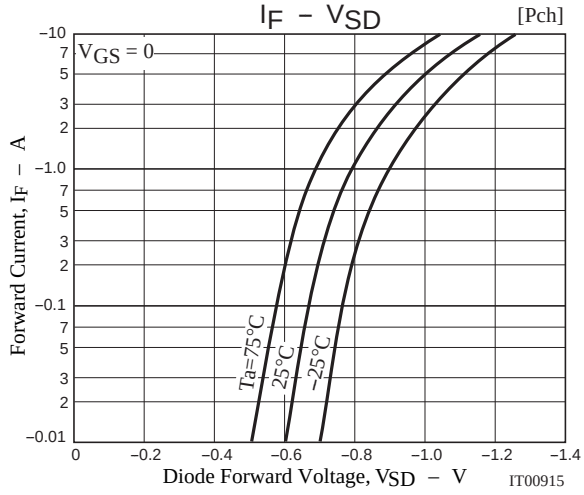

ID – VDS
[Pch]
–8.0V
–10.0V
–6.0V
–4.0V
–3.0V
–2.5V
VGS=–2.0V
Drain Current, ID – A
Drain-to-Source Voltage, VDS – V
IT00910


ID – VGS
[Pch]
VDS=–10V
Ta=75°C
25°C
–25°C
Drain Current, ID – A
Gate-to-Source Voltage, VGS – V
IT00911

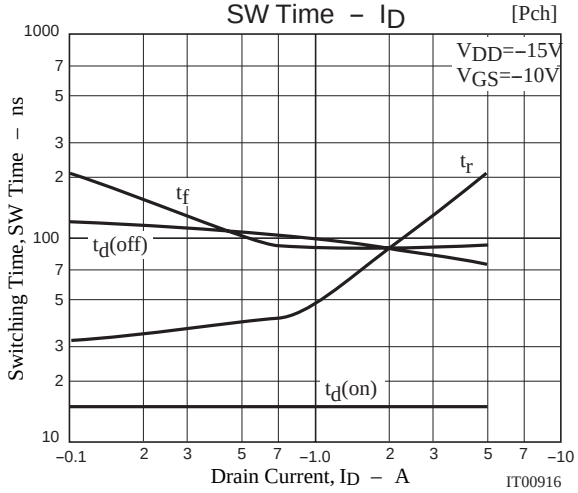

RDS(on) – VGS
[Pch]
Ta=25°C
ID=–2A
–5A
Static Drain-to-Source
On-State Resistance, RDS(on) – mΩ
Gate-to-Source Voltage, VGS – V
IT00912


RDS(on) – Ta
[Pch]
ID=–2A, VGS=–4V
ID=–5A, VGS=–10V
Static Drain-to-Source
On-State Resistance, RDS(on) – mΩ
Ambient Temperature, Ta – °C
IT00913

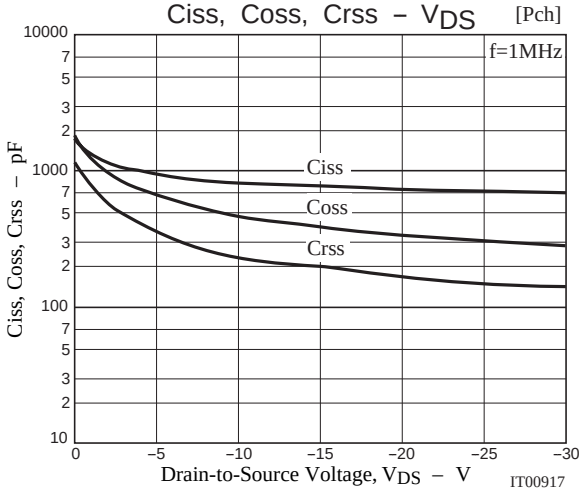

|yfs| – ID
[Pch]
VDS=–10V
25°C
Ta=–25°C
75°C
Forward Transfer Admittance, |yfs| – S
Drain Current, ID – A
IT00914


IF – VSD
[Pch]
VGS = 0
Ta=75°C
25°C
–25°C
Forward Current, IF – A
Diode Forward Voltage, VSD – V
IT00915

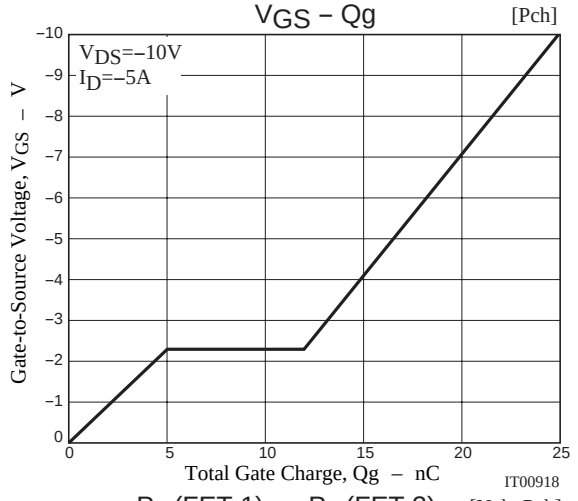
SW Time – I_D [Pch]



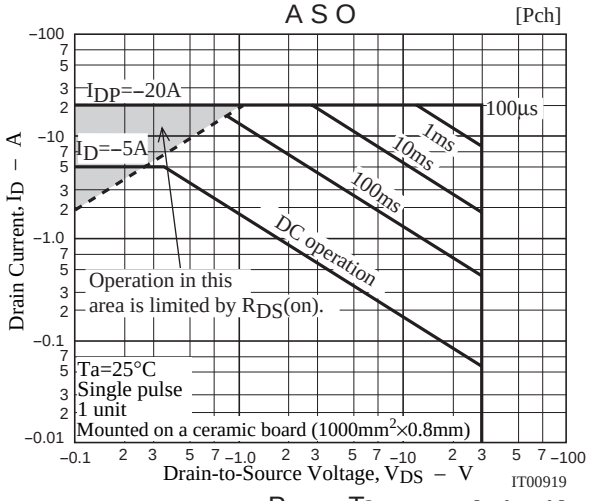
Ciss, Coss, Crss – V_{DS} [Pch]



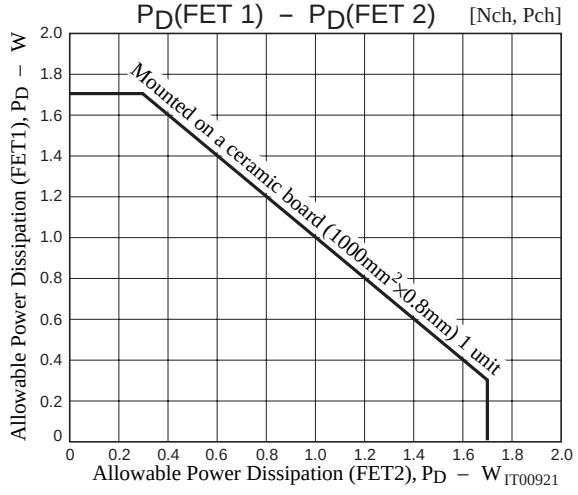
V_{GS} – Qg [Pch]



A S O [Pch]



P_D(FET 1) – P_D(FET 2) [Nch, Pch]



P_D – Ta [Nch, Pch]