Ordering number:ENN5048

N-Channel MOS Silicon FET

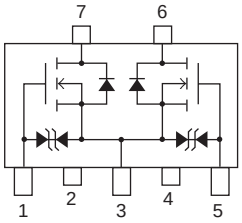
FP402

Ultrahigh-Speed Switching Applicaitons

Features

- Low ON resistance.
- Very high-speed switching.
- Complex type with 2 low-voltage-drive N-channel MOSFETs facilitating high-density mounting.

Electrical Connection



1:Gate
2:Drain
3:Source
4:Drain
5:Gate
6:Drain
7:Drain

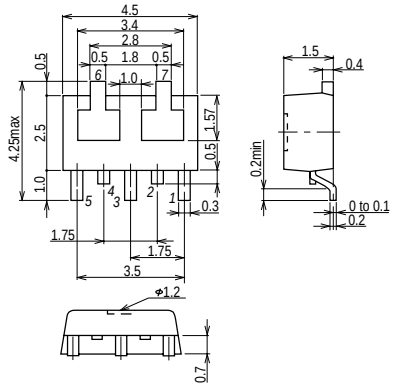
(Top view)

Package Dimensions

unit:mm

2102A

[FP402]



1:Gate
2:Drain
3:Source
4:Drain
5:Gate
6:Drain
7:Drain

SANYO:PCP5
(Bottom view)

Specifications

Absolute Maximum Ratings at Ta = 25˚C

Parameter	Symbol	Conditions	Ratings	Unit
Drain-to-Source Voltage	V_{DSS}		20	V
Gate-to-Source Voltage	V_{GSS}		±15	V
Drain Current (DC)	I_D		1	A
Drain Current (Pulse)	I_{DP}	PW≤10μs, duty cycle ≤1%	4	A
Allowable Power Dissipation	P_D	Tc=25˚C, 1 unit	2.0	W
	P_D	Mounted on ceramic board (250mm²×0.8mm) 1 unit	0.8	W
Total Power Dissipation	P_T	Mounted on ceramic board (250mm²×0.8mm)	1.1	W
Channel Temperature	Tch		150	˚C
Storage Temperature	Tstg		–55 to +150	˚C

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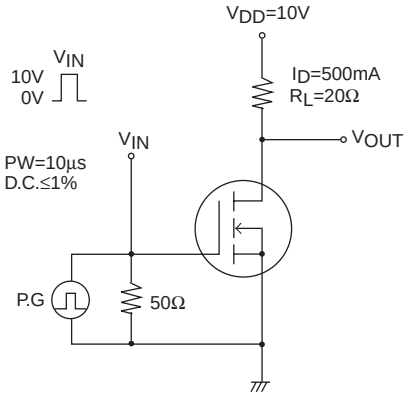
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

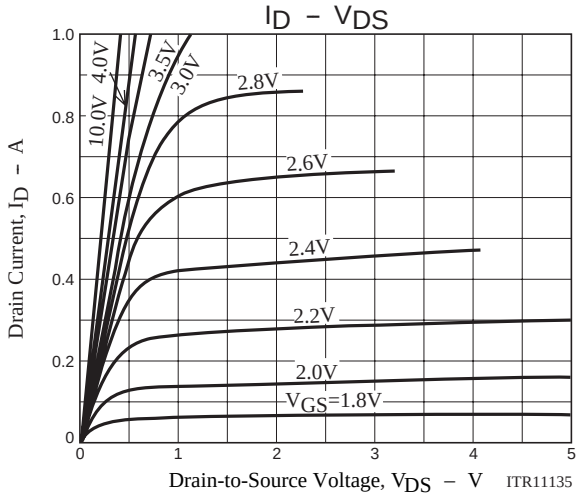
Electrical Characteristics at Ta=25˚C

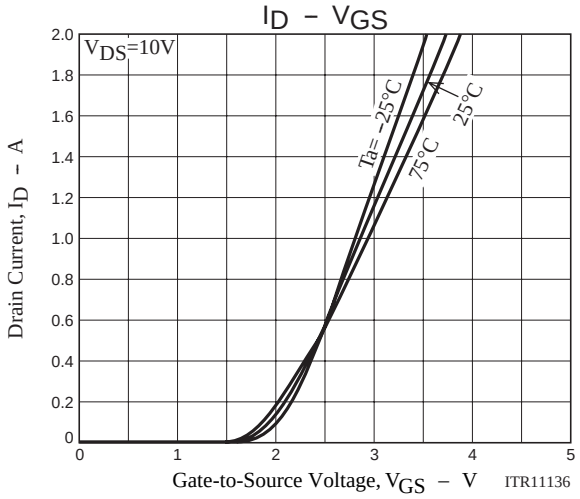
Parameter	Symbol	Conditons	Ratings			Unit
			min	typ	max	
D-S Breakdown Voltage	$V_{(BR)DSS}$	I_D=1mA, V_{GS}=0	20			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=20V, V_{GS}=0			100	μA
Gate-to-Source Leakage Current	I_{GSS}	V_{GS}=±12V, V_{DS}=0			±10	μA
Cutoff Voltage	$V_{GS(off)}$	V_{DS}=10V, I_D=1mA	0.8		2.0	V
Forward Transfer Admittance	$\lvert Y_{fs} \rvert$	V_{DS}=10V, I_D=500mA	0.6	1.0		S
Static Drain-to-Source ON-State Resistance	$R_{DS(on)}$	I_D=500mA, V_{GS}=10V		350	480	mΩ
	$R_{DS(on)}$	I_D=500mA, V_{GS}=4V		550	750	mΩ
Input Capacitance	Ciss	V_{DS}=10V, f=1MHz		50		pF
Output Capacitance	Coss	V_{DS}=10V, f=1MHz		45		pF
Reverse Transfer Capacitance	Crss	V_{DS}=10V, f=1MHz		15		pF
Turn-ON Delay Time	$t_{d(on)}$	See specified Test Circuit		8		ns
Rise Time	t_r	See specified Test Circuit		10		ns
Turn-OFF Delay Time	$t_{d(off)}$	See specified Test Circuit		30		ns
Fall Time	t_f	See specified Test Circuit		20		ns
Diode Forward Voltage	V_{SD}	I_S=1A, V_{GS}=0		1.0		V

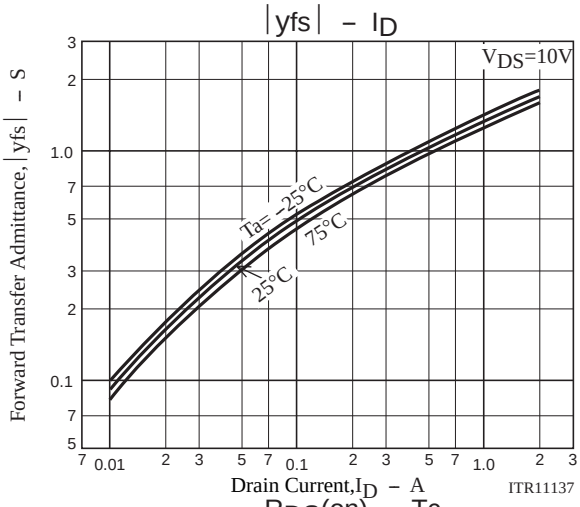
Marking:402

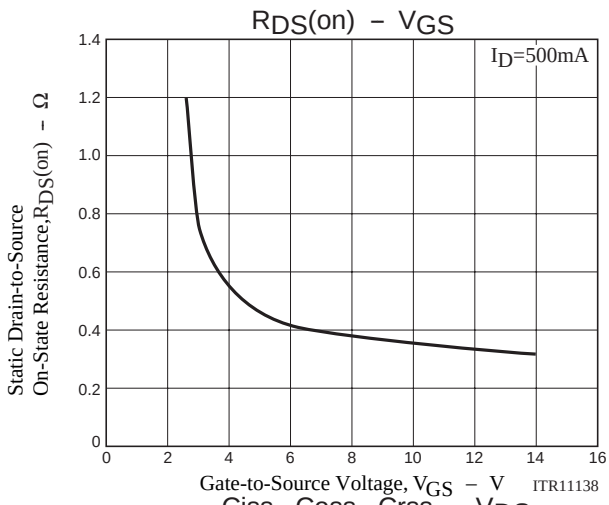
Switching Time Test Circuit

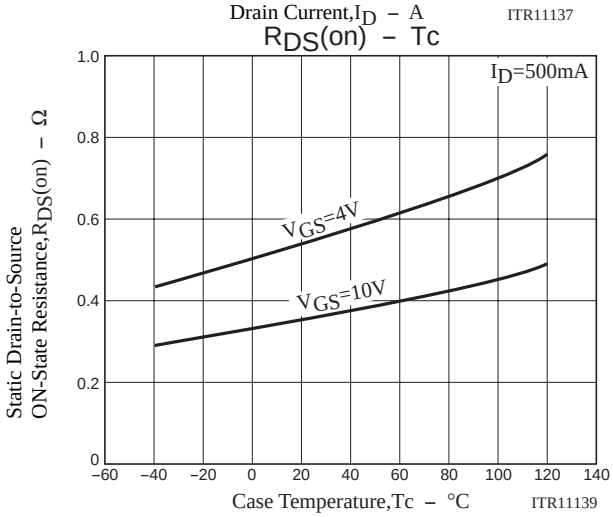


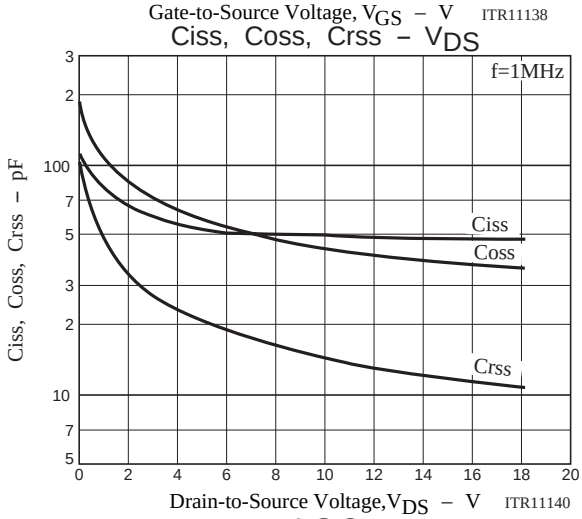


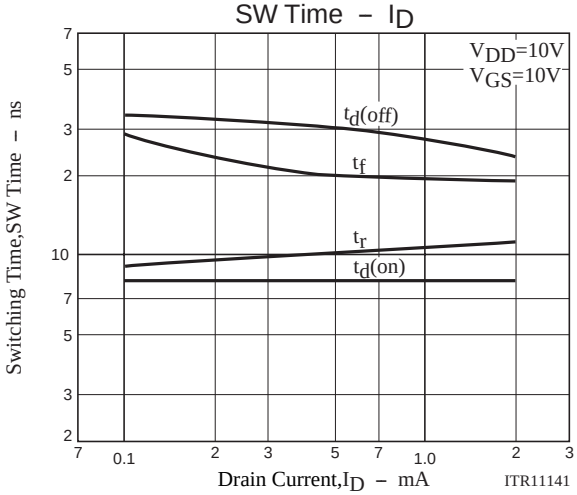


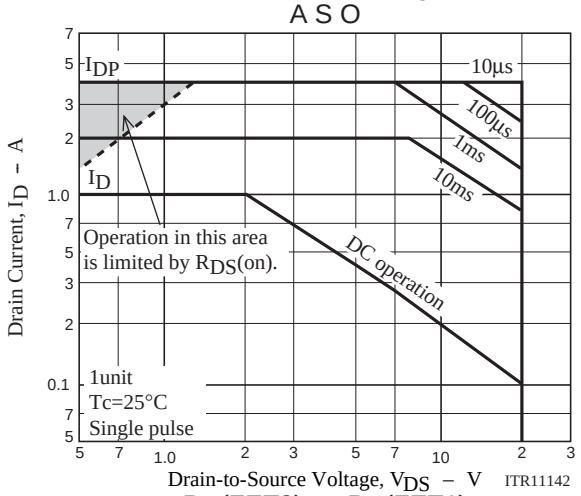

|yfs| – ID
VDS=10V
Ta= –25°C
75°C
25°C
Forward Transfer Admittance, |yfs| – S
Drain Current, ID – A
ITR11137

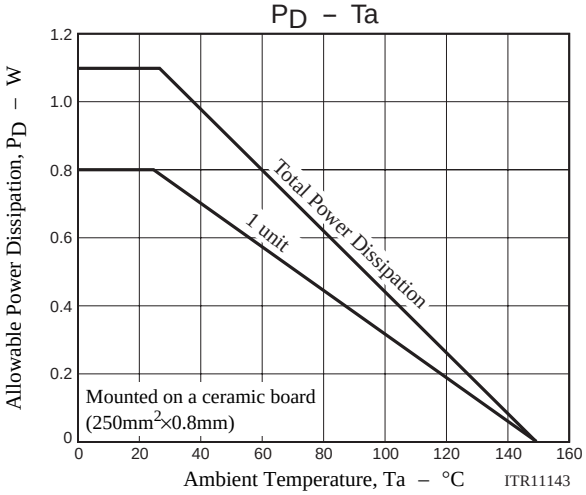

RDS(on) – VGS
ID=500mA
Static Drain-to-Source On-State Resistance, RDS(on) – Ω
Gate-to-Source Voltage, VGS – V
ITR11138

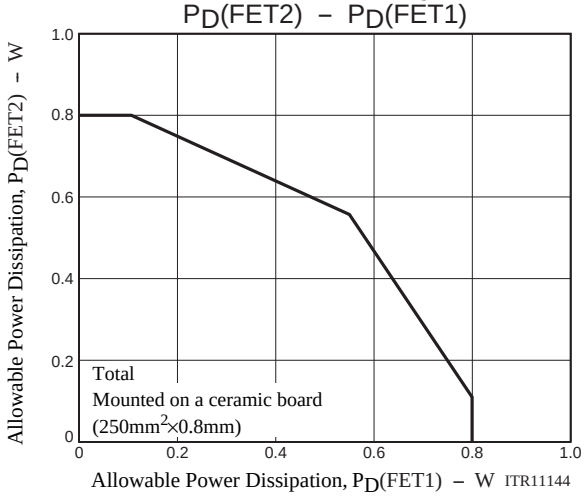

RDS(on) – Tc
ID=500mA
VGS=4V
VGS=10V
Static Drain-to-Source ON-State Resistance, RDS(on) – Ω
Case Temperature, Tc – °C
ITR11139


Ciss, Coss, Crss – VDS
f=1MHz
Ciss
Coss
Crss
Ciss, Coss, Crss – pF
Drain-to-Source Voltage, VDS – V
ITR11140


SW Time – ID
VDD=10V
VGS=10V
td(off)
tf
tr
td(on)
Switching Time, SW Time – ns
Drain Current, ID – mA
ITR11141


A S O
IDP
ID
10µs
100µs
1ms
10ms
DC operation
Operation in this area is limited by RDS(on).
1unit
Tc=25°C
Single pulse
Drain Current, ID – A
Drain-to-Source Voltage, VDS – V
ITR11142


PD – Ta
Total Power Dissipation
1 unit
Mounted on a ceramic board
(250mm2×0.8mm)
Allowable Power Dissipation, PD – W
Ambient Temperature, Ta – °C
ITR11143


PD(FET2) – PD(FET1)
Total
Mounted on a ceramic board
(250mm2×0.8mm)
Allowable Power Dissipation, PD(FET2) – W
Allowable Power Dissipation, PD(FET1) – W
ITR11144