FM573/574

Nonvolatile Octal Latch/Register

Features

8-bit Nonvolatile Latch

- Logic state is preserved in the absence of power
- Over 10 Billion (10^{10}) nonvolatile state changes
- Advanced high-reliability ferroelectric process

Operates like conventional CMOS logic

- Transparent (573) or D-Flip-flop (574) operation
- FM573 transparent for C high, latched for C low
- FM574 data is clocked on the rising edge of C
- 33/80 ns data propagation delay (5V/3V)
- 30 MHz/12 MHz Maximum frequency (5V/3V)

Automatic Nonvolatile Operation

- Latched state is stored automatically
- State is automatically restored on power-up
- Power supply monitor prevents low-VDD writes

Low Power Operation

- Supply voltage of 2.7V to 5.5V
- 100 µA standby current

Industry Standard Configuration

- Industrial temperature -40° C to +85° C
- 20-pin SOP or DIP

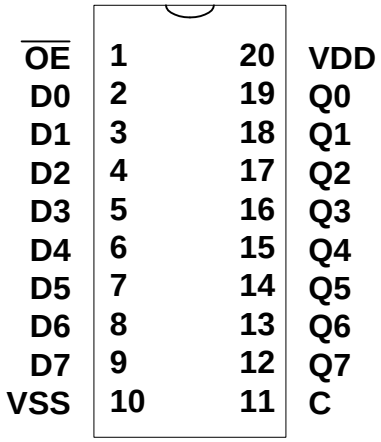
Description

The FM573 and FM574 are innovative circuits that store inputs like conventional logic families, and then retain the stored state in the absence of power. These products solve three basic problems in an elegant fashion. First, they provide continuous access to nonvolatile system settings without performing a memory read operation or using dedicated processor I/O pins. Second, they allow the storage of signals or data that may change frequently and possibly without notice. Third, they allow the nonvolatile storage of a few bits of data or system settings without the system overhead and extra pins of a serial memory. The FM573 is a transparent latch. The inputs are passed to the outputs when the clock is high; the state is latched when the clock goes low. The FM574 is a D-type register. Inputs are stored and passed to the outputs on the rising edge of the clock. The nonvolatile latch is a unique product that serves a variety of applications. A few ideas as follows:

- ✓ Controls relays and valves with automatic setting on power-up without processor intervention.
- ✓ Interface to soft/momentary front-panel switches and indicator lamps. Capture switch settings and light LED's without processor intervention.
- ✓ Replaces jumpers & control signal routing
- ✓ Initialize state of I/O card signals.
- ✓ Save system errors or status codes when power fails with a fast, no overhead write and automatic restore on power up.
- ✓ Eliminate the overhead of serial memory for systems needing only a few bits of data.

The FM573 and FM574 are provided in a 20-pin DIP or SOP. They are rated from –40C to +85C.

Pin Configuration



Pin Names	Function
D0-D7	Data in
Q0-Q7	Data Out
C	Clock/Latch Enable
/OE	Output enable
VSS	Ground
VDD	Supply Voltage

Ordering Information

FM573-P	Transparent latch, 20-pin plastic DIP
FM573-S	Transparent latch, 20-pin SOP
FM574-P	Register, 20-pin plastic DIP
FM574-S	Register, 20-pin SOP

Other package types may be available. Contact the factory for more information.

This data sheet contains design specifications for product development.
This product is still under development and these specifications
may change in any manner without notice

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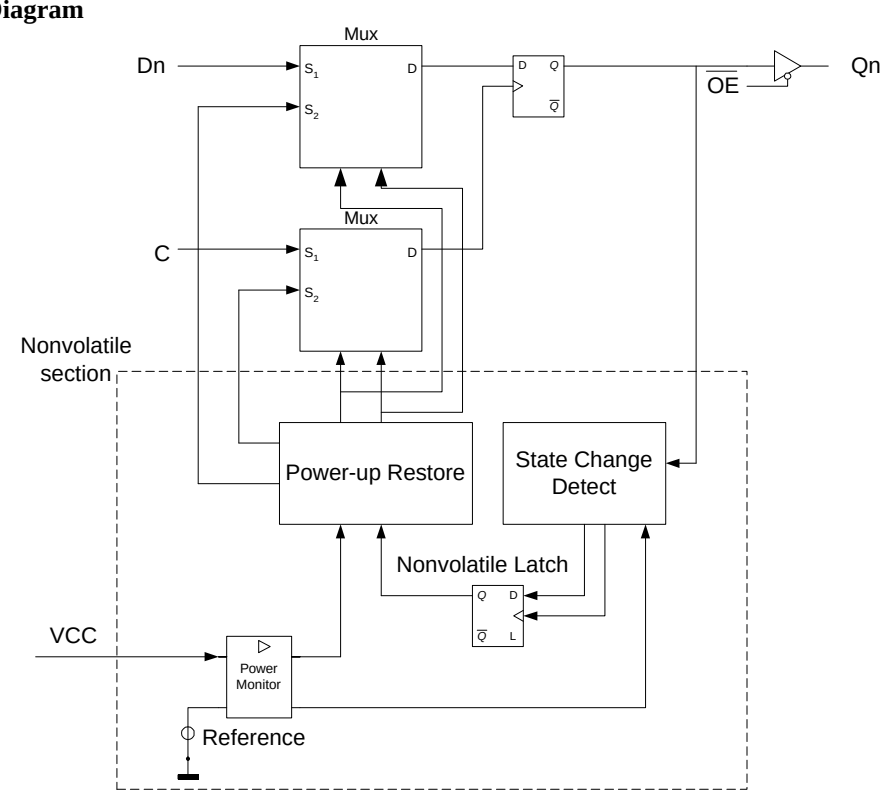
Figure 1. Block Diagram



Pin Description

Pin Name	Pin Number	I/O	Pin Description
/OE	1	I	Output enable. When low, the outputs are driven. When high, the outputs are tri-stated.
C	11	I	Controls the latching of data according to the truth tables below.
D0-D7	2-9	I	Data in.
Q0-Q7	12-19	O	Data out.
VSS	10	I	Ground
VDD	20	I	Supply Voltage

Functional Tables

FM573 Table

/OE	C	Dn	Internal Qn	Output Qn	Description
1	X	X	X	Hi-Z	Tri-state outputs
0	0	X	Qn	Qn	Outputs enabled, hold state
0	1	Dn	Dn	Dn	Transparent
1	1	Dn	Dn	Hi-Z	Load data, outputs tri-state

FM574 Table

/OE	C	Dn	Internal Qn	Output Qn	Description
1	X	X	X	Hi-Z	Tri-state outputs
0	X	X	Qn	Qn	Outputs enabled, hold state
0	↑	Dn	Dn	Dn	Load data, outputs enabled
1	↑	Dn	Dn	Hi-Z	Load data, outputs tri-state

Overview

Nonvolatile logic is a revolutionary product family that simplifies the design of system control functions. The FM573 is a transparent octal latch; the FM574 is an octal D-type register. These products are unique because the stored values also are retained in the absence of power. They are pin and functionally compatible with their industry standard CMOS equivalents. Any change in the latched state automatically is written into a nonvolatile ferroelectric latch. This function is possible due to the fast write time and extremely high write endurance of the underlying ferroelectric memory technology. A new state becomes nonvolatile no more than 500 ns (VDD=5V) after the write begins.

Users interface to a conventional latch rather than directly to the nonvolatile latch. Equivalent ferroelectric nonvolatile latches shadow the user's latches. They offer a very high but not unlimited number of write-cycles. Therefore, the internal state machine writes to the nonvolatile latch only if the latched state has changed in order to minimize the actual number of nonvolatile write-cycles. This determination is made independently for each bit. Due to the short write-time and realistic power slew rates, it is virtually impossible for the system to lose power before the nonvolatile state is acquired.

Power Down Sequence

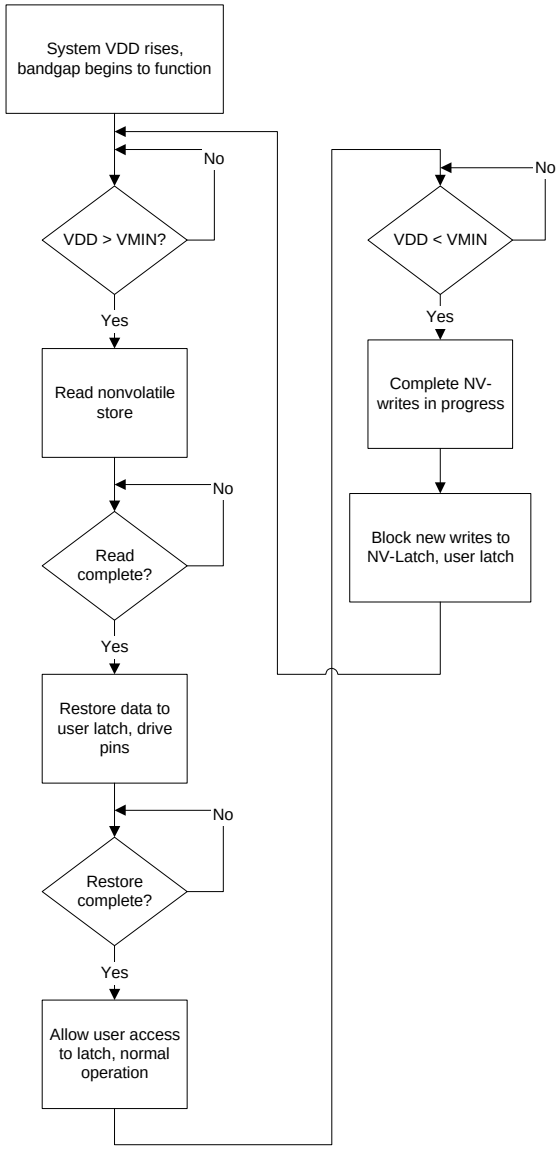
An internal power monitor blocks updates to the nonvolatile latch when VDD is below V_{MIN} (internal voltage reference). The power supply monitor also blocks write access to the user latch when VDD is below V_{MIN}. To guarantee a proper nonvolatile write of the last value, state changes should cease t_{PDS} before VDD reaches V_{MIN}. The V_{MIN} threshold is low enough that no special action may be needed in systems with slow slew rates. For fast power supply slew-rates or for systems that run down to relatively low supply voltages, the user should employ some form of low-VDD reset that trips above V_{MIN}.

Power Up

The V_{MIN} threshold is a critical parameter for several aspects of product operations. On power-up, the FM573/574 automatically restores the Qn outputs (and internal latches) to the previously stored state. This process begins as VDD rises to V_{MIN} and is completed t_{RES} afterward. Thus for all practical purposes, the nonvolatile values have been restored as soon as the system logic is functional on power-up. After the restore process, the latch is indistinguishable from its last state prior to power down and operates normally.

This power up sequence occurs as follows. On detection of a power-up, the internal nonvolatile latch is read. This value is then placed on an internal version of the Dn input. A single internal clock is generated to cause the user latch to accept the restored data. After this process is complete, the latch provides normal user-controlled operation. Users should not attempt to latch externally supplied data prior to t_{PUH} after VDD reaches V_{MIN}. The following diagram illustrates the power-up and down sequences.

Figure 2. Power Cycle Flow Chart



Functional Description - FM573

The FM573 is an octal transparent latch. The Qn outputs track the Dn inputs while the Clock C signal is logic 1. When the C signal goes to logic 0, the Dn inputs are latched. In this aspect, the FM573 operates identically to a conventional latch of the same type. As shown above, it has the same functional truth table as an ordinary 573-type product. The FM573 is unique in its behavior during power up and power down. It also is unique in providing behind the scenes intelligence to manage the storage of settings.

Each latched state is compared to the stored nonvolatile state. Comparison is made for each individual bit. If any bit has changed from its stored value, the new bit value automatically is written to the corresponding nonvolatile ferroelectric latch. Only the changed bits are written. For the transparent version, unlatched changes on the Qn outputs are not written to nonvolatile storage. This operation continues as long as power is within tolerance (above V_{MIN}). The nonvolatile circuit operates entirely in the background and has no operating impact. When power is lost, the nonvolatile shadow-latches retain the final latched state.

On power up, the ferroelectric latches are read. The outputs of these latches will be placed on the internal Dn inputs. The power control circuit will then cause the internal 'C' signal to go high. Rather than passing the inputs signal to the output in transparent fashion, it will pass the nonvolatile value instead. After satisfying the minimum high clock-time, the internal Clock is released and the nonvolatile value is loaded into the user latch. This entire restore process takes t_{RES} from $V_{DD} > V_{MIN}$. After the restored nonvolatile value is loaded into the user latch, normal operation begins. The first user write should occur t_{PUH} after $VDD > V_{MIN}$.

Functional Description - FM574

The FM574 is an octal D-register. Its behavior is similar to the FM573 except that Qn outputs do not change until the rising edge of the Clock. On the rising edge of the clock signal, the inputs are loaded and passed to the Qn outputs. In this aspect, the FM574 operates identically to a conventional latch of the same type.

The latched state is compared to the stored nonvolatile state for each bit. If any bit has changed from its stored value, the new value automatically is written to the nonvolatile ferroelectric latch. This operation continues as long as power is within tolerance. The nonvolatile circuit operates entirely in the background and has no operating impact. When power is lost, the nonvolatile shadow-latches retain the last latched state.

On power up, the ferroelectric latches are read. The outputs of these latches will be placed on the internal Dn inputs. The power control circuit will then cause the internal 'C' signal to go high. This rising edge passes the nonvolatile value instead of the external input into the user register. The internal Clock will then be released and the nonvolatile value will be stored into the user register. This entire restore process takes t_{RES} from $VDD > V_{MIN}$. After the restored nonvolatile value is loaded into the user register, normal operation begins. The first user write should occur t_{PUH} after $VDD > V_{MIN}$.

Applications

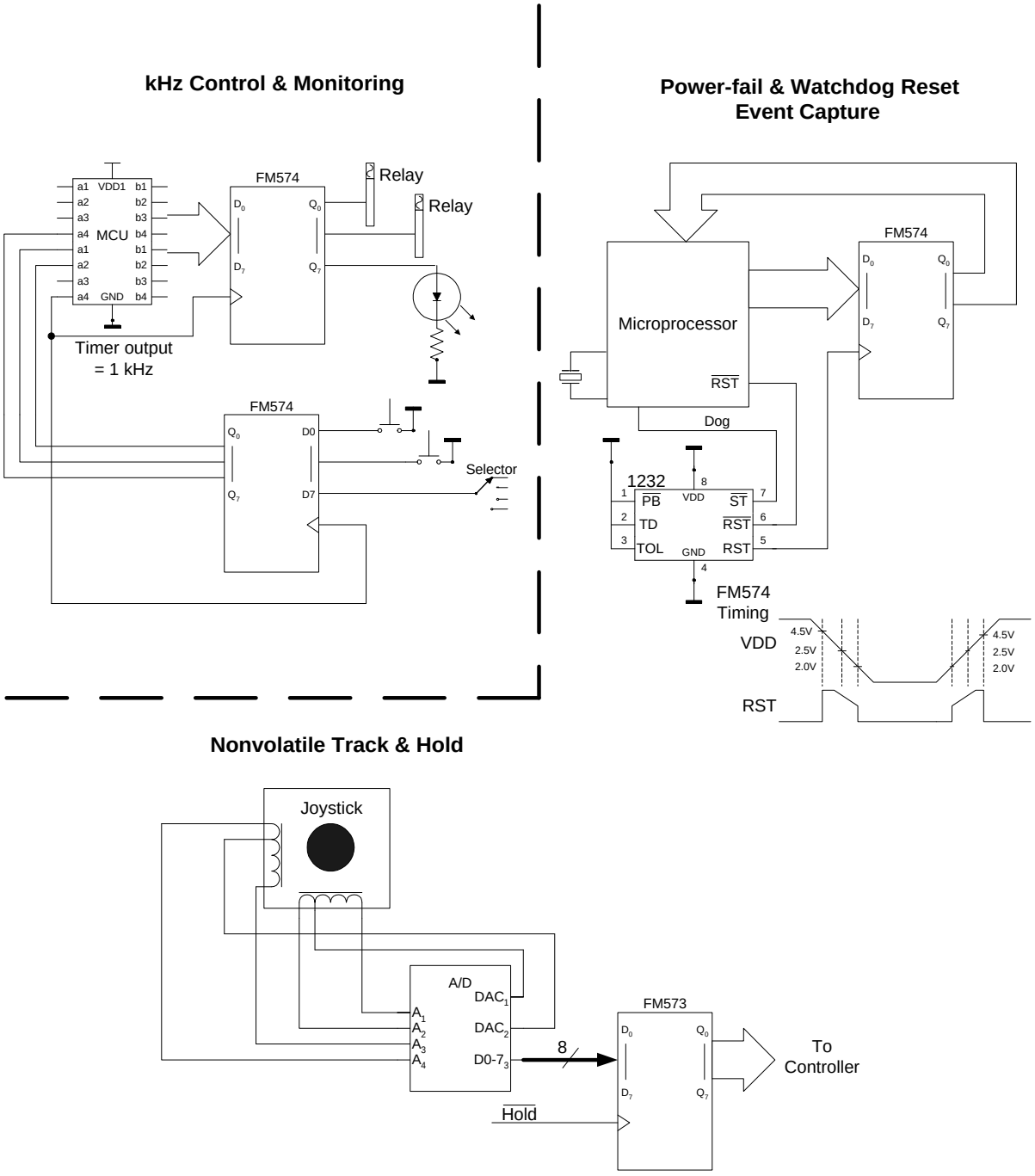
The FM573/FM574 runs at a speed that is comparable to the industry standard HC family logic. However, the nonvolatile-write operations, while fast in nonvolatile memory terms, are slower. Therefore, the nonvolatile logic runs 'behind' the user logic. Three practical scenarios are identified in this data sheet. One scenario that is not practical is to have rapidly changing states, at high speed, continuing indefinitely. For example, an address latch on a microprocessor bus is not feasible due to limited nonvolatile write endurance.

First, a free running clock in the kHz (or less) range is applied to the FM574. In this application, the nonvolatile logic can keep pace with state changes and continue for relatively long periods to indefinitely depending on the clock frequency. Slow mechanisms such as relays and valves can be controlled, and front panel interfaces can be made.

The second scenario is to employ an event driven clock. The host issues one clock or a high-speed burst as needed to an FM573 or FM574. In the case of a high speed burst, the nonvolatile logic may get behind, but will catch up when the burst is completed. A special variation is to connect the clock input to a power-down reset device. This circuit captures a snapshot of the inputs on power-down. In this application, care must be taken in the system design to avoid capturing the inputs on power-up and thereby losing the old setting. A clock that is either software generated or controlled by other logic may be used as well.

The third scenario is to monitor a continuous data stream and to hold it when an event occurs. This is analogous to a nonvolatile track-and-hold function. For this case, the hold signal is applied to an FM573. Diagrams of these applications are shown below.

Figure 3. Applications



This figure is a conceptual illustration of different modes of operation, not a complete circuit design.

Electrical Specifications

Absolute Maximum Ratings

Description	*Ratings*
Ambient storage or operating temperature	-40°C to + 85°C
Voltage on any pin with respect to ground	-1.0V to +7.0V
D.C. output current on any pin	TBD
Lead temperature (Soldering, 10 seconds)	300° C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and the functional operation of the device at these or any other conditions above those listed in the operational section of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

DC Operating Conditions TA = -40° C to + 85° C, VDD = 2.7V to 5.5V unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{DD}	Main Power Supply	2.7		5.5	V	1
V_{MIN}	State change blocked/restored	2.40	2.5	2.54	V	1,8
I_{SB}	Quiescent Supply Current			100	µA	2
I_{DDDY}	Dynamic Supply Current ex. 3.3V, 10 MHz, 8 inputs			20pF*V*f*n 5.28	A mA	3,4,5
I_{DDNV}	State Change Supply Current			500	µA	5
I_{LI}	Input Leakage Current			10	µA	6
I_{LO}	Output Leakage Current			10	µA	6
V_{IL}	Input Low Voltage	-0.3		0.3*VDD	V	1
V_{IH}	Input High Voltage	0.7*VDD		VDD + 0.5	V	1
V_{OH}	Output High Voltage @ IOH = -8 mA	VDD-0.8			V	1,7
V_{OL}	Output Low Voltage @ IOL = 8 mA			0.8	V	1,7

Notes

1. Referenced to VSS.
2. C = VSS, all other inputs at VDD or VSS
3. Dynamic supply current depends on the clock frequency, the frequency of inputs toggling, and the number of bits toggling. In the formula, V = VDD; f is clock frequency; n is the number of bits switching. The Dn inputs toggle at approximately a 50% duty-cycle at ½ of the frequency of C and comply with the minimum setup time. Outputs are tri-stated. All input levels at VDD and VSS. If C is static but the inputs toggle (573 in transparent mode), then the f should be the frequency of the inputs.
4. In a realistic system, the IDD needed to drive the loads also should be considered. $I_L = C_L*V*f_o$ *n where C_L is the load capacitance, V is the output swing voltage, f_o is the output frequency, and n is the number of bits switching.
5. Changes in state cause a nonvolatile write which adds a DC current component to the static power or dynamic for the duration of the nonvolatile write operation. The total current consumption after each state change = I_{SB} + I_{DDNV} + I_{DDDY}. After the state change is recorded, total current consumption = I_{SB} + $I_{DDDY.}$
6. VIN or VOUT = VSS to VDD
7. This parameter is characterized but not tested.
8. All state changes will be ignored when VDD is below V_{MIN}. VDD rising above V_{MIN} causes the user latch to be restored from the nonvolatile latch.

AC Parameters TA = -40° C to + 85° C, CL = 50 pF unless otherwise specified

		VDD=2.7V – 3.6V		VDD=5.0V +/- 10%			
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
f_{MAX}	Maximum clock frequency		12		30	MHz	
t_{CW}	Clock minimum pulse width	30		8		ns	
t_{PD}	Propagation delay Dn to Qn Propagation delay C to Qn		80		33	ns	
t_{EN}	Output enable time /OE to Qn		70		28	ns	
t_{DIS}	Output disable /OE to Qn Hi-Z		60		25	ns	1
t_{DS}	Data setup Dn to C low (573) Data setup Dn to C ↑ (574)	20		5		ns	
t_{DH}	Data hold Dn after C low (573) Data hold after C high (574)	5		5		ns	

Notes:
1 This parameter is characterized but not tested.

Capacitance TA = 25° C , f=1.0 MHz, VDD = 5V

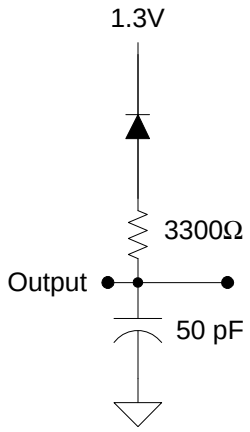
Symbol	Parameter	Max	Units	Notes
C_{IN}	Input capacitance	6	pF	1

Notes
1 This parameter is characterized but not tested.

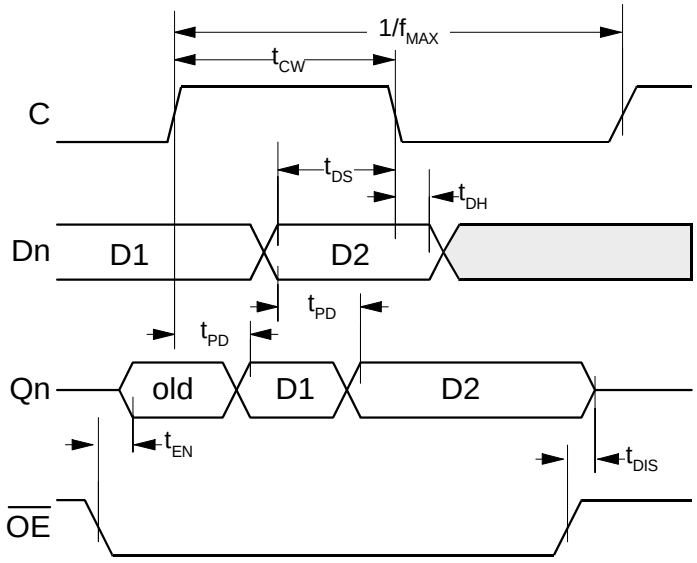
AC Test Conditions

Input Pulse Levels	0.1VDD to 0.9VDD
Input rise and fall times	10 ns
Input and output timing levels	0.3VDD, 0.7 VDD

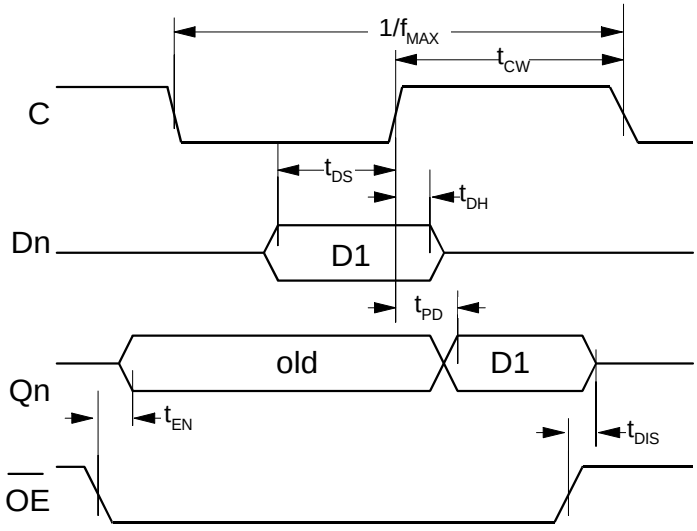
Equivalent AC Load Circuit



FM573 Timing



FM574 Timing



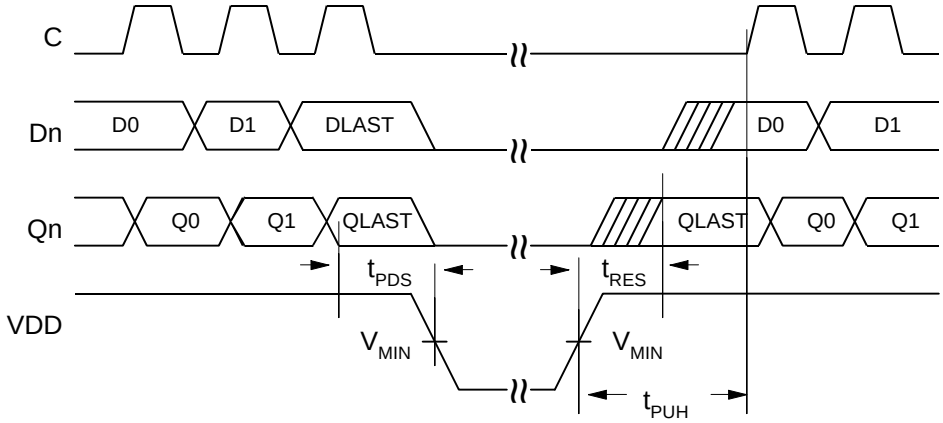
Power Cycling and Data Retention TA = -40° C to + 85° C, VDD = 2.7V to 5.5V unless otherwise specified

		VDD=2.7V – 3.6V		VDD=5.0V +/- 10%			
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
	Nonvolatile data retention	1		1		Year	1
	Latched state changes	1E10		1E10		Changes	2
t_{PDS}	Last state change to V_{MIN}	2		1		µS	3
t_{RES}	V_{MIN} to output valid		1		1	µS	4
t_{PUH}	V_{MIN} to first user write	1.5		1.5		µS	4,5

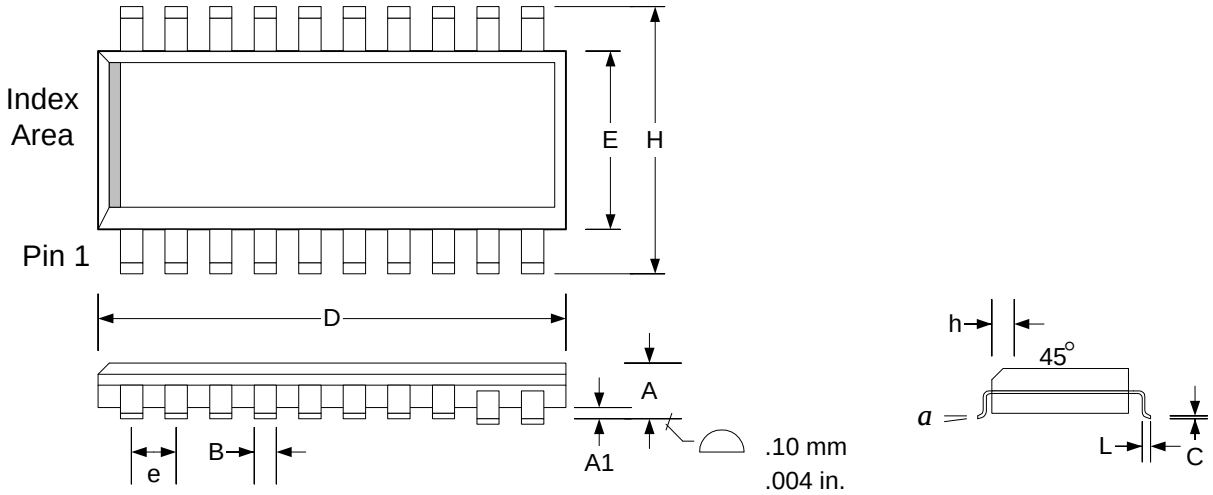
Notes:

1. Data retention is measured from the last state change, and is the time that a state will be retained at 55 °C and correctly restored on power-up. The process of powering up (and reading the nonvolatile state) refreshes the stored state and re-starts the data retention period even if the state is unchanged.
2. The nonvolatile elements are written when the latched state changes. Changes on either Dn or Qn that are not latched have no effect.
3. The last write to the nonvolatile latch element must occur prior to reaching V_{MIN} during a power down.
4. After the power supply reaches approximately V_{MIN} during a power up, the nonvolatile latch is read and the value restored to the user latch. This spec. provides the time needed to restore the FM573/FM574 pins to the restored state depending on the state of /OE.
5. The user should not attempt to write during the restore process. In particular, powering up in transparent mode (FM573) defeats the purpose of using a nonvolatile latch.

Power Cycle Timing (574-timing shown)



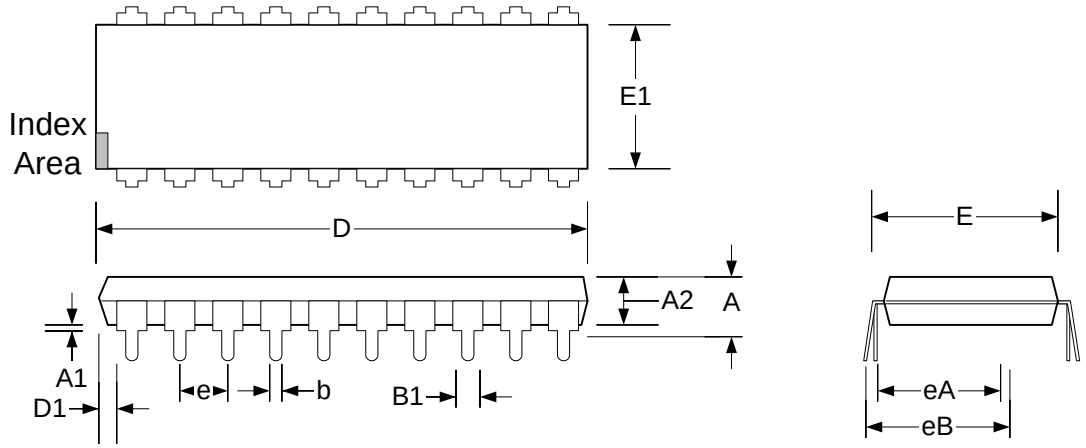
20-pin SOP



Controlling dimensions is in millimeters. Conversions to inches are not exact.

Symbol	Dim	Min	Nom.	Max
A	mm in.	2.35 0.0926		2.65 0.1043
A1	mm in.	0.10 0.004		0.30 0.0118
B	mm in.	0.33 0.013		0.51 0.020
C	mm in.	0.23 0.0091		0.32 0.0125
D	mm in.	12.6 0.4961		13.0 0.5118
E	mm in.	7.40 0.2914		7.60 0.2992
e	mm in.		1.27 BSC 0.050 BSC	
H	mm in.	10.00 0.394		10.65 0.419
h	mm in.	0.25 0.010		0.75 0.029
L	mm in.	.40 0.016		1.27 0.050
α		0°		8°

20-pin DIP



Controlling dimensions is in inches. Conversions to millimeters are not exact.

Symbol	Dim	Min	Nom.	Max
A	in. mm	.140 3.56		.190 4.83
A1	in. mm	.015 .381		.060 1.52
A2	in. mm	.120 3.05		.140 3.56
B	in. mm	.015 .381		.020 .508
B2	in. mm	.055 1.40		.065 1.65
D	in. mm	.970 24.64		1.04 26.42
E	in. mm	.280 7.11		.325 8.26
E1	in. mm	.250 6.35		.270 6.86
e	in. mm	.090 2.29	.100 2.54	.110 2.79
eA	in. mm		.300 BSC 7.62 BSC	
eB	in. mm	.310 7.87		.385 9.78