Product Preview

FM3808

256Kb Bytewide FRAM w/Real-time Clock

Features

256K bit Ferroelectric Nonvolatile RAM

- Organized as 32,752 x 8 bits
- High endurance 10 Billion (10^{10}) read/writes
- 10 year data retention at 55° C
- NoDelay™ write
- 70 ns access time/120 ns cycle time
- Built-in Low VDD protection

Real-time clock/calendar function in BCD format

- Clock registers in top 16 bytes of address space
- Backup power from external capacitor or battery
- Tracks seconds through centuries in BCD format
- Tracks leap years through 2100
- Runs from a 32.768 kHz timekeeping crystal

System supervisor function

- Programmable clock/calendar alarm
- Programmable watchdog timer
- Programmable power supply monitor
- Interrupt output programmable active high/low
- Control settings inherently nonvolatile
- Generates either processor reset or interrupt

Low Power Operation

- 5V Operation for memory and clock interface
- VBAK backup voltage 2.5V to 5.5V
- 15 mA IDD active current
- 1 µA IBAK clock backup current

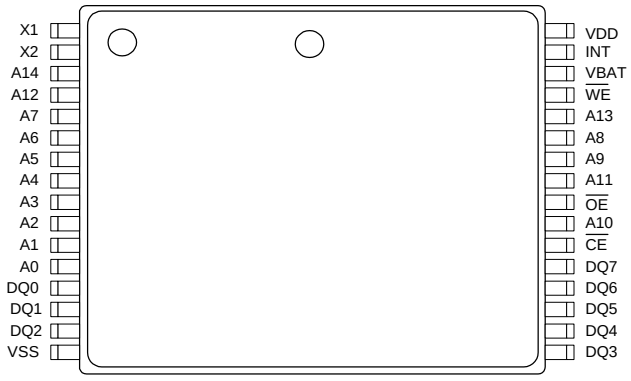
Description

The FM3808 combines a 256Kb FRAM array with a real-time clock and a system supervisor function. The timekeeping function is driven by a user supplied 32.768 kHz crystal. It maintains time and date settings in the absence of system power through the user's choice of backup power source – either capacitor or battery. In either case data does not depend on the backup source, it remains nonvolatile in FRAM. In addition to timekeeping, the FM3808 includes a system supervisor to manage low VDD power conditions and a watchdog timer function. A programmable interrupt output pin allows the user to select the supervisor functions and the polarity of the signal.

Both the FRAM array and the timekeeping function are accessed through the memory interface. The upper 16-address locations of the memory space are allocated to the timekeeping registers rather than to memory.

The FRAM array provides data retention for 10 years in the absence of system power, and is not dependent on the backup power source used for the clock. This eliminates system concerns over data loss in a traditional battery backed RAM solution. In addition, clock and supervisor control settings are implemented in FRAM rather than battery-backed RAM, making them more dependable. The FM3808 offers guaranteed operation over an industrial temperature range of -40°C to +85°C.

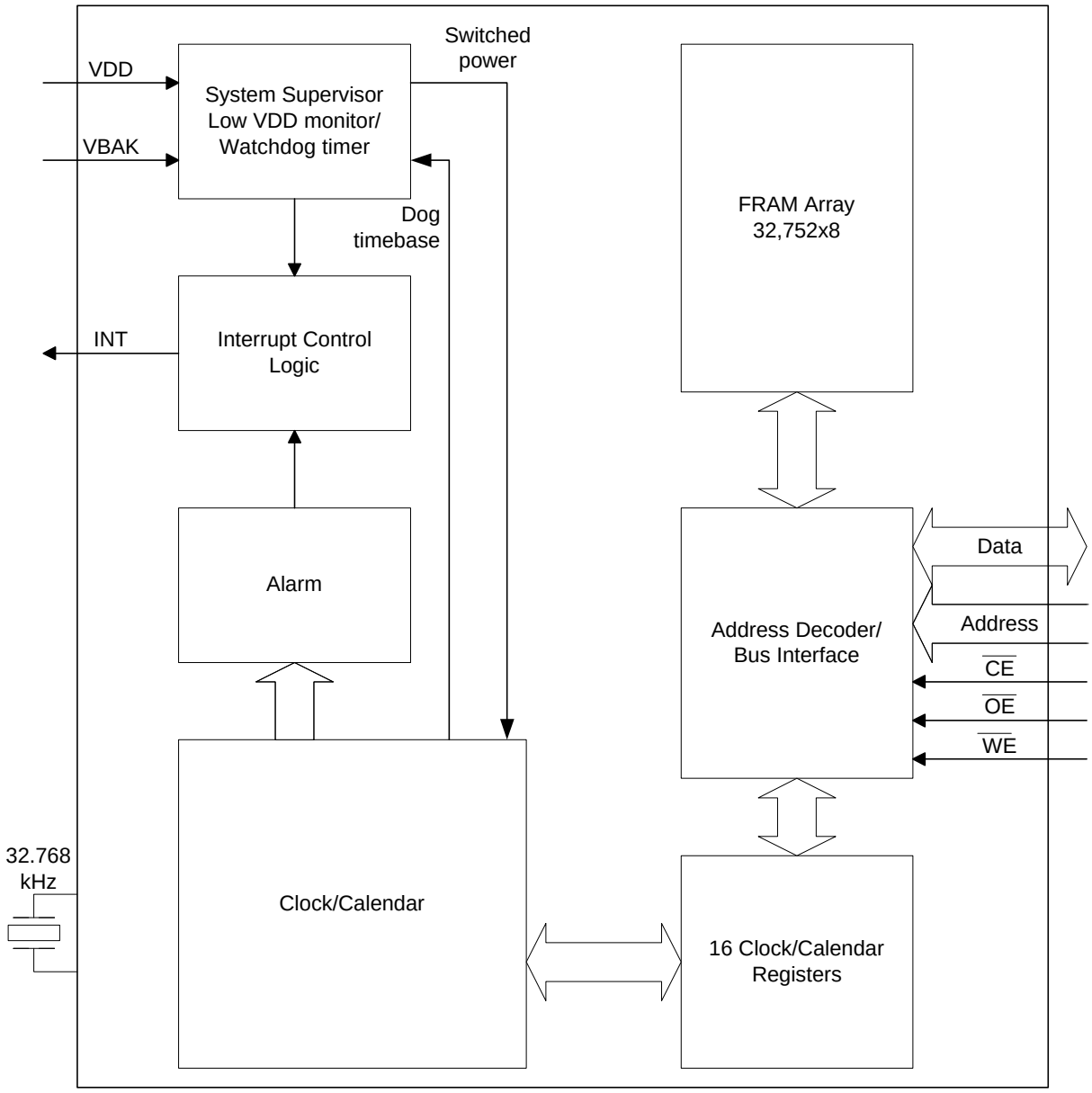
Pin Configuration



Ordering Information	
FM3808-70-T	70 ns access, 32-pin TSOP

Note: 600-mil 32-pin DIP package is available for prototypes only.

Figure 1. Block Diagram



Pin Description

Pin Name	Pin Number	I/O	Pin Description
A0-A14	3-12, 23, 25-28	I	Address. The 15 address lines select one of 32,752 bytes in the FRAM array or one of 16 bytes in the clock/calendar. The address value will be latched on the falling edge of /CE.
DQ0-7	13-15, 17-21	I/O	Data. 8-bit bi-directional data bus for accessing the FRAM array or clock.
/CE	22	I	Chip Enable. /CE selects the device when low. The falling edge of /CE causes the address to be latched internally. Address changes that occur after /CE goes low will be ignored until the next falling edge occurs.
/OE	24	I	Output Enable. When /OE is low the FM3808 drives the data bus when valid data is available. Taking /OE high causes the DQ pins to be tri-stated.
/WE	29	I	Write Enable. Taking /WE low causes the FM3808 to write the contents of the data bus to the address location latched by the falling edge of /CE.
X1, X2	1,2	I	Connect 32.768 kHz
INT	31	O	Interrupt output. Programmable to either active high or open-drain, active low. INT can be programmed to respond to the clock alarm, the watchdog timer, and the power monitor.
VBAK	30	I	Backup supply voltage for the clock. Must be between 2.5V and VDD-0.3V. Normally supplied by either capacitor or a battery. Current is drawn from VBAK when VDD is below the programmable V_{SW}.
VDD	32	I	Supply Voltage. 5V
VSS	14	I	Ground.

Functional Truth Table

/CE	/WE	/OE	Function
H	X	X	Standby/Precharge
↘	X	X	Latch Address
L	H	L	Read
L	L	X	Write

Overview

The FM3808 integrates three complementary but distinct functions under a common interface in a single package. First, is the 32Kx8 FRAM memory block (minus 16 bytes), second is the real-time clock/calendar, and third is the system supervisor. The functions are integrated to enhance their individual performance, so that each provides better capability than three similar stand-alone devices. All functions use the same bytewide address/data interface and are memory mapped. Special functions including the clock and supervisor are controlled by registers that reside in the top of the combined memory map. The register map is described below, followed by a detailed description of each functional block.

Register Map

The interface to clock and supervisor functions is via 16 address locations at the top of the address space. The registers contain timekeeping data, control bits, or information flags. A short description of each register follows. Detailed descriptions of each function follow the register summary.

Figure 2 Register Map

Address	Data								Function	Range
	D7	D6	D5	D4	D3	D2	D1	D0		
7FFFh	10 years				years				Years	00-99
7FFEh	0	0	0	10 mo	months				Month	1-12
7FFDh	0	0	10 date		date				Date	1-31
7FFCh	0	0	0	0	0	day			Day	1-7
7FFBh	0	0	10 hours		hours				Hours	0-23
7FFAh	0	10 minutes			minutes				Minutes	0-59
7FF9h	0	10 seconds			seconds				Seconds	0-59
7FF8h	/OSCEN	reserved	reserved	CALS	CAL3	CAL2	CAL1	CAL0	Control-NV	
7FF7h	WDS	WDW	WDT5	WDT4	WDT3	WDT2	WDT1	WDT0	Watchdog	
7FF6h	WIE	AIE	PFE	ABE	H/L	P/L	VINT	VSW	Interrupts	
7FF5h	/Match	0	Alarm 10 date		Alarm date				Alarm Date	1-31
7FF4h	/Match	0	Alarm 10 hours		hours				Alarm Hours	0-23
7FF3h	/Match	Alarm 10 minutes			Alarm minutes				Alarm Minutes	0-59
7FF2h	/Match	Alarm 10 seconds			Alarm seconds				Alarm Seconds	0-59
7FF1h									User-NV	
7FF0h	WDF	AF	PF	CF	TST	CAL	W	R	Flags/Control	

Note that the shaded bits are implemented in FRAM and therefore are nonvolatile even without backup power.

Address Description

7FFFh Timekeeping – Years

D7	D6	D5	D4	D3	D2	D1	D0
10 year.3	10 year.2	10 year.1	10 year.0	Year.3	Year.2	Year.1	Year.0

Contains the lower two BCD digits of the year. Lower nibble contains the value for years; upper nibble contains the value for 10s of years. Each nibble operates from 0 to 9. The maximum value for the register is 99.

7FFEh Timekeeping – Months

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	10 Month	Month.3	Month.2	Month.1	Month.0

Contains the BCD digits for the month. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble (one bit) contains the upper digit and operates from 0 to 1. The maximum value for the register is 12.

7FFDh Timekeeping – Date of the month

D7	D6	D5	D4	D3	D2	D1	D0
0	0	10 date.1	10 date.0	Date.3	Date.2	Date.1	Date.0

Contains the BCD digits for the date of the month. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble contains the upper digit and operates from 0 to 3. The maximum value for the register is 31.

7FFCh Timekeeping – Day of the week

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	Day.2	Day.1	Day.0

Lower nibble contains a value that correlates to day of the week. Day of the week is a ring counter that counts from 1 to 7 then returns to 1. The user must assign meaning to the day value, as the day is not integrated with the date.

7FFBh Timekeeping – Hours

D7	D6	D5	D4	D3	D2	D1	D0
0	0	10 hours.1	10 hours.0	Hours.3	Hours2	Hours.1	Hours.0

Contains the BCD value of hours in 24-hour format. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble (two bits) contains the upper digit and operates from 0 to 2. The maximum value for the register is 23.

7FFAh Timekeeping – Minutes

D7	D6	D5	D4	D3	D2	D1	D0
0	10 min.2	10 min.1	10 min.0	Min.3	Min.2	Min.1	Min.0

Contains the BCD value of minutes. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble contains the upper minutes digit and operates from 0 to 5. The maximum value for the register is 59.

7FF9h Timekeeping – Seconds

D7	D6	D5	D4	D3	D2	D1	D0
0	0	10 sec.1	10 sec.0	Seconds.3	Seconds.2	Seconds.1	Seconds.0

Contains the BCD value of seconds. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble contains the upper digit and operates from 0 to 5. The maximum value for the register is 59.

7FF8h Control-Nonvolatile

D7	D6	D5	D4	D3	D2	D1	D0
$\overline{\text{OSCEN}}$	Reserved	Reserved	CALS	CAL.3	CAL2	CAL.1	CAL.0

OSCEN /Oscillator Enable. When set to 1, the oscillator is halted. When set to 0, the oscillator runs. Can be used to save battery power during storage. This bit is implemented in FRAM.

Reserved Do not use.

CALS Calibration sign. Determines if the calibration adjustment is applied as an addition to or as a subtraction from the time-base. This bit is implemented in FRAM.

CAL3-0 These four bits control the calibration of the clock. These bits are implemented in FRAM.

7FF7h Watchdog Timer

D7	D6	D5	D4	D3	D2	D1	D0
WDS	WDW	WDT.5	WDT.4	WDT.3	WDT.2	WDT.1	WDT.0

WDS Watchdog Strobe. Setting this bit to 1 reloads and restarts the watchdog timer. Setting the bit to 0 has no affect. The bit is cleared automatically once the watchdog timer is reset. The WDS bit is write only. Reading it always will return a 0. Changes to the watchdog timeout value (WDT.5-0) will not take effect until WDS is set to 1.

WDW Watchdog Write. Setting this bit to 1 masks the watchdog timeout value (WDT.5-0) so it can not be written while the WDS bit is set to 1. Setting this bit to 0 allows bits 5-0 to be written while WDS is set to 1. This function is explained in more detail in the watchdog Timer section below.

WDT.5-0 Watchdog Timeout selection. The watchdog timer interval is selected by the 6-bit value in this register. It represents a multiplier of the 32 Hz count (31.25 ms). The minimum range or timeout value is 31.25 ms (a setting of 1) and the maximum timeout is 2 seconds (setting of 3Fh). Setting the watchdog timer register to 0 disables the timer. These bits can be written only if the WDS and WDW bits also are 1.

7FF6h Interrupts

D7	D6	D5	D4	D3	D2	D1	D0
WIE	AIE	PFE	ABE	$\overline{\text{H/L}}$	$\overline{\text{P/L}}$	VINT	VSW

WIE Watchdog Interrupt Enable. When set to 1, the watchdog timer drives the interrupt pin as well as an the WDF flag when a watchdog timeout occurs. When set to 0, the alarm match affects only the WDF flag.

AIE Alarm Interrupt Enable. When set to 1, the alarm match drives the interrupt pin as well as the AF flag. When set to 0, the alarm match only affects the AF flag.

PFE Power-fail Interrupt Enable. When set to 1, the power-fail monitor drives the pin as well as the PF flag. When set to 0, the power-fail monitor affects only the PF flag.

ABE Alarm Battery-backup Enable. When set to 1, the alarm interrupt (as controlled by AIE) will function even in battery backup mode. When set to 0, the alarm will occur only when VDD>VSW.

H/L High/Low. When set to a 1, the Interrupt pin is active high. When set to a 0, the interrupt pin is active low.

P/L Pulse/Level. When set to a 1, the interrupt pin is driven active (determined by H/L) by an interrupt source for approximately 200 ms. When set to a 0, the interrupt pin is driven to an active level (as set by H/L) until the flag register is read.

VINT Voltage Interrupt. Selects the voltage on VDD that generates a power-fail interrupt. When set to a 1, the interrupt occurs at 4.75V. When set to 0 the interrupt occurs at 4.6V. The interrupt pin is enabled by the AIE bit, otherwise only an internal flag is set.

VSW Voltage Switchover. Selects the voltage on VDD that causes the clock to switch to backup and that protects the memory from low voltage access. When set to 1, the switch occurs at 4.5V. When set to 0 the switch occurs when VDD < VBAK.

7FF5h Alarm – Date of the month

D7	D6	D5	D4	D3	D2	D1	D0
$\overline{M}$	0	10 date.1	10 date.0	Date.3	Date.2	Date.1	Date.0

Contains the alarm value for the date of the month and the mask bit to select or deselect the date value.

/M Match. Setting this bit to 0 causes the date value to be used in the alarm match. Setting this bit to 1 causes the match circuit to ignore the date value.

7FF4h Alarm – Hours

D7	D6	D5	D4	D3	D2	D1	D0
$\overline{M}$	0	10 hours.1	10 hours.0	Hours.3	Hours2	Hours.1	Hours.0

Contains the alarm value for the hours and the mask bit to select or deselect the hours value.

/M Match. Setting this bit to 0 causes the hours value to be used in the alarm match. Setting this bit to 1 causes the match circuit to ignore the hours value.

7FF3h Alarm – Minutes

D7	D6	D5	D4	D3	D2	D1	D0
$\overline{M}$	10 min.2	10 min.1	10 min.0	Min.3	Min.2	Min.1	Min.0

Contains the alarm value for the minutes and the mask bit to select or deselect the minutes value.

/M Match. Setting this bit to 0 causes the minutes value to be used in the alarm match. Setting this bit to 1 causes the match circuit to ignore the minutes value.

7FF2h Alarm – Seconds

D7	D6	D5	D4	D3	D2	D1	D0
$\overline{M}$	0	10 sec.1	10 sec.0	Seconds.3	Seconds.2	Seconds.1	Seconds.0

Contains the alarm value for the minutes and the mask bit to select or deselect the minutes value.

/M Match. Setting this bit to 0 causes the seconds value to be used in the alarm match. Setting this bit to1 causes the match circuit to ignore the seconds value.

7FF1h User-Nonvolatile

D7	D6	D5	D4	D3	D2	D1	D0

This register is an uncommitted nonvolatile register. It can be used to store century information or other user data. The user register is not manipulated by the real-time clock other than to provide nonvolatile storage of the contents.

7FF0h Flags/Control

D7	D6	D5	D4	D3	D2	D1	D0
WDF	AF	PF	CF	-	CAL	W	R

WDF Watchdog Timer Flag. This bit is set to 1 when the watchdog timer is allowed to reach 0 without being reset by the user. It is cleared to 0 when the Flags register is read. It is read-only for the user.

AF Alarm Flag. This bit is set to 1 when the time and date match the values stored in the alarm registers with the match bit(s) = 0. It is cleared when the Flags register is read. It is read-only for the user.

PF Power-fail Flag. This bit is set to 1 when power falls below the power-fail interrupt threshold VINT. It is cleared to 0 when the Flags register is read. It is read-only for the user.

CF Century Overflow Flag. This bit is set to a 1 when the values in the years register overflows from 99 to 00. This indicates a new century, such as going from 1999 to 2000 or 2099 to 2100. The user should record the new century information as needed. This bit is cleared to 0 when the Flags register is read. It is read-only for the user.

- Reserved

CAL Calibration Mode. When set to 1, the clock enters calibration mode. When CAL is set to 0, the clock operates normally.

W Write Time. Setting the W bit to 1 freezes updates of the timekeeping registers. The user can then write them with updated values. Setting the W bit to 0 causes the contents of the time registers to be transferred to the timekeeping counters. This bit affects registers xF, xE, xD, xC, xB, xA, and x9.

R Read Time. Setting the R bit to 1 freezes updates of the timekeeping registers. The user can then read them without concerns over changing values causing system errors. The updates will be disabled until the R bit is cleared to 0. This bit affects registers xF, xE, xD, xC, xB, xA, and x9.

Real-time Clock Operation

The real-time clock (RTC) consists of an oscillator divider and a register system for accessing the information. It divides down the 32.768 kHz time-base and provides a minimum resolution of seconds (1Hz) to the user. Static registers provide the user with read/write access to the time values. The synchronization of these registers with the timekeeper core is performed using R and W bits in register 7FF0h.

Setting the R bit to 1 causes update of the time registers to be frozen. The user can then read them. If a timekeeper update is in progress when the R is set, the update will be completed prior to loading the registers. Otherwise setting R causes the timekeeper to stop updating while R is a 1.

Setting the W bit causes the timekeeper to freeze updates. Clearing it to 0 causes the values in the time registers to be written into the timekeeper core. Writing an invalid value, such as FFh to the hours register, will cause the write to be ignored.

Updates to the timekeeping core occur continuously except when frozen. A diagram of the timekeeping core is shown below.

Backup Power

The real-time clock/calendar is intended for permanently powered operation. When primary system power fails, the voltage on VDD will drop. When it crosses a programmable threshold level, the clock will switch to using the backup power supply on the VBAK pin. The supervisor function, described below, controls the switchover process as part of a more complete power management circuit.

The clock operates using extremely low current to maximize battery life. However, an advantage of combining a clock function with FRAM is that the data is nonvolatile without regard to the backup power source. Thus is more practical in this scenario to use a capacitor as a backup energy source than in a RAM/clock combo. In the FM3808, the user has the choice of using a battery or a capacitor as the backup source. Parameters that would be used in the decision are the expected duration of power outages, the difficulty of resetting the time if lost, and the cost tradeoff of using a small battery versus a capacitor.

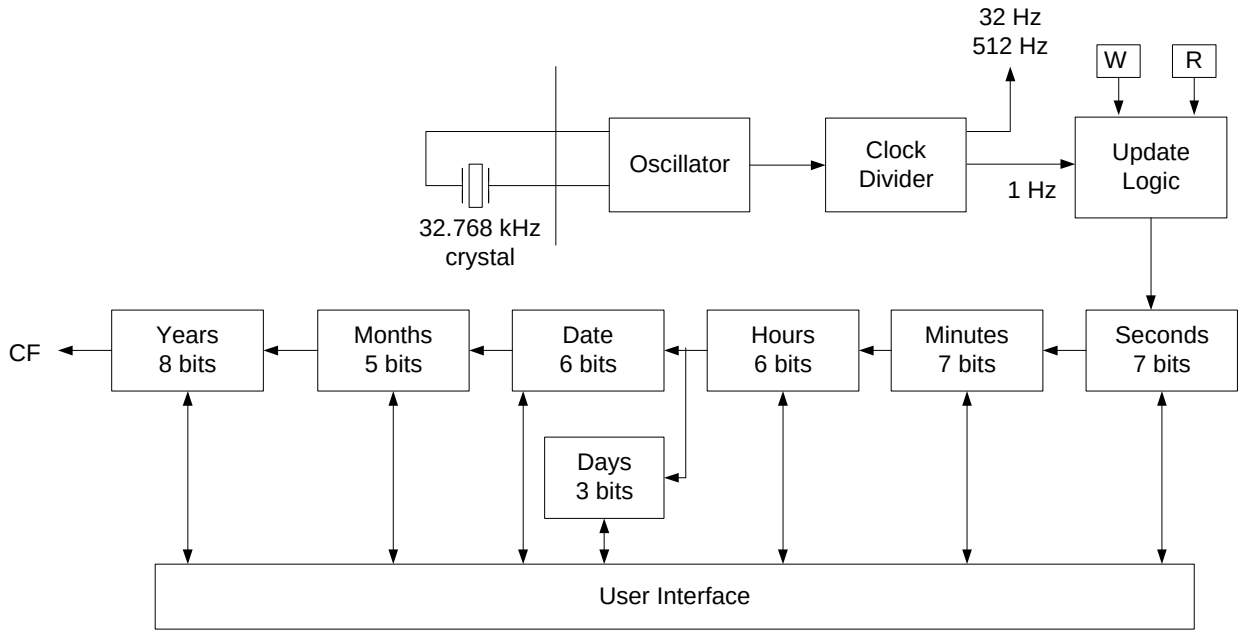
The following functions are powered from the backup power source when VCC < VSW (backup mode).

- Clock/calendar core
- Alarm interrupt/comparator
- INT pin driver (determined by AIE bit)
- Flags connected to related functions

The following functions are not powered and are disabled when VCC < VSW.

- User interface
- Watchdog timer
- Power monitor & band-gap (VDD < ≈ 2.0V)
- Flags connected to related functions
- All FRAM access & updates
- Calibration operation

Figure 3. Real-time Clock Core Block Diagram



Calibration

When the CAL bit in register 7FF0.2 is set to 1, the clock enters calibration mode. Interrupts are disabled in CAL mode. Calibration operates by applying a digital correction to the counter based on the frequency error. The INT pin in is driven with a 512 Hz nominal square wave. Any measured deviation from 512 Hz is converted into an error in ppm. This error corresponds to a correction value that is then written by the user into the calibration register 7FF8h. Positive adjustments have the CALS bit set to 1, where as negative adjustments have CALS = 0. The calibration setting is nonvolatile and is stored in 7FF8.4-0. This value can only be written when the CAL bit is set to a 1. To exit calibration mode, the user should clear the CAL bit to a 0.

Once the calibration mode is entered, the user can measure the frequency error on the INT pin. This error expressed in ppm translates directly into timekeeping error. An offsetting calibration adjustment can correct his error. However the correction is applied by adding or swallowing pulses on a periodic basis. Therefore, it will not appear on the 512 Hz output. The calibration correction must be applied using a lookup table.

CAL PROCEDURE

Supervisor Operation

The Supervisor function includes a clock/calendar alarm, a watchdog timer and power monitor. A programmable interrupt pin provides maximum functionality to permit the host processor to benefit from the supervisor functions. It is designed to allow either reset or interrupt capability to the external processor host.

Alarm

The alarm function compares user-programmed values to the corresponding time of day values. When a match occurs, the alarm event occurs. The alarm offers an internal flag bit and an optional external interrupt.

There are four alarm match values They are date of the month, hours, minutes, and seconds. The match select bits determine if a value is used in the alarm match selection. Setting the match select bit to '0' indicates that the corresponding value should be used in the match process.

Depending on the match select bits, the alarm can occur as specifically as one particular second on one day of the month, or as frequently as once per second continuously. Each match select bit is contained in the MSB of the match value register. The match select bits work in concert as shown in the table below. Selecting none of the match bits (all '1's) indicates that no match is required. The alarm occurs every second. Setting the match select bit for seconds to '0' causes the logic to match the seconds alarm value to the time of day. Since a match will occur for only one value per minute, the alarm occurs once per minute. Likewise setting the seconds and minutes match select bits causes an exact match of these values. Thus, an alarm will occur once per hour. Setting seconds, minutes, and hours causes a match once per day. Lastly, selecting all match-values causes an exact time and date match. Selecting other bit combinations will not produce meaningful results, however the alarm circuit should follow the functions described.

The alarm event can be detected by the user in two ways. First, the AF flag bit in the register 7FF0.6 will indicate that a match has occurred. The AF bit will be set to 1 when a valid match occurs. Reading the flag register clears the alarm flag bit (and all others). Second, a hardware interrupt pin will be provided. The interrupt function is described below.

Watchdog Timer

The Watchdog timer is a free running counter that uses the 32 Hz clock (31.25 ms) derived from the crystal oscillator. The crystal must be running for the watchdog to function. It begins counting down from the value loaded from the Watchdog timer register (7FF7h). Counting starts by setting the Watchdog Strobe (WDS – 7FF7.7) WDS bit to 1. The counter runs at 32 Hz and its value is compared to 0. If the counter reaches this value, it causes an internal flag and an optional interrupt output (see interrupts below). The user can prevent the timeout interrupt by setting WDS bit to 1 prior to the counter reaching 0. This causes the counter to be reloaded with the watchdog timeout value and to be restarted. As long as the user sets the WDS bit prior to the counter reaching the terminal value, the interrupt never occurs.

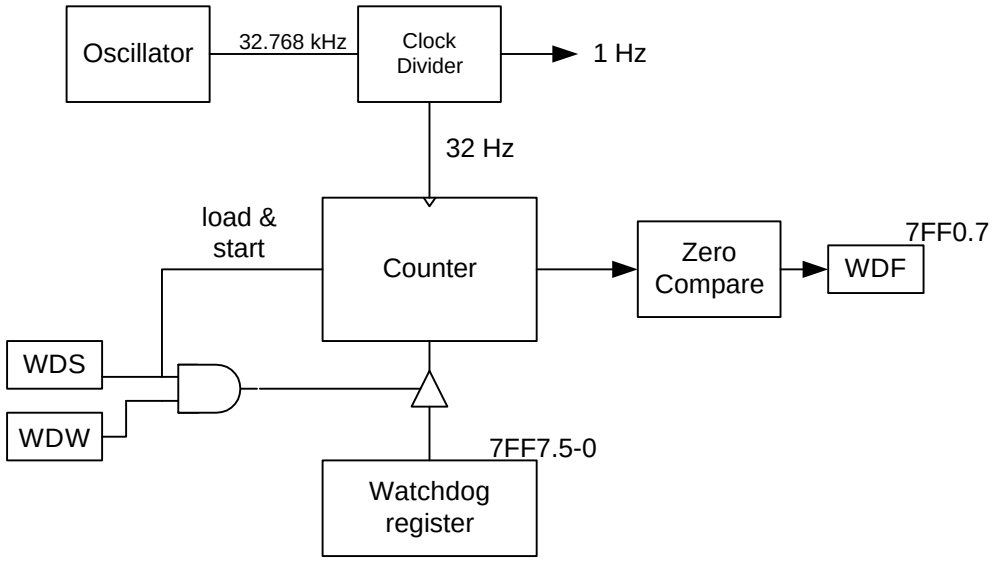
New timeout values can be written and are loaded by setting the WDS bit to 1 and the watchdog write bit (WDW – 7FF7.6) to 0. If WDW is set to 1, then the remaining bits in the watchdog time register will be ignored when restarting the timer. If WDW is set to 0, then the new value will be loaded. The WDW function allows a user to set the WDS bit without concern that the watchdog timer value will be modified. A logical diagram of the watchdog timer is shown below. Note that setting the watchdog timeout value to 0 would be otherwise meaningless and therefore disables the watchdog function.

The output of the watchdog timer is a flag bit (WDF – 7FF0.7) that is set if the watchdog is allowed to timeout. The flag is set upon a watchdog timeout and cleared when the flag register is read by the user. The user can also enable an optional interrupt source to drive the interrupt pin if the watchdog timeout occurs. The interrupt function is described below.

Figure X Alarm Match Bits

Seconds	Minutes	Hours	Date	Alarm condition
1	1	1	1	No match required = alarm 1/second
0	1	1	1	Alarm when seconds match, = alarm 1/minute
0	0	1	1	Alarm when seconds, minutes match, = alarm 1/hour
0	0	0	1	Alarm when seconds, minutes, hours match, = alarm 1/day
0	0	0	0	Alarm when seconds, minutes, hours, date match, = alarm 1/month

Figure X. Watchdog Timer Block Diagram



Power Monitor

The FM3808 provides a power management scheme with either power-fail interrupt or processor-reset capability. It also controls the internal switch to backup power for the timekeeper and protects the memory from low-VDD access. The power monitor is based on a band-gap reference circuit that compares the incoming VDD to programmable thresholds. VDD is sampled internally to reduce the likelihood that noise will cause an incorrect power warning.

The power monitor compares VDD to two thresholds. The first is an interrupt threshold (VINT), which can be selected between two levels as shown below. When VDD drops below the programmed VINT level, the event will set the power fail flag (PF – 7FF0.5). It also can drive the interrupt pin as described in the interrupt section below. The interrupt level selection is controlled via the voltage interrupt bit (VINT – 7FF6.1) as follows.

Power fail	VINT
4.6V	0
4.75V	1

If the power monitor is used to reset the external processor, then the lower threshold is more likely to be used. If the power monitor is providing an early warning interrupt, then either may be suitable depending on expected slew rates and the amount of data to be saved on power failure.

The second threshold is the switch of the internal supply from VDD to VBAK for the timekeeper. There also are two programmable levels for this event. When VDD drops below the programmed switchover (VSW), the clock will begin to draw power from VBAK rather than VDD. At this time, access to the memory array and clock registers will be blocked until VDD rises above VSW. The switchover selection is controlled by the voltage switch bit (VSW – 7FF6.0) as follows.

Switchover/Low VDD protect	VSW
VDD<VBAK	0
4.5V	1

The first setting, VDD<VBAK is primarily intended for battery-backed operation where the battery voltage is nominally 3V, but certainly is well below VDD under operating conditions. In this case the clock is powered by the VDD until it reaches the

battery voltage. The switch to battery backup occurs at the lowest possible point thus preserving battery life. The second case, 4.5V, is suitable for capacitor backup where the nominal backup source could be above VDD during normal operation. In these cases, a comparison with the VBAK level would lead to incorrect operation. For example, VDD nominal could be 5.0V and the backup capacitor could be charged to 4.7V. When VDD begins to drop, and reaches 4.6V, it is still within operating tolerance for the memory but is below the backup source. Switching at 4.5V will provide the full power supply tolerance for memory operation.

Note that in either case, memory access is a blocked when VDD is below the selected VSW. Since the 4.5V selection provides the optimal write protection, it may be desirable to use this choice even with battery-backup.

To conserve the life of the backup source, the power monitor circuit is only operated from VDD. When VDD has dropped too low for the monitor to work, it ceases operation. However, the power monitor will reenergize as VDD rises on power-up. On power-up, after the band-gap energizes, the reverse sequence will occur. As soon as the band gap is functional, it will re-assert both selections for switch over and power fail. As the VDD rises further, the switchover will be removed, allowing memory access and operating the clock from VDD. As the VDD rises above VINT, the power-fail condition will be removed. Note that the PF flag will not \be cleared until the flags register is read.

The following figure illustrates the various events tracked by the power monitor.

Figure X. Power Monitor Events

In the diagram, BG is the voltage at which the band-gap will function. This voltage is not precisely specified but is well below the range of operation for the memory or other circuits. On power down, the band-gap will monitor VDD as long as possible. This allows a brownout to occur where VDD returns to a proper level prior to the band-gap failing. Since the band-gap runs only from VDD, it does not reduce the life of the backup source.

Interrupts

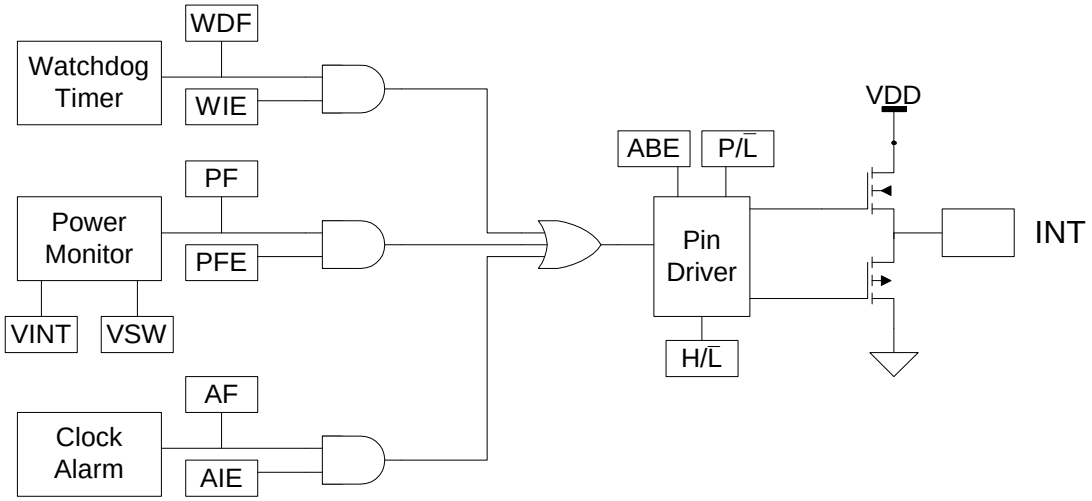
The supervisor was designed to serve diverse applications. Its sophistication is managed by the interrupt block, which makes this functionality available to the host system. The interrupt block is capable of providing interrupt or reset conditions, an even to power up a system at a preprogrammed time. The function is described as an interrupt, even though the output may be used as a reset source.
The supervisor provides three potential interrupt sources. They include the watchdog timer, the power monitor, and the clock/calendar alarm. Each can be individually enabled and assigned to drive the single INT pin. In addition, each has a flag bit associated with it so that the host processor can determine the cause of the interrupt.

Some of the sources have additional control bits that determine functional behavior. In addition, the pin driver has three bits that specify its behavior when an interrupt occurs. A functional diagram of the interrupt logic is shown below.

As shown, the three interrupts each have a source and an enable. Both the source and the enable must be active (1) in order to generate an interrupt output. Only one source is necessary to drive the pin. The user can identify the source by reading the flag register, which contains the flags associated with each source. All flags are cleared to 0 when the register is read. The power monitor has two programmable settings that are explained above in the power monitor section.

Once an interrupt source is active, the pin driver determines the behavior of the output pad. It has three programmable settings as shown above. All of the pin driver control bits are located in the Interrupts register 7FF6h bits 4, 3, and 2.

Figure X. Interrupt Block Diagram



According to the programming selections, the pin can be driven in the backup mode for an alarm interrupt or not. Also, the pin can be active low with an active low (open-drain) or active high (push-pull) driver. It can only be active low if programmed for backup operation. Lastly, the pin can provide a one-shot function so that the active condition is a pulse, or a level operation. In one-shot mode, the pulse width is fixed at approximately 200 ms. This mode is intended to reset a host microcontroller. In level mode, the pin goes to its active polarity until the Flags register is read by the user. This mode is intended for use as an interrupt to a host microcontroller. The control bits are summarized as follows.

Watchdog Interrupt Enable - WIE. When set to 1, the watchdog timer drives the interrupt pin as well as an internal flag when a watchdog timeout occurs. When set to 0, the watchdog timer affects only the internal flag.

Alarm Interrupt Enable – AE. When set to 1, the alarm match drives the interrupt pin as well as an internal flag. When set to 0, the alarm match only affects the internal flag.

Power-fail Interrupt Enable - PFE. When set to 1, the power-fail monitor drives the pin as well as an internal flag. When set to 0, the power-fail monitor affects only the internal flag.

Alarm Battery-backup Enable - AIE. When set to 1, the clock alarm interrupt (as controlled by AIE) will function even in battery backup mode. When set to 0, the alarm will occur only when VDD>VSW. AIE should only be set when the interrupt pin is programmed for active low operation. Also, it only functions with the clock alarm, not the watchdog or power monitor. The application for AIE is intended for power control, where a system powers up at a predetermined time.

High/Low – H/L. When set to a 1, the Interrupt pin is active high. This only works when VDD>VSW. When set to a 0, the interrupt pin is active low. It can function as a pull down even in battery backup mode.

Pulse/Level – P/L. When set to a 1, the interrupt pin is driven (by an interrupt source) for approximately 200 ms. When set to a 0, the interrupt pin is driven to a level (as set by H/L) until the flag register is read.

When an enabled interrupt source activates the INT pin, an external host can read the flags register to determine the cause. One or more flags may be set when the register is read, however all will be cleared when the register is read. If the INT pin is programmed for level mode, then the condition will clear and he INT pin will return to its inactive state. If the pin is programmed for pulsed operation, then reading the flag will clear the flag but not the pin. The pulse will complete its specified duration regardless of the flag. Of course, if the INT pin is used to reset the host, then the flag register could not be read during an active pulse. Care should be exercised in reading the flags as a new source may occur after the pin goes active but before the register is read.

FRAM Memory Operation

The memory array is logically organized as 32,768 x 8 with the upper 16 bytes disabled and allocated to the RTC. It is accessed using an industry standard SRAM-type parallel interface. It is virtually identical to the 32Kx8 FM1808 in function. The memory array in the FM3808 is inherently nonvolatile via its unique ferroelectric process. All data written to the part is immediately nonvolatile with no delay. Functional operation of the FRAM memory is similar to SRAM type devices. The major operating difference between the FRAM array and an SRAM (beside nonvolatile storage) is that the FM3808 latches the address on the falling edge of /CE.

Users access 32,752 memory locations each with 8 data bits through a parallel interface. The complete address of 15-bits specifies each of 32,768 bytes uniquely, with the upper 16 locations allocated to timekeeping functions. Internally, the memory array is organized into 32 blocks of 1Kb each. The 5 most-significant address lines decode one of 32 blocks. This block segmentation has no effect on operation, however the user may wish to group data into blocks by its endurance requirements as explained in a later section.

The access and cycle time are the same for read and write memory operations. Writes occur immediately at the end of the access with no delay. A pre-charge operation, where /CE goes inactive, is a part of every memory cycle. Thus unlike SRAM, the access and cycle times are not equal.

The FM3808 is designed to operate in a manner very similar to other bytewide memory products. For users familiar with BBSRAM, the performance is comparable but the bytewide interface operates in a slightly different manner as described below. For users familiar with EEPROM, the obvious differences result from the higher write-performance of FRAM technology including NoDelay writes and much higher write-endurance.

Read Operation

A read operation begins on the falling edge of /CE. At this time, the address bits are latched and a memory cycle is initiated. Once started, a full memory cycle must be completed internally regardless of the state of /CE. Data becomes available on the bus after the access time has been satisfied.

After the address has been latched, the address value may be changed upon satisfying the hold time parameter. Unlike an SRAM, changing address values will have no effect on the memory operation after the address is latched.

The FM3808 will drive the data bus when /OE is asserted to a low state. If /OE is asserted after the memory access time has been satisfied, the data bus will be driven with valid data. If /OE is asserted prior to completion of the memory access, the data bus will not be driven until valid data is available. This feature minimizes supply current in the system by eliminating transients due to invalid data. When /OE is inactive the data bus will remain tri-stated.

Write Operation

Writes occur in the FM3808 in the same time interval as reads. The FM3808 supports both /CE and /WE controlled write cycles. In all cases, the address is latched on the falling edge of /CE.

In a /CE controlled write, the /WE signal is asserted prior to beginning the memory cycle. That is, /WE is low when /CE falls. In this case, the part begins the memory cycle as a write. The FM3808 will not drive the data bus regardless of the state of /OE.

In a /WE controlled write, the memory cycle begins on the falling edge of /CE. The /WE signal falls after the falling edge of /CE. Therefore, the memory cycle begins as a read. The data bus will be driven according to the state of /OE until /WE falls. The timing of both /CE and /WE controlled write cycles is shown in the electrical specifications.

Write access to the array begins asynchronously after the memory cycle is initiated. The write access terminates on the rising edge of /WE or /CE, whichever is first. Data set-up time, as shown in the electrical specifications, indicates the interval during which data cannot change prior to the end of the write access.

Unlike other truly nonvolatile memory technologies, there is no write delay with FRAM. Since the read and write access times of the underlying memory are the same, the user experiences no delay through the bus. The entire memory operation occurs in a single bus cycle. Therefore, any operation including read or write can occur immediately following a write. Data polling, a technique used with EEPROMs to determine if a write is complete, is unnecessary.

Pre-charge Operation

The pre-charge operation is an internal condition where the state of the memory is prepared for a new access. All memory cycles consist of a memory access and a pre-charge. The pre-charge is user initiated by taking the /CE signal high or inactive. It must remain high for at least the minimum pre-charge timing specification. The user dictates the beginning

of this operation since a pre-charge will not begin until /CE rises. However, the device has a maximum /CE low time specification that must be satisfied.

Endurance and Memory Architecture

Data retention is specified in the electrical specifications below. This section elaborates on the relationship between data retention and endurance.

FRAM offers substantially higher write endurance than other nonvolatile memories. Above a certain level, however, the effect of increasing memory accesses on FRAM produces an increase in the soft error rate. There is a higher likelihood of data loss but the memory continues to function properly. This effect becomes significant only after 100 million (1E8) read/write cycles, far more than allowed by other nonvolatile memory technologies.

Endurance is a soft specification. Therefore, the user may operate the device with different levels of cycling for different portions of the memory. For example, critical data needing the highest reliability level could be stored in memory locations that receive comparatively few cycles. Data with frequent changes or shorter-term use could be located in an area receiving many more cycles. A scratchpad area, needing little if any retention can be cycled virtually without limit.

Internally, a FRAM operates with a read and restore mechanism similar to a DRAM. Therefore each cycle, be it read or write, involves a change of state. The memory architecture is based on an array of rows and columns. Each access causes an endurance cycle for an entire row. Therefore, data locations targeted for substantially differing numbers of cycles should not be located within the same row. To balance the endurance cycles and allow the user the maximum flexibility, the FM3808 employs a unique memory organization as described below.

The memory array is divided into 32 blocks, each 1Kx8. The 5-upper address lines decode the block selection as shown in Figure X. Data targeted for significantly different numbers of cycles should be located in separate blocks since memory rows do not extend across block boundaries.

Each block of 1Kx8 consists of 256 rows and 4 columns. The address lines A0-A7 decode row selection and A8-A9 lines decode column selection. This scheme facilitates a relatively uniform distribution of cycles across the rows of a block. By allowing the address LSBs to decode row selection, the user avoids applying multiple cycles to the same row when accessing sequential data. For example, 256 bytes can be accessed sequentially without accessing the same row twice. In this example, one cycle would be applied to each row. An entire block of 1Kx8 can be read or written with only four cycles applied to each row. Figure X illustrates the organization within a memory block.

Figure x. Address Blocks

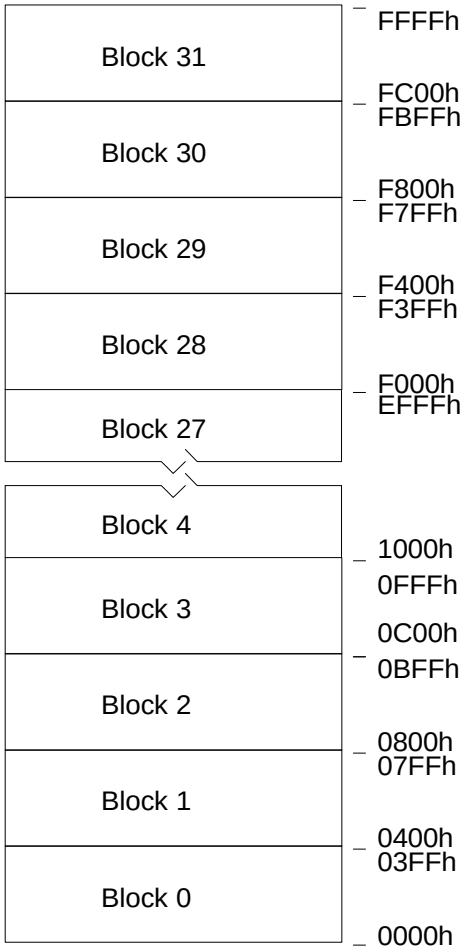
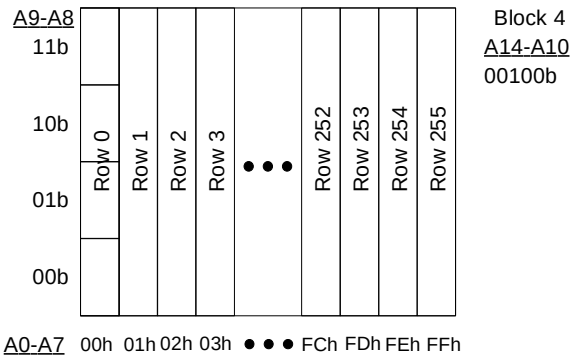


Figure x. Row and Column Organization

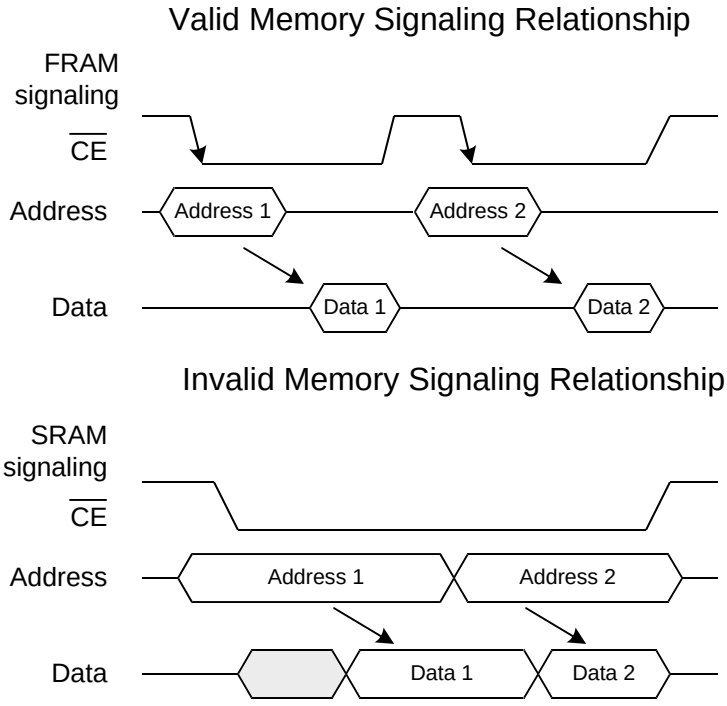


FRAM Design Considerations

When designing with FRAM for the first time, users of SRAM will recognize a few minor differences. First, bytewide FRAM memories latch each address on the falling edge of chip enable. This allows the address bus to change after starting the memory access. Since every access latches the memory address on the falling edge of /CE, users should not ground it as they might with SRAM.

Users that are modifying existing designs to use FRAM should examine the hardware address decoders. Decoders should be modified to qualify addresses with an address valid signal if they do not already. In many cases, this is the only change required. Systems that drive chip enable active, then inactive for each valid address may need no modifications. An example of the target signal relationships are shown in Figure x. Also shown is a common SRAM signal relationship that will not work for the FM3808.

Figure x. Memory Address Relationships



Real-time Clock Design Considerations

The principal design issues in using he real time clock are selection and specification of backup energy source and the selection of the timekeeping crystal. Selection of the backup source is primarily a choice between a capacitor and a battery, and the specifications needed for each. Selection of the crystal is based on mechanical (surface mount versus through-hole) considerations and the characteristic capacitance. Each topic is discussed briefly.

Backup Source

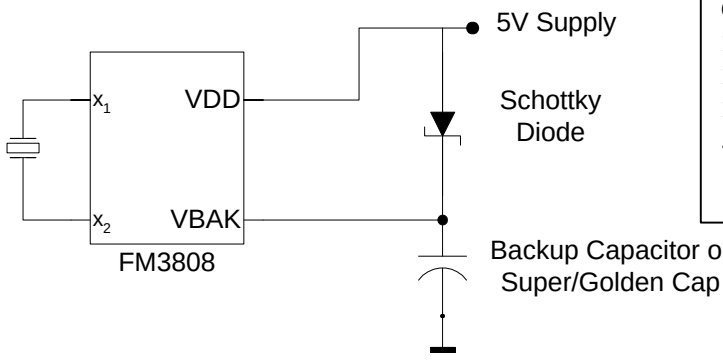
The FM3808 is designed to accommodate either a battery or a capacitor as a backup source. Unlike SRAM based timekeepers that depend on the battery to make data nonvolatile, the FM3808 is unrestricted. Data stored in FRAM is not dependent on the backup battery in any way. This means that capacitor backup, which should be less expensive, is a meaningful option. Selection of a capacitor as being suitable is determined by the expected duration of power outage where timekeeping must be maintained, and the practical difficulty in resetting the time should it be lost. If the time is relatively easy to reset, or a typical power loss is only a brownout, the capacitor may be a good, cost effective choice. In addition, portable systems that use a battery for primary power are good candidates for capacitor backup. If the time is very difficult to reset, or the power outage may be longer than a capacitor can supply, then a small battery is best. Each system and application can be evaluated for the difficulty in setting the time. However, the expected backup times for several capacitor choices are illustrated below. These figures cannot be used as guarantees due to the unknown leakage characteristics in external components, but they provide guidelines for realistic expectations about capacitor use. In the scenario using capacitor backup, the charging circuit must also be considered. A typical representation is shown below.

The backup times are based on a starting backup voltage (fully charged) of 4.7V and minimum backup voltage of 2.5V. A 0.3V forward drop from 5.0V VDD might be expected from a schottky-diode. Note the graph, which shows approximate backup current as a function of backup voltage. Thus, the higher voltages at the beginning of discharge provide less incremental backup time than the lower voltages near the end of discharge. However, the total backup time depends on the capacitor size and the maximum, fully charged voltage.

One important note about capacitor backup is that the times are incremental. Each time power is restored the capacitor is fully recharged. Rather than examining the cumulative time without power in the system over a 10-year period, the capacitor design is only concerned with the maximum time without power for one outage.

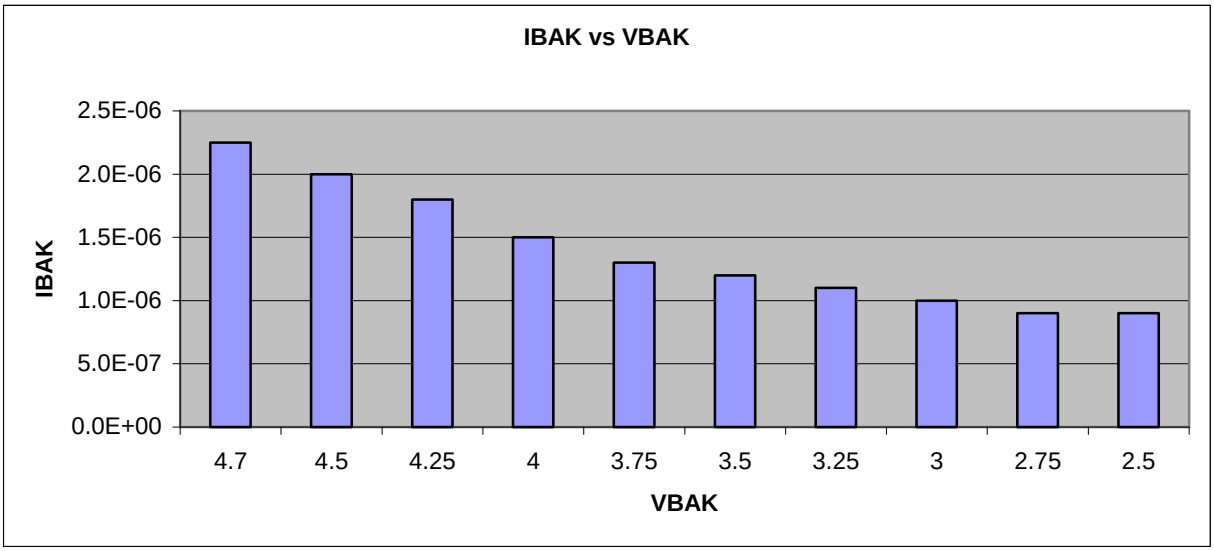
If the times available for a capacitor are not sufficient, then a battery is the best selection. Most users opt for a 3V lithium coin. Note that with non-rechargeable batteries, the reservoir is not replenished so the critical parameter is the total time without power during the useful life of a system. For 1 year without power (total) during a 10-year system life, the battery capacity must be at least 9.25 mAhr. For 5 years without power during a 10-year period, it becomes 46 mAhr.

Figure X Capacitor Backup Circuit



Capacitor Size	Backup Time
100 µF	3 minutes
1000 µF	30 minutes
10000 µF	5.1 hours
.47 F (super cap)	240 hours

Figure X Backup Current over Voltage

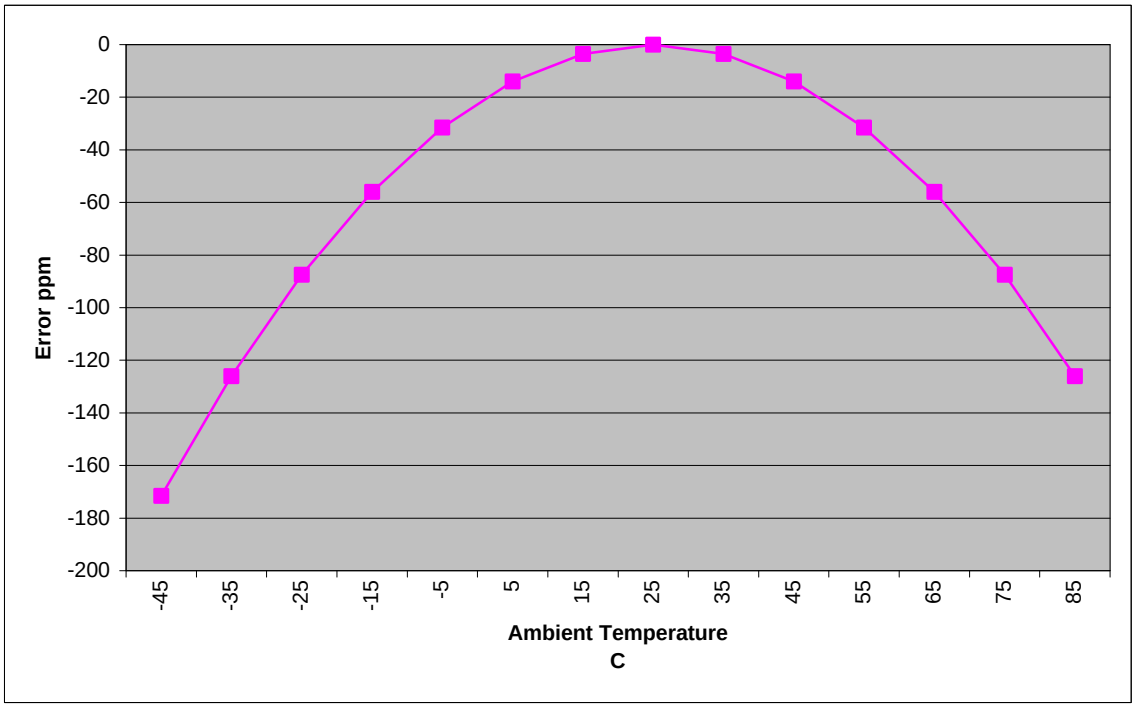


Crystal Selection

The second passive component needed for the RTC function is the timekeeping crystal. A 32.768 kHz time-base is required, and the FM3808 is designed to accept a low cost crystal. The major parameters associated with the crystal are timekeeping accuracy and backup current. The FM3808 is designed to accept a crystal with a characteristic capacitance of 6 pF. Deviations from this specification will lead to different accuracy and IBAK from the specified values. Though accuracy is unlikely to improve, the IBAK may go up or down from the specified value as a function of the capacitive load.

The timekeeping accuracy is also a strong function of the operating temperature due to errors in crystal frequency. Temperature behavior of timekeeping crystals is well known and it follows a curve like the one shown below. The specific crystal manufacturer should be consulted for the behavior of their specific device. Note the error in frequency ppm. One ppm is roughly 2.6 seconds per month in timekeeping error.

Figure X Typical Crystal Error versus Temperature



Electrical Specifications

Absolute Maximum Ratings

Description	*Ratings*
Ambient storage or operating temperature	-40°C to + 85°C
Voltage on any pin with respect to ground	-1.0V to +7.0V
Lead temperature (Soldering, 10 seconds)	300° C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and the functional operation of the device at these or any other conditions above those listed in the operational section of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

DC Operating Conditions TA = -40° C to + 85° C, VDD = 4.5V to 5.5V unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Units	Notes
VDD	Power Supply	4.5	5.0	5.5	V	1
IDD	VDD Supply Current - Active		5	15	mA	2
VINT	INT output supply level	4.65 4.5		4.75 4.6	V V	1,3
VBAK	Clock backup voltage	2.5	3.0	VDD	V	1
IBAK	Clock backup current		500	1000	nA	4
VSW	Supply switch to battery; memory access blocked	 4.5	 4.55	VBAK 4.6	V V	1,5
VBG	Power monitor active	2.0			V	1,6
ISB	Standby Current - TTL			500	µA	7
ISB	Standby Current - CMOS		50	120	µA	8
ILI	Input Leakage Current			10	µA	9
ILO	Output Leakage Current			10	µA	9
VIL	Input Low Voltage	-1.0		0.8	V	1
VIH	Input High Voltage	2.0		VDD + 1.0	V	1
VOL	Output Low Voltage			0.4	V	1,10
VOH	Output High Voltage	2.4V			V	1,11

Notes

1. Referenced to VSS.
2. VDD = 5.5V, /CE cycling at minimum cycle time. All inputs at CMOS levels, all outputs unloaded.
3. Voltage for VINT depends on selection of VINT control bit.
4. VBAK = 3.0V, VDD < V_{SW}; oscillator running.
5. Memory access is blocked when VDD < VSW. The parameter VSW can be programmed by the user between two selections using the VSW control bit. For one selection, the VSW occurs when VDD drops below VBAK. For the second, it occurs at no less than 4.5V. VSW is also the point at which the timekeeper draws current from the VBAK pin, rather than from VDD.
6. Signals controlled by the power monitor (such as the INT output) are active.
7. VDD = 5.5V, /CE at VIH, All inputs at TTL levels, all outputs unloaded.
8. VDD = 5.5V, /CE at VIH, All inputs at CMOS levels, all outputs unloaded.
9. VIN, VOUT between VDD and VSS.
10. IOL = 4.2 mA.
11. IOH = -2.0 mA.

Read Cycle AC Parameters TA = -40° C to + 85° C, VDD = 4.5V to 5.5V unless otherwise specified

Symbol	Parameter	Min	Max	Units	Notes
tCE	Chip Enable Access Time (to data valid)		70	ns	
tCA	Chip Enable Active Time	70	10,000	ns	
tRC	Read Cycle Time	100		ns	
tPC	Precharge Time	50		ns	
tAS	Address Setup Time	0		ns	
tAH	Address Hold Time	10		ns	
tOE	Output Enable Access Time		10	ns	
tHZ	Chip Enable to Output High-Z		15	ns	1
tOHZ	Output Enable to Output High-Z		15	ns	1

Write Cycle AC Parameters TA = -40° C to + 85° C, VDD = 4.5V to 5.5V unless otherwise specified

Symbol	Parameter	Min	Max	Units	Notes
tCA	Chip Enable Active Time	70	10,000	ns	
tCW	Chip Enable to Write High	70		ns	
tWC	Write Cycle Time	100		ns	
tPC	Precharge Time	50		ns	
tAS	Address Setup Time	0		ns	
tAH	Address Hold Time	10		ns	
tWP	Write Enable Pulse Width	30		ns	
tDS	Data Setup	30		ns	
tDH	Data Hold	0		ns	
tWZ	Write Enable Low to Output High Z		15	ns	1
tWX	Write Enable High to Output Driven	10		ns	1
tHZ	Chip Enable to Output High-Z		15	ns	1
tWS	Write Setup	0		ns	2
tWH	Write Hold	0		ns	2

Notes

1 This parameter is periodically sampled and not 100% tested.

2 The relationship between /CE and /WE determines if a /CE- or /WE-controlled write occurs. There is no timing specification associated with this relationship.

Power Cycle Timing TA = -40° C to + 85° C

Symbol	Parameter	Min	Max	Units	Notes
tINT	INT signal active after VINT		100	ns	1,2
tPD	Last Access Complete to VSW	0		ns	1,3
tRI	VSW to inputs recognized on power-up	1		µs	1,4
TR	Rise time of VDD from VBG VSW	1		µs	1,5
TF	Fall time of VDD from VSW to VBG	1		µs	1,5

Notes

1 This parameter is periodically sampled and not 100% tested.

2 If power monitor is programmed to generate INT.

3 Access is blocked at VSW. The last access should be complete. If VSW is programmed to occur at VBAK and VBAK > VDDMIN, the system may need an early warning that VSW will occur.

4 Failing to satisfy tRI may result in the first access being ignored.

5 Slew rate for proper transition between the locked-out condition and normal operation.

Supervisor AC Parameters TA = -40° C to + 85° C, VDD = 4.5V to 5.5V unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Units	Notes
tIPU	INT output pulse width	150	200	300	ms	1
tFCO	Flag register access to INT pin clear			100	ns	2

Notes

1 P/L = 1; pulse mode.

2 P/L= 0; level mode. From the end of the access where the flag register is read and the flag cleared.

Capacitance TA = 25° C , f=1.0 MHz, VDD = 5V

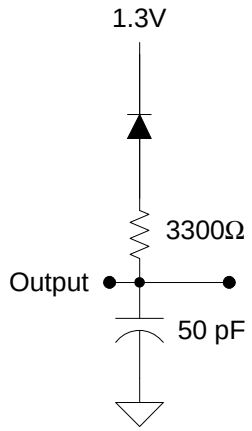
Symbol	Parameter	Min	Typ	Units	Notes
CI/O	Input Output Capacitance	8		pF	
CIN	Input Capacitance	6		pF	
CXTAL	Crystal characteristic capacitance		6	pF	

Equivalent AC Load Circuit

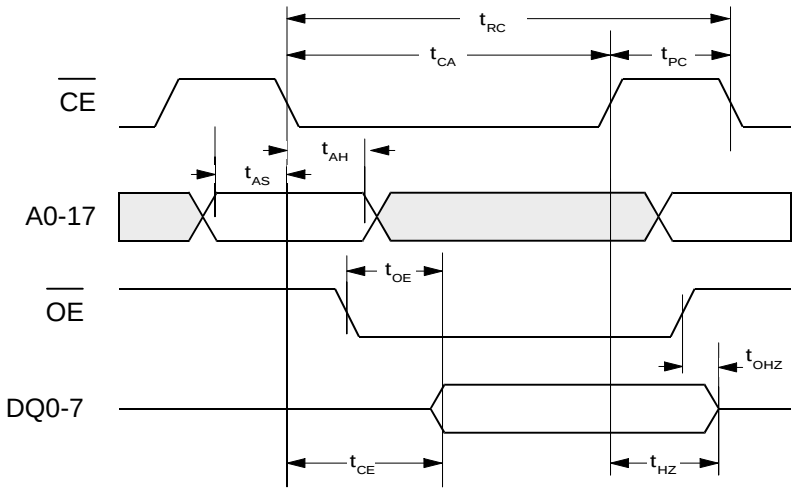
AC Test Conditions

Input Pulse Levels	0 to 3V
Input rise and fall times	10 ns
Input and output timing levels	1.5V

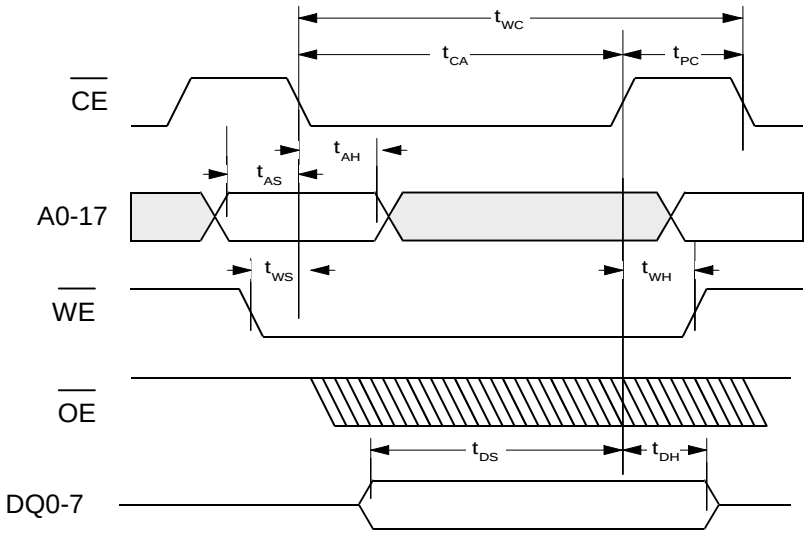
Equivalent AC Load Circuit



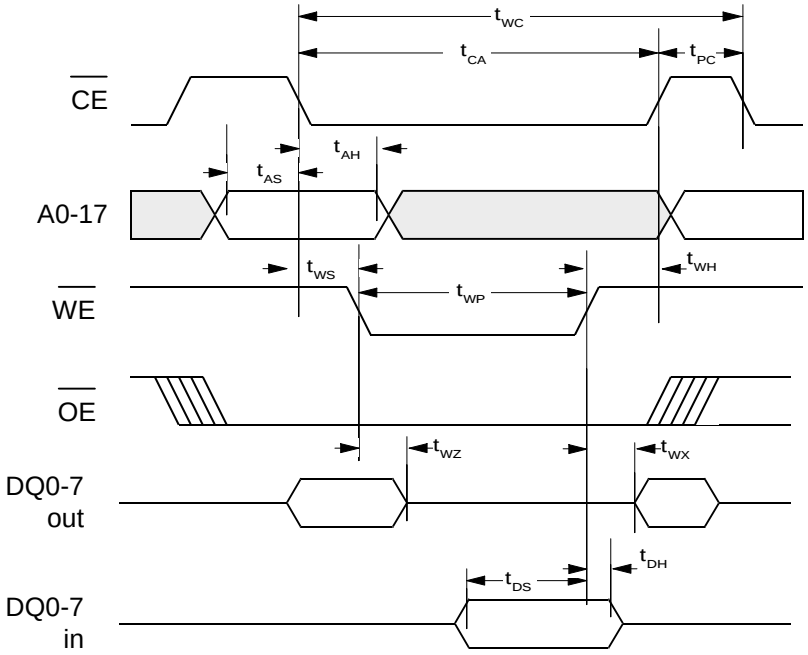
Read Cycle Timing



Write Cycle Timing - /CE Controlled Timing

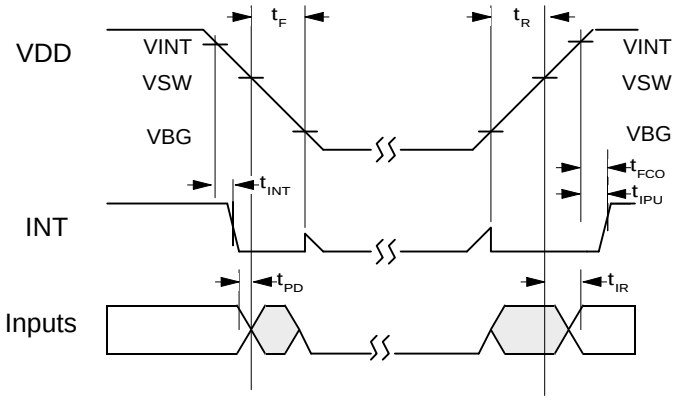


Write Cycle Timing - /WE Controlled Timing

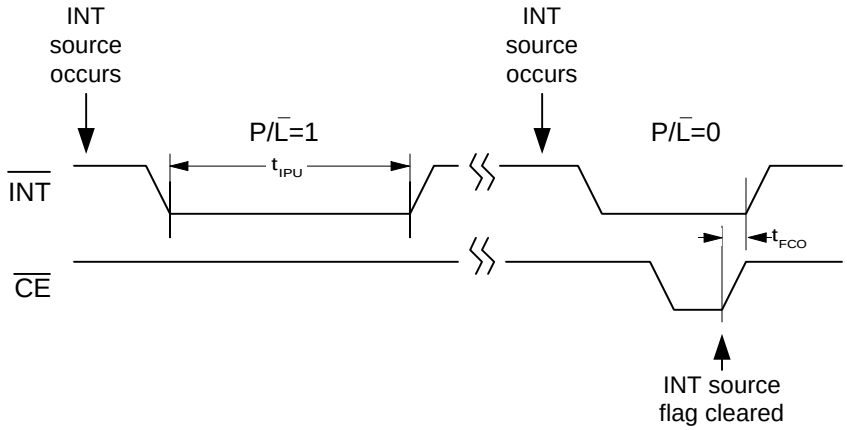


Power Cycle Timing

Picture assumes VSW < VINT



INT Pin Timing



Data Retention TA = -40° C to + 85° C, VDD = 4.5V to 5.5V unless otherwise specified

Parameter	Min	Units	Notes
Data Retention	10	years	1

Notes

1. Data retention is specified at 55° C. The relationship between retention, temperature, and the associated reliability level will be characterized in a separate reliability report.

32-pin TSOP (EIAJ IC-74-2-III)