FM20L08

1Mbit Bytewide FRAM Memory

Features

1Mbit Ferroelectric Nonvolatile RAM
- Organized as 128Kx8
- Unlimited Read/Write Cycles
- NoDelay™ Writes
- Advanced High-Reliability Ferroelectric Process

Superior to Battery-backed SRAM Modules
- No battery concerns
- Monolithic reliability
- True surface mount solution, no rework steps
- Superior for moisture, shock, and vibration
- Resistant to negative voltage undershoots

SRAM Compatible
- JEDEC Standard 128Kx8 SRAM pinout
- 55 ns Access Time
- 95 ns Cycle Time

Low Power Operation
- 2.7V – 3.6V Power Supply
- 15 mA Active Current
- 10 µA Standby Current

Industry Standard Configurations
- Industrial Temperature -40° C to +85° C
- 32-pin SOIC and PDIP packages

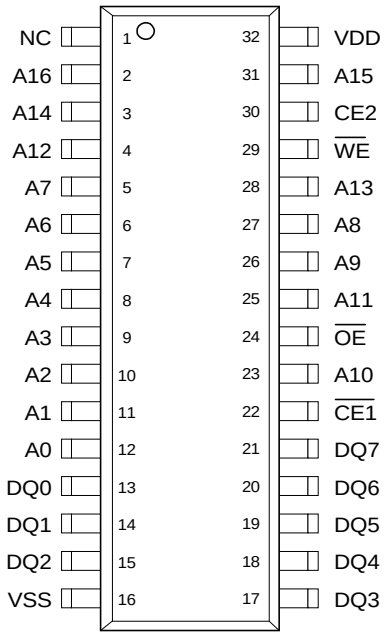
Description

The FM20L08 is a 1-Mbit nonvolatile memory employing an advanced ferroelectric process. A ferroelectric random access memory or FRAM is nonvolatile and reads and writes like a RAM. It provides data retention for 10 years while eliminating the reliability concerns, functional disadvantages and system design complexities of battery-backed SRAM (BBSRAM). Fast write timing and unlimited write endurance make FRAM superior to other types of nonvolatile memory.

In-system operation of the FM20L08 is very similar to other RAM devices. Read- and write-cycle times are equal. The FRAM memory, however, is nonvolatile due to its unique ferroelectric memory process. Unlike BBSRAM, the FM20L08 is a truly monolithic nonvolatile memory. It provides the same functional benefits of a fast write without the disadvantages associated with modules and batteries or hybrid memory solutions.

These capabilities make the FM20L08 ideal for nonvolatile memory applications requiring frequent or rapid writes in a bytewide environment. A truly surface-mount package solution improves the manufacturability of new designs. Device specifications are guaranteed over industrial temperature range –40°C to +85°C.

Pin Configuration



Ordering Information	
FM20L08-55-S	55 ns access, 32-pin SOIC (S)
FM20L08-55-P	55 ns access, 32-pin PDIP (P)
FM20L08-70-S	70 ns access, 32-pin SOIC (S)
FM20L08-70-P	70 ns access, 32-pin PDIP (P)

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1850 Ramtron Drive, Colorado Springs, CO 80921
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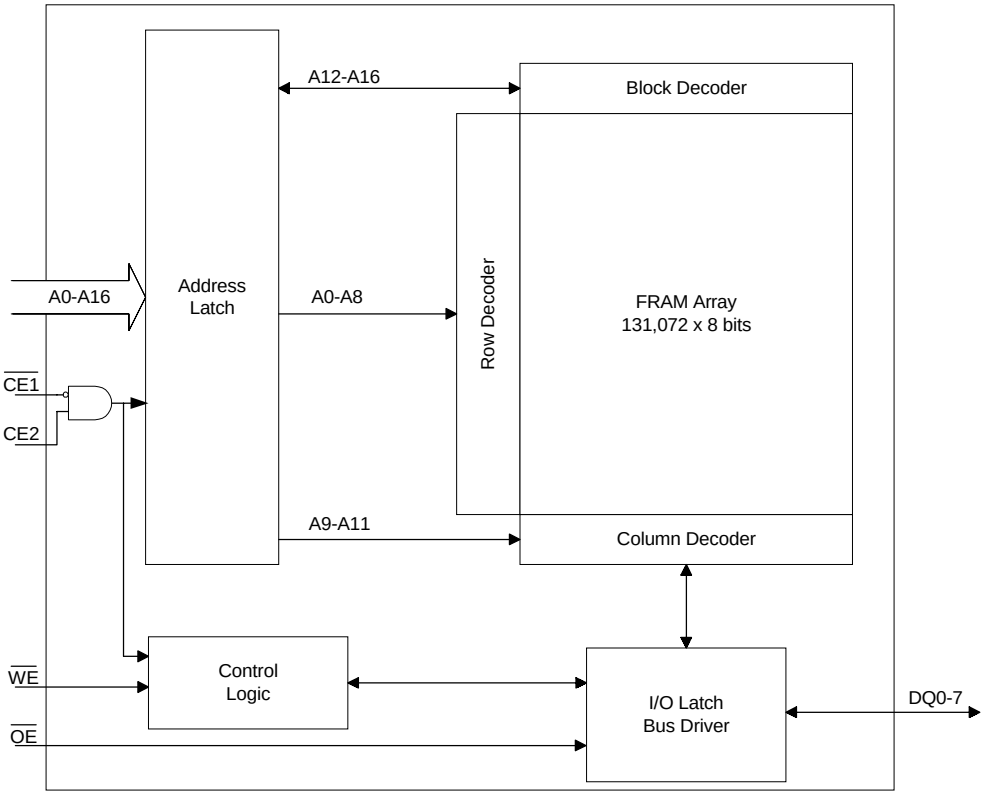


Figure 1. Block Diagram

Pin Description

Pin Name	Type	Pin Description
A0-A16	Input	Address inputs: The 17 address lines select one of 131,072 bytes in the FRAM array. The address value is latched on the falling edge of /CE.
/CE1, CE2	Input	Chip Enable inputs: The device is selected and a new memory access begins when both /CE1 is low and CE2 is high. The address is latched internally when both chip enable inputs are logically true. Subsequent changes to the address inputs are ignored until the next access occurs. CE2 is internally pulled up to V_{DD}.
/WE	Input	Write Enable: Asserting /WE low causes the FM20L08 to write the contents of the data bus to the latched address location.
/OE	Input	Output Enable: When /OE is low the FM20L08 drives the data bus when valid data is available. Deasserting /OE high tri-states the DQ pins.
DQ0-7	I/O	Data: 8-bit bi-directional data bus for accessing the FRAM array.
VDD	Supply	Supply Voltage: 3V
VSS	Supply	Ground

Functional Truth Table

/CE1	CE2	/WE	Function
H	X	X	Standby/Precharge
X	L	X	Standby/Precharge
↓	H	X	Latch Address (and Begin Write if /WE=low)
L	↑	X	Latch Address (and Begin Write if /WE=low)
L	H	H	Read
L	H	↓	Write

Note: The /OE pin controls only the DQ output buffers.

Overview

The FM20L08 is a bytewide FRAM memory. The memory array is logically organized as 131,072 x 8 and is accessed using an industry standard parallel interface. All data written to the part is immediately nonvolatile with no delay. Functional operation of the FRAM memory is the same as SRAM type devices, except the FM20L08 requires a CE transition (both /CE1 and CE2 true) to start each memory cycle.

Memory Architecture

Users access 131,072 memory locations, each with 8 data bits through a parallel interface. The cycle time is the same for read and write memory operations. This simplifies memory controller logic and timing circuits. Likewise the access time is the same for read and write memory operations. When /CE is deasserted high, a precharge operation begins, and is required on every memory cycle. Thus unlike SRAM, the access and cycle times are not equal. Writes occur immediately at the end of the access with no delay. Unlike an EEPROM, it is not necessary to poll the device for a ready condition since writes occur at bus speed.

Note that the FM20L08 has no special power-down demands. It will not block user access and it contains no power-management circuits other than a simple internal power-on reset. It is the user's responsibility to ensure that VDD is within data sheet tolerances to prevent incorrect operation.

Memory Operation

The FM20L08 is designed to operate in a manner similar to other bytewide memory products. For users familiar with bytewide SRAM, the performance is comparable but the bytewide interface operates in a slightly different manner as described below. For users familiar with EEPROM, the obvious differences result from the higher write-performance of FRAM technology including NoDelay writes and much higher write-endurance.

Read Operation

A read operation begins on the falling edge of /CE. At this time, the address bits are latched and a memory cycle is initiated. Once started, a full memory cycle must be completed internally regardless of the state of /CE. Data becomes available on the bus after the access time has been satisfied.
After the address has been latched, the address value may be changed upon satisfying the hold time parameter. Unlike an SRAM, changing the address has no effect on the memory operation after the address is latched.

The FM20L08 will drive the data bus when /OE is asserted to a low state. If /OE is asserted after the memory access time has been satisfied, the data bus will be driven with valid data. If /OE is asserted prior to completion of the memory access, the data bus will not be driven until valid data is available. This feature minimizes supply current in the system by eliminating transients caused by invalid data being driven onto the bus. When /OE is inactive the data bus will remain tri-stated.

Write Operation

Writes occur in the FM20L08 in the same time interval as reads. The FM20L08 supports both /CE- and /WE-controlled write cycles. In all cases, the address is latched on the falling edge of /CE.

In a /CE-controlled write, the /WE signal is asserted prior to beginning the memory cycle. That is, /WE is low when /CE falls. In this case, the device begins the memory cycle as a write. The FM20L08 will not drive the data bus regardless of the state of /OE.

In a /WE-controlled write, the memory cycle begins on the falling edge of /CE. The /WE signal falls after the falling edge of /CE. Therefore, the memory cycle begins as a read. The data bus will be driven according to the state of /OE until /WE falls. The timing of both /CE- and /WE-controlled write cycles is shown in the electrical specifications.

Write access to the array begins asynchronously after the memory cycle is initiated. The write access terminates on the rising edge of /WE or /CE, whichever is first. Data set-up time, as shown in the electrical specifications, indicates the interval during which data cannot change prior to the end of the write access.

Unlike other truly nonvolatile memory technologies, there is no write delay with FRAM. Since the read and write access times of the underlying memory are the same, the user experiences no delay through the bus. The entire memory operation occurs in a single bus cycle. Therefore, any operation including read or write can occur immediately following a write. Data polling, a technique used with EEPROMs to determine if a write is complete, is unnecessary.

Precharge Operation

The precharge operation is an internal condition where the state of the memory is prepared for a new access. All memory cycles consist of a memory access and a precharge. The precharge is user

initiated by taking the /CE signal high or inactive. It must remain high for at least the minimum precharge timing specification.

The user dictates the beginning of this operation since a precharge will not begin until /CE rises. However, the device has a maximum /CE low time specification that must be satisfied.

Applications

As the first truly nonvolatile RAM, the FM20L08 fits into many diverse applications. Clearly, its monolithic nature and high performance make it superior to battery-backed SRAM in many applications. This applications guide is intended to facilitate the transition from BBSRAM to FRAM. It is divided into two parts. First is a treatment of the advantages of FRAM memory compared with battery-backed SRAM. Second is a design guide, which highlights design considerations that should be reviewed in both retrofit and new design situations.

FRAM Advantages

Although battery-backed SRAM is a mature and established solution, it has many weaknesses. These stem, directly or indirectly from the presence of the battery. FRAM uses an inherently nonvolatile storage mechanism that requires no battery. It therefore eliminates these weaknesses. The major considerations in upgrading to FRAM are as follows.

Construction Issues

1. Cost

The cost of both the component and the manufacturing overhead of battery-backed SRAM is high. FRAM with its monolithic construction is inherently a lower cost solution. In addition, there is no 'built-in' rework step required for battery attachment when using surface mount parts. Therefore, assembly is streamlined and more cost effective. In the case of DIP battery-backed modules, the user is constrained to through-hole assembly techniques and a board wash using no water.

2. Humidity

A typical battery-backed SRAM module is qualified at 60º C, 90% Rh, but under no bias and no pressure. These conditions are chosen because the multi-component assemblies are vulnerable to moisture and dirt. FRAM is qualified using HAST – highly accelerated stress test. This requires 120º C at 85% Rh, 24.4 psia at 5.5V.

3. System reliability

Data integrity must be questioned when using a battery-backed SRAM. They are inherently vulnerable to shock and vibration. If the battery contact comes loose, data will be lost. In addition a negative voltage, even a momentary undershoot, on any pin of a battery-backed SRAM can cause data loss. The negative voltage causes current to be drawn directly from the battery. These momentary short circuits can greatly weaken a battery and reduce its capacity over time. In general, there is no way to monitor the lost battery capacity. Should an undershoot occur in a battery backed system during a power down, data can be lost immediately.

4. Space

Certain disadvantages of battery-backed, such as susceptibility to shock, can be reduced by using the old fashioned DIP module. However, this alternative takes up board space, height, and dictates through-hole assembly. FRAM offers a true surface-mount solution that uses 25% of the board space.

Direct Battery Issues

5. Field maintenance

No matter how mature batteries become, they are a built-in maintenance problem. They eventually must be replaced. Despite long life projections, it is impossible to know if any individual battery will last considering all of the factors that can degrade them.

6. Environmental

Lithium batteries are widely regarded as an environmental problem. They are a potential fire hazard and proper disposal can be a burden. In addition, shipping of lithium batteries may be restricted.

7. Style!

Backing up an SRAM with a battery is an old-fashioned approach. In many cases, such modules are the only through-hole component in sight. FRAM is the latest memory technology and it is changing the way systems are designed.

FRAM is nonvolatile and writes fast -- no battery required!

FRAM Design Considerations

When designing with FRAM for the first time, users of SRAM will recognize a few minor differences. First, bytewide FRAM memories latch each address on the falling edge of chip enable. This allows the address bus to change after starting the memory access. Since every access latches the memory address on the falling edge of /CE1 (or rising edge of

CE2), users cannot tie off both pins as they might with SRAM.

Users who are modifying existing designs to use FRAM should examine the memory controller for timing compatibility of address and control pins. Each memory access must be qualified with a low transition of /CE. In many cases, this is the only change required. An example of the signal relationships is shown in Figure 2 below. Also shown is a common SRAM signal relationship that will not work for the FM20L08.

The reason for /CE to strobe for each address is two-fold: it latches the new address and creates the necessary precharge period while /CE is high.

A second design consideration relates to the level of V_{DD} during operation. Battery-backed SRAMs are forced to monitor V_{DD} in order to switch to battery backup. They typically block user access below a certain V_{DD} level in order to prevent loading the battery with current demand from an active SRAM. The user can be abruptly cut off from access to the nonvolatile memory in a power down situation with no warning or indication.

FRAM memories do not need this system overhead. The memory will not block access at any V_{DD} level. The user, however, should prevent the processor from accessing memory when V_{DD} is out-of-tolerance. The common design practice of holding a processor in reset when V_{DD} drops is adequate; no special provisions must be taken for FRAM design.

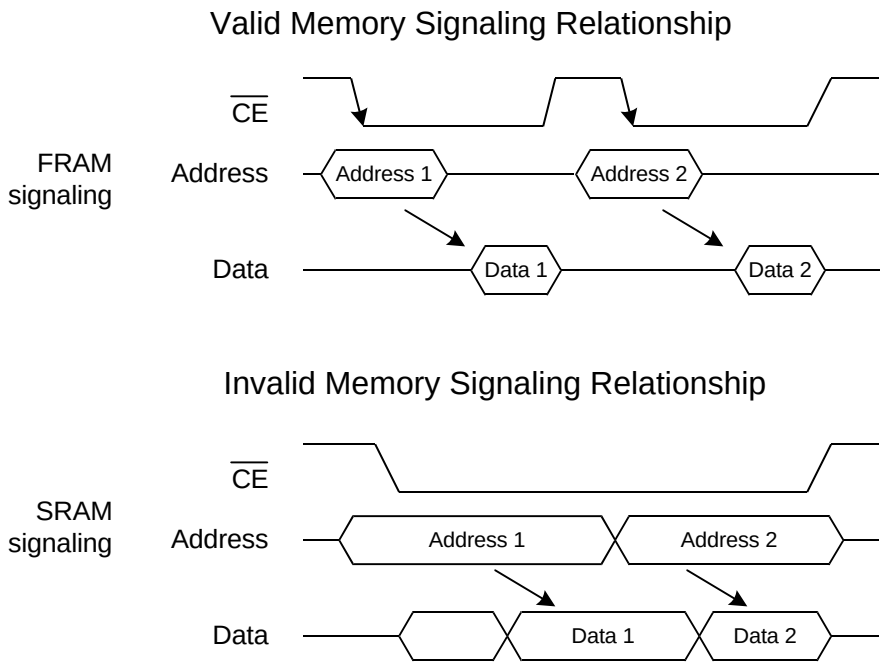


Figure 2. Memory Address and /CE Relationships

Electrical Specifications

Absolute Maximum Ratings

Symbol	Description	Ratings
V_{DD}	Power Supply Voltage with respect to V_{SS}	-1.0V to +5.0V
V_{IN}	Voltage on any signal pin with respect to V_{SS}	-1.0V to +5.0V and $V_{IN} < V_{DD}$+1V
T_{STG}	Storage temperature	-40°C to +85°C
T_{LEAD}	Lead temperature (Soldering, 10 seconds)	300° C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and the functional operation of the device at these or any other conditions above those listed in the operational section of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

DC Operating Conditions (T_A = -40° C to + 85° C, V_{DD} = 2.7V to 3.65V unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{DD}	Power Supply	2.7	-	3.65	V	
I_{DD}	V_{DD} Supply Current - t_{RC}/t_{WC} 95 ns - t_{RC}/t_{WC} 130 ns			 20 15	 mA mA	 1 1
I_{SB1}	Standby Current - TTL			400	µA	2
I_{SB2}	Standby Current - CMOS			10	µA	3
I_{LI}	Input Leakage Current			±1	µA	4
I_{LO}	Output Leakage Current			±1	µA	4
V_{IH}	Input High Voltage	2.0		V_{DD} + 0.5	V	
V_{IL}	Input Low Voltage	-0.5		0.8	V	
V_{OH}	Output High Voltage (I_{OH} = -1.0 mA)	2.4			V	
V_{OL}	Output Low Voltage (I_{OL} = 3.2 mA)			0.4	V	

Notes

1. V_{DD} = 3.65V, /CE cycling at minimum cycle time. All inputs at CMOS levels, all outputs unloaded.
2. V_{DD} = 3.65V, /CE at V_{IH}, All inputs at TTL levels, all outputs unloaded.
3. V_{DD} = 3.65V, /CE at V_{DD}, All inputs at CMOS levels, all outputs unloaded.
4. V_{IN}, V_{OUT} between V_{DD} and V_{SS}.

Read Cycle AC Parameters (T_A = -40° C to + 85° C, V_{DD} = 2.7V to 3.65V unless otherwise specified)

Symbol	Parameter	-55		-70		Units	Notes
		Min	Max	Min	Max		
t_{CE}	Chip Enable Access Time (to data valid)		55		70	ns	
t_{CA}	Chip Enable Active Time	55	10,000	70	10,000	ns	
t_{RC}	Read Cycle Time	95		130		ns	
t_{PC}	Precharge Time	40		60		ns	
t_{AS}	Address Setup Time	0		0		ns	
t_{AH}	Address Hold Time	10		10		ns	
t_{OE}	Output Enable Access Time		10		10	ns	
t_{HZ}	Chip Enable to Output High-Z		15		15	ns	1
t_{OHZ}	Output Enable to Output High-Z		15		15	ns	1

Write Cycle AC Parameters (T_A = -40° C to + 85° C, V_{DD} = 2.7V to 3.65V unless otherwise specified)

Symbol	Parameter	-55		-70		Units	Notes
		Min	Max	Min	Max		
t_{CA}	Chip Enable Active Time	55	10,000	70	10,000	ns	
t_{CW}	Chip Enable to Write High	55		70		ns	
t_{WC}	Write Cycle Time	95		130		ns	
t_{PC}	Precharge Time	40		60		ns	
t_{AS}	Address Setup Time	0		0		ns	
t_{AH}	Address Hold Time	10		10		ns	
t_{WP}	Write Enable Pulse Width	40		40		ns	
t_{DS}	Data Setup	40		40		ns	
t_{DH}	Data Hold	0		0		ns	
t_{WZ}	Write Enable Low to Output High Z		15		15	ns	1
t_{WX}	Write Enable High to Output Driven	10		10		ns	1
t_{HZ}	Chip Enable to Output High-Z		15		15	ns	1
t_{WS}	Write Setup	0		0		ns	2
t_{WH}	Write Hold	0		0		ns	2

Notes

1 This parameter is periodically sampled and not 100% tested.

2 The relationship between /CE and /WE determines if a /CE- or /WE-controlled write occurs. There is no timing specification associated with this relationship.

Data Retention (V_{DD} = 2.7V to 3.65V unless otherwise specified)

Parameter	Min	Units	Notes
Data Retention	10	Years	1

Notes

1. The relationship between retention, temperature, and the associated reliability level is characterized separately.

Power Cycle Timing (T_A = -40° C to + 85° C, V_{DD} = 2.7V to 3.65V unless otherwise specified)

Symbol	Parameter	Min	Units	Notes
t_{PU}	VDD Min to First Access Start	1	µS	
t_{PD}	Last Access Complete to VDD Min	0	µS	

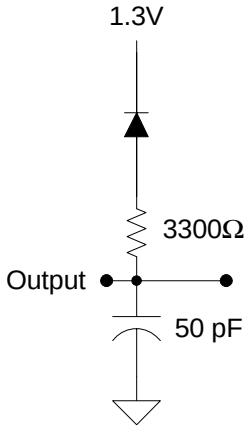
Capacitance (T_A = 25° C , f=1 MHz, V_{DD} = 3V)

Symbol	Parameter	Max	Units	Notes
$C_{I/O}$	Input Output Capacitance	8	pF	
C_{IN}	Input Capacitance	6	pF	

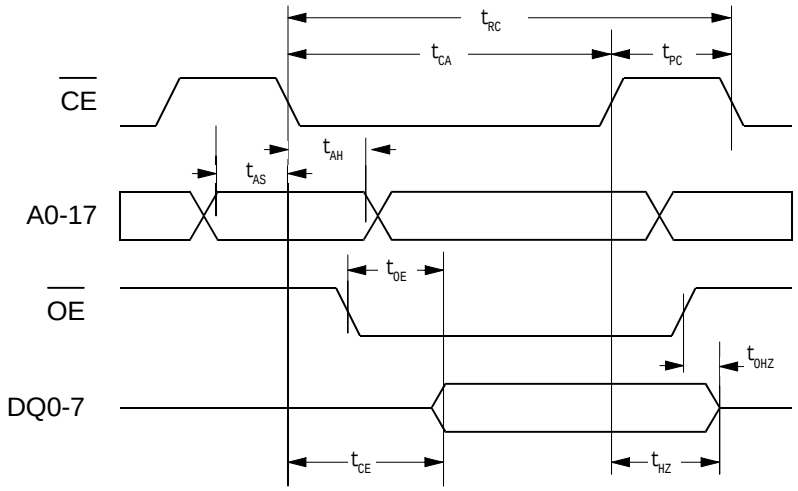
AC Test Conditions

Input Pulse Levels	0 to 3V
Input rise and fall times	10 nS
Input and output timing levels	1.5V

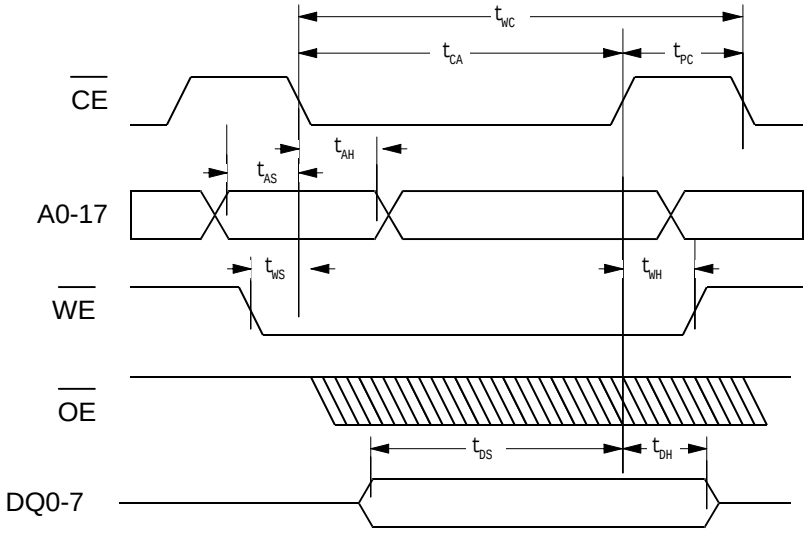
Equivalent AC Load Circuit



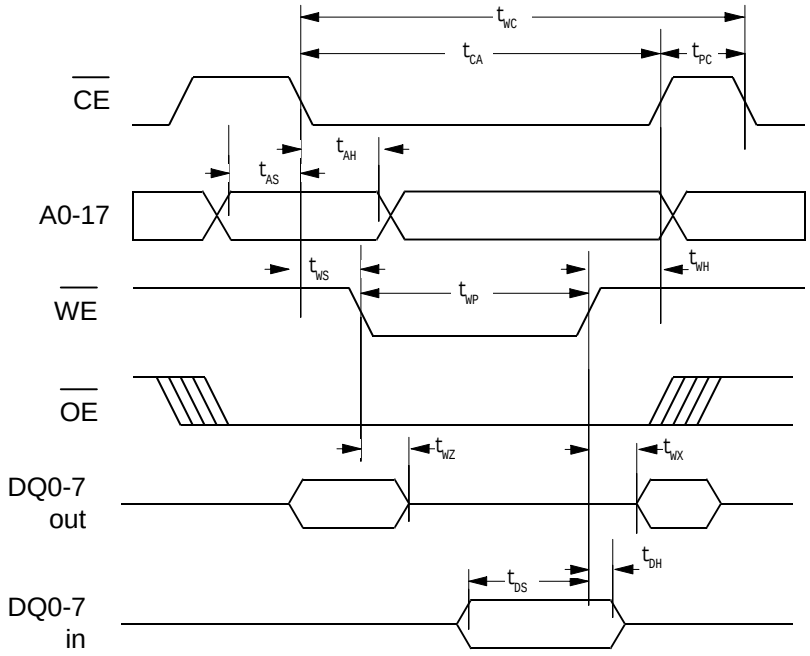
Read Cycle Timing



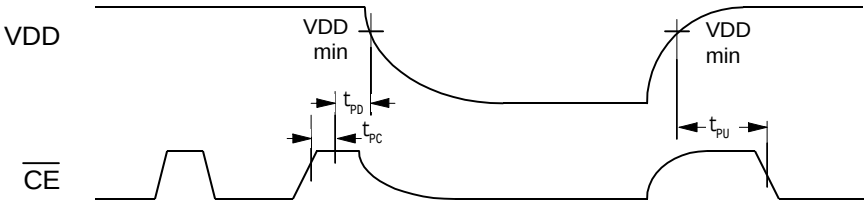
/CE-Controlled Write Cycle Timing



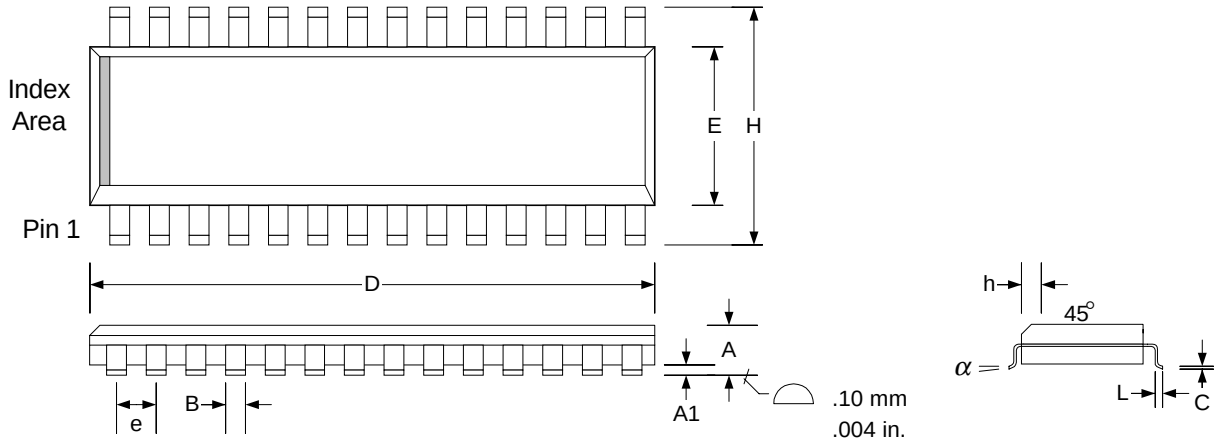
/WE-Controlled Write Cycle Timing



Power Cycle Timing



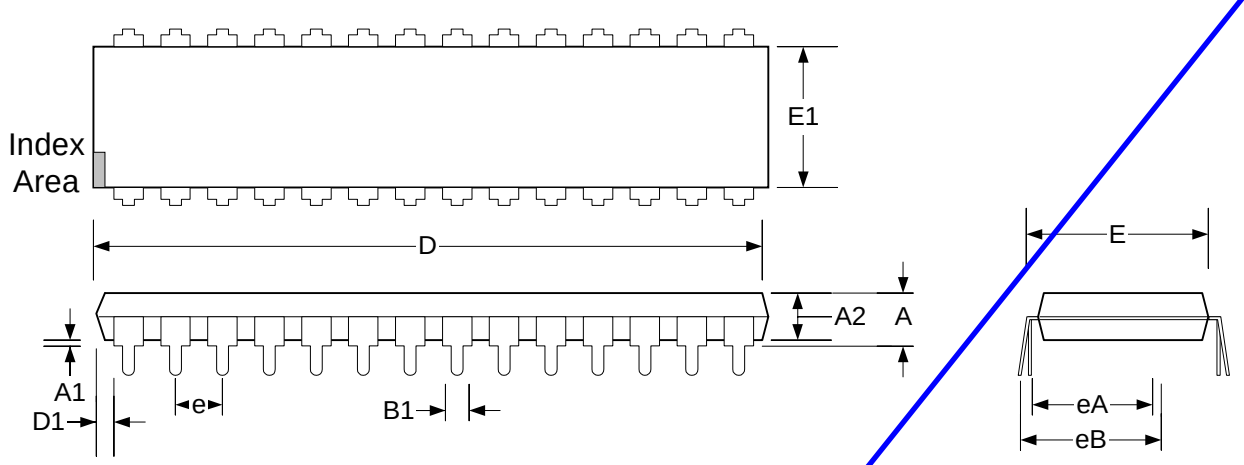
32-pin SOIC (450-mils Wide)



Selected Dimensions
Controlling dimensions in millimeters.
Conversions to inches are not exact.

Symbol	Dim	Min	Nom.	Max
A	mm in.	TBD		
A1	mm in.	TBD		
B	mm in.	0.356 0.014		0.508 0.020
C	mm in.	TBD		
D	mm in.	20.14 0.793		20.75 0.817
E	mm in.	11.17 0.440		11.43 0.450
e	mm in.	TBD	1.27 0.050	
H	mm in.	13.86 0.546		14.38 0.566
h	mm in.	TBD		
L	mm in.	TBD		
α		TBD		

32-pin PDIP (600-mils Wide)



Selected Dimensions

For complete dimensions and notes, refer to JEDEC MS-011
Controlling dimensions in inches.
Conversions to millimeters are not exact.

Symbol	Dim	Min	Nom	Max
A	in.			0.250
	mm			6.35
A1	in.	0.015		
	mm	0.39		
A2	in.	0.125		0.195
	mm	3.18		4.95
B	in.	0.014		0.022
	mm	0.356		0.558
B1	in.	0.030		0.070
	mm	0.77		1.77
D	in.	1.580		1.765
	mm	35.1		39.7
D1	in.	0.005		
	mm	0.13		
E	in.	0.600		0.625
	mm	15.24		15.87
E1	in.	0.485		0.580
	mm	12.32		14.73
e	in.		0.100 BSC	
	mm		2.54 BSC	
eA	in.		0.600 BSC	
	mm		15.24 BSC	
eB	in.			0.700
	mm			17.78