FAIRCHILD SEMICONDUCTOR TM

April 1998

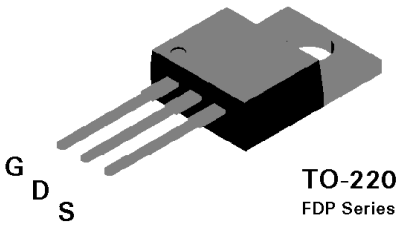
FDP7030L / FDB7030L
N-Channel Logic Level Enhancement Mode Field Effect Transistor

General Description

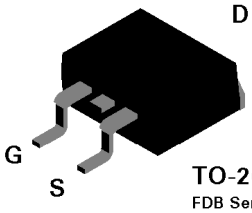
These N-Channel logic level enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage applications such as DC/DC converters and high efficiency switching circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

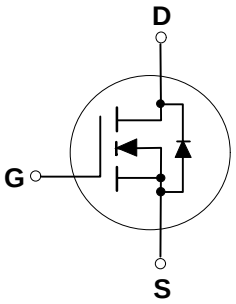
- 100 A, 30 V. $R_{DS(ON)}$ = 0.007 Ω @ V_{GS}=10 V
  $R_{DS(ON)}$ = 0.010 Ω @ V_{GS}=5 V.
- Critical DC electrical parameters specified at elevated temperature.
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.
- High density cell design for extremely low $R_{DS(ON)}$.
- 175°C maximum junction temperature rating.



TO-220
FDP Series



TO-263AB
FDB Series



Absolute Maximum Ratings

T_C = 25°C unless otherwise noted

Symbol	Parameter	FDP7030L	FDB7030L	Units
V_{DSS}	Drain-Source Voltage	30		V
V_{GSS}	Gate-Source Voltage - Continuous	±20		V
I_D	Drain Current - Continuous (Note 1)	100		A
		75		
	- Pulsed (Note 1)	300		
P_D	Total Power Dissipation @ T_C = 25°C	125		W
	Derate above 25°C	0.83		W/°C
T_J,T_{STG}	Operating and Storage Temperature Range	-65 to 175		°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	275		°C
THERMAL CHARACTERISTICS				
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1.2		°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5		°C/W

Electrical Characteristics (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DRAIN-SOURCE AVALANCHE RATINGS (Note 1)						
W_{DSS}	Single Pulse Drain-Source Avalanche Energy	V_{DD} = 15 V, I_D = 38 A			200	mJ
I_{AR}	Maximum Drain-Source Avalanche Current				38	A
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	30			V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	I_D = 250 µA, Referenced to 25 °C		36		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V			10	µA
		T_J =125 °C			1	mA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	1	1.5	2	V
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Temp.Coefficient	I_D = 250 µA, Referenced to 25 °C		-5		mV/°C
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 50 A		0.006	0.007	Ω
		T_J = 125°C		0.009	0.011	
		V_{GS} = 5 V, I_D = 40 A		0.009	0.01	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 10 V	60			A
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 50 A		50		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1.0 MHz		2150		pF
C_{oss}	Output Capacitance			1290		pF
C_{rss}	Reverse Transfer Capacitance			420		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = 15 V, I_D = 75 A, V_{GS} = 10 V, R_{GEN} = 6 Ω, R_{GS} = 10 Ω		10	20	nS
t_r	Turn - On Rise Time			160	225	nS
$t_{D(off)}$	Turn - Off Delay Time			70	95	nS
t_f	Turn - Off Fall Time			140	195	nS
Q_g	Total Gate Charge	V_{DS} = 12 V, I_D = 50 A, V_{GS} = 4.5 V		35	50	nC
Q_{gs}	Gate-Source Charge			12		nC
Q_{gd}	Gate-Drain Charge			18		nC
DRAIN-SOURCE DIODE CHARACTERISTICS						
I_S	Maximum Continuos Drain-Source Diode Forward Current (Note 1)				100	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current (Note 2)				300	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 50 A (Note 2)		1	1.3	V
		T_J = 125°C		0.85	1.1	

Notes
1. Calculated continuous current based on maximum allowable junction temperature. Actual maximum continuous current limited by package constraints to 75A.
2. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.