

FAN8038C(KA3038)

4-Channel Motor Drive IC

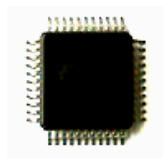
Features

- 4-CH H-Bridge driver
- Built-in DC-DC converter controller
- Built-in Power-on reset (POR) circuit
- Built-in battery charging circuit
- Built-in battery voltage monitoring circuit
- Built-in thermal shutdown (TSD) circuit
- Built-in general OP-Amplifier
- Low power consumption
- Built-in power controller circuit

Description

FAN8038C is monolithic IC for portable CD player.

44-QFP-1010B



Typical application

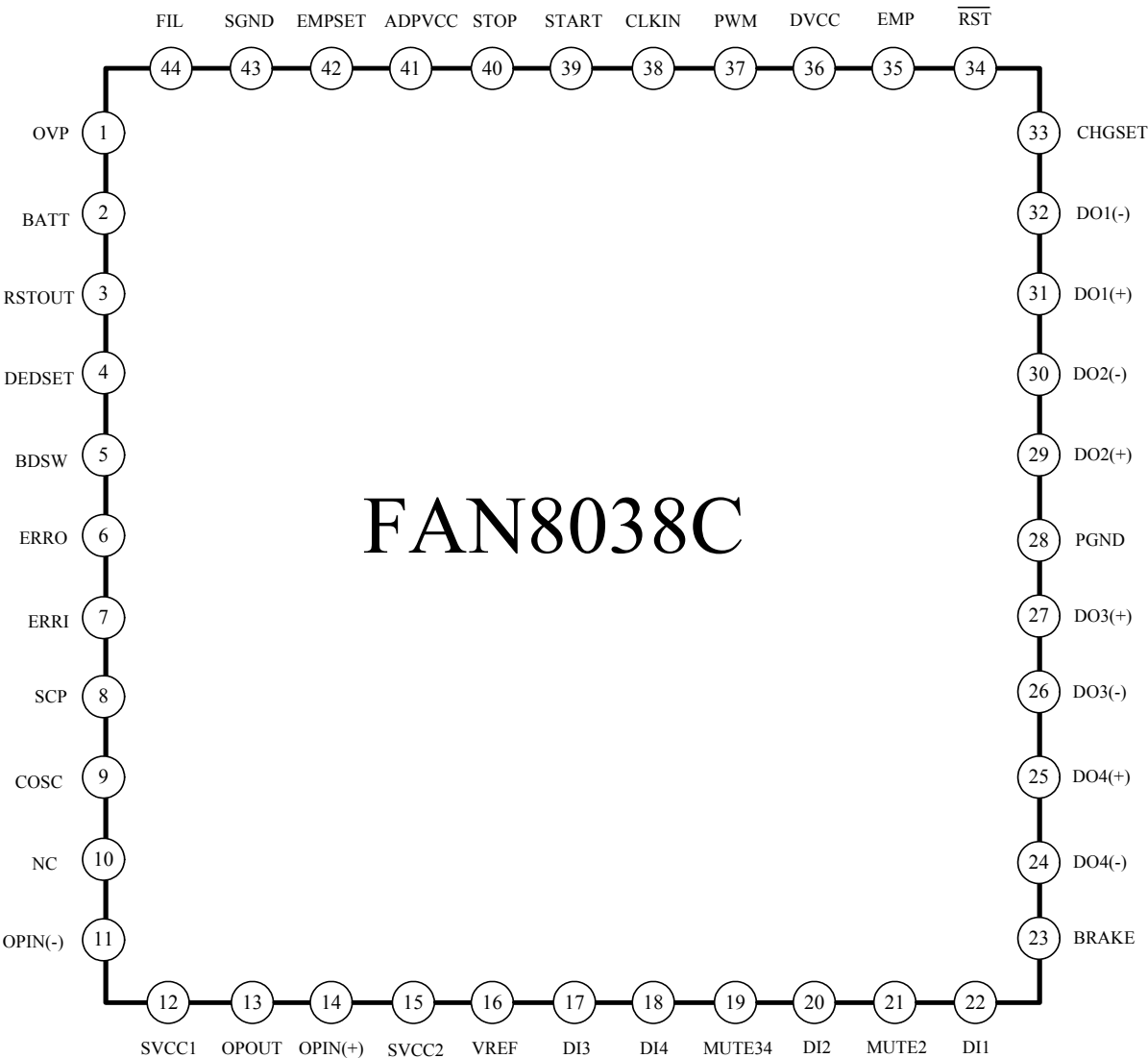
- Portable Compact Disk Player (CDP)
- Portable Mini Disk Player (MD)
- Disc-Man
- Other Potable Compact Disk Media

Ordering Information

Device	Package	Operating Temp.
FAN8038C	44-QFP-1010B	-35°C ~ +85°C

Preliminary Specification

Pin Assignments

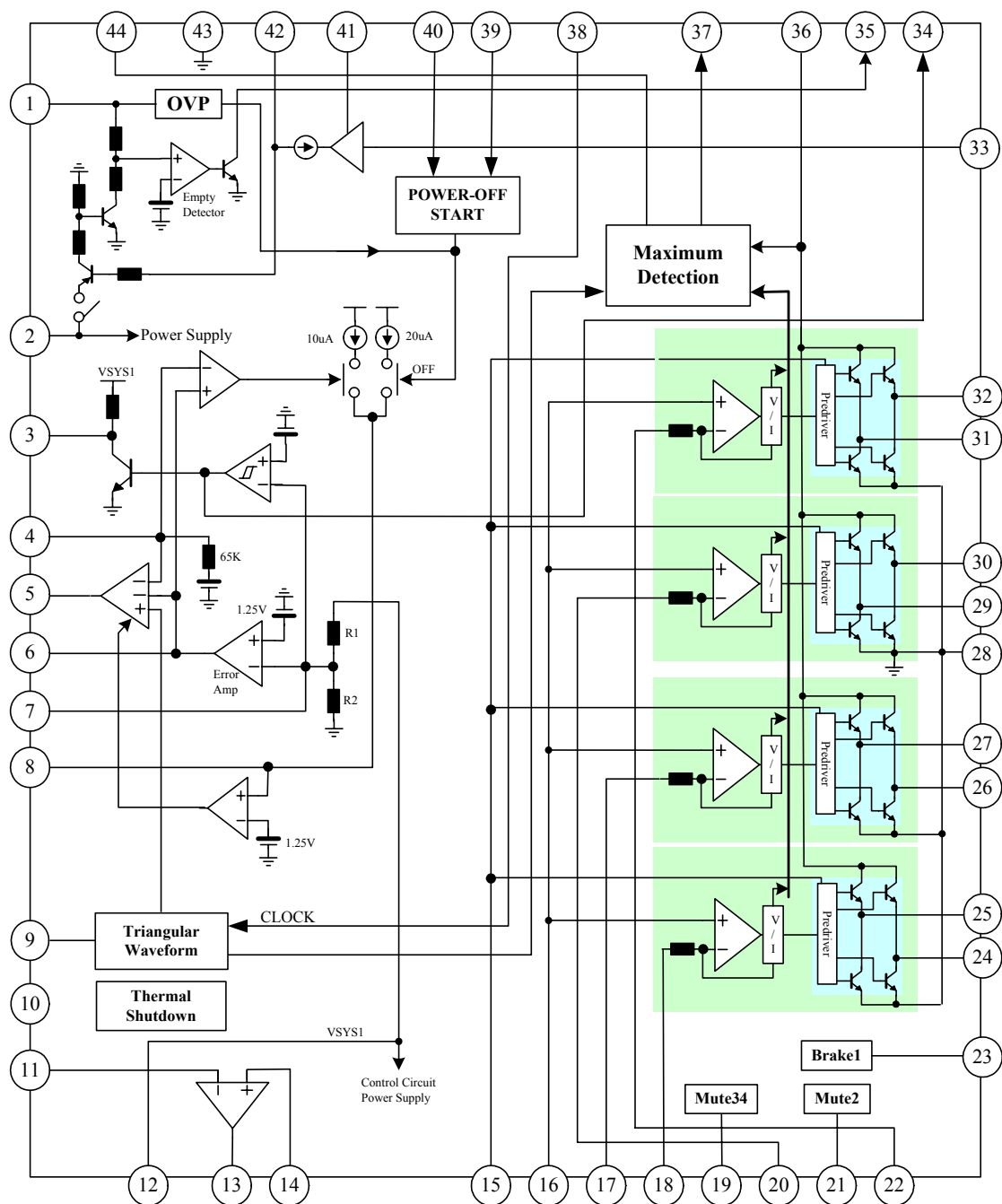


Preliminary Specification

Pin Definitions

Pin Number	Pin Name	I/O	Pin Function Description
1	OVP	I	Battery voltage motor
2	BATT	-	Battery power supply input
3	RSTOUT	O	Power-on reset output
4	DEDSET	I	Dead time setting capacitor
5	BDSW	O	Transistor drive for voltage step-up
6	ERRO	O	Error amplifier output
7	ERRI	I	Error amplifier Input
8	SCP	I	Short circuit protection time setting capacitor
9	COSC	O	Triangular waveform output
10	N.C	-	No connection
11	OPIN(-)	I	OP-amplifier negative input
12	SVCC1	-	Control circuit power supply
13	OPOUT	O	OP-amplifier output
14	OPIN(+)	I	OP-amplifier positiveinput
15	SVCC2	-	Pre-driver power supply
16	VREF	I	Reference voltage input
17	DI3	I	Channel 3 control signal Input
18	DI4	I	Channel 4 control signal Input
19	MUTE34	I	Channel 3 and 4 mute signal input
20	DI2	I	Channel 2 control signal Input
21	MUTE2	I	Channel 2 mute signal inpu
22	DI1	I	Channel 1 control signal Input
23	BRAKE	I	Channel 1 brake signal input
24	DO4(-)	O	Channel 4 negative output
25	DO4(+)	O	Channel 4 positive output
26	DO3(-)	O	Channel 3 negative output
27	DO3(+)	O	Channel 3 positive output
28	PGND	-	Power block power Ground
29	DO2(+)	O	Channel 2 positive output
30	DO2(-)	O	Channel 2 negative output
31	DO1(+)	O	Channel 1 positive output
32	DO1(-)	O	Channel 1 negative output
33	CHGSET	I	Charge current setting resistance
34	RST	O	Power-on reset inverting output
35	EMP	O	Battery voltage detection output (Empty detection)
36	DVCC	-	H-Bridge block power supply
37	PWM	O	PWM transistor drive output
38	CLKIN	I	External clock input
39	START	I	DC-DC converter start control input
40	STOP	I	DC-DC converter off control input
41	ADPVCC	-	Charging circuit power supply
42	EMPSET		Empty dection level switch
43	SGND	-	Signal ground
44	FIL	I	PWM phase compensation

Internal Block Diagram



Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Value	Unit
Maximum supply voltage	V _{CC}	13.2	V
Maximum output current	I _O	500	mA
Power dissipation	P _D	1.0	W
Operating temperature	T _{OPR}	-35 ~ +85	°C
Storage temperature	T _{STG}	-55 ~ +150	°C

Recommended Operating Conditions (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Charging circuit power supply voltage	ADPVCC	3.0	4.5	8.0	V
Power supply voltage	BATT	1.5	2.4	8.0	V
Control circuit power supply voltage	SVCC1	2.7	3.2	5.5	V
Pre-driver power supply voltage	SVCC2	2.7	3.2	5.5	V
H-Bridge power supply voltage	DVCC	-	PWM	BATT	V
Operating Temperature	Ta	-10	25	70	°C

Electrical characteristics

(Ta=25°C, BATT=2.4V, SVCC1=SVCC2=3.2V, VREF=1.6V, ADPVCC=0V, fCLKIN=88.2KHz, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
COMMON SECTION						
BATT Stand-by Current	IST	BATT=10.5V, SVCC1=SVCC2=VREF=0V	-	-	5	μA
BATT Supply Current (No Load)	IBATT	DVCC=0.45V, MUTE34=3.2V	-	2.5	3.5	mA
SVCC Supply Current (No Load)	ISVCC1	DVCC=0.45V, MUTE34=3.2V, ERRI=0V	-	3.0	3.5	mA
SVCC2 Supply Current (No Load)	ISVCC2	DVCC=0.45V, MUTE34=3.2V	-	3.5	5.0	mA
ADPVCC Supply Current (No Load)	IADPVCC	ADPVCC=4.5V, ROUT=OPEN	-	0.2	1.0	mA
H-BRIDGE DRIVER PART						
Voltage Gain CH1, 3, 4	GVC134	-	12	14	16	dB
Voltage Gain CH2	GVC2	-	21.5	23.5	24.5	dB
Gain Error By Polarity	ΔGVC	-	-2	0	2	dB
Input pin Resistance CH1, 3, 4	RDI134	IN=1.7 and 1.8V	9	11	13	KΩ
Input pin Resistance CH2	RDI2	IN=1.7 and 1.8V	6	7.5	9	KΩ
Maximum Output Voltage	VOOUT	RL=8Ω, DVCC=BATT=4V, IN=0 ~ 3.2V	1.9	2.1	-	V
Saturation Voltage (Lower)	VSAT1	IO= -300mA, IN=0 and 3.2V	-	240	400	mV
Saturation Voltage (Upper)	VSAT2	IO=300mA, IN=0 and 3.2V	-	240	400	mV
Input offset Voltage	VIO	-	-8	0	8	mV
Output Offset Voltage CH1, 3, 4	VOO134	VREF=IN=1.6V	-70	0	70	mV
Output Offset Voltage CH2	VOO2	VREF=IN=1.6V	-130	0	130	mV
DEAD Zone	VDB	-	-20	0	20	mV
Brake1 On Voltage	VM1ON	DI1=1.8V	2.0	-	-	V
Brake1 Off Voltage	VM1OFF	DI1=1.8V	-	-	0.8	V
MUTE2 On Voltage	VM2ON	DI2=1.8V	2.0	-	-	V
MUTE2 Off Voltage	VM2OFF	DI2=1.8V	-	-	0.8	V
MUTE34 On Voltage	VM34ON	DI3=DI4=1.8V	-	-	0.8	V
MUTE34 Off Voltage	VM34OFF	DI3=DI4=1.8V	2.0	-	-	V
VREF On Voltage	VREFON	IN1=IN2=IN3=IN4=1.8V	1.2	-	-	V
VREF Off Voltage	VREFOFF	IN1=IN2=IN3=IN4=1.8V	-	-	0.8	V

*Granted Design Value

Electrical Characteristics

(Ta=25°C, BATT=2.4V, SVCC1=SVCC2=3.2V, VREF=1.6V, ADPVCC=0V, fCLKIN=88.2KHz, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
PWM POWER SUPPLY DRIVING						
PWM Sink Current	IPWM	DI1=2.1V	10	13	17	mA
*DVCC Level Shift Voltage	VSHIF	DI1=1.8V, DVCC-OUT1F	0.35	0.45	0.55	V
DVCC Leak Current	IDLK	DVCC=9V, SVCC1,2=BATT=0V	-	0	5	μA
*PWM Amp Transfer Gain	GPWM	DI1=1.8V, DVCC=1.2V ~ 1.4V	1/60	1/50	1/40	1/KΩ
DC-DC CONVERTER						
ERROR AMP						
SVCC1 Pin Threshold Voltage	VS1TH	-	3.05	3.20	3.35	V
ERRO Pin Output Voltage H	VEOH	ERRI=0.7V, IO = -100μA	1.4	1.6	-	V
ERRO Pin Output Voltage L	VEOL	ERRI=1.3V, IO = 100μA	-	-	0.3	V
SHORT CIRCUIT PROTECTION						
SCP Pin Voltage	VSCP	ERRI=1.3V	-	0	0.1	V
SCP Pin Current 1	ISCP1	ERRI=0.7V	6	10	16	μA
SCP Pin Current 2	ISCP2	ERRI=1.3V, OFF=0V	12	20	32	μA
SCP Pin Current 3	ISCP3	ERRI=1.3V, BATT=9.5V	12	20	32	μA
*SCP Pin Impedance	RSCP	-	175	220	265	KΩ
SCP Pin Threshold Voltage	VSCPTH	ERRI=0.7V, COSC=470PF	1.10	1.20	1.30	V
Over Voltage Protection Detect	VOVP	OVP Voltage	9.5	10	10.5	V
TRANSISTOR DRIVING						
BDSW Pin Output Voltage 1H	VSW1H	BATT=COSC=1.5V =SVCC2=0V, 10mA	0.78	0.98	1.13	V
BDSW Pin Output Voltage 2H	VSW2H	COSC=0V, IO = -10mA, ERRI=0.7V SCP=0V	1.0	1.5	-	V
BDSW Pin Output Voltage 2L	VSW2L	CT=2V, IO=1-mA	-	0.3	0.45	V
BDSW Pin Oscillating Reequency1	fSW1	COSC=470pF, =SVCC2=0V	65	80	95	KHz
SW Pin Oscillating Reequency 2	fSW2	COSC=470pF, CLKIN=0V	60	70	82	KHz
BDSW Pin Oscillating Reequency 3	fSW3	COSC=470pF	-	88.2	-	KHz
*BDSW Pin Minimum Pulse Width	TSWMIN	COSC=470pF, ERRO=0.5 → 0.7V	0.01	-	0.6	μs
Pulse Duty Start	DSW1	COSC=470PF, SVSS1,SVCC2=0V	40	50	60	%
MAX. Pulse Duty at Self-Running	DSW2	COSC=470pF, ERRO=0.8V, CLKIN=0V	55	65	75	%
MAX. Pulse Duty at CLKIN Synchronization	DSW3	ERRO=0.8V, COSC=470pF	45	55	65	%

*Granted Design Value

Electrical Characteristics

(Ta=25°C, BATT=2.4V, SVCC1=SVCC2=3.2V, VREF=1.6V, ADPVCC=0V, fCLKIN=88.2KHz, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
DEAD TIME						
*DEDSET Pin Impedance	RDEDSET	-	52	65	78	KΩ
DEDSET Pin Output Voltage	VDEDSET	-	0.78	0.88	0.98	V
INTERFACE						
STOP Pin Threshold Voltage	VSTOPTH	ERRI=1.3V	2.0	-	-	V
STOP Pin Bias Current	ISTOP	OFF=0V	75	95	115	μA
START Pin On Threshold Voltage	VSTATH1	SVCC1,SVCC2=0V, COSC=2V	1.3	-	-	V
START Pin Off Threshold Voltage	VSTATH2	SVCC1,SVCC2=0V, COSC=2V	-	-	2.1	V
START Pin Bias Current	ISTART	START=0V	13	16	19	μA
CLKIN Pin Threshold Voltage H	VCLKINTH H	-	2.0	-	-	V
CLKIN Pin Threshold Voltage L	VCLKINTH L	-	-	-	0.8	V
CLKIN Pin Bias Current	ICLKIN	CLKIN=3.2V	-	-	10	μA
START CURCUIT						
Starter Switching Voltage	VSSV	SVCC1,SVCC2=0V → 3.2V START=0V	2.05	2.25	2.45	V
Starter Switching Hysteresis Width	VSSHS	START=0V	50	150	250	mV
Discharge Release Voltage	VDIS	-	1.55	1.75	1.95	V
RESET CIRCUIT						
*SVCC1 RESET Threshold Voltage Ratio	RRSTOTH	-	85	90	95	%
RESET Detection Hysteresis Width	VRSTHS	-	25	50	100	mV
RSTOUT Pin Output Voltage	VRSTO	IO=1mA, SVCC1,SVCC2=2.8V	-	-	0.5	V
RSTOUT Pin Pull Up Resistance	RRSTO	-	72	90	108	KΩ
RST Pin Output Voltage 1	VRST1	IO= -1mA, SVCC1,SVCC2=2.8V	2.0	-	2.4	V
RST Pin Output Voltage 2	VRST2	IO= -1mA, SVCC1,SVCC2=0V	2.0	-	2.4	V
*RST Pin Pull Up Resistance	RRST	-	77	95	113	KΩ

*Granted Design Value

Electrical Characteristics

(Ta=25°C, BATT=2.4V, SVCC1=SVCC2=3.2V, VREF=1.6V, ADPVCC=0V, fCLKIN=88.2KHz, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
OP-AMP						
Input Bias Current	IBIAS	IN(+)=1.6V	-	-	300	nA
Input Offset Voltage	VOFOP	IN(+)=1.6V	-5.5	0	5.5	mV
High Level Output Voltage	VOHOP	RL=OPEN	2.8	-	-	V
Low Level Output Voltage	VOLOP	RL=OPEN	-	-	0.2	V
Output Drive Current (Source)	ISOURCE	50Ω GND	-	-6.5	-3.0	mA
Output Drive Current (Sink)	ISINK	50Ω SVCC	0.4	0.7	-	mA
*Open Loop Voltage Gain	GVO	VIN= -75dB, F=1kHz	-	70	-	dB
*Slew Rate	SR	-	-	0.5	-	V/μs
BATTERY CHARGING CURCUIT						
CHGSET Pin Bias Voltage	VCHGSET	ADPVCC=4.5V, CHGSET=1.8kΩ	0.71	0.81	0.91	V
*CHGSET Pin Output Resistance	RCHGSET	ADPVCC=4.5V	0.75	0.95	1.20	KΩ
EMPSET Pin Leak Current 1	IEMPSET	ADPVCC=4.5V, CHGSET=OPEN	-	-	1.0	μA
EMPSET Pin Leak Current 2	IEMPSET	ADPVCC = 0.6V, CHGSET = 1.8kΩ	-	-	1.0	μA
EMPSET Pin Saturation Voltage	VEMPSET	ADPVCC = 4.5V, IO = 300mA, CHGSET = 0Ω	-	0.45	1.0	V
EMPTY DETECTION						
EMP Detection Voltge 1	VEMPTY1	VEMPSET = 0V	2.1	2.2	2.3	V
EMP Detection Voltge 2	VEMPTY2	IEMPSET = -2μA	1.7	1.8	1.9	V
EMP Detection Hysteresis Voltage 1	VEMHS1	VEMPSET = 0V	25	50	100	mV
EMP Detection Hysteresis Voltage 2	VEMHS2	IEMPSET = -2μA	25	50	100	mV
EMP Pin Output Voltage	VEMP	IO = 0.8mA, OVP = 1V	-	-	0.5	V
EMP Pin Output Leak Current	IEMPLK	OVP = 2.4V	-	-	1.0	μA
*OVP Pin Input Resistance	ROVP	VEMPSET = 0V	17	23	27	KΩ
OVP Pin Leak Current	IOVPLK	SVCC1 = SVCC2 = 0V, OVP = 4.5V	-	-	1.0	V
EMP_SET Pin Detection Voltage	VEMPSET	VEMPSET = BATT-EMPSET, OVP = 2V	1.5	-	-	V
EMP_SET Pin Detection Current	IEMPSET	EMPSET	-2	-	-	μA

*Granted Design Value

Application Information

1. BRAKE AND MUTE FUNCTION

- Channel 1 has a brake function and other channels have mute functions.
- When the BRAKE (pin23) is set to high level, both channel 1 outputs go low level. (Brake mode).
- When the MUTE2 (pin21) is set to high level, the channel 2 output is muted.
- When the MUTE34 (pin19) is set to high level, the channel 3 and 4 outputs are muted.

2. REFERENCE VOLTAGE(VREF) DROP MUTE

- When the voltage applied to VREF (pin16) is 1.0V or less (typical), the H-bridge driver outputs are set to high impedance.

3. THERMAL SHUTDOWN (TSD)

- If a junction temperature reaches 150°C (typical), the H-bridge driver output current is cut-off and the thermal shut down circuit has a hysteresis temperature of 25°C.

4. H-BRIDGE DRIVER (4-CHANNELS)

- The driver input resistance is 11KΩ(typical) for channel 1, 3 , and 4, and 7.5KΩ for channel 2. The gain can be set as the following fomula.

Channel	Gain	Unit
CH1 CH3 CH4	$Gv = 20 \log \left \frac{55K}{11K + R_{EXT}} \right $	dB
CH2	$Gv = 20 \log \left \frac{110K}{7.5K + R_{EXT}} \right $	dB

where, R_{EXT} is an externally connected input resistance.

5. SWITCHING REGULATED POWER SUPPLY DRIVE

- The power supply of H-bridge driver consists of DVCC(pin36) for output stage power supply and VSYS2 (pin15) for predriver power supply.

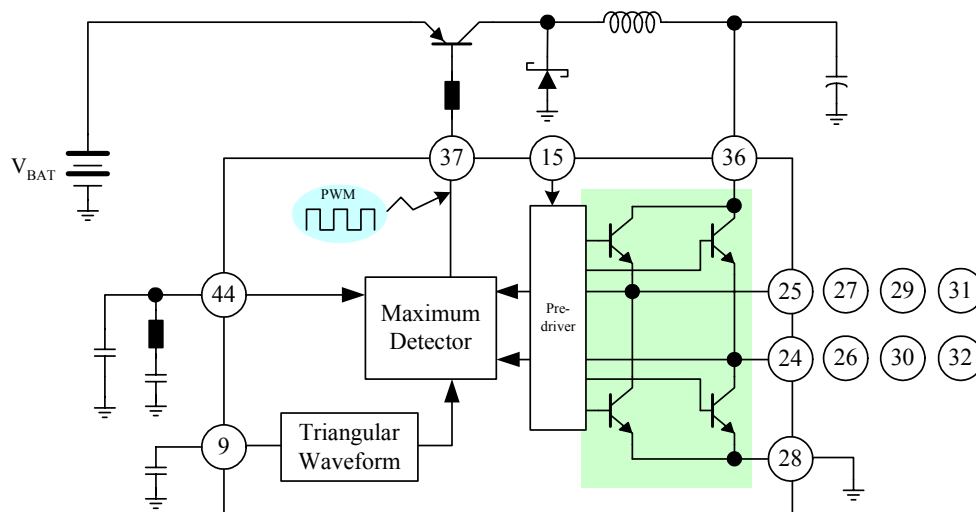


Figure 1. Switching Regulated Power Supply

- The switching off time can be set by the capacitor, CSCP as belows.

$$t_{SCP} = \frac{C_{SCP} \times V_{SCP}}{i_{SCP}} [\text{sec}]$$

$$\text{where, } V_{SCP} = 1.25[V], i_{SCP} = 10[\mu A]$$

6-4. Soft Start Function

- The soft start function operates when a capacitor is connected between DEDSET(pin4) and GND. Also, the maximum duty can be varied by connecting a resistor to pin4.

$$t_{SOFT} = C_{DEDSET} \times R$$

$$\text{Where, } R = 65[K\Omega]$$

7. POWER OFF FUNCTION

- When a 'L' signal is applied to STOP (pin40), SCP (pin8) is charged, and when the voltage reaches 1.25V (typical), the PWM comparator output, BDSW(pin5), is switched-off.
- The switching off time can be set by the capacitor, CSCP as belows.

$$t_{OFF} = \frac{C_{SCP} \times V_{TH}}{i_{OFF}} [\text{sec}]$$

$$\text{Where, } V_{TH} = 1.25[V], i_{OFF} = 20[\mu A]$$

8. BATTERY CHARGER AND MONITORING FUNCTION

8-1. Set to Battery Charging Current

- Battery charging circuit can operate independent of other blocks. The ADPVCC on pin41 is the power supply for charging circuit.
- The charging current, iCHG, which is derived from EMPSET (pin42), is set by the resistor between CHGSET (pin33) and GND
- The thermal shutdown circuit is provided, and when the chip temperature reaches to 150°C, the charging current, iCHG, is cut-off and it has the temperature hysteresis of about 30°C.

8-2. Over Voltage Protection

- When the voltage applied to the OVP (pin1) reaches 9.7V, SCP (pin8) is charged, and when the voltage reaches 1.25V (typical), the PWM comparator output, BDSW(pin5), is switched-off.
- The switching off time can be set by the capacitor, CSCP as belows.

$$t_{OVP} = \frac{C_{SCP} \times V_{TH}}{i_{OVP}} [\text{sec}]$$

$$\text{Where, } V_{TH} = 1.25[V], i_{OVP} = 20[\mu A]$$

8-3. Empty Detecting Circuit

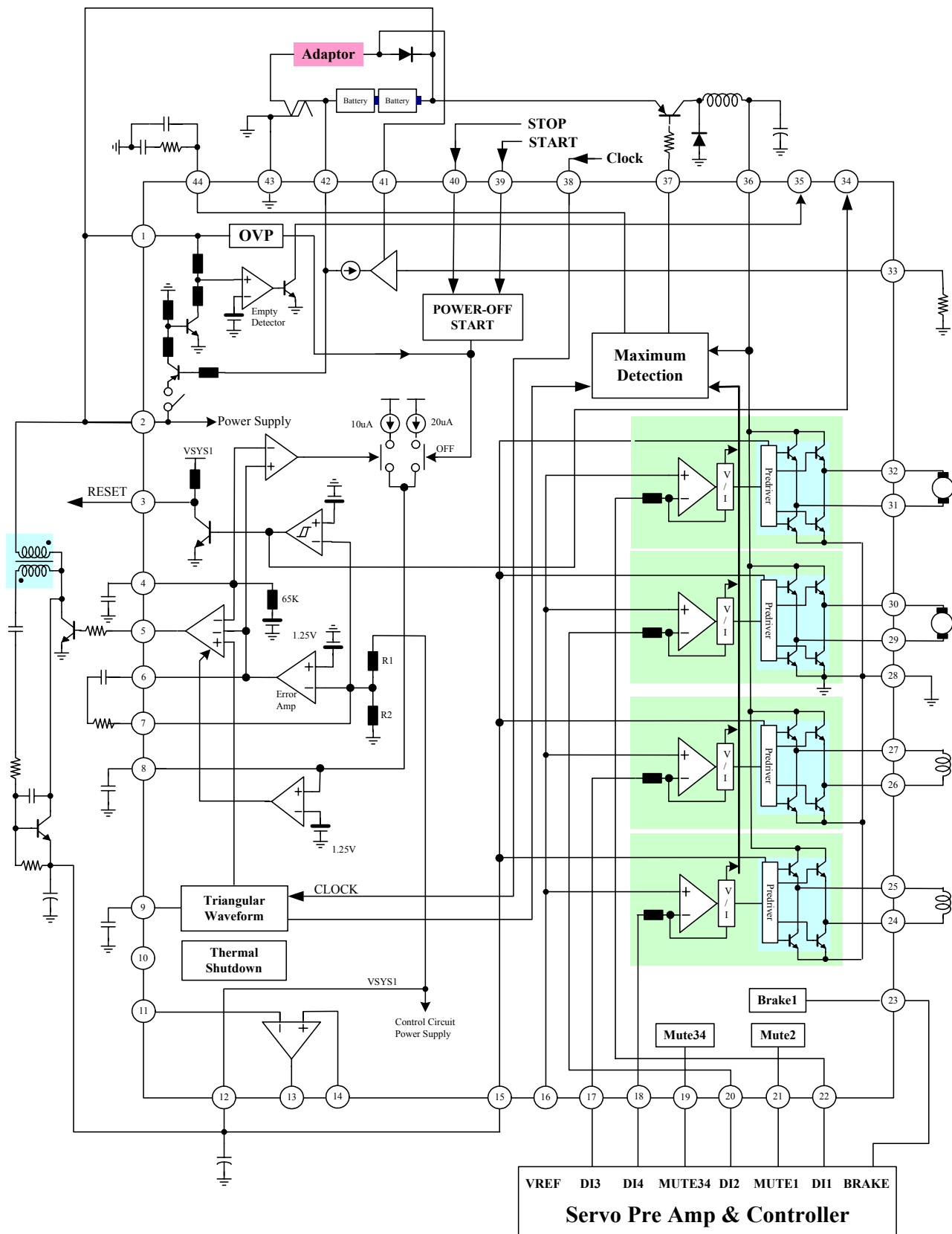
- when the voltage applied to the OVP (pin1) falls below the detector voltage, EMP (pin35) turns from high level to low level (open collector output).
- The detector voltage has 50mV of hysteresis to prevent noise variation.
- EMPSEL (pin42) is to switch the detection voltage as shown below.
- .

EMPSET	Detect Voltage	Hysteresis	Mode
LOW	2.2V	50mV	Battery Mode
HIGH-Z	1.8V	50mV	Adapter Mode

Preliminary Specification

Typical Performance Characteristics

Preliminary Specification



Application Circuits

Preliminary Specification

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.