

ESDR6V1-27FUx

Application Specific Discretes A.S.D.™

ESD PROTECTION MONOLITHIC 9-BIT WIDE TRANSIL[™] ARRAY

MAIN APPLICATIONS

Where high level protection in ESD sensitive equipment is required, such as:

- Computers
- Printers
- Business machines
- Communication systems

DESCRIPTION

The ESDR6V1-27FUx is a monolithic array designed to provide a 9-line undershoot and overshoot clamping function.

It includes an ESD protection circuitry which prevents the protected device from destruction when subjected to ESD surges up to 15 kV. The first Transil diode suppresses coarsely the ESD transient, while the second stage finely clamps the remaining overvoltage.

The layout of the ESDR6V1-27FUx device allows immediate and easy implementation on high density board.

FEATURES

- 9-line undershoot or overshoot clamping functions.
- Breakdown voltage: V_{BR} = 6.1V min.
- Low clamping voltage : due to internal structure
- Forward voltage V_F = 1.25V max. @ I_F=200mA
- Low capacitance: C =130pF @ 0V (per diode).
- 200W peak pulse power (8/20µs)

BENEFITS

- EnhancedESD protection for the protected device
- High flexibility in the design of high density boards
- Board space saving
- Four points structure, avoiding all ESD effects at the outputs
- High immunity against latch-up phenomena

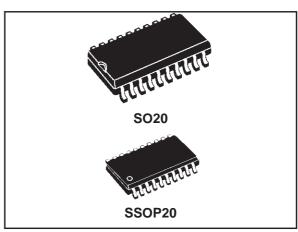
COMPLIES WITH THE FOLLOWING STANDARDS:

- ESD standard:

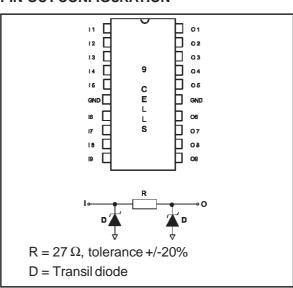
. IEC 1000-4-2 15kV (air discharge) level4 8kV (contact discharge)

- MIL STD 883C Method 3015-6 25kV class 3 (human body test)

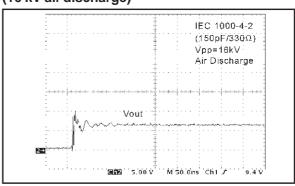
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PIN-OUT CONFIGURATION



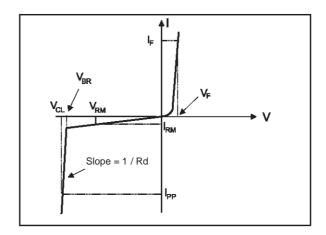
Typical response to IEC1000-4-2 (16 kV air discharge)



ABSOLUTE MAXIMUM RATINGS $(T_{amb} = 25^{\circ}C)$

Symbol	Parameter	Value	Unit
VPP	Maximum electrostatic discharge in following measurement conditions: MIL STD 883C - METHOD 3015-6 IEC1000-4-2 - air discharge IEC1000-4-2 - contact discharge	25 16 9	kV
P _{PP}	Peak pulse power (8/20μs)	200	W
T _{stg} T _j	Storage temperature range Junction temperature	- 55 to + 150 150	ို ပိ
Top	Operating temperature range	- 40 to + 85	°C

Symbol	Parameter		
V _{RM}	Stand-offvoltage		
V_{BR}	Breakdownvoltage		
V _C L	Clamping voltage		
V _F	Forward voltage drop		
С	Capacitance		
Rd	Dynamic impedance		
I _{RM}	Leakage current		
lpp	Peak pulse current		



Symbol	Test conditions	Min.	Тур.	Max.	Unit
I _{RM}	V _{RM} = 5.25 V, between any I/O pin and GND			20	μΑ
V_{BR}	I _R = 1 mA, between any I/O pin and GND			7.2	V
VF	IF = 200 mA, between any I/O pin and GND			1.25	V
Rd	$I_{PP} = 15 \text{ A}, t_p = 2.5 \mu s \text{ (note 2)}$		0.3		Ω
С	0V bias V _{RMS} = 30mV F = 1MHz (note 3)		130		pF

Note 1: V_{CL} corresponds to the voltage level seen at the output pin Note 2: Rd is given per diode Note 3: C is given per diode

Fig 1: Peak power dissipation versus initial junction temperature.

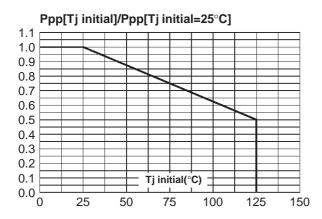


Fig 3: Clamping voltage versus peak pulse current (Tj initial=25°C). Rectangular waveform: $tp = 2.5\mu s$

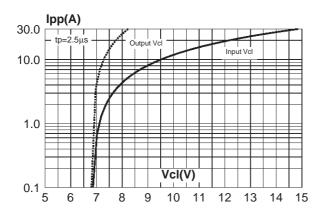


Fig 5: Relative variation of leakage current versus junction temperature (typical values).

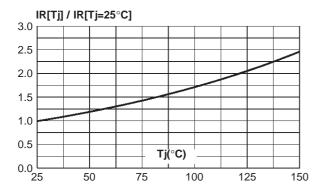


Fig 2: Peak pulse power versus exponential pulse duration (Tj initial= 25° C).

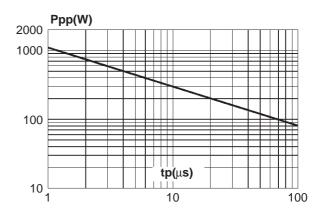


Fig 4: Input capacitance versus reverse applied voltage (typical values).

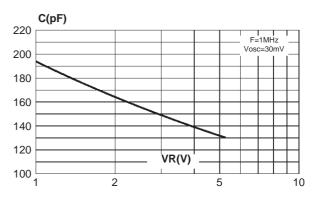
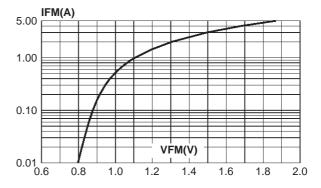


Fig 6: Peak forward voltage drop versus peak forward current (typical values). Rectangular waveform: tp = 2.5μs



ESD protection by the ESDR6V1-27FUx

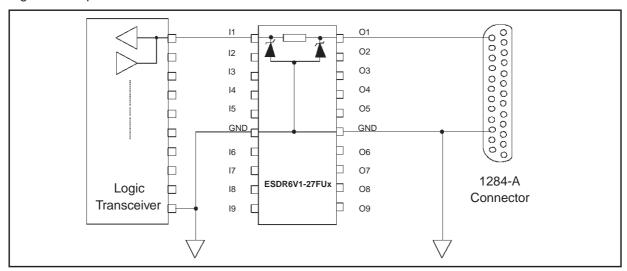
Electrostatic discharge (ESD) is a major cause of failure in electronic systems.

Transient Voltage Suppressors are an ideal choice for ESD protection. They are capable of clamping the incoming transient to a low enough level such that damage to the protected semiconductor is prevented.

Surface mount TVS arrays offer the best choice for minimal lead inductance.

They serve as parallel protection elements, connected between the signal line to ground. As the transient rises above the operating voltage of the device, the TVS array becomes a low impedance path diverting the transient current to ground.

Fig. 7: Example of connection for one cell of the ESDR6V1-27FUx



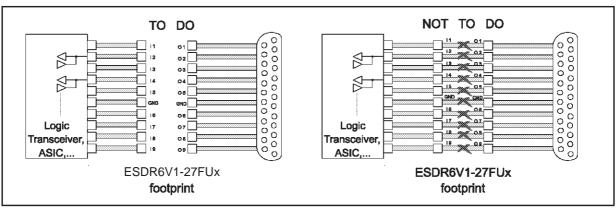
The ESDR6V1-27FUx array is the ideal board level protection of ESD sensitive semiconductor components. It provides best efficiency when using separated inputs and outputs, in the so called 4-points structure.

Circuit Board Layout

Circuit board layout is a critical design step in the suppression of ESD induced transients. The following guidelines are recommended:

- The ESDR6V1-27FUx should be placed as near as possible to the input terminals or connectors.
- The path length between the ESD suppressor and the protected line should be minimized.
- All conductive loops, including power and ground loops should be minimized.
- The ESD transient return path to ground should be kept as short as possible.
- Ground planes should be used whenever possible.

Fig. 8: Recommended PCB layout to benefit from 4-point structure



ESDR6V1-27FUx

TECHNICAL INFORMATION

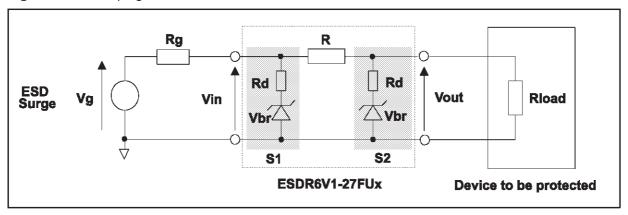
ESD PROTECTION

The ESDR6V1-27FUx is particularly optimized to perform high level ESD protection. The clamping voltage is given by the formula:

$$V_{CL} = V_{br} + R_{d} \cdot I_{PP}$$

The protection function is splitted in 2 stages. As shown in figure A1, the ESD strike is clamped by the first stage S1 and then its remaining overvoltage is applied to the second stage through the resistor R. Such a configuration makes the output voltage very low at the Vout level.

Fig. A1: ESD clamping behavior



To determine the remaining voltages at both Vin and Vout stages, we give the typical dynamic resistance value Rd. Considering that: R>>Rd, Rg>>Rd and Rload>>Rd, the voltages are given by the following formulas:

$$Vin = \frac{R_g.V_{br} + R_{d.}V_g}{R_g}$$

$$Vout = \frac{R.V_{br} + R_{d}.Vin}{R}$$

The result of the calculation made for V_G= 8kV, Rg= 330 Ω (IEC1000-4-2 standard), V_{br}=6.6V, Rd=0.3 Ω and R=27 Ω is:

$$Vin = 13.87V$$

Vout = 6.75 V

This confirms the very low remaining voltage across the device to be protected. It is also important to note that in this approximation the parasitic inductance effect was not taken into account. This could be few tenths of volts during few ns at the Vin side. This parasitic effect is not present at the Vout side because the current involved after the resistance R is low.

LATCH-UP PHENOMENA

The early aging and destruction of IC's is often due to latch-up phenomena which is principally induced by dV/dt. Thanks to its RC structure, the ESDR6V1-27FUx provides a high immunity to latch-up by integration of fast edges. (See the response of ESDR6V1-27FUx to a 1ns edge on Fig. A3)

The measurements performed as described below show very clearly the high efficiency of the ESD protection:

- no influence of the parasitic inductances on Vout stage
- Vout clamping voltage very close to Vbr

Fig. A2: Measurement conditions

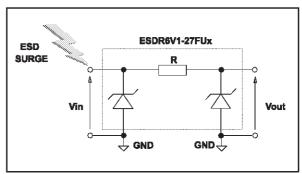
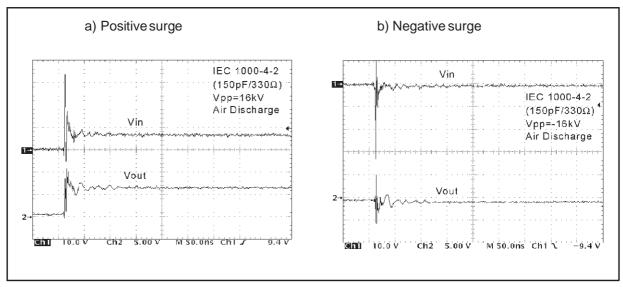


Fig. A3: Remaining voltage at both stages S1 (Vin) and S2 (Vout) during ESD surge



It should be noted that the ESDR6V1-27FUx is not only active for positive ESD surges but also for negative ones. For this kind of disturbance, it clamps close to ground voltage as shown in Fig A3b.

NOTE: DYNAMIC RESISTANCE MEASUREMENT

Generally the PCB designers need to calculate easily the clamping voltage VCL. This is why we give the dynamic resistance in addition to the classical parameters. Figure A4 illustrates the current waveform used to measure the Rd.

As the value of the dynamic resistance remains stable for a surge duration lower than $20\mu s$, the $2.5\mu s$ rectangular surge is well adapted. In addition both rise and fall times are optimized to avoid any parasitic phenomenon during the measurement of Rd.

2 μs 2.5 μs 2.5 μs

Fig. A4: Rd measurement current wave

FREQUENCY BEHAVIOR

In addition to the ESD protection, the ESDR6V1-27FUx offers an EMI / RFI filtering function thanks to its Pi-filter structure. This low-pass filter is characterized by the following parameters:

- Cut-off frequency- Insertion loss- High frequency rejection- 18dBm

Fig. A5: ESDR6V1-27FUx filtering response curves

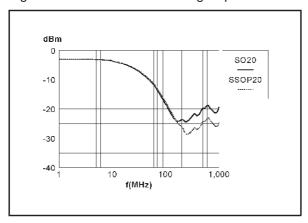
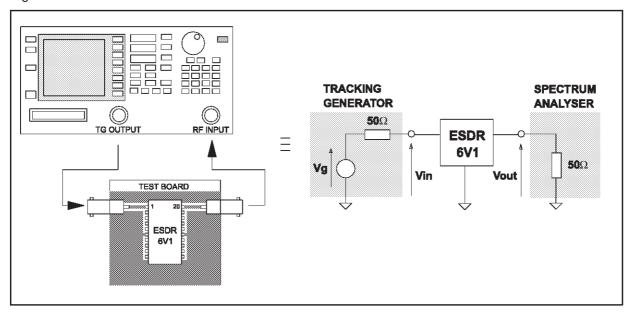


Figure A5 gives these parameters, in particular the signal rejection at the 900MHz GSM frequency is measured at about -21dBm (SO20) and -26dBm (SSOP20), while the attenuation for FM broadcast range (around 100MHz) is better than -17dBm for both SO20 and SSOP20.

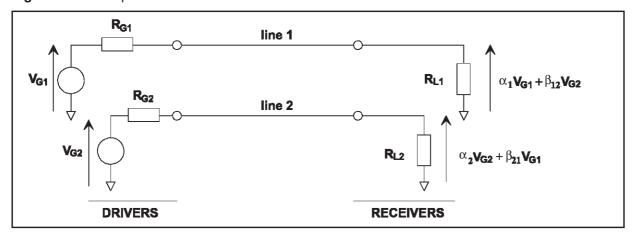
Fig. A6: Measurement conditions



CROSSTALK BEHAVIOR

1- Crosstalk phenomena

Fig. A7: Crosstalk phenomena



The crosstalk phenomena are due to the coupling between 2 lines. The coupling factor ($\beta12$ or $\beta21$) increases when the gap across lines decreases, particularly in silicon dice. In the example above the expected signal on load RL2 is $\alpha2VG2$, in fact the real voltage at this point has got an extra value $\beta21VG1$. This part of the VG1 signal represents the effect of the crosstalk phenomenon of the line 1 on the line 2. This phenomenon has to be taken into account when the drivers impose fast digital data or high frequency analog signals in the disturbing line. The perturbed line will be more affected if it works with low voltage signal or high load impedance (few $k\Omega$). The following chapters give the value of both digital and analog crosstalk.

2- Digital Crosstalk

Fig. A8: Digital crosstalk measurements

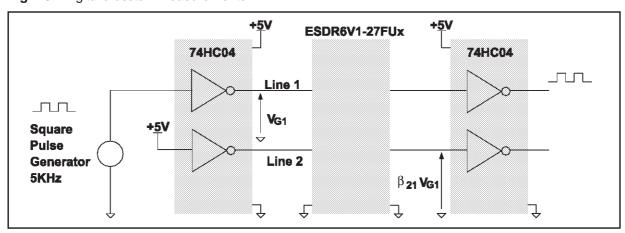


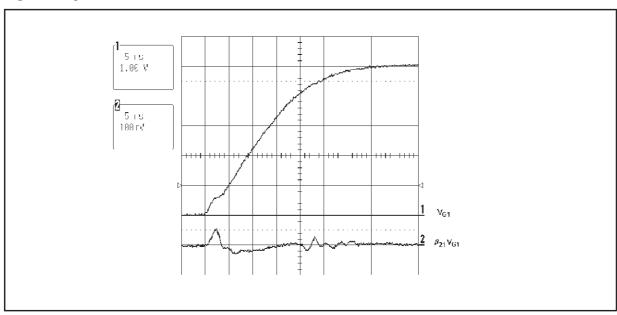
Figure A8 shows the measurement circuit used to quantify the crosstalk effect in a classical digital application.

Figure A9 shows that in the case of a signal from 0 to 5V with a rise time of a few tenths of ns, the impact on the disturbed line is less than 100mV peak to peak. No data disturbance is noted on the concerned line. The same results are obtained with falling edges.

Note: The measurements have been performed in the worst case i.e. on two adjacent cells (1/20 & 2/19).

ESDR6V1-27FUx

Fig. A9: Digital crosstalk results



3- Analog Crosstalk

Fig. A10: Analog crosstalk measurements

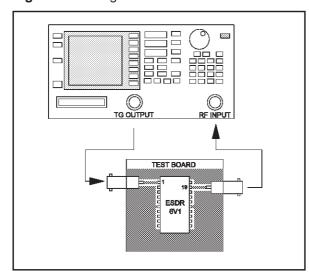


Fig. A11: Typical analog crosstalk results

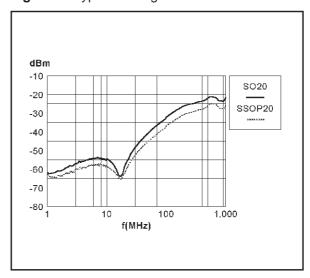


Figure A10 gives the measurement circuit for the analog application. In figure A11, the curves show the effect of cell 1/20 on cell 2/19, no difference is found with other couples of adjacent cells. In usual frequency range of analog signals (up to 100MHz) the effect on disturbed line is less than -32 dBm for SO20 package and -37dBm for SSOP20 package.

4- PSpice model

Fig. A12: PSpice model of one ESDR6V1-27FUx cell

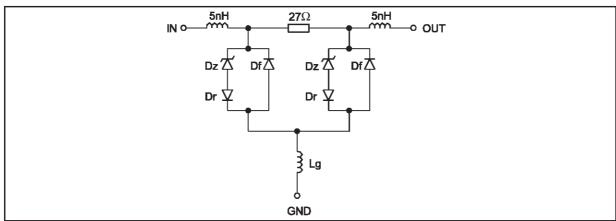


Figure A12 shows the PSpice model of one cell of the ESDR6V1-27FUx. In this model, the diodes are defined by the following PSpice parameters:

	Dz	Df	Dr	
BV	5.6	1000	1000	
Cjo	130p	130p	1p	
IBV	1m	100u	100u	
IKF	1000	0	1000	
IS	10E-21	2.0861E-21	10E-15	
ISR	1p	1n	100p	
N	1	1	0.6	
M	0.3333	0.3333	0.3333	
RS	0.3	0.3	1m	
VJ	0.6	0.6	0.6	
TT	1u	1u	1n	

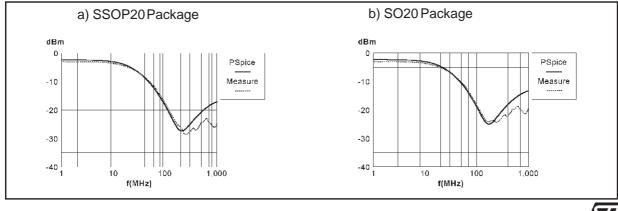
Note: This simulation model is given for an ambient temperature of 27°C.

The value of Lg is depending on the package:

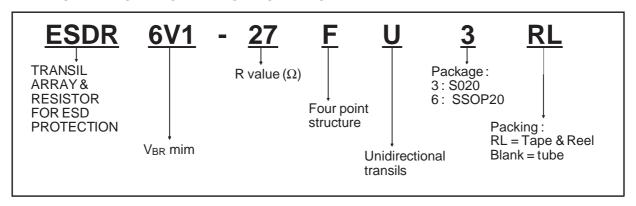
- SSOP20 --> Lg=0.7nH
- SO20 --> Lg=1.4nH

The comparison between the PSpice simulation and the measured frequency response is given in fig A13a & A13b. This shows that the PSpice model is very close to the product behavior.

Fig. A13: Comparison between PSpice simulation and measured frequency response

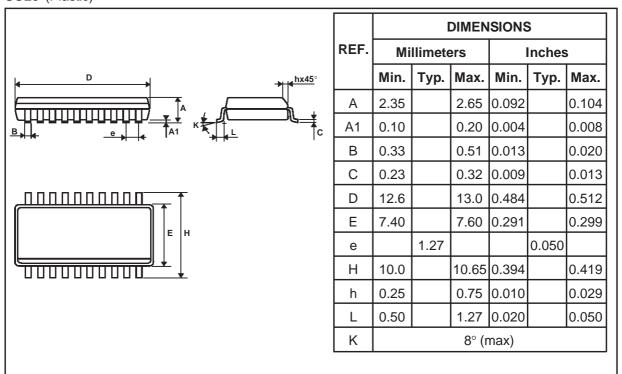


PART NUMBERING AND ORDERING INFORMATION



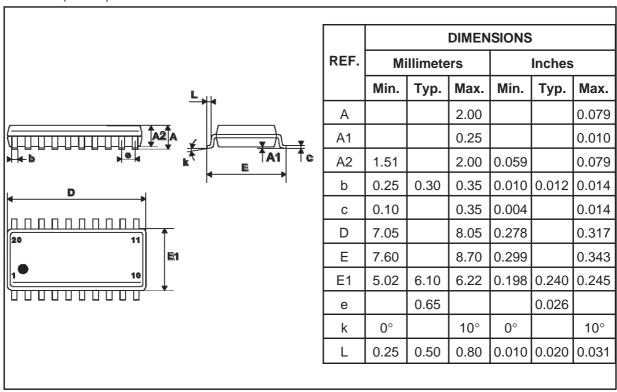
PACKAGE MECHANICAL DATA

SO20 (Plastic)



PACKAGE MECHANICAL DATA

SSOP20 (Plastic)



ORDERING CODE

Order code	Marking	Package	Weight	Delivery mode	Base qty (pcs)
ESDR6V1-27FU3	ESDR6V1-27	SO20	0.52g	Tube	50
ESDR6V1-27FU3RL	ESDR6V1-27	SO20	0.52g	Tape & reel	1000
ESDR6V1-27FU6	ESDR6V1-27	SSOP20	0.18g	Tube	66
ESDR6V1-27FU6RL	ESDR6V1-27	SSOP20	0.18g	Tape & reel	2000

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