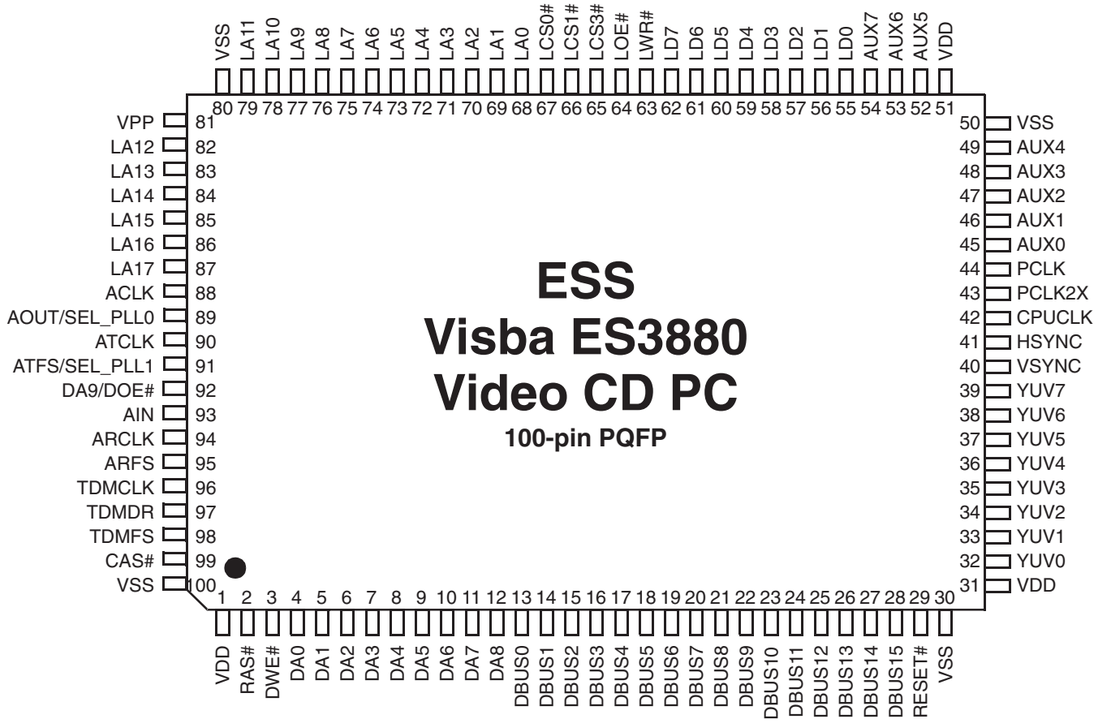
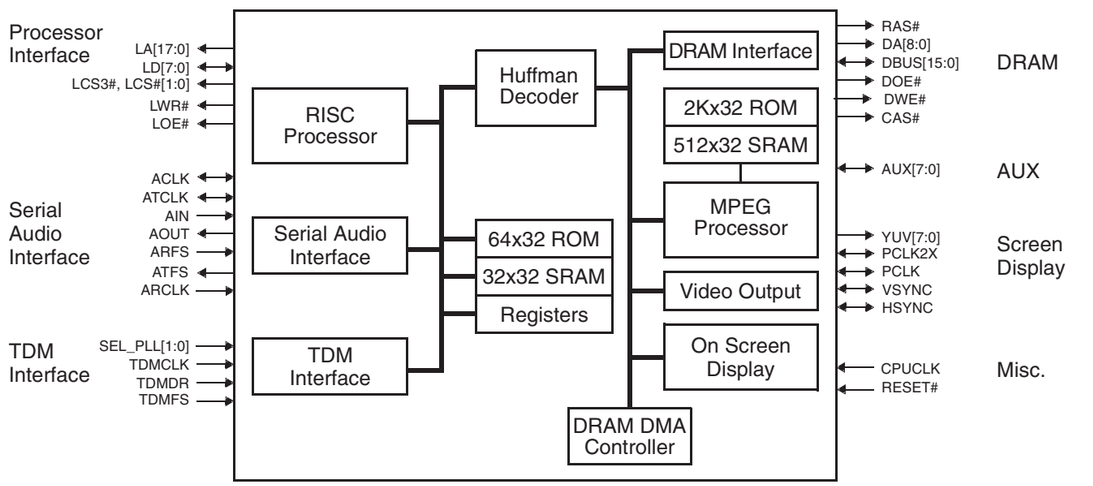
ES3880 VIDEO CD PROCESSOR CHIP





Visba Video CD PC Block Diagram

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VISBA VIDEO PC PROCESSOR CHIP PIN DESCRIPTION

Name	Number	I/O	Definition
VDD	1, 31, 51	I	Voltage supply for 3.3 V.
RAS#	2	O	DRAM row address strobe (active low).
DWE#	3	O	DRAM write enable (active low).
DA[8:0]	12:4	O	DRAM multiplexed row and column address bus.
DBUS[15:0]	28:13	I/O	DRAM data bus.
RESET#	29	I	System reset (active low).
VSS	30, 50, 80, 100	I	Ground.
YUV[7:0]	39:32	O	Y is luminance, UV are chrominance data bus for screen video interface. YUV[7:0] for 8-bit YUV mode.
VSYNC	40	I/O	Vertical sync for screen video interface, programmable for rising or falling edge.
HSYNC	41	I/O	Horizontal sync for screen video interface, programmable for rising or falling edge.
CPUCLK	42	I	RISC and system clock input. CPUCLK is used only if SEL_PLL[1:0] = 00.
PCLK2X	43	I/O	Pixel clock; two times the actual pixel clock for screen video interface.
PCLK	44	I/O	Pixel clock qualifier in for screen video interface.
AUX[7:0]	54, 52, 53, 49:45	I/O	Auxiliary control pins (AUX0 and AUX1 are open collectors).
LD[7:0]	62:55	I/O	RISC interface data bus.
LWR#	63	O	RISC interface write enable (active low).
LOE#	64	O	RISC interface output enable (active low).
LCS[3,1,0]#	65,66,67	O	RISC interface chip select (active low).
LA[17:0]	87:82, 79:68	O	RISC interface address bus.
VPP	81	I	Digital supply voltage for 5 V.
ACLK	88	I/O	Master clock for external audio DAC (8.192 MHz, 11.2896 MHz, 12.288 MHz, 16.9344 MHz, and 18.432 MHz).
AOUT/ SEL_PLL0	89	O	Dual-purpose pin. AOUT is the audio interface serial data output
		I	Pins SEL_PLL[1:0] select phase-lock loop (PLL) clock frequency CPUCLK for the Visba: 00 = bypass PLL. 01 = 54 MHz PLL. 10 = 67.5 MHz PLL. 11 = 81 MHz PLL.
ATCLK	90	I/O	Audio transmit bit clock.
ATFS/ SEL_PLL1	91	O	Dual-purpose pin. ATFS is the audio interface transmit frame sync.
		I	Pins SEL_PLL[1:0] select phase-lock loop (PLL) clock frequency CPUCLK for the Visba. See the SEL_PLL0 pin above for the settings.
DA9/DOE#	92	O	Dual purpose pin: DRAM output enable (active low)/DRAM multiplexed row and column address bus.
AIN	93	I	Audio interface serial data input.
ARCLK	94	I	Audio receive bit clock.
ARFS	95	I	Audio interface receive frame sync.
TDMCLK	96	I	TDM interface serial clock.
TDMDR	97	I	TDM interface serial data receive.
TDMFS	98	I	TDM interface frame sync.
CAS#	99	O	DRAM column address strobe bank 0 (active low).

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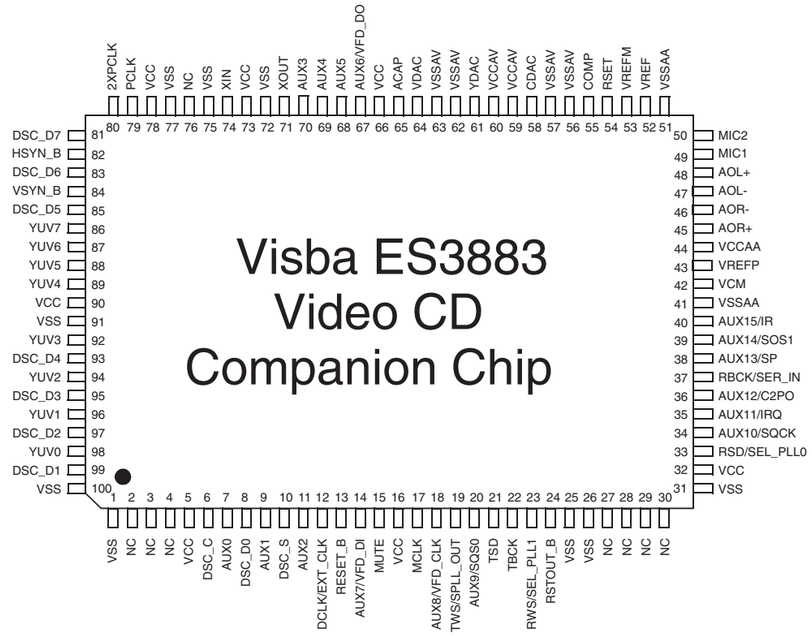
ES3883 VIDEO CD COMPANION CHIP



PIN DESCRIPTION

Name	Number	I/O	Definition
VSS	1,25:26,31,72,75,77,91,100	I	Ground.
VCC	5,16,32,66,73,78,90	I	Voltage supply, 5 V.
DSC_C	6	I	Clock for programming to access internal registers.
AUX0	7	I/O	Servo Forward or Control Pin.
AUX1	9	I/O	Servo Reverse or Control Pin.
AUX2	11	I/O	Servo LDON or Control Pin.
AUX3	70	I/O	Servo CW/Limit or Control Pin.
AUX4	69	I/O	Servo CCW/Close or Control Pin.
AUX5	68	I/O	Servo Data or Control Pin.
AUX6	67	I/O	Servo XLAT or Control Pin/VFD_DO.
AUX7	14	I/O	Servo BRKM/Sense or Control Pin/VFD_DI.
AUX8	18	I/O	Servo Mute/Open or Control Pin/VFD_CLK.
AUX9	20	I/O	Servo SQS0 or Control Pin.
AUX10	34	I/O	Servo SQCK or Control Pin.
AUX11	35	I/O	3880 IRQ or Interrupt Output or Control Pin.
AUX12	36	I/O	CD C2PO or Interrupt Input or Control Pin.
AUX13	38	I/O	Serial Interrupt/CD-Mute or Control Pin.
AUX14	39	I/O	Servo SCOR (S0S1) or Interrupt Input or Control Pin.
AUX15	40	I/O	Interrupt Input or Control Pin.
DSC_D[7:0]	81,83,85,93,95,97,99,8	I/O	Data for programming to access internal registers.
DSC_S	10	I	Strobe for programming to access internal registers.
DCLK	12	O	Dual-purpose pin DCLK is the MPEG decoder clock.
EXT_CLK		I	EXT_CLK is the external clock EXT_CLK is an input during bypass PLL mode.
RESET_B	13	I	Video reset (active-low).
MUTE	15	O	Audio mute.
MCLK	17	I	Audio master clock.
TWS	19	I	Dual-purpose pin TWS is the transmit audio frame sync.
SPLL_OUT		O	SPLL_OUT is the select PLL output.
RWS	23	O	Dual-purpose pin RWS is the receive audio frame sync.
SEL_PLL1		I	Pins SEL_PLL[1:0] select the PLL clock frequency for the DCLK output. SEL_PLL1 SEL_PLL0 DCLK 0 0 Bypass PLL (input mode) 0 1 27 MHz (output mode) 1 0 32.4 MHz (output mode) 1 1 40.5 MHz (output mode)
RSTOUT_B	24	O	Reset output (active-low).
NC	2:4,27:30,76		No connect. Do not connect to these pins.
RSD	33	O	Dual-purpose pin. RSD is the receive audio data input.
SEL_PLL0		I	SEL_PLL0 along with SEL_PLL1 select the PLL clock frequency for the DCLK output. See the table for pin number 23.
RBCK	37	O	Dual-purpose pin. RBCK is the receive audio bit clock.
SER_IN		I	SER_IN is the serial input DSC mode. 0 - Parallel DSC mode. 1 - Serial DSC mode.
VSSAA	41,51	I	Audio Analog Ground.
VCM	42	I	ADC Common Mode Reference (CMR) buffer output. CMR is approximately 2.25 V. Bypass to analog ground with 47 mF electrolytic in parallel with 0.1 mF.
VREFP	43	I	DAC and ADC maximum reference. Bypass to VCMR with 10 mF in parallel with 0.1 mF.
VCCAA	44	I	Analog VCC, 5 V.
AOR+, AOR-	45:46	O	Right channel output.
AOL-, AOL+	47:48	O	Left channel output.
MIC1	49	I	Microphone input 1.
MIC2	50	I	Microphone input 2.
VREF	52	I	Internal resistor divider generates Common Mode Reference (CMR) voltage. Bypass to analog ground with 0.1 mF.
VREFM	53	I	DAC and ADC minimum reference. Bypass to VCMR with 10 mF in parallel with 0.1 mF.
RSET	54	I	Full scale DAC current adjustment.
COMP	55	I	Compensation pin.
VSSAV	56:57,62:63	I	Video Analog Ground
CDAC	58	O	Modulated chrominance output.
VCCAV	59,60	I	Video VCC, 5 V
YDAC	61	O	Y luminance data bus for screen video port.
VDAC	64	O	Composite video output.
ACAP	65	I	Audio CAP
XOUT	71	O	Crystal output.
XIN	74	I	27 MHz crystal input.
PCLK	79	I/O	13.5 MHz pixel clock.
2XPCLK	80	I/O	27 MHz (2 times pixel clock).
HSYN_B	82	O	Horizontal sync (active-low).
VSYN_B	84	O	Vertical sync (active-low).
YUV[7:0]	86:89,92,94,96,98	I	YUV data bus for screen video port.