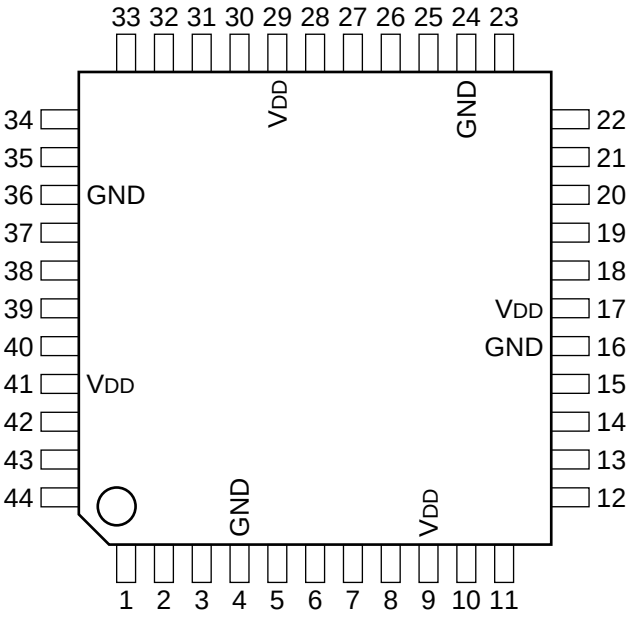
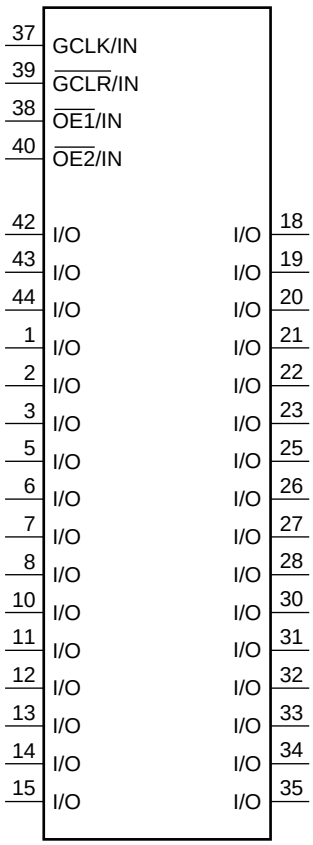
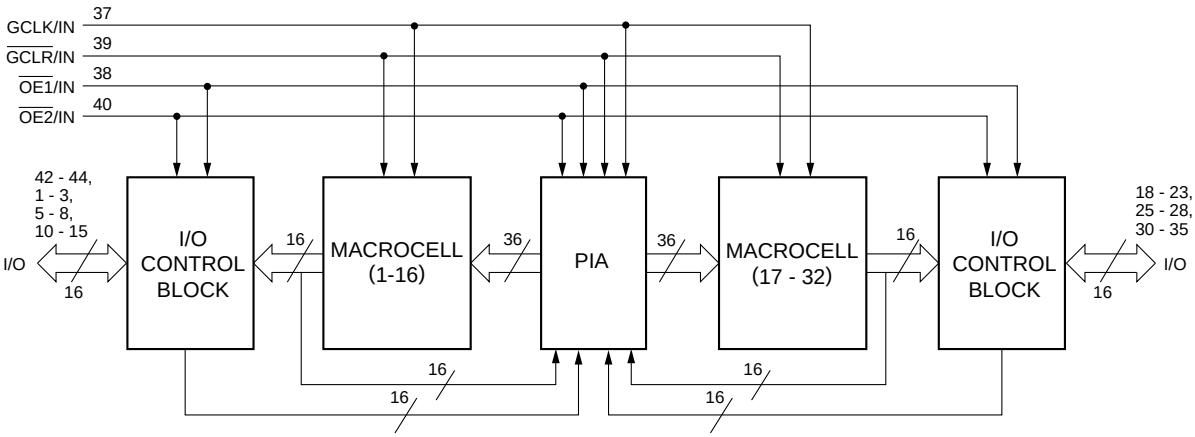
C-MOS ERASABLE PLD

—TOP VIEW—





PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	I/O	I/O	12	I/O	I/O	23	I/O	I/O	34	I/O	I/O
2	I/O	I/O	13	I/O	I/O	24	—	GND	35	I/O	I/O
3	I/O	I/O	14	I/O	I/O	25	I/O	I/O	36	—	GND
4	—	GND	15	I/O	I/O	26	I/O	I/O	37	I	GCLK/IN
5	I/O	I/O	16	—	GND	27	I/O	I/O	38	I	$\overline{OE1}$/IN
6	I/O	I/O	17	—	V_{DD}	28	I/O	I/O	39	I	$\overline{GCLR}$/IN
7	I/O	I/O	18	I/O	I/O	29	—	V_{DD}	40	I	$\overline{OE2}$/IN
8	I/O	I/O	19	I/O	I/O	30	I/O	I/O	41	—	V_{DD}
9	—	V_{DD}	20	I/O	I/O	31	I/O	I/O	42	I/O	I/O
10	I/O	I/O	21	I/O	I/O	32	I/O	I/O	43	I/O	I/O
11	I/O	I/O	22	I/O	I/O	33	I/O	I/O	44	I/O	I/O



* ABOVE DIAGRAM SHOWS CONDITIONS BEFORE PROGRAMMING