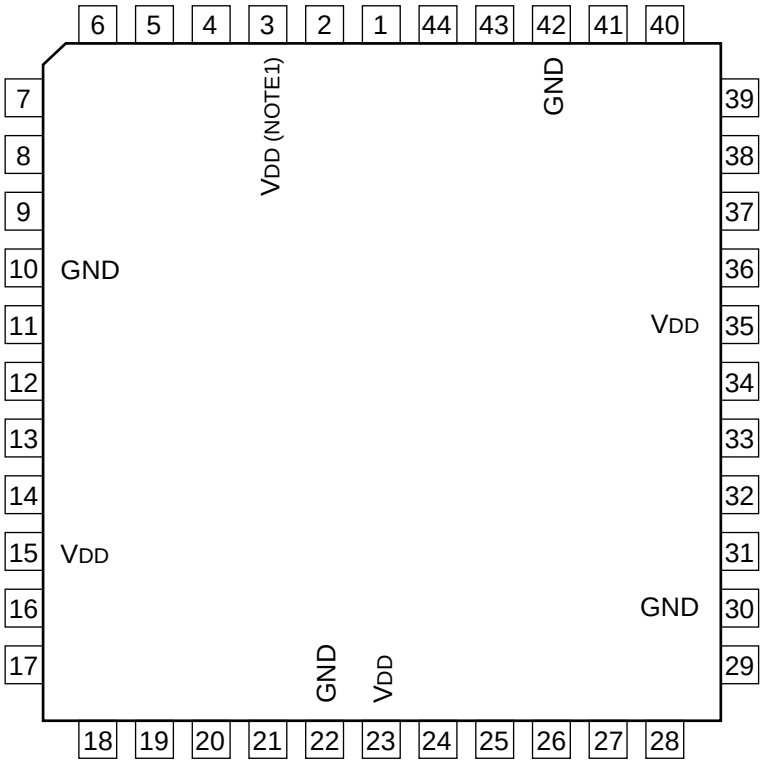
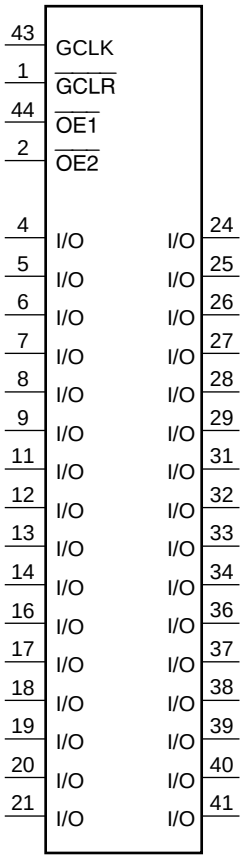
C-MOS ERASABLE PLD

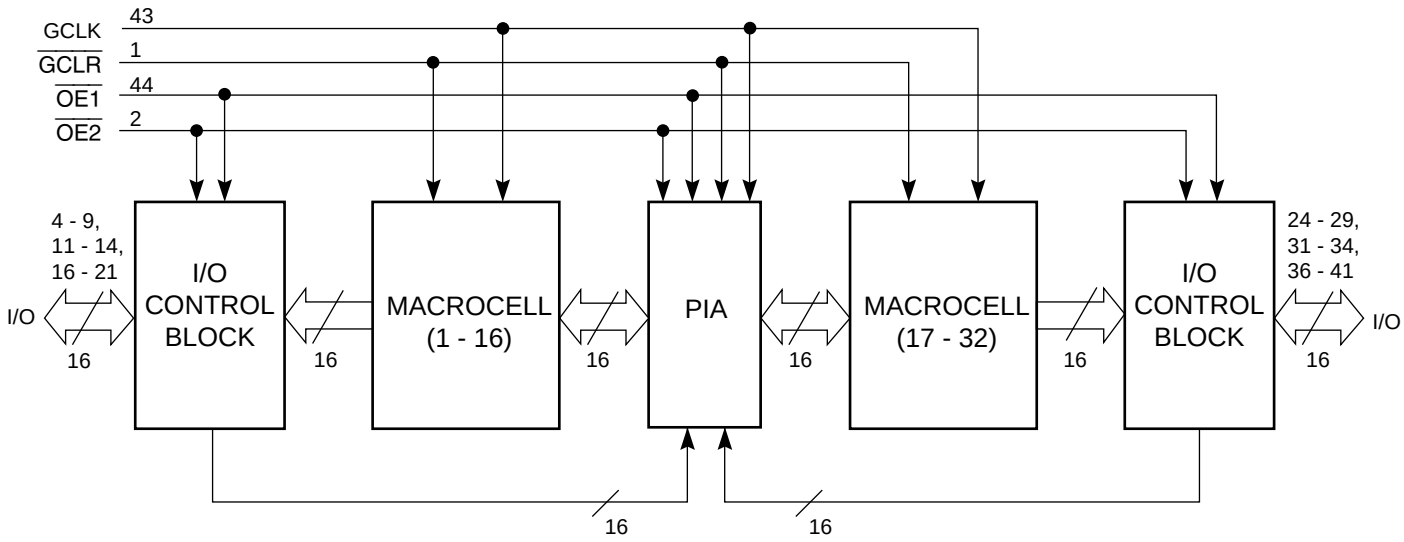
—TOP VIEW—





PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	I	$\overline{\text{GCLR}}$	12	I/O	I/O	23	—	V_{DD}	34	I/O	I/O
2	I	$\overline{\text{OE2}}$	13	I/O	I/O	24	I/O	I/O	35	—	V_{DD}
3	—	V_{DD} (NOTE1)	14	I/O	I/O	25	I/O	I/O	36	I/O	I/O
4	I/O	I/O	15	—	V_{DD}	26	I/O	I/O	37	I/O	I/O
5	I/O	I/O	16	I/O	I/O	27	I/O	I/O	38	I/O	I/O
6	I/O	I/O	17	I/O	I/O	28	I/O	I/O	39	I/O	I/O
7	I/O	I/O	18	I/O	I/O	29	I/O	I/O	40	I/O	I/O
8	I/O	I/O	19	I/O	I/O	30	I/O	I/O	41	I/O	I/O
9	I/O	I/O	20	I/O	I/O	31	—	GND	42	—	GND
10	—	GND	21	I/O	I/O	32	I/O	I/O	43	I	GCLK
11	I/O	I/O	22	—	GND	33	I/O	I/O	44	I	$\overline{\text{OE1}}$

NOTE1 : IN THE CASE OF EPM7032V, THIS PIN IS PDn (POWER DOWN CONTROL INPUT)



✻ABOVE DIAGRAM SHOWS CONDITIONS BEFORE PROGRAMMING