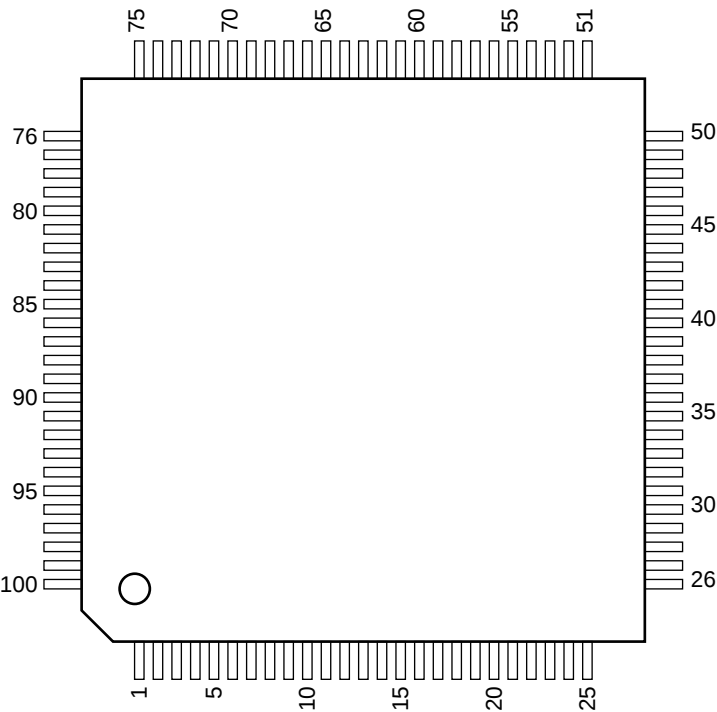


AUDIO TIMING GENERATOR AND MULTIPLEXER
—TOP VIEW—



PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	O	CONF DONE	26	I	RESERVED	51	—	IC	76	O	ADD1
2	—	GND	27	O	24 MHz	52	—	GND	77	—	IC
3	—	IC	28	—	IC	53	—	GND	78	O	ADD0
4	I	DATA1	29	—	IC	54	—	IC	79	—	IC
5	I	DATA0	30	—	GND	55	O	ADD15	80	—	GND
6	—	Vcc	31	O	CNT2048	56	—	Vcc	81	—	IC
7	I	EXTCMD11	32	—	IC	57	O	ADD14	82	O	DA LRCK
8	I	BIDT	33	—	IC	58	O	ADD13	83	—	IC
9	O	AD LRCK	34	—	TEST	59	O	ADD12	84	O	DT
10	I	24 MHz	35	—	IC	60	O	ADD11	85	—	IC
11	I	AD2DT	36	—	IC	61	O	ADD10	86	—	IC
12	I	AD1DT	37	—	Vcc	62	O	ADD9	87	—	Vcc
13	—	GND	38	O	DEC DATA1	63	—	GND	88	—	IC
14	O	BCK	39	—	IC	64	O	ADD8	89	—	IC
15	I	DA2DT	40	—	IC	65	O	ADD7	90	I	DATA7
16	I	EXTCMD2	41	—	IC	66	O	ADD6	91	I	DATA6
17	I	EXTCMD1	42	—	IC	67	O	ADD5	92	I	DATA5
18	O	DA1DT	43	O	ENC DATA	68	O	ADD4	93	—	IC
19	O	RX LRCK	44	—	GND	69	O	ADD3	94	—	GND
20	—	Vcc	45	—	IC	70	—	Vcc	95	I	DATA4
21	O	DA2DT	46	O	AD1DT	71	O	ADD2	96	I	DA1DT
22	O	DEC DATA	47	—	IC	72	O	LRCK	97	I	DATA3
23	—	GND	48	—	IC	73	—	GND	98	O	AD2DT
24	—	Vcc	49	—	IC	74	—	GND	99	I	DATA2
25	I	CONFIG	50	—	GND	75	—	Vcc	100	—	IC

INPUTS

24 MHz	: 24 MHz CLOCK
AD1DT, AD2DT	: A/D CONVERTER DATA 1, 2
BIDT	: AES/EBU DATA
CONFIG	: PLD INITIALIZING TRIGGER
DA1DT, DA2DT	: AUDIO 5/6-CH, 7/8-CH DATA
DATA0 - DATA7	: PLD INITIALIZING DATA
EXTCMD1, EXTCMD11	: EXTERNAL COMMAND 1, 2
EXTCMD2	: AUDIO 3/4-CH DATA
RESERVED	: SPARE

OUTPUTS

24 MHz	: 24 MHz CLOCK
AD LRCK	: SAMPLING CLOCK FOR A/D CONVERTER
AD1DT, AD2DT	: AUDIO 5/6-CH, 7/8-CH DATA
ADD0 - ADD15	: PLD INITIALIZING ADDRESS
BCK	: BIT CLOCK
CNT2048	: CLOCK FOR PLL
CONF DONE	: PLD INITIALIZING END FLAG
DA LRCK	: SAMPLING CLOCK FOR D/A CONVERTER
DA1DT, DA2DT	: D/A CONVERTER DATA 1, 2
DEC DATA, DEC DATA1	: EXTERNAL COMMAND 1, 2
DT	: AUDIO 1/2-CH DATA
ENC DATA	: AUDIO 3/4-CH DATA
LRCK	: SAMPLING CLOCK FOR TRANSMISSION
RX LRCK	: SAMPLING CLOCK FOR RECEIVING

OTHER

IC	: INTERNAL CONNECTION
TEST	: TEST

