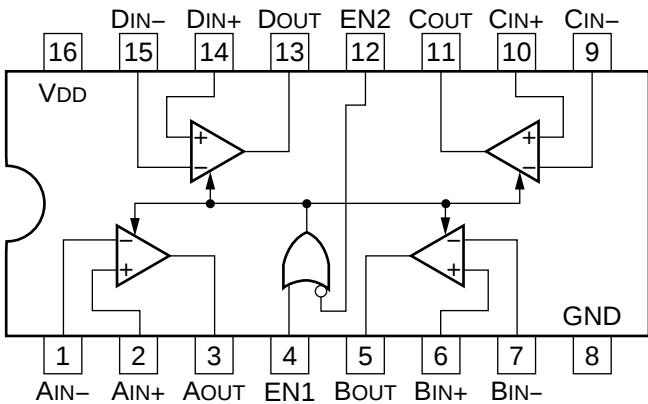


C-MOS QUAD DIFFERENTIAL LINE RECEIVER

—TOP VIEW—



INPUTS			OUTPUTS
EN2	EN1	IN+ - IN-	OUT
1	0	x	HI-Z
ALL OTHER COMBINATIONS OF ENABLE INPUTS		$V_{ID} \geq 0.1V$	1
		$V_{ID} \leq -0.1V$	0
		FULL FAILSAFE OPEN/SHORT OR TERMINATED	1

0 : LOW LEVEL
1 : HIGH LEVEL
x : DON'T CARE
HI-Z : HIGH IMPEDANCE