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Section 1:Introduction

This document is provided as a supplement to the High-Speed Microcontrollers User's Guide, covering new or modified features specific to the DS87C550. *This document must be used in conjunction with the High-Speed Microcontroller User's Guide, available from Dallas Semiconductor*. Addenda are arranged by section number, which correspond to sections in the High-Speed Microcontroller User's Guide.

The following additions and changes, with respect to the High-Speed Microcontroller User's Guide, are contained in this document. This document is a work in progress, and updates/additions will be added as available.

Section 2:Ordering Information

Information on new members of the High-Speed Microcontroller family has been added.

Section 3: Architecture

No Changes. Information containing new architectural features is contained in the DS87C550 data sheet.

Section 4:Programming Model

Descriptions of new and modified Special Function Registers in the DS87C550 have been included.

Section 5:CPU Timing

Descriptions of the clock multiply/divide modes have been added.

Section 6:Memory Access

Information on EPROM size and the DPTR auto-select feature have been added.

Section 7: Power Management

Changes in the power management clock divisor are discussed.

Section 8:Reset Conditions

A discussion of the reset output has been included.

Section 9: Interrupts

The interrupt structure found on the DS87C550 is described.

Section 10:Parallel I/O

Descriptions of the new I/O ports have been added.

Section 11:Programmable Timers

New clock multiply and divide functions added to the DS87C550's Timers are described.

Section 12:Serial I/O

No changes.

Section 13:Timed Access Protection

Additional/modified Timed Access bits in the DS87C550 are listed.

Section 14:Real-Time Clock

No changes.

Section 15:Battery Backup

No changes.

Section 16:Instruction Set Details

No changes.

Section 17: Troubleshoooting

No changes.

Section 18: Analog-to-Digital Converter

This is a new section describing the A/D converter found on the DS87C550.

Section 19:Pulse Width Modulator

This is a new section describing the PWM functions found on the DS87C550.

SECTION 2:ORDERING INFORMATION

The High-Speed Microcontroller family follows the part numbering convention shown below. Note that not all combinations of devices are planned to be made available. Refer to individual data sheet for available versions.

DS87C550-QCL		
SPEED:	D G L R S	18 MHz 25 MHz 33 MHz 40 MHz 50 MHz
TEMPERATURE:	С	0 °C to 70 °C
PACKAGE:	M Q F W K	DIP PLCC Thin Quad Flat Pack (TQFP) Quad Flat Pack (QFP) Windowed Ceramic DIP Windowed Ceramic PLCC
OPERATING VOLTAGE:	0 3	+5V +3V OR WIDE VOLTAGE
MEMORY TYPE:	0 3 7 9	ROMLESS FACTORY PROGRAMMED MASK ROM EPROM (WINDOWED OR OTP PACKAGES) FLASH

SECTION 3:ARCHITECTURE

No changes.

SECTION 4: PROGRAMMING MODEL

SPECIAL FUNCTION REGISTERS

The following table identifies the complete SFR map for the DS87C550.

DD0100000		01101101							
REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	ADDRESS
P0	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0	80h
SP									81h
DPL									82h
DPH									83h
DPL1									84h
DPH1									85h
DPS	ID1	ID0	TSL	-	-	-	-	SEL	86h
PCON	SMOD_0	SMOD0	OFDF	OFDE	GF1	GF0	STOP	IDLE	87h
TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	88h
TMOD	GATE	C/\overline{T}	M1	M0	GATE	C/\overline{T}	M1	M0	89h
TL0									8Ah
TL1									8Bh
TH0									8Ch
TH1									8Dh
CKCON	WD1	WD0	T2M	T1M	TOM	MD2	MD1	MD0	8Eh
P1	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0	90h
	TXD1	RXD1	T2EX	<i>T2</i>	INT5/CT3	INT4/CT2	INT3/CT1	INT2/CT0	
RCON	-	-	-	-	CKRDY	RGMD	RGSL	BGS	91h
SCON0	SM0/FE_0	SM1_0	SM2_0	REN_0	TB8_0	RB8_0	TI_0	RI_0	98h
SBUF0									99h
PMR	CD1	CD0	SWB	СТМ	$4X/\overline{2X}$	ALEOFF	DME1	DME0	9Fh
P2	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0	A0
SADDR0									A1h
SADDR1									A2h
IE	EA	EAD	ES1	ES0	ET1	EX1	ET0	EX0	A8h
CMPL0									A9h
CMPL1									AAh
CMPL2									ABh
CPTL0									ACh
CPTL1									ADh
CPTL2									AEh
CPTL3									AFh
P3	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0	B0h
_	\overline{RD}	WR	T1	Т0	INT1	INTO	TXD0	RXD0	_
ADCON1	STDT / DSV	EOC		ADEX	WCO	WCM	ADON	WCIO	B2h
	51K1/651	LOC	CON1/55	MDL A	wey				D2n
ADCON2	OUTCF	MUX2	MUX1	MUX0	APS3	APS2	APS1	APS0	B3h
ADMSB									B4h
ADLSB									B5h
WINHI					1				B6h
WINLO					1				B7h
IP	- 1	PAD	PS1	PS0	PT1	PX1	PT0	PX0	B8h
SADEN0			_ ~ ~						B9h
SADEN1									BAh
T2CON	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	$C/\overline{T2}$		BEh
		2.11 2					T2OF	DCEN	BFh
		-		-			1200		DUII

DS87C550 SPECIAL FUNCTION REGISTER LOCATIONS : Table 550UG-1

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REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	ADDRESS
P4	P4.7	P4.6	P4.5	P4.4	P4.3	P4.2	P4.1	P4.0	C0h
	CMT1	CMT0	CMSR5	CMSR4	CMSR3	CMSR2	CMSR1	CMSR0	
ROMSIZE	-	-	-	-	-	RMS2	RMS1	RMS0	C2h
STATUS	PIP	HIP	LIP	-	SPTA1	SPRA1	SPTA0	SPRA0	C5h
TA	1	1	1	1	1	1	1	1	C7h
T2IR	-	CM2F	CM1F	CM0F	IE5/CF3	IE4/CF2	IE3/CF1	IE2/CF0	C8h
CMPH0									C9h
CMPH1									CAh
CMPH2									CBh
CPTH0									CCh
CPTH1									CDh
CPTH2									CEh
CPTH3									CFh
PSW	CY	AC	F0	RS1	RS0	OV	F1	Р	D0h
PW0FG									D2h
PW1FG									D3h
PW2FG									D4h
PW3FG									D5h
PWMADR	ADRS	-	-	-	-	-	PWE1	PWE0	D6h
SCON1	SM0/FE_1	SM1_1	SM2_1	REN_1	TB8_1	RB8_1	TI_1	<i>RI_1</i>	D8h
SBUF1									D9h
PWM0									DCh
PWM1									DDh
PWM2									DEh
PWM3									DFh
ACC									E0h
PW01CS	PW0S2	PW0S1	PW0S0	PW0EN	PW1S2	PW1S1	PW1S0	PW1EN	E1h
PW23CS	PW2S2	PW2S1	PW2S0	PW2EN	PW3S2	PW3S1	PW3S0	PW3EN	E2h
PW01CON	PW0F	PW0DC	PW0OE	PW0T/C	PW1F	PW1DC	PW1OE	PW1T/C	E3h
PW23CON	PW2F	PW2DC	PW2OE	PW2T/C	PW3F	PW3DC	PW3OE	PW3T/C	E4h
RLOADL									E6h
RLOADH									E7h
EIE	ET2	ECM2	ECM1	ECM0	EX5/EC3	EX4/EC2	EX3/EC1	EX2/EC0	E8h
T2SEL	TF2S	TF2BS	-	TF2B	-	-	T2P1	T2P0	EAh
CTCON	CT3	СТ3	$\overline{\text{CT2}}$	CT2	CT1	CT1	CT0	СТО	EBh
TL2									ECh
TH2									EDh
SETR	TGFF1	TGFF0	CMS5	CMS4	CMS3	CMS2	CMS1	CMS0	EEh
RSTR	CMT1	CMT0	CMR5	CMR4	CMR3	CMR2	CMR1	CMR0	EFh
В									FOh
P6	P6.7	P6.6	P6.5	P6.4	P6.3	P6.2	P6.1	P6.0	F1h
EIP	PT2	PCM2	PCM1	PCM0	PX5/PC3	PX4/PC2	PX3/PC1	PX2/PC0	F8h
WDCON	SMOD_1	POR	EPFI	PFI	WDIF	WTRF	EWT	RWT	FFh

Note: Registers and bits in bold are new to the DS87C550. Registers and bits in bold AND Italic existed in previous high-speed microcontrollers, but at different locations.

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Instruct BIT 5 BIT 4 BIT 3 BIT 2 BIT 1 I <thi<< th=""><th colspan="9">DS87C550 SPECIAL FUNCTION REGISTER RESET VALUES : Table 550UG-2</th><th>0UG-2</th></thi<<>	DS87C550 SPECIAL FUNCTION REGISTER RESET VALUES : Table 550UG-2									0UG-2
P0 1 1 1 1 1 1 1 1 80h DPL 0 <th>REGISTER</th> <th>BIT 7</th> <th>BIT 6</th> <th>BIT 5</th> <th>BIT 4</th> <th>BIT 3</th> <th>BIT 2</th> <th>BIT 1</th> <th>BIT 0</th> <th>ADDRESS</th>	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	ADDRESS
SP 0 0 0 0 0 1 1 1 1 81h DPH 0 <td>P0</td> <td>1</td> <td>1</td> <td>1</td> <td>1</td> <td>1</td> <td>1</td> <td>1</td> <td>1</td> <td>80h</td>	P0	1	1	1	1	1	1	1	1	80h
DFL 0 0 0 0 0 0 0 0 22h DPLI 0 0 0 0 0 0 0 0 83h DPLI 0 0 0 0 0 0 0 84h DPS 0 0 0 0 0 0 0 84h DPS 0 0 0 0 0 0 0 84h PCON 0 0 0 0 0 0 0 0 84h TCON 0 0 0 0 0 0 0 0 0 0 84h TL1 0 0 0 0 0 0 0 0 84h TH1 0 0 0 0 0 0 0 0 0 0 84h TH0 1 1 1 1 <td>SP</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>1</td> <td>1</td> <td>81h</td>	SP	0	0	0	0	0	1	1	1	81h
DPH 0 0 0 0 0 0 83h DPH1 0 0 0 0 0 0 0 0 84h DPS 0 0 0 0 0 0 0 84h DPS 0 0 0 0 0 0 0 84h DCN 0 0 0 0 0 0 0 84h TCON 0 0 0 0 0 0 0 0 88h TLO 0 0 0 0 0 0 0 0 88h THI 0 0 0 0 0 0 0 0 88h PI 1 1 1 1 1 1 1 1 90h SCKON 0 0 0 0 0 0 0 99h SADD	DPL	0	0	0	0	0	0	0	0	82h
DPL1 0 0 0 0 0 0 0 84h DPSH 0 0 0 0 0 0 0 85h DS 0 0 0 0 0 0 0 85h PCON 0 0 0 0 0 0 0 87h TCON 0 0 0 0 0 0 0 88h TMOD 0 0 0 0 0 0 0 88h TL1 0 0 0 0 0 0 0 88h TH1 0 0 0 0 0 0 0 88h SCON 0 0 0 0 0 0 0 99h SDER0 0 0 0 0 0 0 0 99h SDEV 0 0 0 <	DPH	0	0	0	0	0	0	0	0	83h
DPHI 0 0 0 0 0 0 0 85h PCON 0 0 0 0 0 0 0 86h PCON 0 0 0 0 0 0 0 87h TCON 0 0 0 0 0 0 0 88h TMOD 0 0 0 0 0 0 0 88h TI.1 0 0 0 0 0 0 0 88h THI 0 0 0 0 0 0 0 88h PI 1	DPL1	0	0	0	0	0	0	0	0	84h
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	DPH1	0	0	0	0	0	0	0	0	85h
PCON 0	DPS	0	0	0	0	0	1	0	0	86h
TCON 0	PCON	0	0	Special	0	0	0	0	0	87h
TMOD 0 0 0 0 0 0 0 89h TL0 0 0 0 0 0 0 0 88h TH0 0 0 0 0 0 0 0 0 88h TH0 0 0 0 0 0 0 0 0 88h TH1 0 0 0 0 0 0 0 0 88h RCON - - - Special Special 0 91h SCON0 0 0 0 0 0 0 0 98h SBUF0 0 0 0 0 0 0 0 0 98h SADDR 0	TCON	0	0	0	0	0	0	0	0	88h
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	TMOD	0	0	0	0	0	0	0	0	89h
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	TL0	0	0	0	0	0	0	0	0	8Ah
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	TL1	0	0	0	0	0	0	0	0	8Bh
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	TH0	0	0	0	0	0	0	0	0	8Ch
CKCON 0 0 0 0 0 1 8Eb PI 1 1 1 1 1 1 1 90h RCON - - Special Special Special 0 91h SCON0 0 0 0 0 0 0 0 99h SBUF0 0 0 0 0 0 0 0 99h PMR 1 0 0 0 0 0 0 99h P2 1 1 1 1 1 1 1 1 1 SADDR0 0	TH1	0	0	0	0	0	0	0	0	8Dh
PI 1 1 1 1 1 1 1 90h RCON - - - Special Special Special 0 91h SCON0 0 0 0 0 0 0 0 92h SBUF0 0 0 0 0 0 0 0 99h PMR 1	CKCON	0	0	0	0	0	0	0	1	8Eh
RCON - - Special Special Special 0 91h SCON0 0 0 0 0 0 0 0 98h SBUF0 0 0 0 0 0 0 0 99h PMR 1 0 0 0 0 0 0 97h P2 1 1 1 1 1 1 1 1 A0 SADDR0 0 0 0 0 0 0 0 0 AAh SADDR1 0 0 0 0 0 0 0 AAh CMPL0 0 0 0 0 0 0 AAh CMPL1 0 0 0 0 0 0 AAh CPTL1 0 0 0 0 0 0 AAh CPTL3 0 0 0 0	P1	1	1	1	1	1	1	1	1	90h
SCON0 0 0 0 0 0 0 0 98h SBUF0 0 0 0 0 0 0 0 99h PMR 1 0 0 0 0 0 0 0 99h P2 1 1 1 1 1 1 1 1 A0 SADDR0 0 0 0 0 0 0 0 A1h SADDR1 0 0 0 0 0 0 0 A1h SADDR1 0 0 0 0 0 0 A2h EWD0 0 0 0 0 0 0 A2h CMPL0 0 0 0 0 0 0 AAh CPTL1 0 0 0 0 0 0 ACh CPTL2 0 0 0 0 0	RCON	-	-	-	-	Special	Special	Special	0	91h
SBUF0 0 0 0 0 0 0 0 99h PMR 1 0 0 0 0 0 0 0 99h P2 1 <t< td=""><td>SCON0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>98h</td></t<>	SCON0	0	0	0	0	0	0	0	0	98h
PMR 1 0 0 0 0 0 0 9Fh P2 1 <td>SBUF0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>99h</td>	SBUF0	0	0	0	0	0	0	0	0	99h
P2 1	PMR	1	0	0	0	0	0	0	0	9Fh
SADDR0 0 0 0 0 0 0 0 Alh SADDR1 0 0 0 0 0 0 0 0 Alh E 0 0 0 0 0 0 0 Ash CMPL0 0 0 0 0 0 0 0 Ash CMPL1 0 0 0 0 0 0 0 Ash CMPL2 0 0 0 0 0 0 Ash CPTL1 0 0 0 0 0 0 Ach CPTL2 0 0 0 0 0 0 Ach ADCON1 0 0 0 0 0 0 Bsh ADMSB 0 0 0 0 0 0 Bsh MIH 0 0 0 0 0 0 Bsh </td <td>P2</td> <td>1</td> <td>1</td> <td>1</td> <td>1</td> <td>1</td> <td>1</td> <td>1</td> <td>1</td> <td>A0</td>	P2	1	1	1	1	1	1	1	1	A0
SADDR1 0 0 0 0 0 0 0 A2h IE 0 0 0 0 0 0 0 0 A8h CMPL0 0 0 0 0 0 0 0 AAh CMPL2 0 0 0 0 0 0 0 AAh CPTL0 0 0 0 0 0 0 AAh CPTL1 0 0 0 0 0 0 AAh CPTL2 0 0 0 0 0 0 AAh CPTL3 0 0 0 0 0 0 AAh CPTL3 0 0 0 0 0 0 ABh ADCON1 0 0 0 0 0 0 BAh ADMSB 0 0 0 0 0 0 BBh	SADDR0	0	0	0	0	0	0	0	0	Alh
IE 0 0 0 0 0 0 0 A8h CMPL0 0 0 0 0 0 0 0 0 AAh CMPL1 0 0 0 0 0 0 0 AAh CMPL2 0 0 0 0 0 0 AAh CMPL2 0 0 0 0 0 0 AAh CPTL0 0 0 0 0 0 0 AAh CPTL1 0 0 0 0 0 0 ACh CPTL2 0 0 0 0 0 0 AEh CPTL3 0 0 0 0 0 0 AEh CPTL3 0 0 0 0 0 0 AEh CON2 0 0 0 0 0 0 AEh ADM	SADDR1	0	0	0	0	0	0	0	0	A2h
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	IE	0	0	0	0	0	0	0	0	A8h
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	CMPL0	0	0	0	0	0	0	0	0	A9h
CMPL2 0 0 0 0 0 0 0 ABh CPTL0 0 0 0 0 0 0 0 ACh CPTL1 0 0 0 0 0 0 0 ACh CPTL2 0 0 0 0 0 0 ACh CPTL3 0 0 0 0 0 0 ACh CPTL3 0 0 0 0 0 0 AEh CPTL4 0 0 0 0 0 BEh ADCON1 0 0 0 0 0 0 BBh ADMSB 0	CMPL1	0	0	0	0	0	0	0	0	AAh
CPTL0 0 0 0 0 0 0 ACh CPTL1 0 0 0 0 0 0 0 ACh CPTL2 0 0 0 0 0 0 0 ACh CPTL3 0 0 0 0 0 0 AEh CPTL3 0 0 0 0 0 0 AEh CPTL3 0 0 0 0 0 AEh AEh CPTL3 0 0 0 0 0 AEh AEh CPTL3 0 0 0 0 0 AFh BB ADCN1 0 0 0 0 0 0 BA BA ADMSB 0 0 0 0 0 0 BA MINL0 0 0 0 0 0 0 BA SADEN1	CMPL2	0	0	0	0	0	0	0	0	ABh
CPTL1 0 0 0 0 0 0 ADh CPTL2 0 0 0 0 0 0 0 AEh CPTL3 0 0 0 0 0 0 0 AEh P3 1 1 1 1 1 1 1 BOh ADCON1 0 0 0 0 0 0 0 BA ADCON2 0 0 0 0 0 0 BA ADLSB 0 0 0 0 0 0 BA ADLSB 0 0 0 0 0 0 BA WINLO 0 0 0 0 0 0 BA SADEN0 0 0 0 0 0 0 BA T2CON 0 0 0 0 0 BA T2CON 0 </td <td>CPTL0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>ACh</td>	CPTL0	0	0	0	0	0	0	0	0	ACh
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	CPTL1	0	0	0	0	0	0	0	0	ADh
CPTL3 0 0 0 0 0 0 0 AFh P3 1<	CPTL2	0	0	0	0	0	0	0	0	AEh
P3 1	CPTL3	0	0	0	0	0	0	0	0	AFh
ADCON1 0 0 0 0 0 0 0 B2h ADCON2 0 0 0 0 0 0 0 0 0 0 0 0 0 B3h ADMSB 0 0 0 0 0 0 0 0 B3h ADLSB 0 0 0 0 0 0 0 0 B4h ADLSB 0 0 0 0 0 0 0 B5h WINLO 0 0 0 0 0 0 B6h WINLO 0 0 0 0 0 0 0 B7h IP - 0 0 0 0 0 0 B8h SADEN0 0 0 0 0 0 0 B8h T2CON 0 0 0 0 0 0 BFh	P3	1	1	1	1	1	1	1	1	B0h
ADCON2 0 0 0 0 0 0 0 0 Bash ADMSB 0 <	ADCON1	0	0	0	0	0	0	0	0	B2h
ADMSB 0 0 0 0 0 0 0 B4h ADLSB 0 <td< td=""><td>ADCON2</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>B3h</td></td<>	ADCON2	0	0	0	0	0	0	0	0	B3h
ADLSB 0 0 0 0 0 0 0 BSh WINHI 0 0 0 0 0 0 0 0 BSh WINLO 0 0 0 0 0 0 0 BSh IP - 0 0 0 0 0 0 BSh SADEN0 0 0 0 0 0 0 BSh SADEN1 0 0 0 0 0 0 BSh SADEN1 0 0 0 0 0 0 BSh SADEN1 0 0 0 0 0 0 BSh T2CON 0 0 0 0 0 0 BEh T2MOD - - - - - 0 0 BFh P4 1 1 1 1 1 1 1 <td>ADMSB</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>B4h</td>	ADMSB	0	0	0	0	0	0	0	0	B4h
WINHI 0 0 0 0 0 0 0 0 B6h WINLO 0 0 0 0 0 0 0 0 0 B7h IP - 0 0 0 0 0 0 0 B8h SADEN0 0 0 0 0 0 0 0 B8h SADEN1 0 0 0 0 0 0 B8h T2CON 0 0 0 0 0 0 BFh T2MOD - - - - - 0 0 BFh P4 1 1 1 1 1 1 1 1 C0h ROMSIZE 0 0 0 0 1 1 1 1 C4h STATUS 0 0 0 1 1 1 1 C7h	ADLSB	0	0	0	0	0	0	0	0	B5h
WINLO 0 0 0 0 0 0 0 B7h IP - 0 0 0 0 0 0 0 0 B8h SADEN0 0 0 0 0 0 0 0 B8h SADEN1 0 0 0 0 0 0 0 B8h T2CON 0 0 0 0 0 0 BEh T2MOD - - - - - 0 BFh P4 1 1 1 1 1 1 1 1 1 ROMSIZE 0 0 0 0 1 <td>WINHI</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>B6h</td>	WINHI	0	0	0	0	0	0	0	0	B6h
IP - 0 0 0 0 0 0 0 B8h SADEN0 0 0 0 0 0 0 0 0 B8h SADEN1 0 0 0 0 0 0 0 B8h T2CON 0 0 0 0 0 0 BAh T2CON 0 0 0 0 0 0 BAh T2CON 0 0 0 0 0 0 BEh T2MOD - - - - - 0 0 BFh P4 1 1 1 1 1 1 1 COh ROMSIZE 0 0 0 0 1 1 1 1 CAh STATUS 0 0 0 1 1 1 1 1 CAh T2IR - 0 <td>WINLO</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>B7h</td>	WINLO	0	0	0	0	0	0	0	0	B7h
SADEN0 0 0 0 0 0 0 0 B9h SADEN1 0 0 0 0 0 0 0 0 0 BAh T2CON 0 0 0 0 0 0 0 BEh T2MOD - - - - - 0 0 BFh P4 1 1 1 1 1 1 1 1 0 0 BFh P4 1 1 1 1 1 1 1 1 1 0 0 0 Ch ROMSIZE 0 0 0 0 1	IP	-	0	0	0	0	0	0	0	B8h
SADEN1 0 0 0 0 0 0 0 0 BAh T2CON 0 0 0 0 0 0 0 0 BEh T2MOD - - - - 0 0 BEh P4 1 1 1 1 1 1 1 0 0 BFh P4 1 1 1 1 1 1 1 0 0 0 ROMSIZE 0 0 0 0 1 <td< td=""><td>SADEN0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>B9h</td></td<>	SADEN0	0	0	0	0	0	0	0	0	B9h
T2CON 0 0 0 0 0 0 0 0 BEh T2MOD - - - - - 0 0 BFh P4 1 1 1 1 1 1 1 1 1 COh ROMSIZE 0 0 0 0 1 1 0 0 C2h P5 1 1 1 1 1 1 1 C4h STATUS 0 0 0 1 0 0 0 C5h TA 1 1 1 1 1 1 1 C7h T2IR - 0 0 0 0 0 0 C8h CMPH0 0 0 0 0 0 0 CAh CMPH1 0 0 0 0 0 0 CAh CMPH2 0	SADEN1	0	0	0	0	0	0	0	0	BAh
T2MOD - - - - 0 0 BFh P4 1 1 1 1 1 1 1 1 1 0 0 BFh ROMSIZE 0 0 0 0 1 1 1 1 1 0 0 C2h P5 1 1 1 1 1 1 1 1 C4h STATUS 0 0 0 1 0 0 0 C5h TA 1 1 1 1 1 1 1 C7h T2IR - 0 0 0 0 0 0 C8h CMPH0 0 0 0 0 0 0 CAh CAh CMPH1 0 0 0 0 0 0 CAh CMPH2 0 0 0 0 0 0	T2CON	0	0	0	0	0	0	0	0	BEh
P4 1	T2MOD	-	-	-	-	-	-	0	0	BFh
ROMSIZE 0 0 0 0 1 1 0 0 C2h P5 1	P4	1	1	1	1	1	1	1	1	C0h
P5 1 1 1 1 1 1 1 1 1 1 1 1 1 C4h STATUS 0 0 0 0 1 0 0 0 0 C5h TA 1 1 1 1 1 1 1 1 C7h T2IR - 0 0 0 0 0 0 0 C8h CMPH0 0 0 0 0 0 0 C9h CMPH1 0 0 0 0 0 0 CAh CMPH2 0 0 0 0 0 0 CBh CPTH0 0 0 0 0 0 0 CCh CPTH1 0 0 0 0 0 0 CDh	ROMSIZE	0	0	0	0	1	1	0	0	C2h
STATUS 0 0 0 1 0 0 0 C5h TA 1 1 1 1 1 1 1 1 1 C7h T2IR - 0 0 0 0 0 0 0 0 C8h CMPH0 0 0 0 0 0 0 0 0 C8h CMPH1 0 0 0 0 0 0 0 0 CAh CMPH2 0 0 0 0 0 0 0 CBh CPTH0 0 0 0 0 0 0 0 0 CCh CPTH1 0 0 0 0 0 0 0 0 0 0 0 0 CCh	P5	1	1	1	1	1	1	1	1	C4h
TA 1	STATUS	0	0	0	1	0	0	0	0	C5h
T2IR - 0 0 0 0 0 0 0 C8h CMPH0 0 0 0 0 0 0 0 0 0 C8h CMPH1 0 0 0 0 0 0 0 CAh CMPH2 0 0 0 0 0 0 CBh CPTH0 0 0 0 0 0 0 CCh CPTH1 0 0 0 0 0 0 CCh	ТА	1	1	1	1	1	1	1	1	C7h
CMPH0 0 0 0 0 0 0 0 0 C9h CMPH1 0 0 0 0 0 0 0 0 CAh CMPH2 0 0 0 0 0 0 0 CBh CPTH0 0 0 0 0 0 0 CCh CPTH1 0 0 0 0 0 0 CDh	T2IR	-	0	0	0	0	0	0	0	C8h
CMPH1 0 0 0 0 0 0 0 CAh CMPH2 0 0 0 0 0 0 0 0 CBh CPTH0 0 0 0 0 0 0 0 CCh CPTH1 0 0 0 0 0 0 CDh	CMPH0	0	0	0	0	0	0	0	0	C9h
CMPH2 0 0 0 0 0 0 0 CBh CPTH0 0 0 0 0 0 0 0 0 CCh CPTH1 0 0 0 0 0 0 0 0 CCh	CMPH1	0	0	0	0	0	0	0	0	CAh
CPTH0 0 0 0 0 0 0 0 CCh CPTH1 0 0 0 0 0 0 0 0 CCh	CMPH2	0	0	0	0	0	0	0	0	CBh
CPTH1 0 0 0 0 0 0 0 0 CDh	CPTH0	0	0	0	0	0	0	0	0	CCh
	CPTH1	0	0	0	0	0	0	0	0	CDh

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REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	ADDRESS
CPTH2	0	0	0	0	0	0	0	0	CEh
CPTH3	0	0	0	0	0	0	0	0	CFh
PSW	0	0	0	0	0	0	0	0	D0h
PW0FG	0	0	0	0	0	0	0	0	D2h
PW1FG	0	0	0	0	0	0	0	0	D3h
PW2FG	0	0	0	0	0	0	0	0	D4h
PW3FG	0	0	0	0	0	0	0	0	D5h
PWMADR	0	-	-	-	-	-	0	0	D6h
SCON1	0	0	0	0	0	0	0	0	D8h
SBUF1	0	0	0	0	0	0	0	0	D9h
PWM0	0	0	0	0	0	0	0	0	DCh
PWM1	0	0	0	0	0	0	0	0	DDh
PWM2	0	0	0	0	0	0	0	0	DEh
PWM3	0	0	0	0	0	0	0	0	DFh
ACC	0	0	0	0	0	0	0	0	E0h
PW01CS	0	0	0	0	0	0	0	0	E1h
PW23CS	0	0	0	0	0	0	0	0	E2h
PW01CON	0	0	0	0	0	0	0	0	E3h
PW23CON	0	0	0	0	0	0	0	0	E4h
RLOADL	0	0	0	0	0	0	0	0	E6h
RLOADH	0	0	0	0	0	0	0	0	E7h
EIE	0	0	0	0	0	0	0	0	E8h
T2SEL	0	0	-	0	-	-	0	0	EAh
CTCON	0	0	0	0	0	0	0	0	EBh
TL2	0	0	0	0	0	0	0	0	ECh
TH2	0	0	0	0	0	0	0	0	EDh
SETR	1		10	0	0	0	0	0	EEh
RSTR	0	0	0	0	0	0	0	0	EFh
В	0	0	0	0	0	0	0	0	FOh
P6	1	-	1	1	1	1	1	1	F1h
EIP	0	0	0	0	0	0	0	0	F8h
WDCON	0	Special	0	Special	0	Special	Special	0	FFh

	<i>vj</i>							
	7	6	5	4	3	2	1	0
SFR 80h	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1

P0.7-0 Port 0. This port functions as a multiplexed address/data bus during external memory access, and as a general purpose I/O port on devices with internal program memory. During external memory cycles, this port drives the LSB of the address when ALE is high, and data when ALE is low. When used as a general purpose I/O, this port is open-drain and requires pull-ups. Writing a 1 to any pin of this port places it in a high impedance mode, which is required if the pin is to be used as an input. Pull-ups are not required when used as a memory interface.

Stack Pointer (SP)

Dort 0 (D0)

	7	6	5	4	3	2	1	0
SFR 81h	SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-1	RW-1	RW-1

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

SP.7-0Stack Pointer. This stack pointer identifies the location where the stack will
begin. The stack pointer is incremented before every PUSH operation. This
register defaults to 07h after reset.

Data Pointer Low 0 (DPL)

	7	6	5	4	3	2	1	0
SFR 82h	DPL.7	DPL.6	DPL.5	DPL.4	DPL.3	DPL.2	DPL.1	DPL.0
	RW-0							

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

DPL.7-0Data Pointer Low 0. This register is the low byte of the standard 80C32 16-bitBits 7-0data pointer. DPL and DPH are used to point to non-scratchpad data RAM.

Data Pointer High 0 (DPH)

	7	6	5	4	3	2	1	0
SFR 83h	DPH.7	DPH.6	DPH.5	DPH.4	DPH.3	DPH.2	DPH.1	DPH.0
	RW-0							

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

DPH.7-0Data Pointer High 0. This register is the high byte of the standard 80C32 16-bitBits 7-0data pointer. DPL and DPH are used to point to non-scratchpad data RAM.

Data Pointer Low 1 (DPL1)										
	7	6	5	4	3	2	1	0		
SFR 84h	DPL1.7	DPL1.6	DPL1.5	DPL1.4	DPL1.3	DPL1.2	DPL1.1	DL1H.0		
	RW-0									

DPL1.7-0Data Pointer Low 1. This register is the low byte of the auxiliary 16-bit dataBits 7-0pointer. When the SEL bit (DPS.0) is set, DPL1 and DPH1 are used in place of
DPL and DPH during DPTR operations.

Data Pointer High 1 (DPH1)

	7	6	5	4	3	2	1	0
SFR 85h	DPH1.7	DPH1.6	DPH1.5	DPH1.4	DPH1.3	DPH1.2	DPH1.1	DPH1.0
	RW-0							

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

DPH1.7-0Data Pointer High 1. This register is the high byte of the auxiliary 16-bit dataBits 7-0pointer. When the SEL bit (DPS.0) is set, DPL1 and DPH1 are used in place of
DPL and DPH during DPTR operations.

Data Pointer Select (DPS)

	7	6	5	4	3	2	1	0			
SFR 86h	ID1	ID0	TSL0	-	-	-	-	SEL			
	RW-0	RW-0	RW-0	R-0	R-0	R-0	R-0	RW-0			
	R=Unrestri	icted Read,	W=Unrestri	cted Write, -	n=Value aft	er Reset					
ID1, ID0		Incremen	t/Decremen	t Select Bits	These bits of	define how t	he INC DPT	'R			
Bits 7-6		instruction	n functions ir	relation to	the current I	OPTR as sele	ected by SEI	۰.			
		ID1 ID0 SEL = 0 SEL = 1									
		0 0	Increm	ent DPTR	Increment	DPTR1					
		0 1	Decrem	ent DPTR	Increment DPTR1						
		1 0	Increm	ent DPTR	Decremen	t DPTR1					
		1 1	Decrem	ent DPTR	Decremen	t DPTR1					
TSL		Toggle Se	elect Bit Ena	able This bit	allows any	instruction	involving th	e data			
Bit 5		pointer to bit will au	toggle the S tomatically t	EL bit auton oggle, other	natically. W	hen this bit	is logic 1, th	e SEL			
Bits 4-1		Reserved.	Read will b	e indetermin	ate.						
SEL		Data Pointer Select. This bit selects the active data pointer.									
Bit 0		Data Pointer Select. This bit selects the active data pointer. 0 = Instructions that use the DPTR will use DPL and DPH. 1= Instructions that use the DPTR will use DPL1 and DPH1.									

Power C	ontrol (P	CON)									
	7	6	5	4	3	2	1	0			
SFR 87h	SMOD_0	SMOD0	OFDF	OFDE	GF1	GF0	STOP	IDLE			
	RW-0	RW-0	RW-*	RW-0	RW-0	RW-0	RW-0	RW-0			
	R=Unrestri	cted Read, W	/=Unrestrie	cted Write, -	n=Value aft	er Reset; *=	see descripti	.on			
SMOD_0 Bit 7		Serial Port serial baud r	0 Baud I ate doublin	Rate Double	e r Enable. For Serial Po	This bit er ort 0.	nables/disabl	es the			
	0 = Serial Port 0 baud rate will be that defined by baud rate generation equation.										
		1 = Serial Po equation	ort 0 baud : n.	rate will be	double that	defined by b	aud rate gen	eration			
SMOD0		Framing E SCON0.7 an	rror Det	ection Ena .7 bits.	ble. This	bit selects	function of	of the			
Bit 6		0 = SCON(SCON(0.7 and S and SCO	CON1.7 co N1 registers	ntrol the S	M0 function	n defined f	or the			
	1 = SCON0.7 and SCON1.7 are converted to the Framing Error (FE) flag for the respective Serial Port.										
OFDF Bit 5		Oscillator F failure and n	Fail Detect nust be cle	t Flag. This ared by soft	bit is set if ware.	a reset is ca	nused by osc	villator			
OFDE Bit 4		Oscillator F when 1 and o	ail Detect disables th	Enable. The feature wh	nis bit enable en 0.	es the oscilla	tor fail dete	ct circuitry			
GF1 Bit 3		General Put control.	rpose Use	r Flag 1. Th	is is a gene	ral purpose f	lag for softw	/are			
GF0 Bit 2		General Pur control.	rpose Use	r Flag 0. Th	iis is a gener	ral purpose f	lag for softw	/are			
STOP Bit 1		Stop Mode s oscillator and will always b device in an	Select. Se d internal t be read as undefined	tting this bit timers, and p a 0. Setting state.	will stop pr lace the CP this bit whit	ogram exect U in a low-p le the Idle bi	ution, halt th power mode. t is set will J	e CPU This bit place the			
IDLE Bit 0		Idle Mode S oscillator, tin as a 0.	Select. Set ners, seria	ting this bit l ports, and i	will stop pro nterrupts ac	ogram execu tive. This b	tion but leav it will alway	e the CPU s be read			

Timer/Co	$\frac{1}{7}$	ontrol (1)	CON)	Δ	3	2	1	0
SFR 88h	, TF1	TR1	TF0	TR0	IE1		IEO	ITO
SI IC OOM	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0
	R=Unrestr	icted Read,	W=Unrestrie	cted Write, -	n=Value aft	ter Reset		
TF1 Bit 7		Timer 1 O maximum software an interrupt se	verflow Fla count as def nd is automa ervice routin	ng. This bit is ined by the outically clear e.	indicates wh current mod ed when the	nen Timer 1 e. This bit c e CPU vector	overflows it an be cleare rs to the Tim	s d by ler 1
		0 = No Tin 1 = Timer	ner 1 overflo 1 has overflo	ow has been owed its max	detected. ximum cour	nt.		
TR1		Timer 1 R	un Control	• This bit en	ables/disab	les the opera	tion of Time	er 1.
Bit 6		0 = Timer 1 = Timer	1 is halted. 1 is enabled.					
TF0 Bit 5		Timer 0 O maximum software an interrupt se	verflow Fla count as def nd is automa ervice routin	ng. This bit is ined by the output of the	indicates wh current mod ed when the vare.	nen Timer 0 e. This bit c cPU vector	overflows it an be cleare ts to the Tim	s d by er 0
		0 = No Tin 1 = Timer	ner 0 overflo 0 has overflo	ow has been owed its max	detected. ximum cour	nt.		
TR0 Bit 4		Timer 0 R Halting thi 0 = Timer	un Control s timer will 0 is halted	• This bit en preserve the	ables/disab current cou	les the opera int in THO a	tion of Time nd TL0.	er 0.
		1 = Timer	0 is enabled.					
IE1 Bit 3		Interrupt by IT1 is d the start of inversely re	1 Edge Det etected. If I the Externa eflect the sta	ect. This bit $T1=1$, this b l Interrupt 1 ate of the \overline{IN}	is set when it will rema service rout $\overline{T1}$ pin.	an edge/lev in set until c tine. If IT1=	el of the typ leared in sof 0, this bit w	e defined tware or ill
IT1 Bit 2		Interrupt or level trig	1 Type Sele ggered interr	ect. This bit rupts.	selects whe	ther the \overline{INT}	ī pin will de	tect edge
		$0 = \overline{\text{INT1}} \text{ is}$ $1 = \overline{\text{INT1}} \text{ is}$	s level trigge s edge trigge	ered. ered.				
IE0 Bit 1		Interrupt by IT0 is d the start of inversely r	0 Edge Det etected. If I the Externa eflect the sta	ect. This bit T0=1, this b 1 Interrupt 0 tte of the \overline{IN}	is set when it will rema service rout $\overline{10}$ pin	an edge/lev in set until c tine. If IT0=	el of the typ leared in sof 0, this bit w	e defined tware or ill
IT0 Bit 0		Interrupt or level trig	0 Type Sele	et. This bit rupts.	selects whe	ther the \overline{INT}	$\overline{0}$ pin will de	etect edge
		$0 = \overline{\text{INT0}} \text{is} \\ 1 = \overline{\text{INT0}} \text{is} $	s level trigge s edge trigge	ered. ered.				

Timer M	ode Con	trol (TMC)D)		-					
	7	6	5	4	3	2	1	0		
SFR 89h	GATE	C/\overline{T}	M1	M0	GATE	C/\overline{T}	M1	M0		
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0		
	D_Unnact	riated Dead	W_IImaatui	atad Writa	n-Volue oft	an Dagat				
	K=Unresu	ncied Read,	w=Onrestric	cied write, -	n= v aiue ait	er Kesel				
GATE		Timer 1 G	ate Control	I. This bit e	nable/disable	es the ability	of Timer 1	to		
Bit 7		increment.								
		0 = Timer	1 will clock	when TR1=	1, regardless	s of the state	of $\overline{INT1}$.			
		1 = Timer	1 will clock	only when T	$\Gamma R1=1$ and \bar{I}	NT1 = 1.				
C/\overline{T}		Timer 1 C	counter/Tim	er Select.						
Bit 6		0 = Timer	1 is increme	nted by inte	rnal clocks (timer).				
		1 = Timer	1 is increme	nted by puls	es on T1 wh	en TR1 (TC	CON.6) is 1 (counter).		
		Timor 1 N	lada Salaat	Those bits	coloct the or	orating mod	o of Timor	1		
MI, MU Bits 5-4		M1	M0	Mode	select the op	erating moo		ι.		
Dits J-4		0	0	Mode	0: 8 bit with	5-bit presca	le			
		0	1	Mode	1: 16 bit wit	h no prescal	e.			
		1	0	Mode	2:8 bit with 2×1	auto-reload	1 11 1			
		1	1	Mode	3: 11mer 1 1	s halted, but	holds its co	unt.		
GATE		Timer 0 G	ate Control	I. This bit e	nables/disab	les that abili	ty of Timer	0 to		
Bit 3		increment.								
		0 = Timer	0 will clock	when TR0=	1, regardless	s of the state	of INT0.			
		1 = Timer	0 will clock	only when 7	$\Gamma R0=1$ and I	$\overline{NT0} = 1.$				
C/\overline{T}		Timer 0 C	counter/Tim	er Select.						
Bit 2		0 = Timer	incremented	by internal	clocks (time	er).				
		1 = Timer	1 is increme	nted by puls	es on T0 wh	en TR0 (TC	CON.4) is 1 ((counter).		
M1, M0 Bits 1-0		Timer 0 Mode Select. These bits select the operating mode of Timer 0. When Timer 0 is in mode 3, TL0 is started/stopped by TR0 and TH0 is started/stopped by TR1. Run control for Timer 1 is then provided via the Timer 1 mode selection.								
		M1	M0	Mode						
		0	0	Mode 0	8 bit with	5-bit prescal	e			
		0	1	Mode 1	: 16 bit no p	orescale				
		1	0	Mode 2	: 8 bit with a	auto-reload				
		1	1	Mode 3	: 11mer 0 1s	two 8 bit co	unters.			

Timer 0 I	LSB (TL	D)						
	7	6	5	4	3	2	1	0
SFR 8Ah	TL0.7	TL0.6	TL0.5	TL0.4	TL0.3	TL0.2	TL0.1	TL0.0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0
	R=Unrestr	icted Read,	W=Unrestric	cted Write, -	n=Value aft	er Reset		
TL0.7-0 Bits 7-0		Timer 0 L	SB. This re	gister contai	ns the least	significant b	yte of Time	r 0.
Timer 1 I	LSB (TL [⁄]	1)						
	7	6	5	4	3	2	1	0
SFR 8Bh	TL1.7	TL1.6	TL1.5	TL1.4	TL1.3	TL1.2	TL1.1	TL1.0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0
	R=Unrestr	icted Read,	W=Unrestric	cted Write, -	n=Value aft	er Reset		
TL1.7-0 Bits 7-0		Timer 1 L	SB. This re	gister contai	ns the least	significant b	yte of Time	r 1.

Timer 0 MSB (TH0)

	7	6	5	4	3	2	1	0
SFR 8Ch	TH0.7	TH0.6	TH0.5	TH0.4	TH0.3	TH0.2	TH0.1	TH0.0
	RW-0							

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

TH0.7-0Timer 0 MSB. This register contains the most significant byte of Timer 0.Bits 7-0

Timer 1 MSB (TH1)

	7	6	5	4	3	2	1	0
SFR 8Dh	TH1.7	TH1.6	TH1.5	TH1.4	TH1.3	TH1.2	TH1.1	TH1.0
	RW-0							

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

TH1.7-0Timer 1 MSB. This register contains the most significant byte of Timer 1.Bits 7-0

CIOCK CO	ntrol (C	KCON)						
	7	6	5	4	3	2	1	0
SFR 8Eh	WD1	WD0	T2M	T1M	TOM	MD2	MD1	MD0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-1

.

WD1, WD0Watchdog Timer Mode Select 1-0. These bits determine the watchdog timerBits 7-6time-out period. The timer divides the crystal (or external oscillator) frequency
by a programmable value as shown below. The divider value is expressed in
crystal (oscillator) cycles. The settings of the system clock control bits 4X/2X
(PMR.3) and CD1:0 (PMR.7-6) will affect the clock input to the watchdog
timer and therefore its time-out period as shown below. All Watchdog Timer
reset time-outs follow the setting of the interrupt flag by 512 clocks. The
DS87C550 does not incorporate a watchdog interrupt, but a similar effect may
be achieved by polling its flag.

	0				
$4X/\overline{2X}$	CD1:0	WD1:0=00	WD1:0=01	WD1:0=10	WD1:0=11
1	00	2^{15}	2^{18}	2^{21}	2^{24}
0	00	2^{16}	2^{19}	2^{22}	2^{25}
Х	01	2^{17}	2^{20}	2^{23}	2^{26}
Х	10	2^{17}	2^{20}	2^{23}	2^{26}
Х	11	2^{25}	2^{28}	2^{31}	2^{34}

Watchdog Interrupt Flag Time-Out Periods (in crystal clocks)

T2M Bit 5	Timer 2 Clock Select. This bit controls the division of the system clock that drives Timer 2. This bit has no effect when the timer is in baud rate generator or clock output modes. Clearing this bit to 0 maintains 80C32 compatibility. This bit has no effect on instruction cycle timing.
	0 = Timer 2 uses a divide by 12 of the crystal frequency.
	1 = The divide ratio of Timer 2 is determined by the CD1, CD0, and $4X/\overline{2x}$ as shown below.
T1M Bit 4	Timer 1 Clock Select. This bit controls the division of the system clock that drives Timer 1. Clearing this bit to 0 maintains 80C32 compatibility. This bit has no effect on instruction cycle timing.
	0 = Timer 1 uses a divide by 12 of the crystal frequency.
	1 = The divide ratio of Timer 1 is determined by the CD1, CD0, and $4X/\overline{2x}$ as shown below.
T0M Bit 3	Timer 0 Clock Select. This bit controls the division of the system clock that drives Timer 0. Clearing this bit to 0 maintains 80C32 compatibility. This bit has no effect on instruction cycle timing.
	0 = Timer 0 uses a divide by 12 of the crystal frequency.
	1 = The divide ratio of Timer 0 is determined by the CD1, CD0, and $4X/\overline{2x}$ as shown below.

		I mer og 1, un		co uo u Iu	neuton of vull	ous ciocit	control bet	1115 5	
		OSCILLATOR CYCLES PER MACHINE. CYCLE	OSC CYCLES PER TIMER 0/1/2 CLOCK.		OSC CYCLES PER TIMER 2 CLK, BAUD BATE CEN	OSC CYCLES PER SERIAL PORT CLK, MODE 0		OSC CYCLES PER SERIAL PORT CLK, MODE 2	
CD1:0	$4X/\overline{2X}$	CICLE	TxM=0	TxM=1	RATE GEN.	SM2=0	SM2=1	SMOD=0	SMOD=1
00	1	1	12	1	2	3	1	64	32
00	0	2	12	2	2	6	2	64	32
01	Х				Reserve	ed			
10	Х	4	12	4	2	12	4	64	32
11	Х	1024	3072	1024	512	3072	1024	64	32

Timer 0. 1. and 2 values as a function of various clock control settings

MD2, MD1, MD0

Bits 2-0

Stretch MOVX Select 2-0. These bits select the time by which external MOVX cycles are to be stretched. This allows slower memory or peripherals to be accessed without using ports or manual software intervention. The \overline{RD} or \overline{WR} strobe will be stretched by the specified interval, which will be transparent to the software except for the increased time to execute to MOVX instruction. All internal MOVX instructions on devices containing MOVX SRAM are performed at the 2 machine cycle rate.

MD2	MD1	MD0	Stretch Value	MOVX Duration
0	0	0	0	2 Machine Cycles
0	0	1	1	3 Machine Cycles (reset default)
0	1	0	2	4 Machine Cycles
0	1	1	3	5 Machine Cycles
1	0	0	4	9 Machine Cycles
1	0	1	5	10 Machine Cycles
1	1	0	6	11 Machine Cycles
1	1	1	7	12 Machine Cycles
				•

	4			0	1			11
Port 1 (P	1)							
	7	6	5	4	3	2	1	0
SFR 90h	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
	TXD1	RXD1	T2EX	T2	INT5/CT3	INT4/CT2	INT3/CT1	INT2/CT0
	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1
	R=Unrestr	icted Read, V	W=Unrestri	cted Write,	-n=Value af	ter Reset		
P1.7-0 Bits 7-0		General Pa port. In ad- contain fun on pins P1. functions is must conta- capacity.	urpose I/O dition, all the actions that 1-0 are ava s controlled in a logic of	Port 1. The pins have are new to tailable on the by several ne before the b	his register fu e an alternati the 80C32 ar e 80C32, but other SFRs. he pin can be	nctions as a ve function l chitecture. T not the 80C The associa used in its a	general purp isted below. The Timer 2 31. Each of ted Port 1 lat lternate func	oose I/O P1.2-7 functions the tch bit tion
TXD1		Serial Port	t 1 Transm	it. This pir	n transmits th	e serial port	1 data in ser	ial port
Bit 7		modes 1, 2	, 3 and emit	ts the synch	ronizing clo	ck in serial p	ort mode 0.	
RXD1		Serial Port	t 1 Receive	. This pin r	eceives the s	erial port 1 d	data in serial	port
Bit 6		modes 1, 2	, 3 and is a	bi-direction	al data trans	fer pin in ser	ial port mod	e 0.
T2EX Bit 5		Timer 2 C. value in the EXEN2 (T will reload enabled by	apture/Rel e T2 registe 2CON.3). V the timer 2 EXEN2 (T	oad Trigge rs to be trar Vhen in aut registers w 2CON.3).	er. A 1 to 0 the sterned into one reload mo ith the value	ransition on the capture r de, a 1 to 0 t in RCAP2L	this pin will registers if er ransition on and RCAP2	cause the habled by this pin H if
T2		Timer 2 E	xternal Inp	out. A 1 to	0 transition of	on this pin w	ill cause tim	er 2
Bit 4		increment of operation is	or decrements enabled by	nt dependin y setting the	g on the time $C/\overline{T2}$ bit (7)	er configurat (2CON.1).	ion. This mo	de of
INT5/CT3		External I	nterrupt 5/	Capture 3	Input. In no	ormal operat	ion, a falling	edge on
Bit 3		this pin wil enabled, th	ll cause an e is pin acts a	external intensis a capture	errupt 5 (if er command in	nabled). If ca put.	pture channe	el 3 is
INT4/CT2		External I	nterrupt 4/	'Capture 2	Input. In no	rmal operati	on, a falling	edge on
Bit 2		this pin wil enabled, th	ll cause an e is pin acts a	external intensis a capture	errupt 4 (if er command in	nabled). If ca put.	pture channe	el 2 is
INT3/CT1 Bit 1		External In this pin will enabled, the	nterrupt 3/ Il cause an e is pin acts a	Capture 1 external intensis a capture	Input. In no errupt 3 (if er command in	rmal operati nabled). If ca put.	on, a falling pture channe	edge on el 1 is
INT2/CT0 Bit 0		External I this pin wil enabled, th	nterrupt 2/ Il cause an e is pin acts a	Capture 0 external intensis a capture	Input. In no errupt 2 (if er command in	rmal operati nabled). If ca put.	on, a falling pture channe	edge on el 0 is

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Ring Osc	cillator Co	ntrol (R	CON)							
	7	6	5	4	3	2	1	0		
SFR 91h	-	-	-	-	CKRDY	RGMD	RGSL	BGS		
					R-*	R-*	RW-*	RT-0		
R=Unrestricted Read, W=Unrestricted Write, T=Timed Access Write Only, -n =Value after Reset, * = See Description										
Bits $7 - 4$	4 Reserved. Read data will be indeterminate.									
CKRDY Bit 3	C es cr nd w C re	lock Read stablish the systal oscill ot. This bit hen the clo KRDY bit emoved, and	y This bit crystal ose ator period is cleared ck multipl is set, the d clock mu	indicates the cillator or cr ds. A 1 indic after a reset ier is enable lockout prev iltiplier may	e status of th ystal multip cates that the or when exi d (CTM bit enting CD1 then be sele	ne start-up pe lier warm-up e period is co ting STOP r of the PMR :CD0 from b ected as the o	eriod delay u o period of 6 omplete othe node. It is al register set). being modific clock source	used to 5536 erwise it is so cleared . Once the ed is		
RGMD Bit 2	R ri bi bi an	ing Oscilla ng is not be e cleared be its (CD1:Cl nd before e	ator Mode eing used, efore the R D0) can be nabling the	This bit ind and if 1, the GSL can be changed to e clock multi	licates the s system is ru modified, b any condition plier (settin	tatus of the r inning from pefore the Cl on other thar g the CTM b	ring oscillato the ring. Thi ock Control n divide by 4 pit).	or. If 0, the s bit must divider mode,		
RGSL Bit 1	R ei S' po sv R	ing Oscilla nabled, the TOP mode eriods). At witched in a eset.	ntor Select ring oscill until the e the end of as the syste	t This bit en ator will be nd of start-u this delay, the em clock sou	ables (1) or used as the s p period del he crystal os urce. This b	disables (0) system clock ay (65536 c scillator will it is reset on	the ring osci source after rystal oscilla automatical ly by a Powe	illator. If exiting tor ly be er-On		
BGS Bit 0	B re	and Gap S ference in	Select This STOP mod	s bit enables de.	(1) or disab	les (0) the b	and-gap volt	age		

Serial Port 0 Control (SCON0)

	7	6	5	4	3	2	1	0
SFR 98h	SM0/FE_0	SM1_0	SM2_0	REN_0	TB8_0	RB8_0	T1_0	R1_0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

SM0-2Serial Port Mode These bits control the mode of serial port 0. In addition theBits 7-5SM0 and SM2_0 bits have secondary functions as shown below.

SM0	SM1	SM2	MODE	FUNCTION	LENGTH	PERIOD
0	0	0	0	Synchronous	8 bits	12 t _{CLK}
0	0	1	0	Synchronous	8 bits	4 t _{CLK}
0	1	Х	1	Asynchronous	10 bits	Timer 1 or 2 baud rate equation
1	0	0	2	Asynchronous	11 bits	64 t _{CLK} (SMOD=0)
						32 t _{CLK} (SMOD=1)
1	0	1	1	Asynchronous w/	11 bits	64 t _{CLK} (SMOD=0)
				communication		$32 t_{CLK} (SMOD=1)$
1	1	0	3	Asynchronous	11 bits	Timer 1 or 2 baud rate equation
1	1	1	3	Asynchronous w/	11 bits	Timer 1 or 2 baud rate equation
				communication		

SM0/FE_0Framing Error Flag. When SMOD0 (PCON.6)=0, this bit (SM0) is used to
select the mode for serial port 0. When SMOD0=1, this bit (FE) will be set upon
detection of an invalid stop bit. When used as FE, this bit must be cleared in
software. Once the SMOD0 bit is set, modifications to this bit will not affect the
serial port mode settings. Although accessed from the same register, internally the
data for bits SM0 and FE are stored in different locations.

SM1_0 No alternate function.

Bit 6

- SM2_0Multiple CPU Communications. The function of this bit is dependent on theBit 5serial port 0 mode.
 - Mode 0: Selects 12 t_{CLK} or 4 t_{CLK} period for synchronous serial port 0 data transfers.
 - Mode 1: When set, reception is ignored (RI_0 is not set) if invalid stop bit received.
 - Mode 2/3: When this bit is set, multiprocessor communications are enabled in modes 2 and 3. This will prevent the RI_0 bit from being set, and an interrupt being asserted, if the 9th bit received is not 1.

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REN_0	Receiver Enable. This bit enable/disables the serial port 0 receiver shift register.
Bit 4	0 = Serial port 0 reception disabled.
	1= Serial port 0 receiver enabled (modes 1, 2, 3). Setting this bit will initiate synchronous reception in mode 0.
TB8_0 Bit 3	9th Transmission Bit State. This bit defines the state of the 9 th transmission bit in serial port 0 modes 2 and 3.
RB8_0 Bit 2	9th Received Bit State. This bit identifies that state of the 9 th reception bit of received data in serial port 0 modes 2 and 3. In serial port mode 1, when SM2_0=0, RB8_0 is the state of the stop bit. RB8_0 is not used in mode 0.
TI_0 Bit 1	Transmitter Interrupt Flag. This bit indicates that data in the serial port 0 buffer has been completely shifted out. In serial port mode 0, TI_0 is set at the end of the 8 th data bit. In all other modes, this bit is set at the end of the last data bit. This bit must be manually cleared by software.
RI_0 Bit 0	Receiver Interrupt Flag. This bit indicates that a byte of data has been received in the serial port 0 buffer. In serial port mode 0, RI_0 is set at the end of the 8 th bit. In serial port mode 1, RI_0 is set after the last sample of the incoming stop bit subject to the state of SM2_0. In modes 2 and 3, RI_0 is set after the last sample of RB8_0. This bit must be manually cleared by software.

Serial Data Buffer 0 (SBUF0)

	7	6	5	4	3	2	1	0
SFR 99h	SBUF0.7	SBUF0.6	SBUF0.5	SBUF0.4	SBUF0.3	SBUF0.2	SBUF0.1	SBUF0.0
	RW-0							

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

SBUF0.7-0Serial Data Buffer 0. Data for serial port 0 is read from or written to thisBits 7-0location. The serial transmit and receive buffers are separate registers, but both
are addressed at this location.

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Power Ma	anagem	ent Re	gister (PM	R)						
_	7	6	5	4	3	2	1	0		
SFR 9Fh	CD1	CD0	SWB	CTM	$4X/\overline{2X}$	ALEOFF	DME1	DME0		
-	R*-1	R*-0	RW-0	R*-0	R*-0	RW-0	RW-0	RW-0		
]	R=Unrestr	icted Rea	d, W=Unrestr	icted Write, -	n=Value aft	er Reset; * =	- See Descri	ption		
CD1,CD0 Bits 7, 6		Clock I determin	Divide Contro	I: These bits of clocks pe	s select the s	ource of the sycle as indicated	system cloc ated in the ta	k and able.		
		CD1	CD0 Clock	source; divise	or					
		0	0 Crysta by the	l multiplier; $\frac{1}{4X}$ bit.	l or 2 clocks	s per machine	e cycle (as d	letermined		
		0	1 Reserv	ved.						
		1	0 Crysta	0 Crystal/external oscillator; 4 clocks per machine cycle (default)						
		1	1 Crystal/external oscillator; 1024 clocks per machine cycle.							
SWB Bit 5		A defau changin only sta attempti or 2) din and CD Switch function switch f	efault of 10b is selected after all forms of reset and Stop mode exits. When aging these bits certain restrictions must be observed. The default state is the state that any other state can be changed to or from. As an example, npting to change from the crystal multiplier clock source (either divide by 1) directly to the crystal/external oscillator divided by 1024 will result in CD1 CD0 remaining unchanged. tch Back Enable This bit enables (1) or disables (0) the switch-back etion. When enabled, switchback will allow the processor to automatically ch from divide by 1024 mode to divide by 4 mode when an external interrunt							
CTM Bit 4		is ackno active se Crystal multipli be saved start-up cleared crystal n RGMD enters S	wledged or w erial port. Multiplier E er function. B d. Setting this period delay. and it will be nultiplier. Als is cleared to 0 top mode.	hen a start bi nable This by y clearing thi bit will autor Until the star impossible to o, CTM cann). This bit is a	t of a serial bit enables (s bit, the po natically cle t-up period o change the not be change utomatically	character is r l) or disables wer required ar the CKRE has elapsed, CD1 & CD0 ed unless CE y cleared to 0	ecognized of (0) the crys by this circ OY bit and in CKRDY wi bits to sele 01 & CD0 =) when the p	stal uitry can nitiate the 11 remain ct the 10b and processor		
$4X/\overline{2X}$ Bit 3		Clock M shown. $4X/\overline{2X}$ $4X/\overline{2X}$ This bit cleared. setting t	Multiplier Sel = 0 Sets the fr = 1 Sets the fr can only be a Therefore it r he CTM bit.	ection This requency mul requency mul ltered when t nust be set fo	bit selects th tiplier to 2 t tiplier to 4 t he Crystal M r the desired	e clock mult imes the inco imes the inco Aultiplier Ena I multiplicati	iplication fa oming clock oming clock able bit (CT on factor pr	ctor as M) is ior to		

ALEOFFALE DisableWhen set to 1, this bit disables ALE during on-board memoryBit 2accesses. Any off-chip memory access will cause ALE to automatically toggle
regardless of the state of this bit. When this bit is 0, ALE toggles for all memory
accesses whether the memory is inside or outside of the chip.

DME1,DME0	DME1	DME0	Data Memory Range	Memory Access
Bits 1, 0	0	0	0000h - FFFFh	External data memory (default)
	0	1	0000h - 03FFh	1K Internal SRAM data memory
			0400h - FFFFh	External data memory
	1	0	Reserved	Reserved
	1	0	0000h - 3FFFh	1K Internal SRAM data memory
			0400h – FFFBh	Reserved.
			FFFCh	System control byte (EPROM Read-Only).
			FFFDh – FFFF	Reserved.

Port 2 (P2)

	7	6	5	4	3	2	1	0
SFR A0h	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0
	RW-1	RW-1						

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

P2.7-0Port 2. This port functions as an address bus during external memory access, and
as a general purpose I/O port on devices which incorporate internal program
memory. During external memory cycles, this port will contain the MSB of the
address. The Port 2 latch does not control general purpose I/O pins on ROMLESS
devices, but is still used to hold the address MSB during register-indirect data
memory operations such as MOVX A, @R1.

Slave Address Register 0 (SADDR0)

	7	6	5	4	3	2	1	0
SFR A1h	SADDR0.7	SADDR0.6	SADDR0.5	SADDR0.4	SADDR0.3	SADDR0.2	SADDR0.1	SADDR0.0
	RW-0							

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

SADDR0.7-0Slave Address Register 0. This register is programmed by the user with the
given or broadcast address assigned to serial port 0.

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Slave Ac	dress R	egister 1	(SADDF	R1)						
_	7	6	5	4	3	2	1	0		
SFR A2h	SADDR1.7	SADDR1.6	SADDR1.5	SADDR1.4	SADDR1.3	SADDR1.2	SADDR1.1	SADDR1.0		
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0		
	R=Unrestr	icted Read,	W=Unrestrie	cted Write, -	n=Value aft	er Reset				
SADDR1.	7-0	Slave Add	ress Registe	er 1. This re	gister is pro	grammed by	the user wi	th the		
Bits 7-0		given or br	oadcast add	ress assigned	d to serial po	ort 1.				
Interrupt	Interrupt Enable (IE)									
	7	6	5	4	3	2	1	0		
SFR A8h	EA	EAD	ES1	ES0	ET1	EX1	ET0	EX0		
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0		
	R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset									
EA Bit 7		Global Int except Pov	t errupt Ena ver-Fail Inte	ble. This bi rrupt, which	t controls th is enabled b	e global mas	sking of all i bit (WDCO	nterrupts N.5).		
		0 = Disable setting	e all interrup s.	ot sources. T	his bit overr	ides individu	ual interrupt	mask		
		1 = Enable enable	all individu d.	al interrupt	masks. Indiv	vidual interru	pts will occ	ur if		
EAD		A/D Intern	rupt Enable	. This bit co	ontrols the n	nasking of th	ne A/D Conv	verter		
Bit 6		interrupt.								
		0 = Disable	the A/D int	errupt.						
-		1 = Enable	interrupt re	quests gener	ated by the	EOC (ADCO	JN.6) flag.			
ESI Bit 5		Enable Se 1 interrupt.	rial Port I I	nterrupt.	This bit cont	rols the mas	king of the s	Serial Port		
Dit 5		0 = Disable	e all Serial P	ort 1 interru	pts.					
		1 = Enable (SCON1.1)	interrupt re) flags.	quests gener	rated by the 1	RI_1 (SCON	11.0) or TI_	1		
ES0		Enable Se	rial Port 0 I	Interrupt.	This bit cont	rols the mas	king of the S	Serial port		
Bit 4		0 interrupt.								
		0 = Disable	e all serial p	ort 0 interruj	pts.					
		1 = Enable (SCON0.1)	interrupt re) flags.	quests gener	ated by the	RI_0 (SCON	10.0) or TI_0)		
ET1 Bit 3		Enable Timinterrupt.	mer 1 Inter	rupt. This l	oit controls t	he masking	of the Time	r 1		
		0 = Disable	e all Timer 1	interrupts.						
		1 = Enable	all interrup	t requests ge	nerated by t	he TF1 flag	(TCON.7).			

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EX1	Enable External Interrupt 1. This bit controls the masking of external interrupt
Bit 2	1.
	0 = Disable external interrupt 1.
	$1 =$ Enable all interrupt requests generated by the $\overline{INT1}$ pin.
ЕТО	Enable Timer 0 Interrupt. This bit controls the masking of the Timer 0
Bit 1	interrupt.
	0 = Disable all Timer 0 interrupts.
	1 = Enable all interrupt requests generated by the TF0 flag (TCON.5).
EX0	Enable External Interrupt 0. This bit controls the masking of external interrupt
Bit 0	0.
	0 = Disable external interrupt 0 .
	1 = Enable all interrupt requests generated by the $\overline{INT0}$ pin.

Compare Register Zero LSB (CMPL0)

	7	6	5	4	3	2	1	0
SFR A9h	CMPL0.7	CMPL0.6	CMPL0.5	CMPL0.4	CMPL0.3	CMPL0.2	CMPL0.1	CMPL0.0
	RW-0							

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

CMPL0.7-0Compare Register Zero LSB. This register is one of three used to store the least
significant 8-bit value for the Timer 2's comparison functions. When a match
occurs between Timer 2 and the contents of 16-bit register pair made of CMPH0
& CMPL0, port pins P4.5 through P4.0 are set if the corresponding compare
match set enable bits (CMS5:0=SETR.5:0) are set.

Compare Register One LSB (CMPL1)

	7	6	5	4	3	2	1	0
SFR AAh	CMPL1.7	CMPL1.6	CMPL1.5	CMPL1.4	CMPL1.3	CMPL1.2	CMPL1.1	CMPL1.0
	RW-0							

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

CMPL1.7-0Compare Register One LSB. This register is one of three used to store the least
significant 8-bit value for the Timer 2's comparison functions. When a match
occurs between Timer 2 and the contents of 16-bit register pair made of CMPH1
& CMPL1, port pins P4.5 through P4.0 are reset if the corresponding compare
match reset enable bits (CMR5:0=RSTR.5:0) are set.

Compare Register Two LSB (CMPL2)										
	7	6	5	4	3	2	1	0		
SFR ABh	CMPL2.7	CMPL2.6	CMPL2.5	CMPL2.4	CMPL2.3	CMPL2.2	CMPL2.1	CMPL2.0		
	RW-0									

CMPL2.7-0Compare Register Two LSB. This register is one of three used to store the least
significant 8-bit value for the Timer 2's comparison functions. When a match
occurs between Timer 2 and the contents of 16-bit register pair made of CMPH2
& CMPL2, port pin P4.6 will toggle if the corresponding compare match toggle
enable bit CMTE0 (RSTR.6) is set. Similarly on a match, P4.7 will toggle if the
corresponding compare match toggle enable bit CMTE1 (RSTR.7) is set.

Capture Register Zero LSB (CPTL0)

	7	6	5	4	3	2	1	0
SFR ACh	CPTL0.7	CPTL0.6	CPTL0.5	CPTL0.4	CPTL0.3	CPTL0.2	CPTL0.1	CPTL0.0
	RW-0							

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

CPTL0.7-0Capture Register Zero LSB. This register is used to capture the least significantBits 7-08-bit value for the Timer 2's channel 0 capture function. When a transition
occurs on the INT2/CT0 pin, the LSB of Timer 2 is captured in this register on
the rising edge if the CT0=CTCON.0 enable bit is set or on the falling edge if the
 $\overline{CT0}$ =CTCON.1 enable is set. Setting both enable bits will cause a capture to
occur on both edges.

Capture Register One LSB (CPTL1)

	7	6	5	4	3	2	1	0
SFR ADh	CPTL1.7	CPTL1.6	CPTL1.5	CPTL1.4	CPTL1.3	CPTL1.2	CPTL1.1	CPTL1.0
	RW-0							

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

CPTL1.7-0Capture Register One LSB. This register is used to capture the least significantBits 7-08-bit value for the Timer 2's channel 1 capture function. When a transition
occurs on the INT3/CT1 pin, the LSB of Timer 2 is captured in this register on
the rising edge if the CT1=CTCON.1 enable bit is set or on the falling edge if the
 $\overline{CT1}$ =CTCON.3 enable is set. Setting both enable bits will cause a capture to
occur on both edges.

CPTL2.7-0Capture Register Two LSB. This register is used to capture the least significantBits 7-08-bit value for the Timer 2's channel 2 capture function. When a transition
occurs on the INT4/CT2 pin, the LSB of Timer 2 is captured in this register on
the rising edge if the CT2=CTCON.4 enable bit is set or on the falling edge if the
 $\overline{CT2}$ =CTCON.5 enable is set. Setting both enable bits will cause a capture to
occur on both edges.

Capture Register Three LSB (CPTL3)

	7	6	5	4	3	2	1	0
SFR AFh	CPTL3.7	CPTL3.6	CPTL3.5	CPTL3.4	CPTL3.3	CPTL3.2	CPTL3.1	CPTL3.0
	RW-0							

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

CPTL3.7-0Capture Register Three LSB. This register is used to capture the leastBits 7-0significant 8-bit value for the Timer 2's channel 3 capture function. When a
transition occurs on the INT5/CT3 pin, the LSB of Timer 2 is captured in this
register on the rising edge if the CT3=CTCON.6 enable bit is set or on the falling
edge if the $\overline{CT3}$ =CTCON.7 enable is set. Setting both enable bits will cause a
capture to occur on both edges.

Port 3 (P	3)				•					
•	7	6	5	4	3	2	1	0		
SFR B0h	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0		
	RD	WR	T1	T0	INT1	INTO	TXD0	RXD0		
	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1		
	R=Unrestr	icted Read,	W=Unrestrie	cted Write, -	n=Value aft	er Reset				
P3.7-0 Bits 7-0	General Purpose I/O Port 3. This register functions as a general purpose I/O port. In addition, all the pins have an alternative function listed below. Each of the functions is controlled by several other SFRs. The associated Port 3 latch bit must contain a logic one before the pin can be used in its alternate function capacity.									
RD Bit 7		External I strobe to an	External Data Memory Read Strobe. This pin provides an active low read strobe to an external memory or peripheral device.							
WR Bit 6		External I strobe to an	External Data Memory Write Strobe. This pin provides an active low write strobe to an external memory or peripheral device.							
T1 Bit 5		Timer/Co Timer 1 if	unter Exter counter mod	nal Input.	A 1 to 0 tran	sition on thi	s pin will in	crement		
T0 Bit 4		Timer/Co Timer 0 if	unter Exter counter mod	nal Input.	A 1 to 0 tran	sition on thi	s pin will in	crement		
INT1 Bit 3		External I interrupt 1	nterrupt 1. if enabled.	A falling ed	lge/low leve	el on this pin	will cause a	ın external		
INTO Bit 2		External Interrupt 0. A falling edge/low level on this pin will cause an external interrupt 0 if enabled.								
TXD0 Bit 1		Serial Por modes 1, 2	t 0 Transmi , 3 and emit	it. This pin s the synchro	transmits the	e serial port k in serial po	0 data in ser ort mode 0.	ial port		
RXD0 Bit 0		Serial Por modes 1, 2	t 0 Receive. , 3 and is a l	This pin re directiona	ceives the se l data transf	erial port 0 d er pin in seri	lata in serial ial port mode	port e 0.		

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A/D Conv	verter Co	ontrol Re	gister 1 (ADCON1)						
Г	7	6	5	4	3	2	1	0			
SFR B2h	STRT/BSY	EOC	CONT/SS	ADEX	WCQ	WCM	ADON	WCIO			
	R*-0	RW-0	RW-0	RW-0	RW-0	R-0	RW-0	RW-0			
	R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset; *=See description										
STRT/BSY	-	Start/Busy	. When this	bit is chang	ed from a 0	to a 1, an A/	D conversio	n starts. It			
Bit 7		remains set for the duration of the conversion process (regardless of attempts to write 0). Hardware automatically clears this bit upon completion of conversion.									
EOC		End Of Co	onversion. T	his bit is set	bv hardwar	e when a co	nversion is o	complete.			
Bit 6		It also serv This bit mu anytime.	es as an inter 1st be cleared	rupt flag qu by software	alified by W e and can be	CQ and ena set or cleare	bled by EAl ed by softwa) (IE.7). re			
$CONT/\overline{SS}$		Continuou	s/Single Sho	ot. When se	t to 1, the A	/D converter	operates in				
Bit 5		continuous When this	mode and re bit is cleared,	peatedly run , the A/D co	nverter perf	ns once a co orms one co	nversion and	nitiated. 1 stops.			
ADEX Bit 4		A/D Externed by the deter	nal Start. W	hen set, this	s bit allows a the STADC	an A/D conv C pin.	version to be	initiated			
WCQ Bit 3		Window C interrupt to conversion EOC is set.	Comparator occur only v . If this bit is	Qualifier. 1 when both E s cleared, an	f set, this bi OC and WC interrupt wi	t allows an A M bits are s ill occur (if e	A/D converted et at the end enabled) eve	er of a ry time			
WCM Bit 2		Window C conversion This bit is 1	Comparator I result that m not set if ther	Match. Thi atches the c e is no matc	s bit is set b riteria set by h, and it mu	y hardware a WINHI, W st be cleared	at the end of INLO, and l by software	an A/D WCIO. e.			
ADON Bit 1		A/D On. This bit enables (ADON=1) or disables (ADON=0) the A/D function. Changing this bit from a 0 to a 1 requires a warm-up period of 4 μ s before a proper conversion can be performed. This bit can be cleared to save power when no conversion is required, and clearing it aborts any conversion in progress. This action also resets the STRT/BSY bit.									
WCIO Bit 0		Window C function lo limits set b inside these	Compare Insi oks for A/D 1 y WINHI and e limits.	ide/Outside results that a d WINLO. V	• When set are outside o When this bi	to 1, the wir f the windov t is cleared,	ndow compa w bounded b the check is	rison y the for values			

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A/D Converter Control Register 2 (ADCON2)												
	7	6		5	4	3	2	1	0			
SFR B3h	OUTCF	MUX2	M	UX1	MUX0	APS3	APS2	APS1	APS0			
	RW-0	RW-0	RV	W-0	RW-0	RW-0	RW-0	RW-0	RW-0			
	R=Unrestr	icted Read	, W=Uı	nrestricte	ed Write, -1	n=Value afte	er Reset					
OUTCF		Output Conversion Format. When this bit is set, the ADMSB register contains										
Bit 7		the two most significant bits of the 10-bit conversion in the two least significant										
		bit positions, and the remaining bits of the conversion. When the OUTCE bit is										
		cleared, th	he ADN	ASB will	l contain th	ne 8 most sig	gnificant bits	s and ADLS	B will			
		contain th	e 8 lea	st signifi	cant bits o	f the conver	sion.					
MUX2:0		Multiplexer Select Bits. These bits select the A/D analog channel										
-Bits 6-4		(ADC7:ADC0) that will be sampled and converted.										
		MUX2 I	MUX1	MUX0	Chan	nel						
		0	0	0	ADC	0						
		0	0	1	ADC	1						
		0	1	0	ADC	2						
		0	1	1	ADC	3						
		1	0	0	ADC	4						
		1	0	1	ADC	5						
		1	1	0	ADC	6						
		1	1	1	ADC	7						
APS3:0		A/D Cloc	k Pres	caler Sel	lect Bits.	These bits d	etermine the	A/D's cloc	k			
Bits 3-0	prescaler value "N" where this clock period is defined as:											
					t _{ACLK}	$= t_{MCLK} x$ (1)	N+1)					
		where t _{M0}	_{CLK} is th	e CPU's	Machine	Cycle Clock	t (the oscilla	tor or crysta	l period			
		multiplied by 1, 2, 4, 64 or 1024 as determined by the $4X/\overline{2X}$ and CD1:CD0 bits										
		of the PM	IR regis	ster). The	e period of	t _{ACLK} must	be in the rar	nge:				
					1.0 us <	$\leq t_{ACLK} \leq t_{ACLK}$	6.25us					

A/D Result Most Significant Byte (ADMSB)

SFR B4h	7	6	5	4	3	2	1	0
	ADMSB.7	ADMSB.						
		6	5	4	3	2	1	0
	R*-0	R*-0	R*-0	R*-0	R*-0	R*-0	R*-0	R*-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset; *=see description

ADMSB7:0A/D Result Most Significant Byte. This register contains either the mostBit 7-0significant 8 or 2 bits of the 10-bit A/D conversion result depending on the setting
of OUTCF (ADCON2.7). Note that due to the specific implementation of this
register, reading back a value written by software will not return identical results.
Therefore, writing this register has no practical purpose and should be avoided.

A/D Result Least Significant Byte (ADLSB)

	7	6	5	4	3	2	1	0
SFR B5h	ADLSB.7	ADLSB.						
		6	5	4	3	2	1	0
	R*-0	R*-0	R*-0	R*-0	R*-0	R*-0	R*-0	R*-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset; *=see description

ADLSB7:0A/D Result Least Significant Byte. This register contains the least significant 8Bit 7-0bits of the A/D conversion. Note that due to the specific implementation of this
register, reading back a value written by software will not return identical results.
Therefore, writing this register has no practical purpose and should be avoided.

A/D Window Comparator High Byte (WINHI)

	7	6	5	4	3	2	1	0
SFR B6h	WINHI.7	WINHI.6	WINHI.5	WINHI.4	WINHI.3	WINHI.2	WINHI.1	WINHI.0
	RW-0							

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

WINHI.7:0A/D Window Comparator High Byte. This register contains the upper limit forBit 7-0the window comparison function. This 8-bit value is compared to the most
significant 8-bits of the previous A/D conversion result.

A/D Window Comparator Low Byte (WINLO)

	7	6	5	4	3	2	1	0
SFR B7h	WINLO.7	WINLO.6	WINLO.5	WINLO.4	WINLO.3	WINLO.2	WINLO.1	WINLO.0
	RW-0							

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

WINLO.7:0A/D Window Comparator Low Byte. This register contains the lower limit forBit 7-0the window comparison function. This 8-bit value is compared to the most
significant 8-bits of the previous A/D conversion result.

Interrup	t Priority	′ (IP)						
	7	6	5	4	3	2	1	0
SFR B8h	-	PAD	PS1	PS0	PT1	PX1	PT0	PX0
	-	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0
	R=Unrestr	icted Read,	W=Unrestric	cted Write, -	n=Value aft	er Reset		
Bit 7		Reserved.	Read data is	s indetermin	ate.			
PAD		A/D Intern	r upt. This b	oit controls th	ne priority o	f the A/D Co	onverter inte	rrupt.
Bit 6		0 = A/D in	terrupt prior	ity is determ	ined by the	natural prior	rity order.	
		1 = A/D in	terrupt is a h	nigh priority	interrupt.			
PS1		Serial Por	t 1 Interrup	ot. This bit o	controls the	priority of th	e serial port	: 1
Bit 6		interrupt.						
		$0 = $ Serial μ	port 1 priorit	y is determi	ned by the n	atural priori	ty order.	
		1 = Serial p	port 1 is a hi	gh priority i	nterrupt.			
PS0		Serial Por	t 0 Interrup	ot. This bit o	controls the	priority of th	e serial port	. 0
Bit 4		interrupt.						
		$0 = $ Serial μ	port 0 priorit	y is determi	ned by the n	atural priori	ty order.	
		1 = Serial I	port 0 is a hi	gh priority i	nterrupt.			
PT1		Timer 1 Ir	nterrupt. T	his bit contro	ols the prior	ty of Timer	1 interrupt.	
Bit 3		0 = Timer	1 is determin	ned by the na	atural priorit	y order.		
		1 = Timer	1 is a high p	riority interr	upt.			
PX1		External I	nterrupt 1.	This bit con	ntrols the pri	ority of exte	ernal interrup	ot 1.
Bit 2		0 = Externa	al interrupt 1	l is determin	ed by the na	tural priorit	y order.	
		1 = Externa	al interrupt 1	l is a high pr	iority interr	upt.		
PT0		Timer 0 Ir	nterrupt. T	his bit contro	ols the prior	ity of Timer	0 interrupt.	
Bit 1		0 = Timer	0 is determin	ned by the na	atural priorit	y order.		
		1 = Timer	0 is a high p	riority interr	upt.			
PX0		External I	nterrupt 0.	This bit con	ntrols the pri	ority of exte	ernal interrup	pt 0.
Bit 0		0 = Externa	al interrupt () is determin	ed by the na	tural priorit	y order.	
		1 = Externation	al interrupt () is a high pr	iority interr	upt.		

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Slave Address Mask Enable Register 0 (SADEN0)								
	7	6	5	4	3	2	1	0
SFR B9h	SADEN0	SADEN0	SADEN0	SADEN0	SADEN0	SADEN0	SADEN0	SADEN0
	.7	.6	.5	.4	.3	.2	.1	.0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

SADEN0.7-0 Slave Address Mask Enable Register 0. This register functions as a mask when comparing serial port 0 addresses for automatic address recognition. When a bit Bits 7-0 in this register is set, the corresponding bit location in the SADDR0 register will be exactly compared with the incoming serial port 0 data to determine if a receiver interrupt should be generated. When a bit in this register is cleared, the corresponding bit in the SADDR0 register becomes a don't care and is not compared against the incoming data. All incoming data will generate a receiver interrupt (if enabled) when this register is cleared.

Slave Address Mask Enable Register 1 (SADEN1)

	7	6	5	4	3	2	1	0
SFR BAh	SADEN1							
	.7	.6	.5	.4	.3	.2	.1	.0
	RW-0							

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

SADEN1.7-0 Slave Address Mask Enable Register 1. This register functions as a mask when Bits 7-0 comparing serial port 1 addresses for automatic address recognition. When a bit in this register is set, the corresponding bit location in the SADDR1 register will be exactly compared with the incoming serial port 1 data to determine if a receiver interrupt should be generated. When a bit in this register is cleared, the corresponding bit in the SADDR1 register becomes a don't care and is not compared against the incoming data. All incoming data will generate a receiver interrupt (if enabled) when this register is cleared.

Timer 2 (Control	(T2CC	DN)			-			
	7	6	2	5	4	3	2	1	0
SFR BEh	TF2	EXF	2 R0	CLK	TCLK	EXEN2	TR2	$C/\overline{T2}$	$\overline{\text{RL2}}$
	RW-0	RW-	0 R	W-0	RW-0	RW-0	RW-0	RW-0	RW-0
	R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset								
TF2 Bit 7		Timer FFFFh cleared	Timer 2 Overflow Flag. This flag will be set when Timer 2 overflows from FFFFh or the count equal to the capture register in down count mode. It must be cleared by software. TF2 will only be set if RCLK and TCLK are both cleared to 0						
EXF2		Timer	2 Extern	al Flag	. A negativ	e transition	on the T2EX	x pin or time	r 2
Bit 6		underf	low/overf	low will	l cause this	flag to be se	et based on	$\overline{RL2}$, EXEN	2, and
		DCEN by soft	(see table ware Set	e below, ting this). If set by a bit in soft	a negative tr ware or dete	ansition, this	s flag must t	tion on
		the T2	EX pin w	ill force	a timer int	errupt if ena	bled.	gative trans	
		RL2	EXEN2	DCEN	RESUL	<u> </u>			
		1	0	X	Negative bit.	transitions	on T2EX v	vill not affe	ect this
		1	1	Х	Negative	transitions of	on T2EX wi	ll set this bit	•
		0	0	0	Negative bit.	transitions	on T2EX v	vill not affe	ect this
		0	1	0	Negative	transitions of	on T2EX wi	ll set this bit	•
		0	Х	1	Bit toggle and can b mode, E2	es whenever be used as a KF2 will not	timer 2 und 17 th bit of re cause an int	erflows/ove solution. In cerrupt.	rflows this
RCLK Bit 5		Receive receivi 0 = Tin 1 = Tin Setting will op	e Clock ng data in ner 1 ove ner 2 ove this bit v erate from	Flag. The serial reflow is reflow is reflow is will force reflow a divide the series of the series o	his bit deter nodes 1 or used to det used to det e timer 2 in de by 2 of t	mines the se 3. termine rece termine rece to baud rate he external	erial port 0 ti iver baud ra iver baud ra generation clock.	mebase whe te for serial te for serial mode. The t	en port 0. port 0. imer
TCLK Bit 4		Trans transm	mit Clocl itting dat	x Flag. [a in seria	This bit det al modes 1	ermines the or 3.	serial port 0	timebase w	hen
DR		0 = Tir	ner 1 ove	rflow is	used to de	termine tran	smitter baud	rate for seri	al port 0.
		1 = Tin Setting operate	ner 2 ove this bit v from a c	rflow is vill force livide by	used to de e timer 2 in 2 of the e	termine tran to baud rate xternal clock	smitter baud generation	rate for seri mode. The t	al port 0. imer will
EXEN2 Bit 3		Timer if Time	2 Extern er 2 is not	al Enal	ole. This bi ing baud ra	t enables the ates for the s	e reload func erial port.	tion on the	Г2EX pin
		0 = Tir	ner 2 will	lignore	all external	events at T	2EX.		
		1 = Tin the T2	ner 2 will EX pin.	l capture	e or reload	a value if a r	negative tran	sition is det	ected on

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TR2	Timer 2 Run Control. This bit enables/disables the operation of timer 2. Halting
Bit 2	this timer will preserve the current count in TH2, TL2.
	0 = Timer 2 is halted.
	1 = Timer 2 is enabled.
$C/\overline{T2}$	Counter/Timer Select. This bit determines whether timer 2 will function as a
Bit 1	timer or counter. Independent of this bit, timer 2 runs at 2 clocks per tick when used in either baud rate generator or clock output mode.
	0 = Timer 2 function as a timer. The speed of timer 2 is determined by the T2M bit (CKCON.5).
	1 = Timer 2 will count negative transitions on the T2 pin.
RL2	Reload Enable. This bit determines if the reload function will be used for timer
Bit 0	function in an auto-reload mode following each overflow.
	0 = Auto-reloads will occur when timer 2 overflows or a falling edge is detected on T2EX if EXEN2=1.
	1 = Timer 2 reload function is disabled.

Timer 2 Mode (T2MOD)

	7	6	5	4	3	2	1	0
SFR BFh	-	-	-	-	-	-	T2OE	DCEN
							RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

	DCEN	T2EX	DIRECTION	
DCEN Bit 0	Down Count Enab direction that timer	le. This bit, in con 2 counts in 16-bit	junction with the T auto-reload mode.	2EX pin, controls the
	1 = Timer 2 will drives rollovers will not ca	ve the T2 pin with use interrupts in th	a clock output if C nis case.	/T2=0. Also, timer 2
	0 = The T2 pin function timer 2.	ctions as either a sta	andard port pin or a	as a counter input for
T2OE Bit 1	Timer 2 Output E the T2 pin.	nable. This bit ena	bles/disables the cl	ock output function of
Bits 7-2	Reserved. Read dat	a will be indetermi	nate.	

DCEN	T2EX	DIRECTION
1	1	Up
1	0	Down
0	Х	Up

Parallel	/O Port	Four (P4)			-					
	7	6	5	4	3	2	1	0		
SFR C0h	P4.7 CMT1	P4.6 CMT0	P4.5 CMSR5	P4.4 CMSR4	P4.3 CMSR3	P4.2 CMSR2	P4.1 CMSR1	P4.0 CMSR0		
	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1		
	R=Unrestr	icted Read,	W=Unrestric	cted Write, -	n=Value aft	er Reset				
P4.7-0		General P	urpose I/O	Port Four.	This registe	r functions a	s a general	purpose		
Bits 7-0		I/O port. If of the func bit must co capacity.	n addition, a tions is cont intain a logic	ll the pins h rolled by sev c one before	ave an altern veral other S the pin can	native functi SFRs. The as be used in it	on listed bel sociated Por s alternate fu	ow. Each t 4 latch inction		
CMT1 Bit 7		Compare 2 Timer 2 co Timer 2 an (RSTR.7) i	Compare Match Toggle Pin. This pin alternately serves as an output for the Timer 2 compare function. This pin will toggle when a match occurs between Timer 2 and compare registers CMPH2:CMPL2 if the enable bit CMTE1 (RSTR.7) is set.							
CMT0 Bit 6		Compare 2 Timer 2 co Timer 2 an (RSTR.6) i	Compare Match Toggle Pin. This pin alternately serves as an output for the Timer 2 compare function. This pin will toggle when a match occurs between Timer 2 and compare registers CMPH2:CMPL2 if the enable bit CMTE0 (RSTR.6) is set.							
CMSR5 Bit 5		Compare Match Set/Reset Pin 5. This pin alternately serves as an output for the Timer 2 compare function. It will be set if CMS5 (SETR.5) is 1 and a match occurs between Timer 2 and 16-bit compare register CMPH0:CMPL0. It will be reset if CMR5 (RSTR.5) is 1 and a match occurs between Timer 2 and 16-bit compare register CMPH1:CMPL1.								
CMSR4 Bit 4		Compare Match Set/Reset Pin 4. This pin alternately serves as an output for the Timer 2 compare function. It will be set if CMS4 (SETR.4) is 1 and a match occurs between Timer 2 and 16-bit compare register CMPH0:CMPL0. It will be reset if CMR4 (RSTR.4) is 1 and a match occurs between Timer 2 and 16-bit compare register CMPH1:CMPL1.								
CMSR3 Bit 3		Compare 2 the Timer 2 occurs betw reset if CM compare re	Match Set/J 2 compare fu ween Timer IR3 (RSTR. 2 egister CMP	Reset Pin 3. Inction. It w 2 and 16-bit 3) is 1 and a H1:CMPL1.	This pin ali ill be set if C compare rea match occu	ternately ser CMS3 (SET) gister CMPH rs between 7	ves as an ou R.3) is 1 and I0:CMPL0. Fimer 2 and	tput for a match It will be 16-bit		

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Compare Match Set/Reset Pin 2. This pin alternately serves as an output for the Timer 2 compare function. It will be set if CMS2 (SETR.2) is 1 and a match occurs between Timer 2 and 16-bit compare register CMPH0:CMPL0. It will be reset if CMR2 (RSTR.2) is 1 and a match occurs between Timer 2 and 16-bit compare register CMPH1:CMPL1.
Compare Match Set/Reset Pin 1. This pin alternately serves as an output for the Timer 2 compare function. It will be set if CMS1 (SETR.1) is 1 and a match occurs between Timer 2 and 16-bit compare register CMPH0:CMPL0. It will be reset if CMR1 (RSTR.1) is 1 and a match occurs between Timer 2 and 16-bit compare register CMPH1:CMPL1.
Compare Match Set/Reset Pin 0. This pin alternately serves as an output for the Timer 2 compare function. It will be set if CMS0 (SETR.0) is 1 and a match occurs between Timer 2 and 16-bit compare register CMPH0:CMPL0. It will be reset if CMR0 (RSTR.0) is 1 and a match occurs between Timer 2 and 16-bit compare register CMPH1:CMPL1.

ROM Size Select (ROMSIZE)

	7	6	5	4	3	2	1	0
SFR C2h	-	-	-	-	-	RS2	RS1	RS0
						RT-1	RT-0	RT-0

R=Unrestricted Read, W=Unrestricted Write, T=Timed Access Write Only, -n=Value after Reset

Bits 7-3 These bits are reserved. Read data is indeterminate.

ROMSIZE.2-0ROM Size Select 2-0. This register is used to select the maximum on-chip
decoded address for ROM. Care must be taken that the memory location of the
current program counter will be valid both before and after modification. These
bits can only be modified using a timed access procedure. The EA pin will
override the function of these bits when asserted, forcing the device to access
external program memory only. Configuring this register to a setting that exceeds
the maximum amount of internal memory may corrupt device operation. These
bits will default on reset to the maximum amount of internal program memory
(i.e., 8K for DS87C550).

RS2	RS1	RS0	MAXIMUM ON-CHIP ROM ADDRESS								
0	0	0	0KB/Disable on-chip ROM								
0	0	1	1KB/03FFh								
0	1	0	2KB/07FFh								
0	1	1	4KB/0FFFh								
1	0	0	8KB/1FFFh (Default Value on Reset DS87C550)								
1	0	1	16KB/3FFFh								
1	1	0	132KB/7FFFh								
1	1	1	64KB/FFFFh								
Parallel I/O Port Five (P5)											
-----------------------------	---	--------------	--------------	--------------	---------------	---------------	--------------	--------------	--	--	--
	7	6	5	4	3	2	1	0			
SFR C4h	P5.7 ADC7	P5.6 ADC6	P5.5 ADC5	P5.4 ADC4	P5.3 ADC3	P5.2 ADC2	P5.1 ADC1	P5.0 ADC0			
	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1			
P5.7-0 Bits 7-0	R=Unrestricted Read, W=Unrestricted Write, -n=Value after ResetP5.7-0General Purpose I/O Port Five. This register functions as an open drain 8-bit bi-directional port. In addition, all the pins have an alternative function listed below. Each of the functions is controlled by several other SFRs. The associated Port 5 latch bit must contain a logic one before the pin can be used in its alternate function capacity, otherwise the pin is forced to a strong zero.										
ADC7-AD	C0	A/D Conv	erter Input	Pins. These	e pins provid	le the inputs	to the 8 ana	log			

ADC7-ADC0A/D Converter Input Pins. These pins provide the inputsBits 7-0multiplexer channels (7-0) of the A/D converter.

Status Register (STATUS)

otatus r	register		' /									
	7	6	5	4	3	2	1	0				
SFR C5	PIP	HIP	LIP	-	SPTA1	SPRA1	SPTA0	SPRA0				
	R-0	R-0	R-0		R-0	R-0	R-0	R-0				
R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset, *=See description												
PIP		Power Fai	l Priority I	nterrupt Sta	atus. When	set, this bit i	ndicates that	at software				
Bit 7	is currently servicing a power-fail interrupt. It is cleared when the program executes the corresponding RETI instruction.											
HP Bit 6		High Priority Interrupt Status. When set, this bit indicates that software is currently servicing a high priority interrupt. It is cleared when the program executes the corresponding RETI instruction.										
LIP Bit 5		Low Priority Interrupt Status. When set, this bit indicates that software is currently servicing a low priority interrupt. It is cleared when the program executes the corresponding RETI instruction.										
Bit 4		Reserved.										
SPTA1 Bit 3		Serial Por is currently hardware s while this b	t 1 Transm being trans ets the TI_1 bit is set or s	it Activity M mitted by se bit. Do not serial port da	Monitor. We trial port 1. I alter the Cloat analysis of the cloa	hen set, this t is cleared v ck Divide C ost.	bit indicates when the int ontrol (CD1	that data ernal :0) bits				

SPRA1 Bit 2	Serial Port 1 Receive Activity Monitor. When set, this bit indicates that data is currently being received by serial port 1. It is cleared when the internal hardware sets the RI_1 bit. Do not alter the Clock Divide Control bits (CD1:0) while this bit is set or serial port data may be lost.
SPTA0 Bit 1	Serial Port 0 Transmit Activity Monitor. When set, this bit indicates that data is currently being transmitted by serial port 0. It is cleared when the internal hardware sets the TI_0 bit. Do not alter the Clock Divide Control bits (CD1:0) while this bit is set or serial port data may be lost.
SPRA0 Bit 0	Serial Port 0 Receive Activity Monitor. When set, this bit indicates that data is currently being received by serial port 0. It is cleared when the internal hardware sets the RI_0 bit. Do not alter the Clock Divide Control bits (CD1:0) while this bit is set or serial port data may be lost.

Timed Access Register (TA)

	7	6	5	4	3	2	1	0
SFR C7h	TA.7	TA.6	TA.5	TA.4	TA.3	TA.2	TA.1	TA.0
	W-1							

W=Unrestricted Write, -n=Value after Reset

TA.7-0Timed Access Register. Correctly accessing this register permits modificationBits 7-0of timed access protected bits. Write AAh to this register first, followed within 3cycles by writing 55h. Timed access protected bits can then be modified for aperiod of 3 cycles measured from the writing of the 55h.

External	Interrup	ot Flag Re	egister (T	'2IR)							
	7	6	5	4	3	2	1	0			
SFR C8h	-	CM2F	CM1F	CM0F	IE5/CF3	IE4/CF2	IE3/CF2	IE2/CF0			
	-	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0			
	R=Unrestr	icted Read,	W=Unrestri	cted Write, -	n=Value aft	er Reset					
Bit 7		Reserved.	Read data is	indetermina	ate.						
CM2F		Compare 1	Match Inte	rrupt 2 Flag	g. This bit w	vill cause an	interrupt if	enabled by			
Bit 6		ECM2 (EIE.6) when a match occurs between Timer 2 and the contents of Compare Match 2 registers (CMPH2:CMPL2). Setting this bit with software will cause an interrupt if enabled, and software must always clear this bit.									
CM1F Bit 5		Compare ECM1 (EII Compare M cause an in	Match Inte E.5) when a Aatch 1 regi terrupt if en	rrupt 1 Flag match occur sters (CMPH abled, and s	g. This bit w rs between T 11:CMPL1). oftware mus	vill cause an Fimer 2 and to Setting this at always cle	interrupt if the contents s bit with so ar this bit.	enabled by of ftware will			
CM0F		Compare	Match Inte	rrupt 0 Flag	g. This bit w	ill cause an i	interrupt if e	nabled by			
Bit 4		ECM0 = EIE.4) when a match occurs between Timer 2 and the contents of Compare Match 0 registers (CMPH1 & CMPL1). Setting this bit with software will cause an interrupt if enabled, and software must always clear this bit.									
IE5/CF3External Interrupt 5 or Capture Interrupt 3 Flag. This bit serveBit 3interrupt flag for External Interrupt 5 and alternatively for the capture (capture register 3) of Timer 2. If either capture trigger bit CT3 or (CTCON.6 or 7) is set, then the capture function register 3 is enable will be set when a capture occurs. If neither of these bits are set, the a flag for external interrupt 5. Regardless of meaning, this bit will interrupt to occur only if the enable bit EX5/EC3 (EIE.3) is set. Set								an unction and this bit t serves as e an this bit			
IE4/CF2 Bit 2		with softwarthis bit. External I interrupt flat (capture reg	are will caus nterrupt 4 ag for Exter gister 2) of '	se an interrup or Capture nal Interrupt Timer 2. If e	pt (if enable Interrupt 2 t 4 and alterr ither capture	d), and softw Flag. This natively for t e trigger bit (vare must al bit serves as he capture f CT2 or CT2	ways clear s an unction			
		(CTCON.4 will be set a flag for e interrupt to with softwa this bit	or 5) is set, when a capt xternal inter occur only are will caus	, then the cap cure occurs. I crupt 4. Rega if the enable se an interrup	oture function If neither of ardless of me bit EX4/EC pt (if enable	on register 2 these bits ar eaning, this b C2 (EIE.2) is d), and softw	is enabled, a e set, this bi bit will cause s set. Setting vare must al	and this bit t serves as e an this bit ways clear			

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IE3/CF1	External Interrupt 3 or Capture Interrupt 1 Flag. This bit serves as an
Bit 1	interrupt flag for External Interrupt 3 and alternatively for the capture function
	(capture register 1) of Timer 2. If either capture trigger bit CT1 or $\overline{\text{CT1}}$
	(CTCON.2 or 3) is set, then the capture function register 1 is enabled, and this bit
	will be set when a capture occurs. If neither of these bits are set, the this bit serves
	as a flag for external interrupt 3. Regardless of meaning, this bit will cause an
	interrupt to occur only if the enable bit EX3/EC1 (EIE.1) is set. Setting this bit with software will cause an interrupt (if enabled), and software must always clear
	this bit
IE2/CF0	External Interrupt 2 or Capture Interrupt 0. This bit serves as an interrupt
Bit 0	flag for External Interrupt 2 and alternatively for the capture function (capture
	register 0) of Timer 2. If either capture trigger bit CT0 or CT0\ (CTCON.0 or 2)
	is set, then the capture function register 0 is enabled, and this bit will be set when
	a capture occurs. If neither of these bits are set, the this bit serves as a flag for
	external interrupt 2. Regardless of meaning, this bit will cause an interrupt to
	will cause an interrupt (if anabled), and software must always clear this bit
	will cause an interrupt (if enabled), and software must always clear tills bit.

Compare Register 0 MSB (CMPH0)

	7	6	5	4	3	2	1	0
SFR C9h	CMPH0.7	CMPH0.6	CMPH0.5	CMPH0.4	CMPH0.3	CMPH0.2	CMPH0.1	CMPH0.0
	RW-0							

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

CMPH0.7-0 Compare Register 0 MSB. This register is used to store the most significant 8bit value for one of the three available Timer 2 comparison functions. Register Bits 7-0 CMPL0 (A9h) contains the least significant byte of this compare function. When a 16-bit match occurs, a Timer 2 interrupt occurs if enabled, and port pins P4.5 through P4.0 are set if the corresponding enable bits are set in the SETR (EEh) register.

Compare Register 1 MSB (CMPH1)

	7	6	5	4	3	2	1	0
SFR CAh	CMPH1.7	CMPH1.6	CMPH1.5	CMPH1.4	CMPH1.3	CMPH1.2	CMPH1.1	CMPH1.0
	RW-0							

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

CMPH1.7-0 Compare Register 1 MSB. This register is used to store the most significant 8bit value for one of the three available Timer 2 comparison functions. Register Bits 7-0 CMPL1 (AAh) contains the least significant byte of this compare function. When a 16-bit match occurs, a Timer 2 interrupt occurs if enabled, and port pins P4.5 through P4.0 are set if the corresponding enable bits are set in the SETR (EEh) register.

			DS87C5	550 High-Sp	eed Microco	ontroller Us	er's Guide S	upplement		
Compare Register 2 MSB (CMPH2)										
	7	6	5	4	3	2	1	0		
SFR CBh	CMPH2.7	CMPH2.6	CMPH2.5	CMPH2.4	CMPH2.3	CMPH2.2	CMPH2.1	CMPH2.0		
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0		

CMPH2.7-0Compare Register 2 MSB. This register is used to store the most significant 8-
bit value for one of the three available Timer 2 comparison functions. Register
CMPL2 (ABh) contains the least significant byte of this compare function. When
a 16-bit match occurs, a Timer 2 interrupt is occurs if enabled and port pins P4.7
or P4.6 are toggled if the corresponding enable bits CMTE1 or CMTE0 are set in
the RSTR (EFh) register.

Capture Register 0 MSB (CPTH0)

	7	6	5	4	3	2	1	0
SFR CCh	CPTH0.7	CPTH0.6	CPTH0.5	CPTH0.4	CPTH0.3	CPTH0.2	CPTH0.1	CPTH0.0
	RW-0							

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

CPTH0.7-0Capture Register 2 MSB. This register loads the most significant 8-bit value ofBits 7-0Timer 2 when a transition occurs on the INT2/CT0 pin if the corresponding
capture trigger is enabled by the appropriate bit in register CTCON (EBh). The
least significant 8-bit value is loaded into register CPTL0 (ACh).

Capture Register 1 MSB (CPTH1)

	7	6	5	4	3	2	1	0
SFR CDh	CPTH1.7	CPTH1.6	CPTH1.5	CPTH1.4	CPTH1.3	CPTH1.2	CPTH1.1	CPT10.0
	RW-0							

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

CPTH1.7-0Capture Register 1 MSB. This register loads the most significant 8-bit value ofBits 7-0Timer 2 when a transition occurs on the INT3/CT1 pin if the corresponding
capture trigger is enabled by the appropriate bit in register CTCON (EBh). The
least significant 8-bit value is loaded into register CPTL1 (ADh).

Capture	Capture Register 2 MSB (CPTH2)											
	7	6	5	4	3	2	1	0				
SFR CEh	CPTH2.7	CPTH2.6	CPTH2.5	CPTH2.4	CPTH2.3	CPTH2.2	CPTH2.1	CPTH2.0				
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0				

CPTH2.7-0Capture Register 2 MSB. This register loads the most significant 8-bit value ofBits 7-0Timer 2 when a transition occurs on the INT4/CT2 pin if the corresponding
capture trigger is enabled by the appropriate bit in register CTCON (EBh). The
least significant 8-bit value is loaded into register CPTL2 (AEh).

Capture Register 3 MSB (CPTH3)

	7	6	5	4	3	2	1	0
SFR CFh	CPTH3.7	CPTH3.6	CPTH3.5	CPTH3.4	CPTH3.3	CPTH3.2	CPTH3.1	CPTH3.0
	RW-0							

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

CPTH3.7-0 Capture Register 3 MSB. This register loads the most significant 8-bit value of Timer 2 when a transition occurs on the INT5/CT3 pin if the corresponding capture trigger is enabled by the appropriate bit in register CTCON (EBh). The least significant 8-bit value is loaded into register CPTL3 (AEh).

			DS87C	550 High-S	peed Microco	ontroller Us	er's Guide	Supplement
Program	Status	Word (PS	6W)					
•	7	6	5	4	3	2	1	0
SFR D0h	CY	AC	F0	RS1	RS0	0V	F1	PARITY
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0
	R=Unrestr	ricted Read, V	W=Unrestrie	cted Write, -	n=Value afte	er Reset		
CY		Carry Flag	g. This bit is	s set when if	the last arith	metic opera	ation resulte	d in a carry
Bit 7		(during add all arithme	lition) or a b tic operatior	oorrow (duri 18.	ng subtractio	on). Otherw	ise it is clea	red to 0 by
AC		Auxiliary	Carry Flag	. This bit is	set to 1 if the	e last arithm	etic operation	on resulted
Bit 6		in a carry i order nibbl	nto (during e. Otherwise	addition), or e it is cleare	a borrow (d d to 0 by all	uring subtra arithmetic c	operations.	the high
F0 Bit 5		User Flag	0. This is a 1	bit-addressa	ble, general _j	purpose flag	g for softwa	re control.
RS1, RS0 Bits 4-3		Register B during regi	ank Select ster accesse	1–0. These I s.	oits select wh	nich register	bank is add	dressed
		RS1	RS0	REGIST	TER BANK	A	DDRESS	
		0	0		0	(00h - 07h	
		0	1		1	(08h – 0Fh	
		1	0		2		10h – 17h	
		1	1		3		18h – 1Fh	
OV Bit 2		Overflow carry (addi Otherwise	Flag. This b tion), borrov it is cleared	it is set to 1 w (subtraction to 0 by all a	if the last ari on), or overfl rithmetic op	ithmetic ope ow (multip) erations.	eration resul	lted in a).
F1 Bit 1		User Flag	1. This is a [bit-addressa	ble, general j	purpose flag	g for softwa	re control.
PARITY Bit 0		Parity Fla	g. This bit is or is 1 (odd j	s set to 1 if t parity); and	he modulo-2 cleared to 0 o	sum of the	eight bits o ity.	f the

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PWM0 Frequency Generator Register (PW0FG)									
	7	6	5	4	3	2	1	0	
SFR D2h	PW0FG.7	PW0FG.6	PW0FG.5	PW0FG.4	PW0FG.3	PW0FG.2	PW0FG.1	PW0FG.0	
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	

PW0FG.7-0PWM0 Clock Generator Register. This register contains the user definedBitS 7-6value, N which determines the repetition rate for 8-bit PWM channel 0 or 16-bitPWM channel 0 if PWEO=1. This repetition rate (frequency) is given by the
equation: Prescaler-Output-Frequency / (N+1).

PWM1 Frequency Generator Register (PW1FG)

	7	6	5	4	3	2	1	0
SFR D3h	PW1FG.7	PW1FG.6	PW1FG.5	PW1FG.4	PW1FG.3	PW1FG.2	PW1FG.1	PW1FG.0
	RW-0							

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

PW1FG.7-0PWM1 Clock Generator Register. This register contains the user definedBitS 7-6value, N which determines the repetition rate for 8-bit PWM channel 1. This
repetition rate (frequency) is given by the equation: Prescaler-Output-Frequency /
(N+1). This register is not used in 16-bit PWM operations.

PWM2 Frequency Generator Register (PW2FG)

	7	6	5	4	3	2	1	0
SFR D4h	PW2FG.7	PW2FG.6	PW2FG.5	PW2FG.4	PW2FG.3	PW2FG.2	PW2FG.1	PW2FG.0
	RW-0							

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

PW2FG.7-0PWM2 Clock Generator Register. This register contains the user definedBitS 7-6value, N which determines the repetition rate for 8-bit PWM channel 2 or 16-bitPWM channel 1 if PWE1=1. This repetition rate (frequency) is given by the
equation: Prescaler-Output-Frequency / (N+1).

			DS87C5	50 High-Sp	eed Microco	ontroller Use	er's Guide S	upplement		
PWM3 Frequency Generator Register (PW3FG)										
	7	6	5	4	3	2	1	0		
SFR D5h	PW3FG.7	PW3FG.6	PW3FG.5	PW3FG.4	PW3FG.3	PW3FG.2	PW3FG.1	PW3FG.0		
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0		

PW3FG.7-0PWM3 Clock Generator Register. This register contains the user definedBitS 7-6value, N which determines the repetition rate for 8-bit PWM channel 3. This
repetition rate (frequency) is given by the equation: Prescaler-Output-Frequency /
(N+1). This register is not used in 16-bit PWM operations.

16-Bit PWM Mode Enable and A/D Reference Select (PWMADR)

	7	6	5	4	3	2	1	0			
SFR D6h	ADRS	-	-	-	-	-	PWE1	PWE0			
	RW-0	-	-	-	-	-	RW-0	RW-0			
	R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset										
ADRS Bit 7	A/D Reference Select. When set to 1, this bit selects an external source provided on pins V_{REF} + and V_{REF} - as the voltage reference for the A/D converter. When cleared to 0, the internal bandgap provides the voltage reference for the A/D.										
Bits 6-2	R	Reserved. Read data will be indeterminate.									
PWE1 Bit 1	16-Bit PWM Enable 1. Setting this bit to 1 enables the 16-bit PWM channel 1. Clearing this bit disables 16-bit mode and enables 8-bit mode.										
PWE0 Bit 1	1 C	6-Bit PWM Clearing thi	A Enable (s bit disabl	0. Setting th es 16-bit mo	is bit to 1 en de and enab	ables the 16 les 8-bit mo	-bit PWM c de.	hannel 0.			

Serial Po	ort Control	(SCON	1)					
	7	6	5	4	3	2	1	0
SFR D8h	SM0/FE_1	SM1_1	SM2_1	REN_1	TB8_1	RB8_1	TI_1	RI_1
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

SM0-2Serial Port 1 Mode. These bits control the mode of serial port 1 as shownBits 7-5below. In addition, the SM0 and SM2 bits have secondary functions as shown
below.

SM0	SM1	SM2	MODE	FUNCTION	LENGTH	PERIOD
0	0	0	0	Synchronous	8 bits	12t _{CLK}
0	0	1	0	Synchronous	8 bits	4t _{CLK}
0	1	Х	1	Asynchronous	10 bits	Timer 1 baud rate equation
1	0	0	2	Asynchronous	11 bits	$\begin{array}{c} 64t_{CLK} (SMOD=0) \\ 32t_{CLK} (SMOD=1) \end{array}$
1	0	1	2	Asynchronous w/ Multiprocessor communication	11 bits	64t _{CLK} (SMOD=0) 32t _{CLK} (SMOD=1)
1	1	0	3	Asynchronous	11 bits	Timer 1 baud rate equation
1	1	1	3	Asynchronous w/ Multiprocessor communication	11 bits	Timer 1 baud rate equation

SM0/FE_1Framing Error Flag. When SMOD0 (PCON.6)=0, this bit (SM0) is used toBit 7select the mode for serial port 1. When SMOD0 (PCON.6)=1, this bit (FE) willbe set upon detection of an invalid stop bit. When used as FE, this bit must becleared in software. Once the SMOD0 bit is set, modifications to this bit will notaffect the serial port mode settings. Although accessed from the same register,internally the data for bits SM0 and FE are stored in different locations.

- SM1_1 No alternate function.
- Bit 6

SM2-2Multiple CPU Communications. The function of this bit is dependent on the
serial port 1 mode.

- Mode 0: Selects 12 t_{CLK} or 4t_{CLK} period for synchronous port 1 data transfers.
- Mode 1: When this bit is set, reception is ignored (RI_1 is not set) if invalid stop bit received.
- Mode 2/3: When this bit is set, multiprocessor communications are enabled in mode 2 and 3. This will prevent RI_1 from being set, and an interrupt being asserted, if the 9th bit received is not 1.

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REN_1	Receive Enable. This bit enables/disables the serial port 1 receiver shift register.
Bit 4	0 = Serial port 1 reception disabled.
	1 = Serial port 1 receiver enabled (modes 1, 2, 3). Initiate synchronous reception (mode 0).
TB8_1 Bit 3	9th Transmission Bit State. This bit defines the state of the 9 th transmission bit in serial port 1 modes 2 and 3.
RB8_1 Bit 2	9th Received Bit State. This bit identifies the state for the 9 th reception bit received data in serial pot 1 modes 2 and 3. In serial port mode 1, when SM2_1=0, RB8_1 is the state of the stop bit. RB8_1 is not used in mode 0.
TI_1 Bit 1	Transmitter Interrupt Flag. This bit indicates that data in the serial port 1 buffer has been completely shifted out. In serial port mode 0, TI_1 is set at the end of the 8 th data bit. In all other modes, this bit is set at the end of the last data bit. This bit must be manually cleared by software.
RI_1 Bit 0	Transmitter Interrupt Flag. This bit indicates that a byte of data has been received in the serial port 1 buffer. In serial port mode 1, RI_1 is set at the end of the 8 th bit. In serial port mode 1, RI_1 is set after the last sample of the incoming stop bit subject to the state of SM2_1. In modes 2 and 3, RI_1 is set after the last sample of RB8_1. This bit must be manually cleared by software.

Serial Data Buffer 1 (SBUF1)

	7	6	5	4	3	2	1	0
SFR D9h	SBUF1.7	SBUF1.6	SBUF1.5	SBUF1.4	SBUF1.3	SBUF1.2	SBUF1.1	SBUF1.0
-	RW-0							

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

SBUF1.7-0Serial Data Buffer 1. Data for serial port 1 is read from or written to thisBits 7-0location. The serial transmit and receive buffers are separate registers, but both
are addressed at this location.

'WM0 Value Register (PWM0)									
	7	6	5	4	3	2	1	0	
SFR DCh	PWM0.7	PWM0.6	PWM0.5	PWM0.4	PWM0.3	PWM0.2	PWM0.1	PWM0.0	
	RW-0								

PWM0.7-0PWM0 Value Register. This register provides read/write access to timer and
compare resources found in the pulse generator section of 8-bit PWM channel 0.
When bit PW0T/C (PW01CON.4) is 1, this register provides access to the timer
portion. Access to the timer allows precise initialization of the PWM function if
desired. When bit PW0T/C is 0, this register provides access to the compare
register that determines the duty cycle of channel 0's output. The duty cycle is
given by the equation Duty-Cycle (%) = PWM0/256. In 16-bit mode, this register
is the LSB value register for 16-bit PWM channel 0, and functions identically to
8-bit mode.

PWM1 Value Register (PWM1) 7 2 0 6 5 4 3 1 SFR DDh **PWM1.7** PWM1.6 **PWM1.5 PWM1.4 PWM1.3 PWM1.2 PWM1.1 PWM1.0** RW-0 RW-0 RW-0 RW-0 RW-0 RW-0 RW-0 RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

PWM1.7-0PWM1 Value Register. This register provides read/write access to timer and
compare resources found in the pulse generator section of 8-bit PWM channel 1.
When bit PW1T/C (PW01CON.0) is 1, this register provides access to the timer
portion. Access to the timer allows precise initialization of the PWM function if
desired. When bit PW1T/C is 0, this register provides access to the compare
register that determines the duty cycle of channel 1's output. The duty cycle is
given by the equation Duty-Cycle (%) = PWM0/256. In 16-bit mode, this register
is the MSB value register for 16-bit PWM channel 0, and functions identically to
8-bit mode.

PWM2 Value Register (PWM2)								
	7	6	5	4	3	2	1	0
SFR DDh	PWM2.7	PWM2.6	PWM2.5	PWM2.4	PWM2.3	PWM2.2	PWM2.1	PWM2.0
	RW-0							

PWM2.7-0PWM2 Value Register. This register provides read/write access to timer and
compare resources found in the pulse generator section of 8-bit PWM channel 2.
When bit PW2T/C (PW23CON.4) is 1, this register provides access to the timer
portion. Access to the timer allows precise initialization of the PWM function if
desired. When bit PW2T/C is 0, this register provides access to the compare
register that determines the duty cycle of channel 2's output. The duty cycle is
given by the equation Duty-Cycle (%) = PWM0/256. In 16-bit mode, this register
is the LSB value register for 16-bit PWM channel 1, and functions identically to
8-bit mode.

PWM3 Value Register (PWM3)

_	7	6	5	4	3	2	1	0
SFR DEh	PWM3.7	PWM3.6	PWM3.5	PWM3.4	PWM3.3	PWM3.2	PWM3.1	PWM3.0
	RW-0							

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

PWM3.7-0PWM3 Value Register. This register provides read/write access to timer and
compare resources found in the pulse generator section of 8-bit PWM channel 3.
When bit PW3T/C (PW23CON.0) is 1, this register provides access to the timer
portion. Access to the timer allows precise initialization of the PWM function if
desired. When bit PW3T/C is 0, this register provides access to the compare
register that determines the duty cycle of channel 3's output. The duty cycle is
given by the equation Duty-Cycle (%) = PWM0/256. In 16-bit mode, this register
is the MSB value register for 16-bit PWM channel 1, and functions identically to
8-bit mode.

	7	6	5	4	3	2	1	0
SFR E0h	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0
	RW-0							

Accumulator A (A or ACC)

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

ACC.7-0Accumulator. This register serves as the accumulator for arithmetic and logicalBits 7-6operations. It is functionally identical to the accumulator found in the 80C32.

PWM0 and PWM1 Clock Select Register (PW01CS)

	7	6	5	4	3	2	1	0
SFR E1h	PW0S2	PW0S1	PW0S0	PW0EN	PW1S2	PW1S1	PW1S0	PW1EN
	RW-0							

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

PW0S2:PW0S0PWM0 Clock Select Bits. These bits determine which of the available prescalerBits 7-5outputs are selected as the PWM0 clock generator inputs as shown below.

PW0S2	PW0S1	PW0S0	Selected Prescaler Output Frequency
0	0	0	Crystal (Oscillator) / 1
0	0	1	Crystal (Oscillator) / 4
0	1	0	Crystal (Oscillator) / 16
0	1	1	Crystal (Oscillator) / 64
1	Х	Х	PWMC0 (input pin)

PW0ENPWM0 Clock Generator Enable. This bit enables (1) or disables (0) the clockBits 4generator for 8-bit PWM channel 0 or 16-bit PWM channel 0 (when PWE0 = 1).

PW1S2:PW1S0PWM1 Clock Select Bits. These bits determine which of the available prescaler
outputs are selected as the PWM1 clock generator inputs as shown below.

PW1S2	PW1S1	PW1S0	Selected Prescaler Output Frequency
0	0	0	Crystal (Oscillator) / 1
0	0	1	Crystal (Oscillator) / 4
0	1	0	Crystal (Oscillator) / 16
0	1	1	Crystal (Oscillator) / 64
1	Х	Х	PWMC1 (input pin)

PW1ENPWM1 Clock Generator Enable. This bit enables (1) or disables (0) the clockBit 0generator for 8-bit PWM channel 1. This bit has no effect in 16-bit mode.

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PWM2 ar	nd PWM	3 Clock S	Select Re	gister (P\	N23CS)				
	7	6	5	4	3	2	1	0	
SFR E2h	PW2S2	PW2S1	PW2S0	PW2EN	PW3S2	PW3S1	PW3S0	PW3EN	
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	
	R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset								
PW2S2:PW2S0PWM2 Clock Select Bits. These bits determine which of the available outputs are selected as the PWM2 clock generator inputs. These bits op indicated in the above description of PW01CS.						e prescaler erate as			
PW2EN Bit 4		PWM2 Clock Generator Enable. This bit enables (1) or disables (0) the clock generator for 8-bit PWM channel 2 or 16-bit PWM channel 1 (when PWE0 = 1).						the clock VE0 = 1).	
PW3S2:PW3S0PWM3 Clock Select Bits. These bits determine which of the available pre outputs are selected as the PWM2 clock generator inputs. These bits operator indicated in the above description of PW01CS.					e prescaler erate as				
PW3EN Bit 0		PWM3 Cl generator f	bck Generator Enable. This bit enables (1) or disables (0) the clock or 8-bit PWM channel 3. This bit has no effect in 16-bit mode.						

PWM0 and PWM1 Control Register (PW01CON)

be cleared by software.

	7	6	5	4	3	2	1	0
SFR E3h	PW0F	PW0DC	PW0OE	PW0T/C	PW1F	PW1DC	PW1OE	PW1T/C
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0
R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset								
PW0F		PWM0 Fla	ag. A 1 in th	his bit indica	tes that the	8-bit (or 16-	bit, if PWE0)=1) PWM
Bit 7	channel 0 timer has rolled over to zero after the maximum count. This bit must							

PW0DCPWM0 DC Overdrive. Setting this bit to a 1 forces the 8-bit (or 16-bit, if
PWE0=1) PWM channel 0 to output a 1 regardless of the PWM match value.

PW00EPWM0 Output Enable. This bit enables (1) or disables (0) the output associatedBit 5with 8-bit (or 16-bit, if PWE0=1) PWM channel 0. If the PWM output is
disabled (reset default condition), its output pin (PWMO0 = P6.0) is available as
a standard I/O pin.

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PW0T/C	PWM0 Timer/Compare Value Select. When this bit is cleared (reset default condition) a read or write to register PWM0 accesses the compare register
Bit 4	portion of the PWM0 Pulse Generator. When this bit is set, a read or write to register PWM0 access the timer portion of the PWM0 Pulse Generator.
PW1F	PWM1 Flag A 1 in this bit indicates that the 8-bit PWM channel 1 timer has
Bit 3	rolled over to zero after the maximum count. This bit must be cleared by software, and has no meaning in 16-bit mode.
PW1DC	PWM1 DC Overdrive Setting this bit to a 1 forces the 8-bit PWM channel 1 to
Bit 2	output a 1 regardless of the PWM match value. This bit has no meaning in 16-bit mode.
PW1OE	PWM1 Output Enable . This bit anables (1) or disables (0) the output associated
Bit 1	with 8-bit PWM channel 1. If the PWM output is disabled (reset default condition), its output pin (PWMO1 = P6.1) is available as a standard I/O pin.
PW1T/C Bit 0	PWM1 Timer/Capture Value Select. When this bit is cleared (reset default condition), a read or write to register PWM1 accesses the compare register portion of the PWM1 Pulse Generator. When this bit is set, a read or write to register PWM1 access the timer portion of the PWM1 Pulse Generator.

			DS870	2550 High-Sp	eed Micro	controller Us	ser's Guide S	Supplement	
PWM2 ar	nd PWM	3 Contro	I Registe	er (PW23C	ON)				
	7	6	5	4	3	2	1	0	
SFR E4h	PW2F	PW2DC	PW2OE	PW2T/C	PW3F	PW3DC	PW3OE	PW3T/C	
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	
	R=Unre	estricted Rea	d, W=Unre	stricted Write	e, -n=Value	after Reset			
PW2F		PWM2 Fla	ag. A 1 in t	his bit indica	tes that the	8-bit PWM	channel 2 (o	r 16-bit	
Bit 7		PWM char count. Thi	PWM channel 1, if PWE1=1) timer has rolled over to zero after the maximum count. This bit must be cleared by software.						
PW2DC		PWM2 DO	C Overdriv	e. Setting thi	is bit to a 1	forces the 8-	-bit PWM cł	nannel 2	
Bit 6		(or 16-bit I match valu	(or 16-bit PWM channel 1, if PWE0=1) to output a 1 regardless of the PWM match value.						
PW2OE		PWM2 Ou	ıtput Enab	le. This bit e	enables (1)	or disables ((0) the output	associated	
Bit 5		with 8-bit PWM channel 2 (or 16-bit PWM channel 1, if $PWE0=1$). If the PWM output is disabled (reset default condition), its output pin ($PWMO2 = P6.2$) is available as a standard I/O pin.							
PW2T/C Bit 4		PWM2 Timer/Compare Value Select. When this bit is cleared (reset default condition), a read or write to register PWM2 accesses the compare register portion of the PWM2 Pulse Generator. When this bit is set, a read or write to register PWM2 access the timer portion of the PWM2 Pulse Generator.							
PW3F Bit 3		PWM3 Flag. A 1 in this bit indicates that the 8-bit PWM channel 3 timer has rolled over to zero after the maximum count. This bit must be cleared by software, and has no meaning in 16-bit mode.							
PW3DC Bit 2		PWM3 D (output a 1 : mode.	C Overdriv regardless o	e. Setting this of the PWM r	s bit to a 1 : natch value	forces the 8- . This bit ha	bit PWM ch s no meaning	annel 3 to g in 16-bit	
PW3OE Bit 1		PWM3 Output Enable. This bit enables (1) or disables (0) the output associated with 8-bit PWM channel 3. If the PWM output is disabled (reset default condition), its output pin (PWMO3 = P6.3) is available as a standard I/O pin.							
PW3T/C Bit 0		PWM3 Ti condition), portion of register PV	mer/Captu a read or w the PWM3	re Value Sel rite to registe Pulse Genera the timer poi	ect. When the per PWM3 a tor. When the trian of the trian t	this bit is cle ccesses the c his bit is set PWM3 Puls	ared (reset d compare regi , a read or w e Generator	lefault ster rite to	

			DS87C	550 High-Sp	peed Microc	ontroller Us	er's Guide S	upplement
Timer 2 Auto Reload Register LSB (RLOADL)								
	7	6	5	4	3	2	1	0
SFR E6h	RLOADL.7	RLOADL.6	RLOADL.5	RLOADL.4	RLOADL.3	RLOADL.2	RLOADL.1	RLOADL.0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0
	R=Unre	stricted Rea	d, W=Unres	stricted Write	e, -n=Value	after Reset		

RLOADL.7-0	Timer 2 Auto Reload Register LSB. This register holds the LSB of the 16-bit
Bits 7-0	reload value when Timer 2 is configured in auto-reload mode ($CP/\overline{RL2} = 0$).

Timer 2 Auto Reload Register MSB (RLOADH)

	7	6	5	4	3	2	1	0
SFR E7h	RLOADH.7	RLOADH.6	RLOADH.5	RLOADH.4	RLOADH.3	RLOADH.2	RLOADH.1	RLOADH.0
	RW-0							

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

RLOADH.7-0Timer 2 Auto Reload Register MSB. This register holds the MSB of the 16-bitBits 7-0reload value when Timer 2 is configured in auto-reload mode ($CP/\overline{RL2} = 0$).

Extended	l Interru	ipt Enabl	e (EIE)					
	7	6	5	4	3	2	1	0
SFR E8h	ET2	ECM2	ECM1	ECM0	EX5/EC3	EX4/EC2	EX3/EC1	EX2/EC0
L	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0
	R–Unre	estricted Rea	d W-Unres	stricted Writ	e -n-Value	after Reset		
ET2	R=0int	Enable Ti	mer 2 Inter	rupt. Settir	ret for the state of the second sec	ables interru	pts from the	Timer 2
Bit 7		TF2 flag (T interrupt.	Г2CON.7) a	nd/or T2FB	flag (T2SEI	4). Clearin	g this bit dis	ables this
ECM2 Bit 6		Compare Timer 2 an interrupt.	Match 2 In d compare r	terrupt Ena register CM2	ble. Setting 2 match. Clea	this bit ena aring this bi	bles interrup t disables thi	ts when s
ECM1 Bit 5		Compare Timer 2 an interrupt.	Match 1 In d compare r	terrupt Ena register CM	ble. Setting match. Clea	this bit ena aring this bi	bles interrup t disables thi	ts when s
ECM0 Bit 4		Compare 2 Timer 2 an interrupt.	Match 0 In d compare r	terrupt Ena register CM(ble. Setting) match. Clea	this bit ena aring this bi	bles interrup t disables thi	ts when s
EX5/EC3 Bit 3		External I disables (0 (P1.3). If t or $\overline{\text{CT3}}$ CT	nterrupt 5) interrupts i he capture f CON.7 bit s	or Capture initiated by f function asso set), a captur	3 Interrupt the proper tra- ociated with e will occur	Enable. Thansition on this pin is eralso.	nis bit enable he INT5/CT nabled (CT3	es (1) or '3 pin CTCON.6
EX4/EC2 Bit 2		External I disables (0 (P1.2). If t CTCON.4	interrupt 4) interrupts in the capture for $\overline{CT2} = C$	or Capture initiated by f function asso TCON.5 bit	2 Interrupt the proper tra- ociated with set), a captu	Enable. Thansition on this pin is erre will occu	nis bit enable he INT4/CT nabled (CT2 r also.	es (1) or 2 pin =
EX3/EC1 Bit 1		External I disables (0 (P1.1). If t CTCON.2	interrupt 3) interrupts in the capture for $\overline{CT1} = C^2$	or Capture initiated by f function asso ICON.3 bit	1 Interrupt the proper tra- ociated with set), a captur	Enable. Thansition on this pin is erre will occur	nis bit enable he INT3/CT nabled (CT1 r also.	es (1) or '1 pin =
EX2/EC2 Bit 2		External I disables (0 (P1.2). If t CTCON.0	interrupt 2) interrupts in the capture for $\overline{CT1} = C$	or Capture initiated by f function asso ICON.1 bit	0 Interrupt the proper tra- ociated with set), a capture	Enable. Thansition on this pin is erre will occur	nis bit enable he INT2/CT nabled (CT0 also.	es (1) or 10 pin =

			DS87	C550 High-S	peed Microc	ontroller Us	er's Guide S	Supplement
Timer 2 I	nterrup	t/Clock S	elect (T	2SEL)				
	7	6	5	4	3	2	1	0
SFR EAh	TF2S	TF2BS	-	TF2B	-	-	T2P1	T2P0
	RW-0	RW-0	-	RW-0	-	-	RW-0	RW-0
	R=Unr	estricted Rea	d, W=Unr	estricted Writ	e, -n=Value	after Reset		
TF2S		Timer 21	6-Bit Ove	rflow Interru	pt Select. S	letting this b	it enables in	terrupts
Bit 7		bit disable	s this inter	er 2 16-bit ove rupt.	erflow (sets	TF2 flag T2	CON.7). Cle	earing this
TF2BS		Timer 28	-Bit Over	flow Interrup	ot Select. Se	etting this bit	t enables inte	errupts
Bit 6		resulting fr bit disable	rom a Tim s this inter	er 2 8-bit over rupt.	flow (sets T	F2B flag T2	2SEL.4). Cle	aring this
Bit 5		Reserved.	Read data	will be indete	rminate.			
TF2B Bit 4		Timer 2 8 LSB overf RCLK and	- Bit Over lows. This l TCLK ar	flow Flag. Th bit must be cl e both cleared	is bit is set l leared by sol (T2 now us	by hardware ftware , and ed as a baud	when the Ti will only be rate generat	mer 2 set if cor).
Bits 3-2		Reserved.	Read data	will be indete	rminate.			
T2P1-T2P Bits 1-0	0	Timer 2 P Timer 2 in	rescaler H put clock a	Bits. These bit as shown:	ts select the	prescaler div	vide values f	or the
DRSTO		T2P1	T2P0	Prescaler Div	visor			
		0	0	1				
		0	1	2				
		1	0	4				
		1	1	8				
		In all but t	he clock o	utput mode of	Timer 2, the	e clock cont	rol bits 4X/2	X and

In all but the clock output mode of Timer 2, the clock control bits 4X/2X and CD1:0 determine the input to this prescaler (see further information in Timer 2 section).

			DS87C	550 High-S	peed Microc	ontroller Us	er's Guide S	Supplement
Capture	Trigger	Control F	Register	(CTCON)				
-	7	6	5	4	3	2	1	0
SFR EBh	CT3	CT3	$\overline{\text{CT2}}$	CT2	CT1	CT1	CT0	СТ0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0
	R=Unre	estricted Rea	d, W=Unres	stricted Writ	e, -n=Value	after Reset		
CT3		Capture F	Register CP	TR3 Negati	ve Trigger	Enable. Set	ting this bit	enables
Bit 7		the transfe	r of Timer 2	contents int	o 16-bit cap	ture register	pair CPTH	3:CPTL3
		on the fall	ng edge of t	the signal on	pin INT5/C	T3 (P1.3). V	Vhen set, thi	s bit also
		Clearing th	nis bit disabl	es both capt	ure and inter	rrupt functio	ns for a falli	u). Ing edge.
		creating u		es sour cupt		in apt ranted o	115 TOT u Tull	ing eager
CT3		Capture F	Register CP	TR3 Positiv	e Trigger E	able. Sett	ing this bit e	nables the
Bit 6		transfer of	Timer 2 con	ntents into 10	5-bit capture	register pai	r CPTH3:CI	PTL3 on
		the rising e	edge of the s	ignal on pin	INT5/CT3 ((P1.3). When	n set, this bi	t also
		Clearing th	External In	es both capt	ure and inter	rupt functio	e (11 enabled	1). 19 edge
		clouring u		es sour capt		rupt runeito	115 TOT u 11511	ig eage.
$\overline{\mathbf{CT2}}$		Capture F	Register CP	TR2 Negati	ve Trigger]	Enable. Set	ting this bit	enables
Bit 5		the transfe	r of Timer 2	contents int	o 16-bit cap	ture register	pair CPTH2	2:CPTL2
DR 5		on the falli	ng edge of t	he signal on	pin INT4/C	T2 (P1.2). V	Vhen set, thi	s bit also
		configures	External In	terrupt 4 to r	espond to a	negative edg	ge (if enable	d). Ing adga
		Cleaning u	lis on disabi	es both capt		inupi nunctio		ng euge.
CT2		Capture F	Register CP	TR2 Positiv	e Trigger E	nable. Sett	ing this bit e	enables the
Bit 4		transfer of	Timer 2 cor	ntents into 10	5-bit capture	register pai	r CPTH2:CI	PTL2 on
		the rising e	edge of the s	ignal on pin	INT4/CT2	(P1.2). When	n set, this bi	t also
		Clearing th	External In	terrupt 4 to r	espond to a	negative edg	ge (if enable	d). Ng edge
		Cleaning u	lis on uisaoi	es both capt		Tupi Tuncio	115 101 a 11511	ig euge.
		Canture F	Register CP	TR1 Negati	ve Trigger]	Enable Set	ting this hit	enables
		the transfer	r of Timer 2	contents int	o 16-bit cap	ture register	pair CPTH	I:CPTL1
Bit 3		on the falli	ng edge of t	he signal on	pin INT3/C	T1 (P1.1). V	Vhen set, thi	s bit also
		configures	External In	terrupt 3 to r	espond to a	negative edg	ge (if enable	d).
		Clearing th	nis bit disabl	es both capt	ure and inter	rrupt functio	ns for a falli	ng edge.
CT1		Canturo L	Register (°P	TR1 Positiv	e Trigger F	nable Sett	ing this hit a	nables the
Rit 7		transfer of	Timer 2 con	tents into 10	5-bit capture	register pai	r CPTH1:CI	PTL1 on
DIL 2		the falling	edge of the	signal on pir	n INT3/CT1	(P1.1). Whe	en set, this b	it also
		configures	External In	terrupt 3 to r	espond to a	positive edg	e (if enabled	1).
		Clearing th	nis bit disabl	es both capt	ure and inter	rrupt functio	ns for a risin	ıg edge.

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CT0	Capture Register CPTR0 Negative Trigger Enable. Setting this bit enables
Bit 1	the transfer of Timer 2 contents into 16-bit capture register pair CPTH0:CPTL0 on the falling edge of the signal on pin INT2/CT0 (P1.0). When set, this bit also configures External Interrupt 2 to respond to a negative edge (if enabled). Clearing this bit disables both capture and interrupt functions for a falling edge.
СТО	Capture Register CPTR0 Positive Trigger Enable. Setting this bit enables the
Bit 0	transfer of Timer 2 contents into 16-bit capture register pair CPTH0:CPTL0 on

the rising edge of the signal on pin INT2/CT0 (P1.0). When set, this bit also configures External Interrupt 2 to respond to a positive edge (if enabled). Clearing this bit disables both capture and interrupt functions for a falling edge.

Timer 2 LSB (T2L)

	7	6	5	4	3	2	1	0
SFR ECh	T2L.7	T2L.6	T2L.5	T2L.4	T2L.3	T2L.2	T2L.1	T2L.0
	RW-0							

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

T2L.7-0Timer 2 LSB. This register contains the least significant byte of timer2.Bits 7-0

Timer 2 MSB (T2H)

	7	6	5	4	3	2	1	0
SFR ECh	T2H.7	T2H.6	T2H.5	T2H.4	T2H.3	T2H.2	T2H.1	T2H.0
	RW-0							

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

T2H.7-0Timer 2 MSB. This register contains the most significant byte of timer2.

Bits 7-0

			DS870	2550 High-S	peed Microc	ontroller Us	er's Guide S	Supplement
Compare	e Match	Set Enab	le Regis	ter (SETF	()			
	7	6	5	4	3	2	1	0
SFR EEh	TGFF1	TGFF0	CMS5	CMS4	CMS3	CMS2	CMS1	CMS0
	R-1	R-1	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0
	R=Unre	estricted Rea	d, W=Unre	stricted Writ	e, -n=Value	after Reset		
TGFF1 Bit 7		Compare 2 Port pin Cl bit register (CMTE1=2	Match Tog MT1 (P4.7) pair CMPH 1).	gle Flip-Flo This bit tog I2:CMPL2 n	p 1. This biggles when the and the	t is used as a he contents o e toggle func	toggle flip- of Timer 2 a ction is enab	flop for and the 16- led
TGFF0 Bit 6		Compare A Port pin Cl bit register (CMTE0=	/ Match To MTO (P4.6). pair CMPH 1).	ggle Flip-Fl . This bit tog I2:CMPL2 n	op 0. This b ggles when the natch and the	bit is used as he contents of toggle func	a toggle flij of Timer 2 a etion is enab	p-flop for and the 16- led
CMS5 Bit 5		Compare pin CMSR CMPH0:C	Match Set 1 5 (P4.5) wh MPL0 matc	Enable 5. S en the conter h. Clearing t	etting this bi nts of Timer his bit disab	t enables the 2 and 16-bi les this func	e set functio t register pa tion.	n on port ir
CMS4 Bit 4		Compare pin CMSR CMPH0:C	Match Set 2 4 (P4.4) wh MPL0 matc	Enable 4. S en the conter h. Clearing	etting this bi nts of Timer this bit disał	it enables the 2 and the 16 bles the set f	e set functio 5-bit register unction.	n on port r pair
CMS3 Bit 3		Compare pin CMSR CMPH0:C	Match Set 3 3 (P4.3) wh MPL0 matc	Enable 3. S en the conter h. Clearing	etting this bi nts of Timer this bit disał	it enables the 2 and the 16 bles the set f	e set functio 5-bit register unction.	n on port r pair
CMS2 Bit 2		Compare pin CMSR CMPH0:C	Match Set 2 2 (P4.2) wh MPL0 matc	Enable 2. S en the conter h. Clearing	etting this bi nts of Timer this bit disał	it enables the 2 and the 16 bles the set f	e set functio 5-bit register unction.	n on port r pair
CMS1 Bit 1		Compare pin CMSR CMPH0:C	Match Set 1 1 (P4.1) wh MPL0 matc	Enable 1. S en the conter h. Clearing	etting this bi nts of Timer this bit disał	it enables the 2 and the 16 bles the set f	e set functio 5-bit register unction.	n on port r pair
CMS0 Bit 4		Compare pin CMSR CMPH0:C	Match Set 1 0 (P4.0) wh MPL0 matc	Enable 0. S en the conter h. Clearing	etting this bi nts of Timer this bit disat	it enables the 2 and the 16 bles the set f	e set functio 5-bit register unction.	n on port r pair

			DS87C	550 High-Sp	peed Microc	ontroller Us	er's Guide S	Supplement
Compar	e Match	Reset/To	ggle Ena	ble Regis	ster (RST	R)		
	7	6	5	4	3	2	1	0
SFR EFh	CMTE1	CMTE0	CMR5	CMR4	CMR3	CMR2	CMR1	CMR0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0
	R=Unre	estricted Read	d, W=Unres	tricted Write	e, -n=Value	after Reset		
CMTE1		Compare I	Match Tog	gle Enable 1	. Setting th	is bit enable	s the toggle	function
Bit 7		on port pin pair CMPH	CMT1 (P4. 12:CMPL2 r	7) when the natch. Clear	contents of ing this bit c	Timer 2 and lisables the t	the 16-bit r toggle funct	egister ion.
CMTE0		Compare I	Match Tog	gle Enable (. Setting th	is bit enable	s the toggle	function
Bit 6		on port pin pair CMPH	CMT0 (P4. I2:CMPL2 r	6) when the natch. Clear	contents of ing this bit c	Timer 2 and lisables the	the 16-bit r toggle funct	egister ion.
CMR5 Bit 5		Compare I port pin CN CMPH1:Cl	Match Rese ASR5 (P4.5 MPL1 matcl	et Enable 5.) when the c h. Clearing t	Setting this ontents of T his bit disab	bit enables imer 2 and t les the reset	the reset fur he 16-bit reg function.	nction on gister pair
CMR4 Bit 4		Compare I port pin CM CMPH1:CI	Match Rese ASR4 (P4.4) MPL1 matcl	e t Enable 4.) when the c h. Clearing t	Setting this ontents of T his bit disab	bit enables imer 2 and t les the reset	the reset fur he 16-bit reg function.	nction on gister pair
CMR3 Bit 3		Compare I port pin CM CMPH1:CI	Match Rese ASR3 (P4.3) MPL1 matcl	et Enable 3.) when the c h. Clearing t	Setting this ontents of T his bit disab	bit enables imer 2 and t les the reset	the reset fur he 16-bit reg function.	nction on gister pair
CMR2 Bit 2		Compare I port pin CM CMPH1:CI	Match Rese ASR2 (P4.2) MPL1 matcl	e t Enable 2.) when the c h. Clearing t	Setting this ontents of T his bit disab	bit enables imer 2 and t les the reset	the reset fur he 16-bit reg function.	nction on gister pair
CMR1 Bit 1		Compare I port pin CN CMPH1:CI	Match Rese ASR1 (P4.1) MPL1 matcl	e t Enable 1.) when the c h. Clearing t	Setting this ontents of T his bit disab	bit enables imer 2 and t les the reset	the reset fur he 16-bit reg function.	nction on gister pair
CMR0 Bit 0		Compare I port pin CN CMPH1:CI	Match Rese MSR0 (P4.0) MPL1 matcl	et Enable 0.) when the c h. Clearing t	Setting this ontents of T his bit disab	bit enables imer 2 and t les the reset	the reset fur he 16-bit reg function.	nction on gister pair

B Regist	er							
	7	6	5	4	3	2	1	0
SFR F0h	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0
	R=Unre	stricted Rea	d, W=Unres	stricted Write	e, -n=Value	after Reset		
B.7-0 Bits 7-0		B Register operations.	• This regis	ter serves as	a second ac	cumulator f	or certain ar	ithmetic

Parallel I/O Port Six (P6)

	7	6	5	4	3	2	1	0
SFR F1h	P6.7	-	P6.5	P6.4	P6.3	P6.2	P6.1	P6.0
	STADC		PWMC1	PWMC0	PWMO3	PWMO2	PWMO1	PWMO0
	RW-1	-	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

P6.7,P6.5-0General Purpose I/O Port 6. This register functions as a 7-bit general purposeBits 7, 5-0I/O port. In addition, all the pins have an alternate function listed below. The
associated Port 6 latch bit must contain a logic one before the pin can be used in
its alternate function capacity.

- STADCStart A/D Conversion. If enabled by ADEX=ADCON1.4=1, a negativeBit 7transition on this pin will initiate an A/D conversion. Otherwise this pin serves as
a standard I/O pin.
- Bit 6 Reserved. Read data will be indeterminate.
- **PWMC1PWM Clock 1 Input.** If enabled by PW2S2 = PW23CS.7 = 1, this pin willBit 5provide an externally generated clock signal to PWM channel 2. If enabled byPW3S2 = PW23CS.3 = 1, this pin will provide an externally generated clocksignal to PWM channel 3. Otherwise this pin serves as a standard I/O pin.
- **PWMC0PWM Clock 0 Input.** If enabled by PW0S2 = PW01CS.7 = 1, this pin willBit 4provide an externally generated clock signal to PWM channel 0. If enabled by
PW1S2 = PW01CS.3 = 1, this pin will provide an externally generated clock
signal to PWM channel 1. Otherwise this pin serves as a standard I/O pin.

DS87C550 High-Speed Microcontroller User's Guide Supplement PWMO3 **PWM Channel 3 Output.** If enabled by PW3OE = PW23CON.1 = 1, this pin serves as the output for PWM channel 3. Otherwise this pin serves as a standard Bit 3 I/O pin. PWMO2 **PWM Channel 2 Output.** If enabled by PW2OE = PW23CON.5 = 1, this pin serves as the output for PWM channel 2. Otherwise this pin serves as a standard Bit 2 I/O pin. **PWM Channel 1 Output.** If enabled by PW1OE = PW01CON.1 = 1, this pin PWM01 serves as the output for PWM channel 1. Otherwise this pin serves as a standard Bit 1 I/O pin. **PWMO0 PWM Channel 0 Output.** If enabled by PW00E = PW01CON.5 = 1, this pin serves as the output for PWM channel 0. Otherwise this pin serves as a standard Bit 0 I/O pin.

Extended Interrupt Priority (EIP)

	7	6	5	4	3	2	1	0
SFR F8h	PT2	PCM2	PCM1	PCM0	PX5/PC3	PX4/PC2	PX3/PC1	PX2/PC0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

PT2 Bit 7	Timer 2 Overflow Interrupt Priority. The Timer 2 overflow interrupt request will be high when this bit is 1 and normal priority when it is 0.
PCM2 Bit 6	Compare Match 2 Interrupt Priority. The compare match 2 interrupt request will be high priority when this bit is 1 and normal priority when it is 0.
PCM1 Bit 5	Compare Match 1 Interrupt Priority The compare match 1 interrupt request will be high priority when this bit is 1 and normal priority when it is 0.
PCM0 Bit 4	Compare Match 0 Interrupt Priority The compare match 0 interrupt request will be high priority when this bit is 1 and normal priority when it is 0.
PX5/PC3 Bit 3	External Interrupt 5 Priority or Capture 3 Interrupt Priority. This bit determines the priority ($0 = normal$, $1 = high$) of the Timer 2 Capture channel 3 if it is in use or External Interrupt 3 if enabled and the capture function is disabled.
PX4/PC2 Bit 2	External Interrupt 4 Priority or Capture 2 Interrupt Priority. This bit determines the priority ($0 = normal$, $1 = high$) of the Timer 2 Capture channel 2 if it is in use or External Interrupt 3 if enabled and the capture function is disabled.
	020173

PX3/PC1 Bit 1	External Interrupt 3 Priority or Capture 1 Interrupt Priority. This bit determines the priority ($0 = normal$, $1 = high$) of the Timer 2 Capture channel 1 if it is in use or External Interrupt 3 if enabled and the capture function is disabled.
PX2/PC0 Bit 0	External Interrupt 2 Priority or Capture 0 Interrupt Priority. This bit determines the priority ($0 = normal$, $1 = high$) of the Timer 2 Capture channel 0 if it is in use or External Interrupt 2 if enabled and the capture function is disabled.

Watchdog Control Register (WDCON) 7 6 5

	7	6	5	4	3	2	1	0
SFR FFh	SMOD_1	POR	EPFI	PFI	WDIF	WTRF	EWT	RWT
	RW-0	RW-*	RW-0	RW-*	RT-0	RW-*	RT-*	RT-0
		R=Unrestric	ted Read, W -n=Va	⁷ =Unrestrictor lue after Res	ed Write, T= set, *=See de	=Timed Acco escription	ess Write Oi	ıly,
SMOD_1 Bit 7		Serial Por serial baud baud rate g	t 0 Baud H rate doublin enerator.	Rate Double	er Enable. For Serial Po	This bit er rt 1 when us	ables/disabl ing Timer 1	es the as the
	 0 = Serial Port 1 baud rate will be that defined by baud rate generation equation. 1 = Serial Port 1 baud rate will be double that defined by baud rate generation equation. 					eration eration		
POR Bit 6	OR Power-on Reset Flag. This bit indicates whether the last reset was a power-on reset. This bit is typically interrogated following a reset to determine if the reset was caused by power-on. It must be cleared by a Timed Access write before th next reset of any kind or the software may erroneously determine that another power-on reset has occurred. This bit is set following a power-on reset and unaffected by all other resets				ower-on the reset efore the nother and			
		0 = Last res	set was from	n a source ot	her than a p	ower-on rese	et	
		1 = Last res	set was a po	wer-on reset	t.			
EPF1 Bit 5	PF1Enable Power Fail Interrupt. This bit enables/disables the ability of the inter band-gap reference to generate a power-fail interrupt when V_{CC} falls below approximately 4.5 volts. While in Stop mode, both this bit and the Band-gap Select bit, BGS (EXIF.0), must be set to enable the power-fail interrupt. $0 =$ Power-fail interrupt disabled. $1 =$ Power-fail interrupt enabled during normal operation. Power-fail interrupt enabled in Stop mode if BGS is set.				he internal low d-gap terrupt			

PF1	Power Fail Interrupt Flag. When set, this bit indicates that a power-fail
Bit 4	interrupt has occurred. This bit must be cleared in software before exiting the interrupt service routine, or another interrupt will be generated. Setting this bit in software will generate a power-fail interrupt, if enabled.
WDIF	Watchdog Time-Out Flag. This bit is set by a watchdog time-out which occurs
Bit 3	512 clocks prior to a watchdog reset. This bit can be considered a watchdog interrupt flag even though there is no interrupt associated with the watchdog timer in the DS87C550. This bit must be cleared by software and can only be modified using a Timed Access Procedure.
WTRF Bit 2	Watchdog Timer Reset Flag. When set, this bit indicates that a watchdog timer reset has occurred. It is typically interrogated to determine if a reset was caused by watchdog timer reset. It is cleared by a power- on reset, but otherwise must be cleared by software before the next reset of any kind or software may erroneously determine that a watchdog timer reset has occurred. Setting this bit in software will not generate a watchdog timer reset. If the EWT bit is cleared, the watchdog timer will have no effect on this bit.
EWT	Enable Watchdog Timer Reset . This bit enables/disables the ability of the
Bit 1	watchdog timer to reset the device. Clearing this bit will disable the ability of the watchdog timer to generate a reset, but have no affect on the timer itself. This bit can only be modified using a Timed Access Procedure, and it is unaffected by all other resets.
	0 = A timeout of the watchdog timer will not cause the device to reset.
	1 = A timeout of the watchdog timer will cause the device to reset.
RWT Bit 0	Reset Watchdog Timer. Setting this bit will reset the watchdog timer count. This bit must be set using a Timed Access procedure before the watchdog timer expires, or a watchdog timer reset will be generated if enabled. This bit will always be 0 when read.

SECTION 5:CPU TIMING

The majority of the information contained in the original "High-Speed Microcontroller User's Guide" applies to the DS87C550. The only differences are found in the clock divider circuits between the crystal oscillator (or external clock source) and the clock distribution circuitry. Early members of the High-Speed Microcontroller family offer the option of 4, 256, or 1024 clocks per machine cycle. The DS87C550 can operate at 1, 2, 4, or 1024 clocks per machine cycle. These selectable clock frequencies not only affect the CPU's frequency of operation (machine cycle clock), but also provide selectable clocks to the on-board timers and other peripherals (system clock). It is important to note the difference in these clocks, as they are sometimes confused, creating errors in timing calculations. The effects of these variable clocks relative to CPU timing are discussed below. Their effect on peripheral timing can be found in the individual peripherals' sections of this document.

Crystal Selection

Some recent introductions to the High-Speed Microcontroller family contain special circuitry to allow more latitude in crystal selection. It is frequently the case that as crystals go up in frequency, they become more expensive, and less likely to be available in fundamental mode. While a fundamental mode, parallel resonant, AT cut crystal is still required for these new family members, a simple clock multiplier has been included to allow selection of more readily available crystals when high frequency operation is required. An illustration of the clock multiplier function specifically and overall system clock generation and control is shown in Figure 5-1.



SYSTEM CLOCK GENERATION AND CONTROL : Figure 5-1

As shown in the figure, the output of the crystal oscillator is provided directly to three blocks of circuitry: the frequency multiplier, a divide by 256 block, and a 3-to-1 multiplexer. The frequency multiplier function is enabled by setting the CTM bit, and produces outputs of Input-times-2 or Input-times-4 as determined by the 4X/2x bit. The multiplied clock is then passed to the multiplexer (MUX) that selects the system clock source, and then to the CPU State Clock Generator. This clock multiplication feature allows peak performance of the processor but with the use of a slower, often more available and less expensive crystal. As an example, recall that the maximum frequency of the DS87C550 is 33 MHz. With this clock multiplier feature, a crystal value of 8.25 MHz (33/4) can be used when the frequency multiplier set to Input-times-4 mode. Alternatively with a crystal value of 16.5 MHz, it is possible to recognize peak processor performance when the frequency multiplier is set to input-times 2 mode. Recognize that regardless of the clock multiplication function, there is a maximum operational frequency of the processor given in the specifications as "Oscillator Frequency". Care must be taken not to violate this specification when using the clock multiplier as unpredictable behavior of the processor can result.

The system clock or some derivative there of is provided to all of the peripherals inside the microcontroller and the machine cycle clock provides the basic 4-state clock for all CPU functions. The relationship of the crystal (or external oscillator) to the system clock and machine cycle clock along with the control settings is shown in Table 5-1.

$4X/\overline{2X}$	CD1:0	System	Machine Cycle
		Clock	Clock
1	00	$F_{\rm osc} * 4$	Fosc
0	00	$F_{\rm OSC} * 2$	$F_{\rm OSC}/2$
Х	01 (Reserved)		
X	10	Fosc	$F_{\rm osc}/4$
X	11	F _{osc} / 256	F _{osc} / 1024

SYSTEM	CLOCK	CONT	ROL :	Table 5-	1.

The case of CD1:0 = 11 is a special case for power savings, and is described in the section on power management.

Changing System Clock Frequency

The microcontroller incorporates a special locking sequence to ensure "glitch-free" switching of the internal clock signals. All changes to the CD1, CD0 bits must pass through the 10 (divide-by-four) state. For example, to change from 00 (frequency multiplier) to 11 (PMM), the software must change the bits in the following sequence: 00 10 11. Attempts to switch between invalid states will fail, leaving the CD1, CD0 bits unchanged.

The following sequence must be followed when switching to the frequency multiplier as the internal time source. This sequence can only be performed when the device is in divide-by-four operation. The steps must be followed in this order, although it is possible to have other instructions between them. Any deviation from this order will cause the CD1, CD0 bits to remain unchanged. Switching from frequency multiplier to non-multiplier mode requires no steps other than the changing of the CD1, CD0 bits.

- 1. Ensure that the CD1, CD0 bits are set to 10, and the RGMD (EXIF.2) bit = 0.
- 2. Clear the CTM (Crystal Multiplier Enable) bit.
- 3. Set the $4X/\overline{2X}$ bit to the appropriate state.
- 4. Set the CTM (Crystal Multiplier Enable) bit.
- 5. Poll the CKRDY bit (EXIF.4), waiting until it is set to 1.
- 6. Set CD1, CD0 to 00. The frequency multiplier will be engaged on the machine cycle following the write to these bits.

SECTION 6:MEMORY ACCESS

The DS87C550 supports the memory access features of the DS87C520 described in the High-Speed Microcontroller User's Guide. Exceptions are noted below.

INTERNAL PROGRAM MEMORY

The DS87C550 contains 8 kbytes of EPROM as on-board program storage. This memory resides at fixed addresses from 0000h to 1FFFh.

ROMSIZE FEATURE

The ROMSIZE feature is used to select the maximum on-chip decoded address for program memory. The ROMSIZE is selected as follows:

RMS2	RMS1	RMS0	Maximum on-chip Program Address
0	0	0	0K
0	0	1	1K (0h – 03FFh)
0	1	0	2K (0h – 07FFh)
0	1	1	4K (0h – 0FFFh)
1	0	0	8K (0h – 1FFFh) default
1	0	1	Invalid – reserved
1	1	0	Invalid – reserved
1	1	1	Invalid – reserved

DATA MEMORY ACCESS

Two new features related to the dual data pointers found in the High-Speed Microcontroller family have been added to the DS87C550. These are a data pointer decrement capability and the ability to automatically toggle the selection bit between the two data pointers.

Although the 8051 architecture has always had an INC DPTR instruction, users have often wished for the ability to decrement the data pointers as well. To maintain instruction set compatibility, the DS87C550 supports a decrement data pointer feature through unused bits in the DPS register. Setting the ID1:0 (DPS.7-6) bits and the SEL (DPS.0) bit before performing an INC DPTR instruction selects the active data pointer and whether it is to be incremented or decremented. By setting these bits, the user can determine the count direction (increment or decrement) for each data pointer. This allows very efficient movement of data regardless of whether it is more convenient to traverse the data (source or destination) from low to high addresses or high to low addresses. The bits were added, and operate in conjunction with to allow DPTR decrementing as follows:

ID1	ID0	SEL = 0	SEL = 1
0	0	Increment DPTR	Increment DPTR1
0	1	Decrement DPTR	Increment DPTR1
1	0	Increment DPTR	Decrement DPTR1
1	1	Decrement DPTR	Decrement DPTR

The other new feature is the ability to automatically toggle the SEL bit. With this feature enabled, i.e., with TSL bit (DPS.5) set, every time an instruction dealing with the DPTR is executed, the SEL bit is toggled to select the other DPTR. The instructions that affect this automatic toggle function are:

INC	DPTR
MOV	DPTR, #data16
MOVC	A, @A+DPTR
MOVX	A, @DPTR
MOVX	@DPTR, A

This feature allows further reduction of code for data movement operations, and therefore even higher performance. The following example demonstrates the improved efficiency.

64 BYTE BLOCK MOVE WITH AUTO SELECT

; SH and SL are high and low bytes of the source address

; DH and DL are high and low bytes of the destination address

; DPS is the data pointer select bit. Reset condition is DPS = 0 (DPTR selected).

/		1		
;				# of cycles
	MOV	R5, #64	; Number of bytes to move	3
	MOV	DPTR, #SHSL	; Load destination address & toggle select bit	2
	MOV	DPTR, #DHDL	; Load destination address & toggle select bit	2
;				
; Th	is loop i	s executed the numbe	er of times contained in R5 (i.e., 64)	
	MOVE	:		
	MOVX	A, DPTR	; Read source data byte & toggle select bit	2
	MOVX	@DPTR, A	; Store at destination & toggle select bit	2
	INC	DPTR	; Increment source address & toggle select bit	3
	INC	DPTR	; Increment destination address & toggle select b	it 3
	DJNZ	R5, MOVE	; Finished with table	3
			Total	= 7 + (13*64) = 839

64 BYTE BLOCK MOVE WITHOUT AUTO SELECT

; SH and SL are high and low bytes of the source address

; DH and DL are high and low bytes of the destination address

; DPS is the data	pointer select bit.	Reset condition is	s DPS = 0 (DPTR)	selected).
-------------------	---------------------	--------------------	------------------	------------

;	I		# of cycles
MOV	R5, #64	; Number of bytes to move	3
MOV	DPTR, #SHSL	; Load source address	2
INC	DPS	; Change active DPTR	2
MOV	DPTR, #DHDL	; Load destination address	2
INC	DPS	; Change active DPTR	2
; This le MOVE :	pop is executed the nur	nber of times contained in R5 (i.e.,	64)
MOVE:	sop is excedice the hul	noter of times contained in R5 (i.e.,	04)
MOVX	A, DPTR	; Read source data byte	2
INC	DPS	; Change active DPTR	2
MOVX	@DPTR, A	; Store at destination	2
INC	DPTR	; Increment destination address	3
INC	DPS	; Change active DPTR	2
INC	DPTR	; Increment destination address	3
INC	DPS	; Change active DPTR	2

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DJNZ	R5, MOVE	; Finished with table	3	

Total = 11 + (64*19) = 1,227

From this example it is evident that the auto-select feature allows much more efficient block moves. This example demonstrates a block move of 64 bytes of data. Obviously, the larger the block, the more improvement will be realized. It is also worth noting that by appropriately setting the ID1 and ID1 bits, either the source or destination addresses could have been traversed in the reverse direction (decrement DPTR) without any other changes.

DATA MEMORY TIMING

Data memory timing of the DS87C550 is identical to earlier members of the High-Speed Microcontroller family with one exception regarding the implementation of the Stretch MOVX feature. In all members of this family (including the DS87C550), increasing the stretch value from 0 to 1 causes setup and hold times to be increased by 1 crystal clock period each. In older members of the family, there is no further change in setup and hold times regardless of the stretch value selected. In the DS87C550 however, when a stretch value of 4 or above is selected the timing of the interface changes dramatically to allow for very slow peripherals.

For stretch values of 4 or above, the ALE high period is increased one machine cycle that increases the address setup time into the peripheral by this amount. The address is then held on the bus for one additional machine cycle increasing the address hold time by this amount. The Read or Write signal is also increased by one machine cycle. Finally, the data is held on the bus (for a write cycle) one additional machine cycle which increases the available peripheral hold time. For every stretch value greater than 4, the setup and hold times remain constant, and only the width of the read or write signals is increased.

A full description of this new stretch MOVX arrangement is given in the DS87C550 data sheet (MOVX Characteristics) along with timing diagrams and timing tables. Please refer to that document for more detail.

SECTION 7: POWER MANAGEMENT

The DS87C550 supports the general power management features of the DS87C520 described in the High-Speed Microcontroller. Exceptions are noted below.

Power Management Modes

Power management mode 2 (divide by 1024) is supported on the DS87C550. However, power management mode 1 (divide by 256) is not.

Switching between clock sources

The ring oscillator on the DS87C550 is similar to that on the DS80C320. As such it does not support the "run from ring" feature which allows the microprocessor to use the ring oscillator as a clock source after the external crystal has stabilized (CKRY=1).

SECTION 8: RESET CONDITIONS

The reset conditions of the DS87C550 are generally described in the High-Speed Microcontroller User's Guide and specific reset default conditions of the SFR bits may be found in the data sheet. However two features have been added to the DS87C550. These new features are discussed below.

Oscillator Fail Detect Reset

Most members of the High-Speed Microcontroller family contain a watchdog timer. The intent of this timer is to force the processor into a known "good" state (reset) if it ever entered a runaway situation where it was not executing code properly. This is very powerful feature, but could be made stronger with a simple addition. Since the watchdog timer clock was derived from the main crystal oscillator, it was possible (though very unlikely) that the oscillator would fail (stop) leaving the processor in an undesirable state. Since the watchdog timer runs from the same clock, the timer would stop counting which prevented a time-out and a resulting reset. This possibility is eliminated in the DS87C550 by the inclusion of an oscillator fail detection circuit. When enabled, this circuit causes the processor to be reset if the oscillator frequency falls below TBD kHz. This puts the processor into a known good state regardless of the watchdog timer if the main crystal oscillator should ever fail. Although the oscillator has failed when this reset occurs, the processor is clocked into the normal reset state by other internal clocks.

The oscillator fail detect feature is enabled by setting the OFDE (PCON.4) bit with software. This bit can be modified at any time. When an oscillator fail detection occurs, the flag OFDF (PCON.5) bit is set by hardware when the processor enters reset. This bit must be cleared by software.

RST Pin as an Output

The DS87C550 is the first member of Dallas' High-Speed Microcontroller family to make the reset pin (RST) both an input and an output. Normally, this pin is an active high input for a reset signal generated elsewhere in the system. With the DS87C550, this pin functions as an input as before, but now will also provide an output when the reset originates from within the processor.

The possible internal sources of reset from the DS87C550 are:

- 1. Power–on/Power-Fail reset
- 2. Watchdog Timer reset
- 3. Oscillator Fail reset

The reset output pulse duration is a function of the internal source of the reset. The worst case (minimum pulse duration) occurs when the reset source is the watchdog timer whose reset cycle may be a single machine-cycle long. When the watchdog timer creates a reset, the RST pin is set at the beginning of the next machine cycle, and will remain active for one full machine cycle. When the internal source of the reset is the power-fail circuit, the RST pin will be set at the beginning of the next machine cycle after the reset trip point, and will remain as long as power will sustain it. When power returns, the RST pin will be held active while the processor is held in power-up reset (65565 clocks). If the internal source of reset is the detection circuit, the RST pin will be driven active asynchronously immediately after the detection, and will be held there as long as the processor is in a reset state (presumably until the oscillator begins operation again).

Since the RST pin is designed so that it can be overdriven by an LS-TTL gate output, it is important to keep this pin lightly loaded (resistance and capacitance). For best results, a single buffer should be connected to the RST pin when it used as an output for a system-wide reset signal. Under no

circumstances should an R-C timing circuit be connected to the RST pin of the DS87C550. If the RST pin is too heavily loaded (capacitance), it may be necessary to add a pull-up resistor to speed up the low-to-high transition. This will of course determine what type of output device will be capable of overdriving the pin when used as an input. Careful analysis of these tradeoffs will ensure desired results.
SECTION 9: INTERRUPTS

The DS87C550 uses the same interrupt and interrupt priority system as all other members of the High-Speed Microcontroller family. The specific interrupts and their related flags and control bits are identified in Table 9-1 below.

Interrupt	Vector	Natural Priority	Flag	Enable	Priority Control
Power Fail	33h	0	PFI (WDCON.4)	EPFI (WDCON.5)	N/A
Ext. Interrupt 0	03h	1	IE0 (TCON.1)**	EX0 (IE.0)	PX0 (IP.0)
Serial Port 1	0Bh	2	RI_1 (SCON1.0) TI_1 (SCON1.1	ES1 (IE.5)	PS1 (IP.5)
A/D	13h	3	EOC (ADCON1.0)	EAD (IE.6)	PAD (IP.6)
Timer 0 Overflow	1Bh	4	TF0 (TCON.5)*	ET0 (IE.1)	PT0 (IP.1)
Ext. Interrupt 2 / Capture 0	23h	5	IE2/CF0 (T2IR.0)	EX2/EC0 (EIE.0)	PX2/PC0 (EIP.0)
Compare Match 0	2Bh	6	CM0F (T2IR.4)	ECM0 (EIE.4)	PCM0 (EIP.4)
Ext. Interrupt 1	3Bh	7	IE1 (TCON.3)**	EX1 (IE.2)	PX1 (IP.2)
Ext. Interrupt 3 / Capture 1	43h	8	IE3/CF1 (T2IR.1)	EX3/EC1 (EIE.1)	PX3/PC1 (EIP.1)
Compare Match 1	4Bh	9	CM1F (T2IR.5)	ECM1 (EIE.5)	PCM1 (EIP.5)
Timer 1 Overflow	53h	10	TF1 (TCON.7)*	ET1 (IE.3)	PT1 (IP.3)
Ext. Interrupt 4 / Capture 2	5Bh	11	IE4/CF2 (T2IR.2)	EX4/EC2 (EIE.2)	PX4/PC2 (EIP.2)
Compare Match 2	63h	12	CM2F (T2IR.6)	ECM2 (EIE.6)	PCM2 (EIP.6)
Serial Port 0	6Bh	13	RI_0 (SCON0.0) TI_0 (SCON0.1)	ES0 (IE.4)	PS0 (IP.4)
Ext. Interrupt 5 / Capture 3	73h	14	IE5/CF3 (T2IR.3)	EX5/EC3 (EIE.3)	PX5/PC3 (EIP.3)
Timer 2 Overflow	7Bh	15	TF2 (T2CON.7) TF2B (T2SEL.4)	ET2 (EIE.7)	PT2 (EIP.7)

INTERRUPT SUMARY : Table 9-1

Unless marked, these flags must be cleared manually by software.

* - Cleared automatically by hardware when the interrupt service routine is vectored to.

** - If edge triggered, cleared automatically by hardware when the service routine is vectored to. If level triggered, flag follows the state of the pin.

SECTION 10: PARALLEL I/O

The DS87C550 contains 55 parallel I/O pins. Ports 0 through 3 follow the standard 8051 I/O configuration as described in the High-Speed Microcontroller User's Guide. Some secondary functions are assigned to different pins than on other members of the family, but their functionality is the same. Ports 4, 5 and 6 are new, and are described in the DS87C550 data sheet. Ports 4 and 6 operate as quasi bi-directional I/O pins, while port 5 function as an 8-bit open-drain bi-directional I/O port. Port 6 contains only 7 I/O lines. The alternate functions of all port pins are identified below.

- P0.0 AD0 Multiplexed address/data bus bit 0
- P0.1 AD1 Multiplexed address/data bus bit 1
- P0.2 AD2 Multiplexed address/data bus bit 2
- P0.3 AD3 Multiplexed address/data bus bit 3
- P0.4 AD4 Multiplexed address/data bus bit 4
- P0.5 AD5 Multiplexed address/data bus bit 5
- P0.6 AD6 Multiplexed address/data bus bit 6
- P0.7 AD7 Multiplexed address/data bus bit 7
- P1.0 INT2/CT0 External Interrupt 2/Capture Trigger 0
- P1.1 INT3/CT1 External Interrupt 3/Capture Trigger 1
- P1.2 INT4/CT2 External Interrupt 4/Capture Trigger 2
- P1.3 INT5/CT3 External Interrupt 5/Capture Trigger 3
- P1.4 T2 External I/O for T2
- P1.5 T2EX Timer/Counter 2 Capture/Reload Trigger
- P1.6 RXD1 Serial Port1 Input
- P1.7 TXD1 Serial Port1 Output
- P2.0 A8 MSB Address bus bit 8
- P2.1 A9 MSB Address bus bit 9
- P2.2 A10 MSB Address bus bit 10
- P2.3 A11 MSB Address bus bit 11
- P2.4 A12 MSB Address bus bit 12
- P2.5 A13 MSB Address bus bit 13
- P2.6 A14 MSB Address bus bit 14
- P2.7 A15 MSB Address bus bit 15
- P3.0 RXD0 Serial Port 0 input
- P3.1 TXD0 Serial port 0 Output
- P3.2 INTO External Interrupt 0
- P3.3 INTI External Interrupt 1

- P3.4 T0 Timer 0 External Input
- P3.5 T1 Timer 1 External Input
- P3.6 WR External Data Memory Write Strobe
- P3.7 RD External Data Memory Read Strobe
- P4.0 CMSR0 Timer 2 compare match set/reset output 0
- P4.1 CMSR1 Timer 2 compare match set/reset output 1
- P4.2 CMSR2 Timer 2 compare match set/reset output 2
- P4.3 CMSR3 Timer 2 compare match set/reset output 3
- P4.4 CMSR4 Timer 2 compare match set/reset output 4
- P4.5 CMSR5 Timer 2 compare match set/reset output 5
- P4.6 CMT0 Timer 2 compare match toggle output 0
- P4.7 CMT1 Timer 2 compare match toggle output1
- P5.0 ADC0 A/D Converter input channel 0
- P5.1 ADC1 A/D Converter input channel 1
- P5.2 ADC2 A/D Converter input channel 2
- P5.3 ADC3 A/D Converter input channel 3
- P5.4 ADC4 A/D Converter input channel 4
- P5.5 ADC5 A/D Converter input channel 5
- P5.6 ADC6 A/D Converter input channel 6
- P5.7 ADC7 A/D Converter input channel 7
- P6.0 PWMO0 PWM channel 0 output
- P6.1 PWMO1 PWM channel 1 output
- P6.2 PWMO2 PWM channel 2 output
- P6.3 PWMO3 PWM channel 3 output
- P6.4 PWMC0 PWM0 clock input
- P6.5 PWMC1 PWM1 clock input
- P6.7 STADC Ext. A/D conversion start signal

SECTION 11: PROGRAMMABLE TIMERS

The DS87C550 contains the three timer/counters found on all other Dallas High-Speed Microcontrollers. Timers 0 and 1 have exactly the same functionality as in other members of the family, but have new clock features for the timer functions. Timer 2 also has the same functionality as earlier members of the family, but also has new capture and compare functions not found on earlier members. While earlier members of the family had a capture function associated with timer 2, this capture function is significantly different. Timer 2 also offers new clock features when operated in timer mode. These three timer/counters are described briefly below. Further detail may be found in the original High-Speed Microcontroller User's Guide. The new features will be described in detail below.

The functionality of these three timers is summarized as follows:

Timer 0	Timer 1	Timer 2
13-bit timer/counter	13-bit timer/counter	16-bit timer/counter
16-bit timer/counter	16-bit timer/counter	16-bit timer with capture
8-bit timer w auto-reload	8-bit timer w auto-reload	16-bit auto-reload timer/counter
Two 8-bit timer/counters	Ext. control pulse timer/counter	16-bit auto-reload up/down counter/timer
Ext. control pulse timer/counter	Baud rate generator	Baud rate generator
-	-	Timer output clock generator
		16-bit timer/counter with compare

TIMERS 0 AND 1

As stated earlier, the only differences in timer/counter 0 and 1 contained in older members of the High-Speed Microcontroller family and those found in the DS87C550 are in the clock selection possibilities. Drawings of these possibilities for various modes are given below.

TIMER/COUNTER 0 AND 1, MODES 0 AND 1: Figure 11-1.



TIMER/COUNTER 0 AND 1, MODE 2: Figure 11-2.



TIMER/COUNTER 0, MODE 3: Figure 11-3.



From the drawings, Table 11-1 can be derived. This table shows that when the timer/counter is used as a timer (i.e., it counts some number of system clocks), the frequency of timer clocks is a function of the crystal oscillator (or external oscillator) and timer clock source settings. The bits CD1, CD0, and $4X/\overline{2X}$ determine the system clock available to the timer, and the bits TxM (i.e., T0M and T1M) determine the clock source. The specific timer mode (8-bit, 16-bit, reload, etc.) does not affect the number of oscillator clocks per timer clock.

CD1	CD0	$4X/\overline{2X}$	$\mathbf{T}\mathbf{x}\mathbf{M} = 0$	$\mathbf{T}\mathbf{x}\mathbf{M} = 1$
0	0	1	12	1
0	0	0	12	2
0	1	Х	Reserved	Reserved
1	0	Х	12	4
1	1	Х	3,072	1,024
1	1	X	3,072	1,024

OSCILLATOR CLOCKS PER TIMER 0 or 1 CLOCK : Table 11-1

Where TxM is either the T0M or T1M SFR bit

TIMER 2

As stated earlier, the functionality of Timer/Counter 2 in the DS87C550 is a superset of the functions found on earlier members of the High-Speed Microcontroller family. However, for the same functions, the clock selection options are slightly different. The available clock selection options for various Timer 2 modes are shown in the drawings below.

TIMER/COUNTER 2, BAUD RATE GENERATOR MODE: Figure 11-4.

/RL2(T2CON.0) = 0; RCLK(T2CON.5) = 1 or TCLK(T2CON.4) = 1



DS87C550 High-Speed Microcontroller User's Guide Supplement TIMER/COUNTER 2, AUTO RELOAD MODE (/RL2 = 0): Figure 11-5.



(b) DCEN = 1



TIMER/COUNTER 2, CLOCK OUTPUT MODE: Figure 11-6.



TIMER 2 CAPTURE MODE

The capture mode of Timer 2 in the DS87C550 is slightly different from that function implemented on other High-Speed Microcontrollers. In the DS87C550, there are four 16-bit registers (eight 8-bit registers concatenated) that can capture values. Timer 2's output is the value that is captured when appropriate. It should be noted that Timer 2 can be configured in a number of different ways (i.e., counter, timer, autoreload, etc.) and still be used for the capture mode. Regardless of the meaning of Timer 2's value, it is this timer's output that is captured under the pre-established conditions.

The secondary function of four I/O pins (P1.0 – P1.3) is used to trigger one of the individual capture functions. If an appropriate edge occurs on the particular pin (as determined by of bits CTCON.7), then Timer 2's output at that time (all 16-bits) will be written into the associated capture register (CPTH0:CPTL0, CPTH1:CPTL1, CPTH2:CPTH2, CPTH3; CPTL3). By setting or clearing the bits on the CTCON register appropriately, the user can determine whether the rising or falling edge of the pin causes a capture.

It should be noted that the pins used to cause a Timer 2 capture are shared with the external interrupt pins. When used as an external interrupt, each pin can be programmed to be active high or low using the same bits (CTCON7:0). This functionality is illustrated in Figure 11-7 below.

TIMER/COUNTER 2 CAPTURE MODE: Figure 11-7.



TIMER 2 COMPARE MODE

Timer 2 of the DS87C550 offers a compare mode not previously included in any of the earlier high-speed microcontroller family members. The actual comparison takes place between Timer 2's 16-bit output and three 16-bit (actually six 8-bit concatenated) compare registers CMPH0:CMPL0, CMPH1:CMPL1, CMPH2:CMPL2. These compare registers are initialized by the user's software, and when/if a match occurs between Timer 2's output and one or more of the compare registers, the related interrupt flag is set and the interrupt is serviced if enabled. There are three separate interrupt flags with related enable and priority bits shown in the table below.

TIMER/COUNTER 2 CAPTURE MODE: Table 11-2.					
COMPARE	FLAG	ENABLE	PRIORITY		
0	CM0F (T2IR.4)	ECM0 (EIE.4)	PCM0 (EIP.4)		
1	CM1F (T2IR.5)	ECM1 (EIE.5)	PCM1 (EIP.5)		
2	CM2F (T2IR.6)	ECM2 (EIE.6)	PCM2 (EIP.5)		

INTED 2 CADTUDE MODE, Table 11-2

In addition to causing an interrupt, it is also possible to cause certain pins of the device (P4.0 - 4.7) to be set, reset or toggled in response to a match. This function is useful for building "PWM-like" operations

using Timer 2. Registers SETR and RSTR contain bits to enable this function. If a match occurs between Timer 2's output and CMPH0:CMPL0, port pins P4.0 to 4.5 are set when the corresponding bits in the set enable register (SETR) are logic 1. If the match is with CMPH1:CMPL1, port pins 4.0 to 4.5 are reset when the corresponding bits of the reset/toggle enable register (RSTR) are logic 1. A match with CMPH2:CMPL2 toggles port pins P4.6 and P4.7 if the corresponding bits in the reset/toggle enable register (RSTR) are logic 1. If any of the bits in SETR or RSTR are 0, then the corresponding port pin function is disabled. This functionality is further illustrated in Figure 11-8.



TIMER/COUNTER 2 COMPARE MODE: Figure 11-8.

WATCHDOG TIMER

The DS87C550 contains a watchdog timer that is very similar to that found in other members of the highspeed microcontroller family. It is driven directly off of the internal crystal oscillator (or external clock attached to XTAL1), and offers several divider chains to provide a wide variety of time-out selections. The watchdog timer in the DS87C550 is slightly different in several minor ways from that found in other high-speed microcontrollers. For one, the available divisors and hence the resulting time-out values are different. In earlier members of the family, divisors of 2^{17} , 2^{20} , 2^{23} , and 2^{26} were available. In the DS87C550, divisors of 2^{15} , 2^{18} , 2^{21} , and 2^{24} are available. Additionally, the system clock generation offers divisors of 1, 2, 3 and 256. Combining these two divisor chains, watchdog time-out periods ranging from 993 us to 130.2 s (2^{15} to 2^{32}) are possible with a 33 MHz crystal (or oscillator). With a crystal of 11.0952 MHz, time-out values from 2.963 ms up to 387.1 s (6.42 minutes) are possible. As can be seen, the watchdog timer can provide extremely log time-out periods that would be more difficult to achieve with the standard 8051 timers.

Another difference unique to the watchdog timer on the DS87C550 is the fact that there is no interrupt associated with it. Since there are so many other interrupt sources on the DS87C550, it was decided that an interrupt for the watchdog was less important than others and therefore not provided. While the interrupt flag still exists (WDCON.3) and it can be polled, there is no actual interrupt or interrupt vector location associated with this flag.

The possible settings for the watchdog interrupt time-out period are given in table 11-3. Remember that the actual reset (if enabled) occurs 512 clocks after the interrupt flag is set.

$4X/\overline{2X}$	CD1:0	WD1:0=00	WD1:0=01	WD1:0=10	WD1:0=11
1	00	2 ¹⁵	2^{18}	2^{21}	2^{24}
0	00	2^{16}	2^{19}	2^{22}	2^{25}
Х	01	2 ¹⁷	2^{20}	2^{23}	2^{26}
Х	10	2^{17}	2^{20}	2^{23}	2^{26}
Х	11	2^{25}	2^{28}	2^{31}	2^{34}

WATCHDOG TIMER INTERRUPT TIME-OUT PERIOD (in clocks): Table 11-3.

WATCHDOG TIMER: Figure 11-9.



Other than those differences described above, the watchdog timer is operated in the same way as earlier versions of the design. The time-out period is selected using the WD1 and WD0 bits (CKCON7:6). As the watchdog timer is a free running timer, it should be reset using the Reset Watchdog Timer bit (RWT= WDCON.0) before enabling the reset with the Enable Watchdog Timer Reset bit (EWT = WDCON.1) This will place the timer into a known state before the reset is enabled. As in the earlier designs, the RWT and EWT bits are timed access protected.

Crystal Failure Detection

An additional feature first introduced on the DS87C550 is the crystal failure detection circuit. While this feature is not directly related to the watchdog timer, it is discussed here because of its intended use. In earlier high-speed microcontroller designs, the watchdog timer was tied directly to the crystal oscillator just as it is in the DS87C550. While it has never been known to happen, it was theorized that it would be possible for the oscillator to stop functioning at a time when the processor was commanding some external action to take place. Since in this case, there is no oscillator to drive the watchdog timer, it would never reach its time-out value causing a processor to be reset. Since this could result in undesirable system performance, the crystal oscillator failure detection circuitry was added. In the event of an oscillator failure, this circuitry will cause the processor to be reset. If the oscillator frequency falls below TBD kHz, the circuitry will be triggered and will cause a processor reset. This feature is enabled by setting the OFDE bit (PCON.4), and disabled by clearing it.

SECTION 18: ANALOG TO DIGITAL CONVERTOR

Some members of the High-Speed Microcontroller family (DS87C550 for example) incorporate an onboard Analog-to-Digital Converter (A/D). When incorporated, these devices provide eight channels of analog input, internal sample & hold circuitry, a 10-bit successive approximation A/D converter, and related output and control registers. Additionally, a window comparison function is provided that allows conversion results to be ignored unless they are "of interest" where "of interest" is defined by the user as being within (or alternatively outside) a particular range of values. An internal precision voltage reference for the A/D function is also provided, along with the ability to select an externally supplied voltage reference for maximum flexibility.

The 10-bit output of the conversion process is read by the processor through two 8-bit registers, and the arrangement of this result is available in two formats as selected by the user. In 8-bit output mode, the most significant 8-bits of the result are placed in the A/D MSB result register (ADMSB). In 10-bit output mode, the two most significant bits of the result ADR9:ADR8 are placed in the two least significant bit positions of the ADMSB result register, and the eight least significant bits of the result are placed in the A/D LSB result register (ADLSB). A prescaler clock divider is included which allows a wide range of conversion clock frequencies to be selected.



A/D CONVERTER BLOCK DIAGRAM : Figure AD1

A block diagram of the complete A/D function is shown in Figure AD1. As can be seen, operation and control of the A/D is very straight forward, and is controlled via ADCON1, ADCON2, and the A/D reference select bit ADRS in the PWMADR register. If the window comparison function is used, then the WINHI and WINLO registers contain the user supplied window comparison values. If the A/D is configured for interrupt driven operation (rather than polled mode), then interrupt enable bits EA (IE.7) EAD (IE.6) bits must also be set.

A/D OPERATIONAL OVERVIEW

To enable the A/D function, the ADON bit (ADCON1.1) must be set. Following the setting of the ADON bit, software should delay 4 μ s before performing a conversion to allow the A/D converter to complete its power-up initialization. The A/D converter will measure one of the eight available input pins, ADC7-0, selected using the MUX2:MUX0 bits of the ADCON2 register. The initial conversion can be started by

writing a "1" to the STRT/BSY bit of the ADCON1 register, or alternately by a falling edge on the STADC pin when the ADEX bit of the ADCON1 is set. When the conversion starts, the analog value on the selected pin is held in the sample and hold circuitry for the remainder of the conversion.

The "latched" analog signal is applied to the input of the 10-bit successive approximation converter. The converter requires 16-clock cycles (provided from the prescaler) to perform a conversion. Due to the dynamic nature of the conversion process, the clock into the converter (t_{ACLK}) must be in the range of 1.0 μ s $\leq t_{ACLK} \leq 6.25 \mu$ s. Therefore the fastest possible conversion requires 16.0 μ s, and the slowest conversion requires 100 μ s. During the conversion process, the STRT/BSY (ADCON1.7) bit remains high until the conversion is complete at which time the hardware resets it. The hardware also sets the EOC bit (ADCON1.6) when the conversion is complete, and software must clear it if it is to be used on the next conversion.

After the first conversion is complete, another can be initiated using the STRT/BSY bit as described. Alternately, another conversion will be started automatically at the end of the first conversion if the CONT/SS bit (ADCON1.5) is set. In this continuous conversion mode, it is probably most convenient to enable the A/D interrupt function otherwise continuous polling (and clearing) the EOC bit would be required.

At the end of a conversion, the result is latched into a 10-bit latch, and is made available to the two A/D result registers ADMSB and ADLSB. As discussed above, the result may be presented in either 10-bit mode or 8-bit mode as selected by the user. Further details of the A/D functions are discussed below.

PRESCALER

The A/D clock Prescaler allows a wide selection of clock frequencies to be used for the conversion process. It divides the machine cycle clock frequency by the value written to the APS3:0 bits (ADCON1.3:0), and provides this resulting clock to the successive approximation converter. Since the machine cycle clock can be osc/1, osc/2, ocs/4, or osc/1024 as determined by bits CD1:0 and $4X/\overline{2X}$ of the PMR register, then the period of the clock output from the prescaler is given in Table AD1.

$4X/\overline{2X}$	CD1:0	t _{ACLK}
1	00	$(t_{OSC}*1)*(APS3:0+1)$
0	00	$(t_{OSC}*2)*(APS3:0+1)$
Х	01	$(t_{OSC}*4)*(APS3:0+1)$
Х	10	$(t_{OSC}*4)*(APS3:0+1)$
Х	11	(t _{OSC} *1024)*(APS3:0+1)

As an brief example of this calculation, assume that the processor is running using a 33.0 MHz crystal, and is in its reset default condition for the machine clock. If it is desired to set the A/D for its fastest possible conversion time (recalling that $1.0 \ \mu s \le t_{ACLK} \le 6.25 \ \mu s$), to what value what should APS3:0 be set. From row 3 of Table A/D1, it can be seen that 8 is the desired value.

 $(1/33Mhz * 4) * (8+1) = 1.091 \ \mu s$

As a further example, if the clock multiplier is used in 2X mode along with an 11.0592 MHz crystal , then from row two of the table it can be shown that 5 is the desired value.

(1/11.0592MHz * 2) *(5 + 1) = 1.085 µs

A/D REFERENCE VOLTAGE

A precision reference voltage is required by the A/D conversion process. Since this reference voltage is used in all conversions, it must be precise and stable. Otherwise the A/D result will be similarly unstable or imprecise (see the A/D result equation below). This reference may be obtained either from an internal band-gap or from a user supplied external source as selected by the ADRS (PWMADR.7) bit.

A/D Result = $1024(Vin - AV_{REF-}) / (AV_{REF+} - AV_{REF-})$

When the ADRS bit is cleared (reset default condition), the internal band-gap is selected as the A/D's positive reference voltage, and analog ground is the negative reference. This internal band-gap produces a positive A/D reference voltage of 2.5 volts typically (see DC specifications) and therefore limits the range of analog voltages on the input pins to the range of 0 to 2.5 volts. If a larger analog input voltage is desirable, an external reference voltage may be used.

When the ADRS bit is set, the user may provide an external voltage reference to the A/D on pins AV_{REF+} and AV_{REF-} . These voltages have minimum and maximum specifications associated with them which must be followed (see DS specifications). However, AV_{REF+} may be in the range of the analog supply voltage AV_{CC} which is most frequently 5 volts. Therefore a larger range of analog input voltages (0 to 5 volts) is possible when an external voltage reference is used.

A/D INTERRUPT

The interrupt flag for the A/D converter is the EOC bit (ADCON1.6) and is set by hardware when the current conversion completes. Once set it must be cleared by software. This interrupt is qualified by several settings. First for an A/D interrupt to be acknowledged, the EAD (Enable A/D Interrupt, IE.6) bit must be set. Additionally as with all interrupts, the global interrupt enable bit, EA (IE.7) must be set before any interrupt will be acknowledged. The A/D interrupt is also qualified by the WCM bit (ADCON1.2) when the user selects the window comparison function by setting the WCQ (ADCON1.3) bit. With WCQ set, an A/D interrupt will occur only when the comparison function is true. If WCQ is not set, then an A/D interrupt will occur any time when EOC is set and enable bits EAD and EA are set. A more detailed description of the window comparison function follows.

WINDOWED COMPARATOR

The A/D Converter found in some Dallas High-Speed Microcontrollers has a unique feature associated with it called the Window Comparator. This feature allows the user to establish boundaries against which each A/D converter result is compared. If the results of the A/D are "of interest" as defined by the user supplied boundary conditions, the feature will allow an interrupt to be generated. Otherwise no interrupt is generated, and the results can be ignored. This relieves the processor of the burden of acknowledging data that is not of interest.

The user enables this feature by setting the Window Comparator Qualifier bit WCQ (ADCON1.3). Of course as described in the discussion of interrupts, the A/D interrupt enable and global interrupt enable bits must also be set for an interrupt to be acknowledged. The user sets the boundaries with the two 8-bit registers WINHI and WINLO. The values loaded into these registers are compared to each A/D result. It is important to note that the comparison is performed between one of these registers and the eight MSBs of the A/D result. This comparison takes place before the 10-bit A/D result is passed to the two 8-bit result registers ADMSB and ADLSB. Therefore the user selected method of displaying the 10-bit result has no affect on the comparison function. The comparison is always performed on the eight MSBs of the

A/D result. This must be taken into account when selecting the values to be loaded into the WINHI and WINLO registers.

The equations for the window comparison function are as follows:

WCM = (WINHI > ADMSB) AND (ADMSB \geq WINLO) when WCIO = 0

Or

WCM = (WINHI \leq ADMSB) OR (ADMSB < WINLO) when WCIO = 1

The WCIO bit defines whether the data of interest is inside (WCIO = 0) or outside (WCIO = 1) the boundaries defined by the contents of WINHI and WINLO. As a specific example suppose that you want to use the windowed comparison function to allow an A/D interrupt to occur when the A/D results are in the range of 256_{10} and 511_{10} . The first thing to recognize is that the comparison takes place between the 8-MSbs of the A/D result and the 8-bit WINHI and WINLO registers which leaves the two LSBs of the result unused. Converting the base 10 numbers to base 16 and truncating to the 8-MSBs, it can be seen that the WINLO register should be loaded with 40_{16} and the WINHI register with $7F_{16}$. Since the two LSBs of the A/D result are ignored in the comparison, the interrupt will occur for values from 256_{10} and 508_{10} . This slight inaccuracy is inherent due to the 8-bit comparison. By setting the global interrupt enable bit EA (IE.7), A/D interrupt enable EAD (IE.6) bit, the Window Compartor qualifier bit WCQ (ADCON1.3), and clearing the Window Compare Inside/Outside bit WCIO (ADCON1.0) the desired function will be implemented. By simply setting the WCIO bit, the data outside the stated boundaries can be acknowledged.

SECTION 19: PULSE WIDTH MODULATION

Some members of the High-Speed Microcontroller family incorporate Pulse Width Modulation (PWM) capability. When incorporated, there are four independent 8-bit channels provided, each of which can operate at a different repetition rate and with an independent pulse width setting. For more precise PWM requirements, two 8-bit PWM channels can be combined into one 16-bit PWM channel. For 16-bit operation, channels PWM0 and PWM1 are combined and/or PWM2 and PWM3 are combined. As shown in Figure PWM1, each channel of PWM can accept any one of four clock signals derived from the processor's machine cycle clock, or an externally generated clock available on the PWMC0 or PWMC1 pins. These two PWM external clock input pins are distributed to the four channels as shown. Each PWM channel has its own output pin that is a second function for one of the processor's parallel I/O pins.

The PWM function is divided into three functional modules: the prescaler, the Clock Generator, and the Pulse Generator. Each of these modules is described in detail below.



PWM Block Diagram (8-Bit Mode) : Figure PWM1.

PRESCALER

There is a single prescaler that divides the machine cycle clock by 1, 4, 16, or 64, and each of these outputs is available to all four PWM channels simultaneously. Since the machine cycle clock is an integer division of the crystal oscillator (or external clock source connected to XTAL1), and this division factor is determined by the user's setting of CD1: 0 and $4X/\overline{2X}$, then these bits will also affect the frequency of operation of the PWM channels as well. The selection of one of the four clock sources available as outputs from the prescaler or one of the externally supplied clocks is made individually, channel by channel with the PW0S2:0 (PW01CS7:5), PW1S2:0 (PW01CS3:1), PW2S2:0 (PW23CS7:5), and PW3S2-0 (PW23CS3:1) bits in SFRs.

CLOCK GENERATOR

As shown in Figure PWM1, the four clock outputs available from the prescaler are all provided to each of the four Clock Generator modules along with the two external PWM clock inputs. The Clock Generator modules simply select one of the available clocks, use this selection to clock an 8-bit auto-reload counter, and provide the output of this counter to the Pulse Generator module. The logical behavior of PWM0's Clock Generator module is shown in Figure PWM2. All other Clock Generators operate in the same way.

PWM0 CLOCK GENERATOR : Figure PWM2



Special Function Registers PW01CS and PW23CS contain the bits that select the prescaler output and also enable/disable the Clock Generator module. The SFR PW01CS contains enable bits for PWM channels 0 (PW0EN = PW01CS.4) and 1 (PW1EN = PW01CS.0). The SFR PW23CS contains similar enables for PWM channels 2 (PW2EN = PW23CS.4) and 3 (PW3EN = PW23CS.0). These enable bits are cleared to 0 (disabled) on a reset, and therefore must be set to 1 before the PWM function can be used.

As illustrated in Figure PWM2, the Clock Generator is an 8-bit auto-reloadable down counter. When the counter decrements to zero in response to the selected clock input, it is reloaded with the value stored by the application software in the PWM frequency generator registers PW0FG, PW1FG, PW2FG, and PW3FG. Because of the design of these counters, the frequency of the clock output from the Clock Generator module is defined as:

PWM-Clock = prescaler Output / (N+1) where N = contents of PWxFG register or N = (prescaler Output/PWM-Clock)-1

Therefore if the frequency generator register (PW0FG, PW1FG, PW2FG, or PW3FG) is loaded with the value of 0, then the clock is divided by 1, and passed to the Pulse Generator module. If the value of 1 is loaded, the clock is divided by 2 and passed to the Pulse Generator. If the value of 255 (maximum value) is loaded, then the clock passed to the Pulse Generator is the prescaler clock divided by 256. With the ability to select the prescaler output (/1, /4, /16, or /64), and the ability to select its divisor from a value between 1 and 256 (inclusive), a large range of PWM-Clock rates is possible. Table PWM1 shows the equations for determining the PWM-Clock rate.

$4X/\overline{2X}$	CD 1:0	PWxS2:0=00 0	PWxS2:0=0 01	PWxS2:0=010	PWxS2:0=01 1	PWxS2:0=1xx	
1	00	(osc/1)/(N+1)	(osc/4)/(N+1)	(osc/16)/(N+1)	(osc/64)/(N+1)	PWMCx/(N+1)	
0	00	(osc/2)/(N+1)	(osc/8)/(N+1)	(osc/32)/(N+1)	(osc/128)/(N+1)	PWMCx/(N+1)	
Х	01	(osc/4)/(N+1)	(osc/16)/(N+1)	(osc/64)/(N+1)	(osc/256)/(N+1)	PWMCx/(N+1)	
Х	10	(osc/4)/(N+1)	(osc/16)/(N+1)	(osc/64)/(N+1)	(osc/256)/(N+1)	PWMCx/(N+1)	
х	11	(osc/1.024)/(N+1)	4.096/(N+1)	(osc/16.384)/(N+1)	(osc/65.536)/(N+1)	PWMCx/(N+1)	

PWM Clock Generation : Table PWM1

where: osc = frequency of the attached crystal or external clock source attached to XTAL1N = contents of PWxFG register

PWMCx = Frequency of the external PWM clock input PWMC0 (P6.4) or PWMC1 (P6.5)

As a simple example of this timing information, assume that the processor is in its reset default condition running from an 11.0592 MHz crystal (or external clock), and the user wants to establish the maximum repetition rate for PWM0 while maintaining a machine cycle clock of divide by 4. In this case, $4X/\overline{2X} = xx$, CD1:0 = 10b, PW01S2:0 = 000b, and PW0FG = 0000000b. Since N = 00h (i.e., PW0FG = 00h), the equation shows this combination will provide the maximum PWM clock rate. Performing the calculation:

PWM Clock =
$$\frac{\text{Osc } / 4}{\text{N} + 1}$$

= $\frac{11.0592 \text{ MHz } / 4}{0 + 1}$
= 2.76 MHz

Since the PWM Pulse Generator section is basically an 8-bit counter (in 8-bit PWM mode), 256 clocks are required for the counter to make one complete cycle. This dictates that the repetition rate of the PWM channel will be the PWM clock/256. Therefore in this example, the repetition rate of PWM0 will be:

Repetition Rate (8-bit mode) = $\frac{\text{PWM Clock}}{256}$ $= \frac{2.76 \text{ MHz}}{256}$ = 10.80 kHz $\therefore 92.59 \text{ us}$

PULSE GENERATOR

The Pulse Generator portion of the PWM function generates the PWM output. The logical operation of the Pulse Generator section of PWM0 in 8-bit mode is illustrated in Figure PWM3. All other PWM channels operate in a similar fashion. From the user's perspective, the Pulse Generator can be considered simply an 8-bit up counter driven by the PWM Clock. As this 8-bit counter rolls over from 0FFh to 00h, the corresponding PWM output is set high. As the counter continues to count up and pass through the user selected value stored in register PWM0, PWM1, PWM2, or PWM3, the PWM output is cleared to zero. In this way, the duty cycle of the PWM output is determined by the value loaded by the user into the PWMx (i.e., PWM0, PWM1, PWM2, PWM3) registers. The duty cycle of the PWM function is given by the following equation:

PWM Duty Cycle(%) = $\frac{PWMx}{256}$

With the minimum value of zero loaded into PWM register, the equation illustrates that this produces a 0% duty cycle signal (never goes high). With the maximum value of 255 loaded into the PWM register, a duty cycle of 99.609% is generated. If a duty-cycle of precisely 100% is required, the DC override bits PW0DC (PW01CON.6), PW1DC (PW01CON.2), PW2DC (PW23CON.6), and PW3DC (PW23CON.2) will force the PWM output to be high for the entire cycle when set.

PWM0 PULSE GENERATOR : Figure PWM3.



The user supplied value contained in the PWMx register is reloaded into the compare value register when there is a match between the counter and the value. This means that changing the value of PWMx more frequently than once every 256 PWM-Clocks will have no effect. This prevents software from creating "glitches" in the PWM output.

The PWMx registers also provide a means to read or write the value of the associated 8-bit counter. When the bits PW0T/C (PW01CON.4), PW1T/C (PW01CON.0), PW2T/C (PW23CON.4), or PW3T/C (WP23CON.0) are cleared (reset default condition), reading or writing the associated PWMx register accesses the PWM user supplied comparison value. When these bits are set, reading or writing the associated PWMx register accesses the Pulse Generator's 8-bit counter. If it is important that the first cycle of the PWM have precisely correct timing, then this feature may be used to initialize the 8-bit counter to zero.

The rollover condition of the Pulse Generator from 0FFh to 00h is detected and causes the PWM output to be set as described previously. This condition also causes the corresponding flag bit PW0F (PW01CON.7), PW1F (PW01CON.3), PW2F (PW23CON.7), or PW3F (PW23CON.3) to be set providing a means for software to determine when the rollover occurs. Software is the only mechanism to clear these bits once they are set.

The outputs of the PWM channels share pins with parallel I/O port pins. To enable the PWM channel's output, the corresponding PWM Output Enable bit must be set. These enable bits PW00E (PW01CON.5), PW10E (PW01CON.1), PW20E (PW23CON.5), and PW30E (PW23CON.1) are all cleared by reset, and must be set before using the PWM outputs.

16-Bit PWM Mode

The four 8-bit PWM functions offer the unique ability to be cascaded into two 16-bit PWM functions. By setting PWE0 (PWMADR.0) or PWE1 (PWMADR.1), 16-bit mode is enabled for PWM0 or PWM1 respectively. Note that the 16-bit PWM function called PWM1 is actually a concatenation of resources from 8-bit PWM2 and PWM3 functions. As an example, the output pin of 16- bit PWM1 is PWMO2, which is normally the output pin for 8-bit PWM2. This relationship is true for a number of registers and bits used in the 16-bit PWM1 function. For 16-bit PWM0, the output pin will be PWM00 as would be expected. These differences will be detailed in the following discussion.

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Achieving 16-bit PWM operation involves the concatenation of resources found in the Pulse Generator section of the PWM function. This is illustrated in Figure PWM4. As shown, two 8-bit counters are combined to form a 16-bit counter and two 8-bit compare value registers are combined to form a 16-bit compare value register. Additionally, two 8-bit zero comparators are combined to form a 16-bit zero comparator, and two 8-bit match comparators are combined to form a 16-bit match comparator.

Other than this concatenation of 8-bit blocks into 16-bit blocks, operation of the Pulse Generator section is the same as in 8-bit mode. As the 16-bit counter passes through zero, the output of the PWM is set. As the counter continues to count and passes through the user supplied value, the PWM output is reset. Therefore the user-supplied value determines the pulse width of the PWM output. The equation for the duty cycle is given by the following equation:

PWM Duty Cycle(%) = $\frac{PWMx}{65,536}$

where PWMx is the 16-bit user-supplied value

The 16-bit user defined value is loaded through two 8-bit SFRs. For the 16-bit PWM0 function, SFR PWM0 loads the LSB of the user defined value, and PWM1 loads the MSB of the user defined value. For the 16-bit PWM1 function, PWM2 loads the LSB and PWM3 loads the MSB. Note that in Figure PWM4, all registers and bits associated with the 16-bit PWM0 function are shown without parentheses. All registers and bits associated with the 16-bit PWM1 functions are shown in parentheses.

If a duty cycle of exactly 100% is required, setting the bit PW0DC (PW01CON.6) forces the output of 16-bit PWM0 high for the entire counter cycle. Similarly, setting the bit PW2DC (PW23CON.6) forces the output of 16-bit PWM1 high for the entire counter cycle.

The user-supplied value loaded into the PWMx registers is reloaded into the associated compare value register when there is a match between the counter and the user supplied value. Therefore, changing the value of PWMx more frequently than once every 65,536 PWM-Clocks will have no effect.

As illustrated in Figure PWM4, the PWMx registers can access either the counters or the compare value register. Setting bit PW0T/C (PW01CON.4) allows register PWM0 to access the LSB of the 16-bit counter. Clearing it accesses the LSB compare value register.



16-BIT PWM MODE PULSE GENERATOR : Figure PWM4.

Similarly, setting bit PW1T/C (PW01CON.0) allows register PWM1 to access the MSB of the 16-bit counter. Clearing it accesses the MSB compare value register.

As described in 8-bit mode, flags PW0F (PW01CON.7) and PW2F (PWM23CON.7) indicate a rollover from 0FFh to 00h of the counters for 16-bit PWM0 and PWM1 respectively.

The PWM outputs are disabled on all forms of reset. To enable the output of 16-bit PWM0 on pin PWM00, the bit PW00E (PW01CON.5) must be set, and to enable the output of 16-bit PWM1 on pin PWM02, the bit PW20E must be set.

All of the Clock Generator sections operate exactly as they did in 8-bit mode. The thing to remember is that only registers and bits for Clock Generators used for 8-bit PWM0 and PWM2 will function in 16-bit mode. Other registers and bits used in 8-bit mode (PWM1, PWM3 as examples) no longer serve a purpose in 16-bit mode.

As before, bits PW0S2:0 and PW0EN (PW01CS7:4) will enable the prescaler and will determine the selected PWM-Clock input for 16-bit PWM0. Similarly, bits PW2S2:0 and PW2EN (PW23CS7:4)) will enable the prescaler and will determine the selected PWM-Clock input for 16-bit PWM1. Bits PW01CS3:0 and PW23CS3:0 have no effect when the corresponding PWM channel is set for 16-bit mode.

The same is true for the Clock Generator divisors. Only those associated with 8-bit PWM functions 0 and 2 will have any effect. It is important to recognize that while the Clock Generators operate in the same way and produce the same clock frequencies as they did in 8-bit mode, the repetition rate will be much longer since the clock now operates a 16-bit counter in the Pulse Generator module. Therefore the equation for the 16-bit mode repetition rate is as follows:

Repetition Rate (8-bit mode) = $\frac{PWM Clock}{65,536}$

Using the previous example where the PWM clock was 2.76 MHz, the 16-bit repetition rate becomes:

Repetition Rate (8-bit mode)	_ PWM Clock
Repetition Rate (6-bit mode)	65,536
	_ 2.76 MHz
	65,536
	= 42.11 Hz
	: 23.74 ms

Since 16-bit mode typically results in a fairly slow repetition rate, it may be desirable to adjust the CD1:0 and $4X/\overline{2X}$ bits to select a divide by 1 or divide by 2 of the crystal as the machine cycle clock. This results in an increased frequency being available to the PWM function.