Rev 0; 1/03

Triple 128-Position Nonvolatile Variable Digital Resistor/Switch

General Description

The DS3904 contains three nonvolatile (NV) low temperature coefficient variable digital resistors. Each resistor has 128 user-selectable positions. Additionally, the DS3904 has a high-impedance option that allows each resistor to function as a digital switch. The DS3904 can operate over a 2.7V to 5.5V supply voltage range, and communication with the device is achieved through a 2-wire serial interface. An address pin allows two DS3904s to operate on the same bus. The low-cost and small size of the DS3904 make it an ideal replacement for conventional mechanical trimming resistors.

Features

- **Three 20kΩ, 128-Position Linear Digital Resistors**
- **Resistor Settings are Stored in NV Memory**
- **Each Resistor has a High-Impedance Setting for Switch Operation to Control Digital Logic**
- **Low Temperature Coefficient**
- **2-Wire Serial Interface**
- **2.7V to 5.5V Operating Range**
- **Industrial Temperature Range: -40°C to +85°C**
- **Packaging: 8-Pin µSOP**

Applications

Power-Supply Calibration

Cell Phones and PDAs

Fibre Optic Transceiver Modules

Portable Electronics

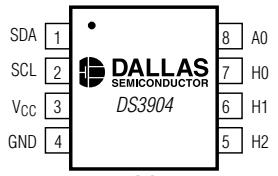
Small and Low-Cost Replacement for Conventional Mechanical Trimming Resistors

Test Equipment

Ordering Information

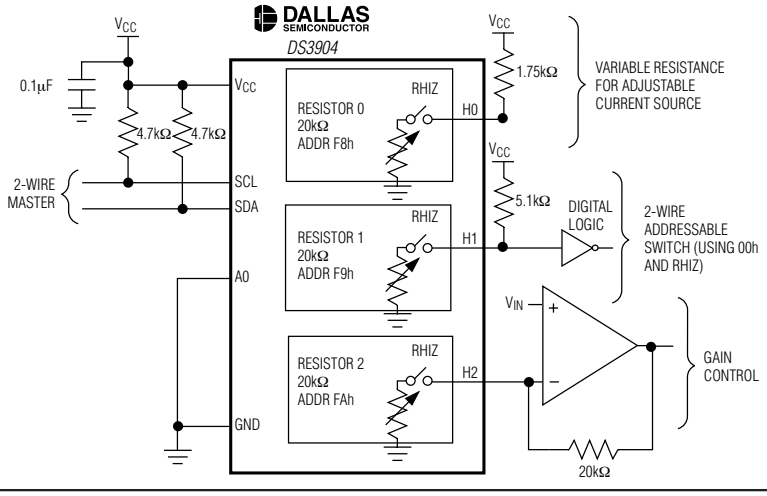
PART	TEMP RANGE	PIN-PACKAGE	RESISTANCE
DS3904	-40°C to +85°C	8 µSOP	20kΩ + Hi-Z

Pin Configuration



µSOP

Typical Operating Circuit



DS3904 Triple 128-Position Nonvolatile Variable Digital Resistor/Switch

ABSOLUTE MAXIMUM RATINGS

Voltage on V_{CC} Pin Relative to Ground.....-0.5V to +6.0V
Voltage on SDA, SCL, and
A0 Relative to Ground*.....-0.5V to V_{CC} + 0.5V
Voltage on H0, H1, and
H2 Relative to Ground.....-0.5V to +6.0V when V_{CC} Powered
Current Through H0, H1, and H2.....3mA

Operating Temperature Range .....-40°C to +85°C
Programming Temperature Range .....0°C to +70°C
Storage Temperature Range .....-55°C to +125°C
Soldering Temperature .....See J-STD-020A Specification

*This voltage must not exceed 6.0V.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A = -40°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	(Note 1)	2.7		5.5	V
Input Logic 1	V_{IH}		0.7 x V_{CC}		V_{CC} + 0.3	V
Input Logic 0	V_{IL}		-0.3		0.3 x V_{CC}	V
Resistor Current	I_R				3	mA
Resistor Terminals H0, H1, H2		V_{CC} = +2.7V to +5.5V	-0.3		+5.5	V

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage	I_L	(Note 2)	-1		+1	µA
Standby Supply Current	I_{STBY}	V_{CC} = 3V (Note 3)		95	200	µA
		V_{CC} = 5V (Note 3)		145		
Low-Level Output Voltage (SDA)	V_{OL1}	3mA sink current	0		0.4	V
	V_{OL2}	6mA sink current	0		0.6	

ANALOG RESISTOR CHARACTERISTICS

(V_{CC} = +2.7V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Absolute Linearity		(Note 4)	-1		+1	LSB
Relative Linearity		(Note 5)	-0.5		+0.5	LSB
Temperature Coefficient		Position 7Fh (Note 6)	-200	+123	+400	ppm/°C
Position 7Fh Resistance	R_{MAX}	T_A = +25°C	14.5	20	25.5	kΩ
Position 00h Resistance	R_{MIN}	T_A = +25°C	200		500	Ω
High Impedance	R_{HI-Z}		5			MΩ

DS3904 Triple 128-Position Nonvolatile Variable Digital Resistor/Switch

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +5.5V, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	Fast mode (Note 7)	0		400	kHz
		Standard mode (Note 7)	0		100	
Bus Free Time between STOP and START Conditions	t_{BUF}	Fast mode (Note 7)	1.3			µs
		Standard mode (Note 7)	4.7			
Hold Time (Repeated) START Condition	$t_{HD:STA}$	Fast mode (Notes 7, 8)	0.6			µs
		Standard mode (Notes 7, 8)	4.0			
Low Period of SCL Clock	t_{LOW}	Fast mode (Note 7)	1.3			µs
		Standard mode (Note 7)	4.7			
High Period of SCL Clock	t_{HIGH}	Fast mode (Note 7)	0.6			µs
		Standard mode (Note 7)	4.0			
Data Hold Time	$t_{HD:DAT}$	Fast mode (Notes 7, 9, 10)	0		0.9	µs
		Standard mode (Notes 7, 9, 10)	0		0.9	
Data Setup Time	$t_{SU:DAT}$	Fast mode (Note 7)	100			ns
		Standard mode (Note 7)	250			
Start Setup Time	$t_{SU:STA}$	Fast mode	0.6			µs
		Standard mode	4.7			
Rise Time of Both SDA and SCL Signals	t_R	Fast mode (Note 11)	$20 + 0.1C_B$		300	ns
		Standard mode (Note 11)	$20 + 0.1C_B$		1000	
Fall Time of Both SDA and SCL Signals	t_F	Fast mode (Note 11)	$20 + 0.1C_B$		300	ns
		Standard mode (Note 11)	$20 + 0.1C_B$		300	
Setup Time for STOP Condition	$t_{SU:STO}$	Fast mode	0.6			µs
		Standard mode	4.0			
Capacitive Load for Each Bus Line	C_B	(Note 11)			400	pF
EEPROM Write Time	t_W	(Note 12)		20		ms
Startup Time	t_{ST}				2	ms

NONVOLATILE MEMORY CHARACTERISTICS

(V_{CC} = +2.7V to +5.5V, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Writes		85°C	50,000			

DS3904 Triple 128-Position Nonvolatile Variable Digital Resistor/Switch

AC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +2.7V to +5.5V, T_A = -40°C to +85°C.)

Note 1: All voltages are referenced to ground.

Note 2: Applies to AO, SCL, SDA as well as H0, H1, and H2 in the high-impedance state.

Note 3: I_{STBY} specified with SDA = SCL = V_{CC} and A0 = GND.

Note 4: Absolute linearity is used to determine expected resistance. Absolute linearity is defined as the deviation from the straight line drawn from the value of the resistance at position 00h to the value of the resistance at position 7Fh.

Note 5: Relative linearity is used to determine the change of resistance between two adjacent resistor positions.

Note 6: Temperature coefficient specifies the change in resistance as a function of temperature. The temperature coefficient varies with resistor position. Guaranteed by design.

Note 7: A fast-mode device can be used in a standard-mode system, but the requirement $t_{SU:DAT}$ > 250ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_{RMAX} + $t_{SU:DAT}$ = 1000ns + 250ns =1250ns before the SCL line is released.

Note 8: After this period, the first clock pulse is generated.

Note 9: The maximum $t_{HD:DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.

Note 10: A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the $V_{IN\ MIN}$ of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.

Note 11: C_B—total capacitance of one bus line in picofarads, timing referenced to 0.9 x V_{CC} and 0.1 x V_{CC}.

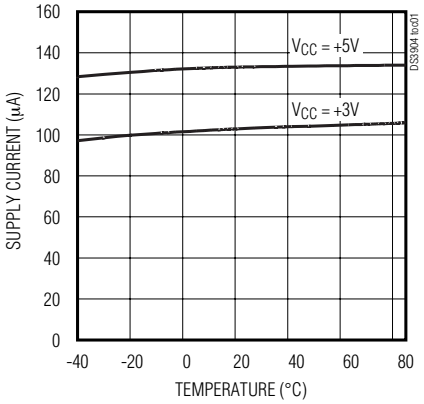
Note 12: EEPROM write begins after a stop condition occurs.

DS3904 Triple 128-Position Nonvolatile Variable Digital Resistor/Switch

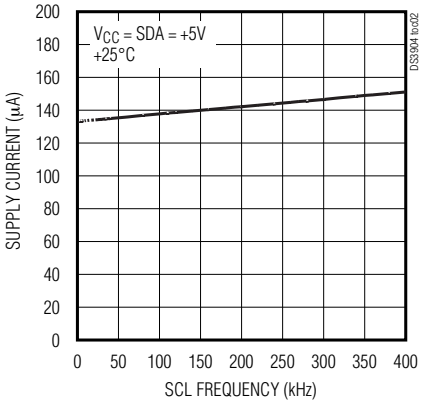
Typical Operating Characteristics

(V_{CC} = +5.0V; 20kΩ plots apply to Res0, Res1, and Res2, T_A = +25°C unless otherwise noted.)

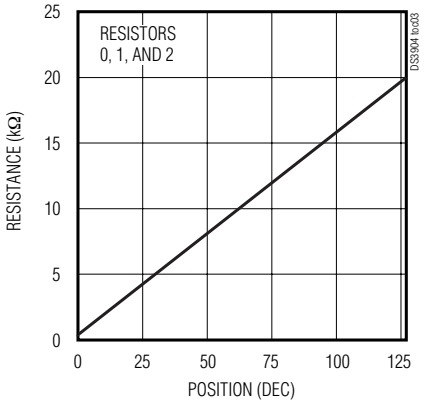
SUPPLY CURRENT vs. TEMPERATURE



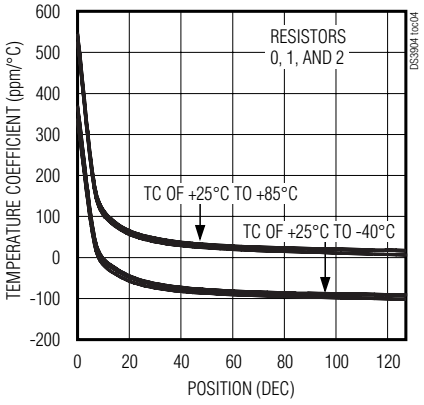
SUPPLY CURRENT vs. SCL FREQUENCY



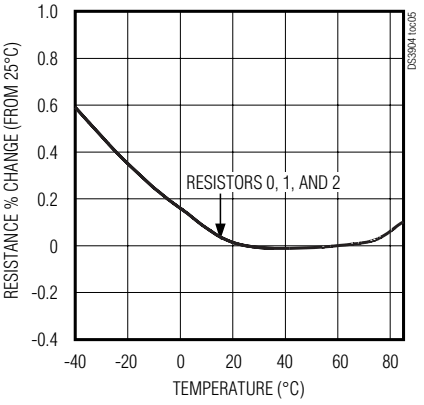
RESISTANCE vs. POSITION



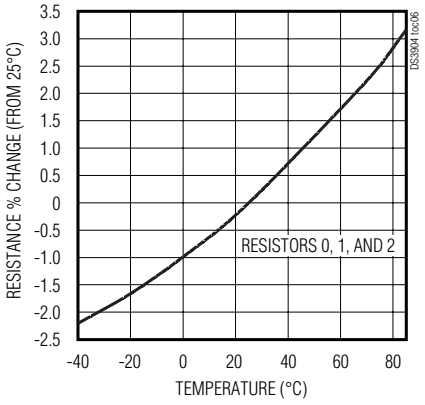
TEMPERATURE COEFFICIENT vs. POSITION



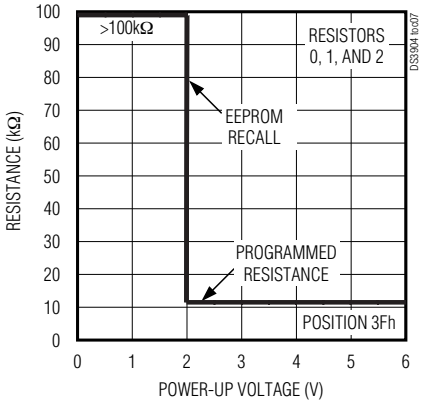
POSITION 7Fh RESISTANCE PERCENT CHANGE FROM +25°C vs. TEMPERATURE



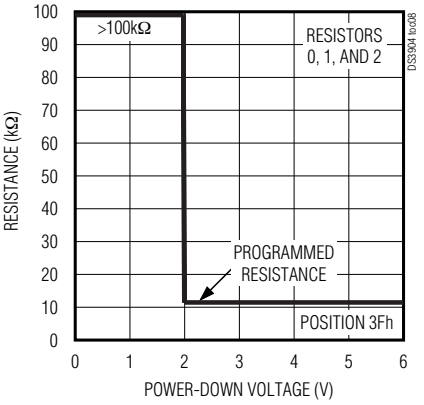
POSITION 00h RESISTANCE PERCENT CHANGE FROM +25°C vs. TEMPERATURE



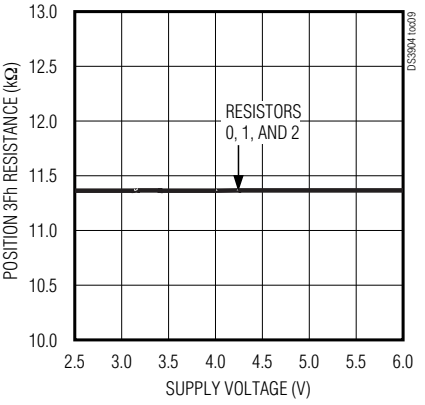
RESISTANCE vs. POWER-UP VOLTAGE



RESISTANCE vs. POWER-DOWN VOLTAGE



POSITION 3Fh RESISTANCE vs. SUPPLY VOLTAGE

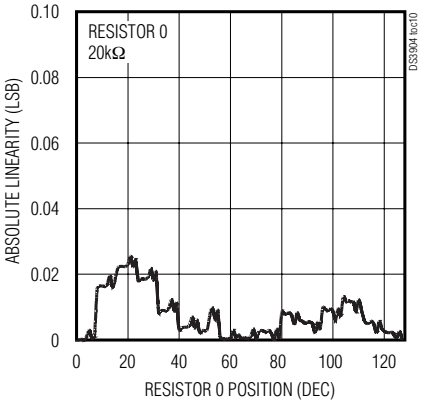


DS3904 Triple 128-Position Nonvolatile Variable Digital Resistor/Switch

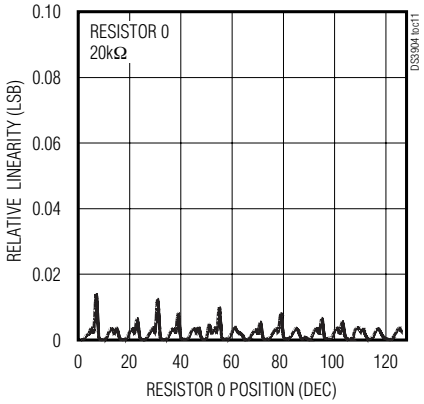
Typical Operating Characteristics (continued)

(V_{CC} = +5.0V; 20kΩ plots apply to Res0, Res1, and Res2, T_A = +25°C unless otherwise noted.)

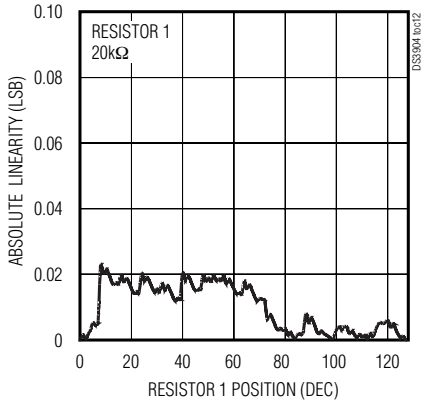
ABSOLUTE LINEARITY vs. RESISTOR 0 POSITION



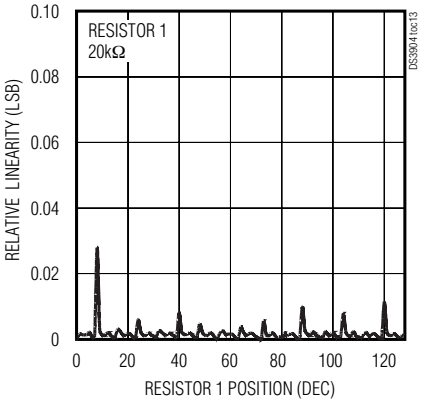
RELATIVE LINEARITY vs. RESISTOR 0 POSITION



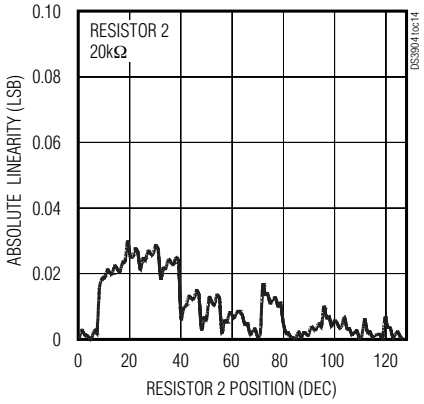
ABSOLUTE LINEARITY vs. RESISTOR 1 POSITION



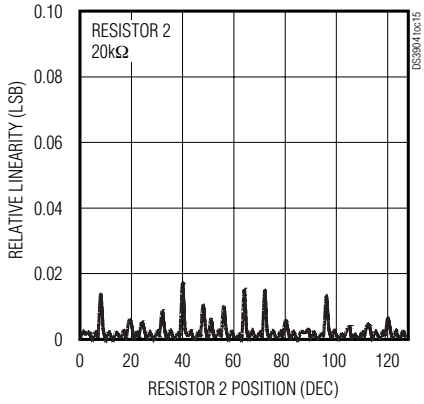
RELATIVE LINEARITY vs. RESISTOR 1 POSITION



ABSOLUTE LINEARITY vs. RESISTOR 2 POSITION



RELATIVE LINEARITY vs. RESISTOR 2 POSITION



DS3904 Triple 128-Position Nonvolatile Variable Digital Resistor/Switch

Pin Description

PIN	NAME	FUNCTION
1	SDA	2-Wire Serial Data. Open-drain input/output for 2-wire data.
2	SCL	2-Wire Serial Clock. Input for 2-wire clock.
3	V_{CC}	Supply Voltage Terminal
4	GND	Ground Terminal
5, 6, 7	H2, H1, H0	Resistor High Terminals
8	A0	Address-Select Input

Detailed Description

The DS3904 contains three, 128-position, NV, low temperature coefficient variable digital resistors. It is controlled through a 2-wire serial interface, and it serves as a low-cost replacement for designs using conventional trimming resistors. Furthermore, the address pin allows two DS3904s to be placed on the same 2-wire bus.

With its low cost and small size, the DS3904 is well tailored to replace larger mechanical trimming variable resistors. This allows the automation of calibration in many instances because the 2-wire interface can easily be adjusted by test/production equipment.

Variable Resistor Memory Organization

The variable resistors of the DS3904 are addressed by communicating with the registers in Table 1.

Table 1. Variable Resistor Registers

ADDRESS	VARIABLE RESISTOR	POSITION 7Fh RESISTANCE	NUMBER OF POSITIONS*
F8h	Resistor 0	20kΩ	128 (00h to 7Fh) + Hi-Z
F9h	Resistor 1	20kΩ	128 (00h to 7Fh) + Hi-Z
FAh	Resistor 2	20kΩ	128 (00h to 7Fh) + Hi-Z

** Writing a value greater than 7Fh to any of the resistor registers sets the high-impedance mode control bit (RHIZ, the MSB of the resistor register) resulting in the resistor going into high-impedance mode.*

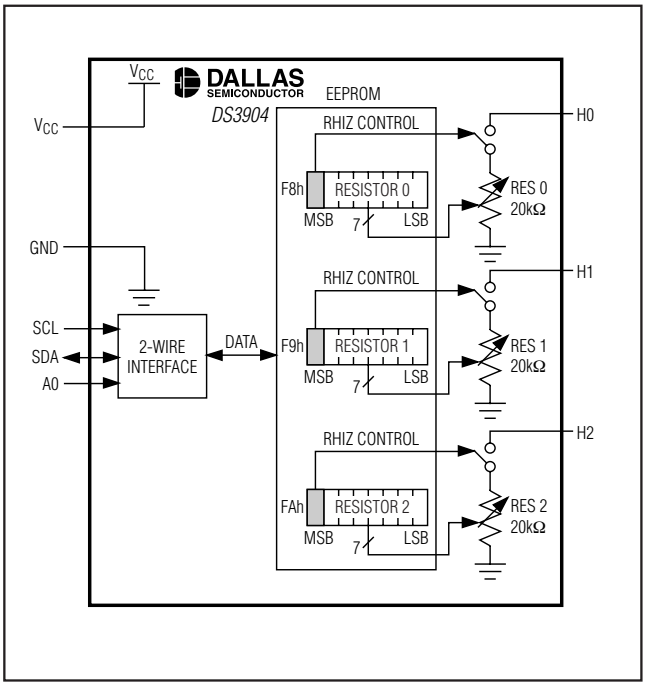


Figure 1. DS3904 Block Diagram

Device Operation

Clock and Data Transitions

The SDA pin is normally pulled high with an external resistor or device. Data on the SDA pin can only change during SCL low time periods. Data changes during SCL high periods indicates a start or stop condition depending on the conditions discussed below. See the timing diagrams for further details (Figures 2 and 3).

Start Condition

A high-to-low transition of SDA with SCL high is a start condition, which must precede any other command. See the timing diagrams for further details (Figures 2 and 3).

Stop Condition

A low-to-high transition of SDA with SCL high is a stop condition. After a read or write sequence, the stop command places the DS3904 into a low-power mode. See the timing diagrams for further details (Figures 2 and 3).

Acknowledge

All address and data bytes are transmitted through a serial protocol. The DS3904 pulls the SDA line low during the ninth clock pulse to acknowledge that it has received each byte.

DS3904 Triple 128-Position Nonvolatile Variable Digital Resistor/Switch

Standby Mode

The DS3904 features a low-power mode that is automatically enabled after power-on, after a stop command, and after the completion of all internal operations.

Bus Reset

After any interruption in protocol, power loss, or system reset, the following steps reset the DS3904:

1) Clock up to nine cycles.
2) Look for SDA high in each cycle while SCL is high.
3) Create a start condition while SDA is high.

Device Addressing

The DS3904 must receive an 8-bit device address byte following a start condition to enable a specific device for a read or write operation. The address byte is clocked into the DS3904 MSB to LSB. The address byte consists of 101000 binary followed by A0 then the R/$\overline{W}$ bit. If the R/$\overline{W}$ bit is high, a read operation is initiated. If the R/$\overline{W}$ bit is low, a write operation is initiated. For a device to become active, the value of the A0 bit must be the same as the hard-wired address pins on the DS3904. Upon a match of written and hard-wired addresses, the DS3904 outputs a zero for one clock cycle as an acknowledge. If the address does not match, the DS3904 returns to a low-power mode.

Write Operations

After receiving a matching device address byte with the R/$\overline{W}$ bit set low, the device goes into the write mode of operation. The master must transmit an 8-bit EEPROM memory address to the device to define the address where the data is to be written. After the byte has been received, the DS3904 transmits a zero for one clock cycle to acknowledge that the memory address has been received. The master must then transmit an 8-bit data word to be written into this memory address. The DS3904 again transmits a zero for one clock cycle to acknowledge the receipt of the data byte. At this point, the master must terminate the write operation with a stop condition. The DS3904 then enters an internally timed write process t_W to the EEPROM memory. All inputs are disabled during this write cycle.

Acknowledge Polling

Once the internally timed write has started and the DS3904 inputs are disabled, acknowledge polling can be initiated. The process involves transmitting a start condition followed by the device address. The R/$\overline{W}$ bit signifies the type of operation that is desired. The read or write sequence is only allowed to proceed if the internal write cycle has completed and the DS3904 responds with a zero.

Read Operations

After receiving a matching address byte with the R/$\overline{W}$ bit set high, the device goes into the read mode of operation. A read requires a dummy byte write sequence to load in the register address. Once the device address and data address bytes are clocked in by the master, and acknowledged by the DS3904, the master must generate another start condition (repeated start). The master now initiates a read by sending the device address with the R/$\overline{W}$ bit set high. The DS3904 acknowledges the device address and serially clocks out the data byte. The master responds with a NACK and generates a stop condition afterwards.

See Figures 4 and 5 for command and data byte structures as well as read and write examples.

2-Wire Serial Port Operation

The 2-wire serial port interface supports a bidirectional data transmission protocol with device addressing. A device that sends data on the bus is defined as a transmitter, and a device receiving data as a receiver. The device that controls the message is called a “master.” The devices that are controlled by the master are “slaves.” The bus must be controlled by a master device that generates the SCL, controls the bus access, and generates the start and stop conditions. The DS3904 operates as a slave on the 2-wire bus. Connections to the bus are made through SCL and open-drain SDA lines. The following I/O terminals control the 2-wire serial port: SDA, SCL, and A0. Timing diagrams for the 2-wire serial port can be found in Figures 2 and 3. Timing information for the 2-wire serial port is provided in the *AC Electrical Characteristics* table for 2-wire serial communications.

The following bus protocol has been defined:

Data transfer can be initiated only when the bus is not busy.

During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high are interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus Not Busy: Both data and clock lines remain high.

Start Data Transfer: A change in the state of the data line from high to low while the clock is high defines a start condition.

Stop Data Transfer: A change in the state of the data line from low to high while the clock line is high defines the stop condition.

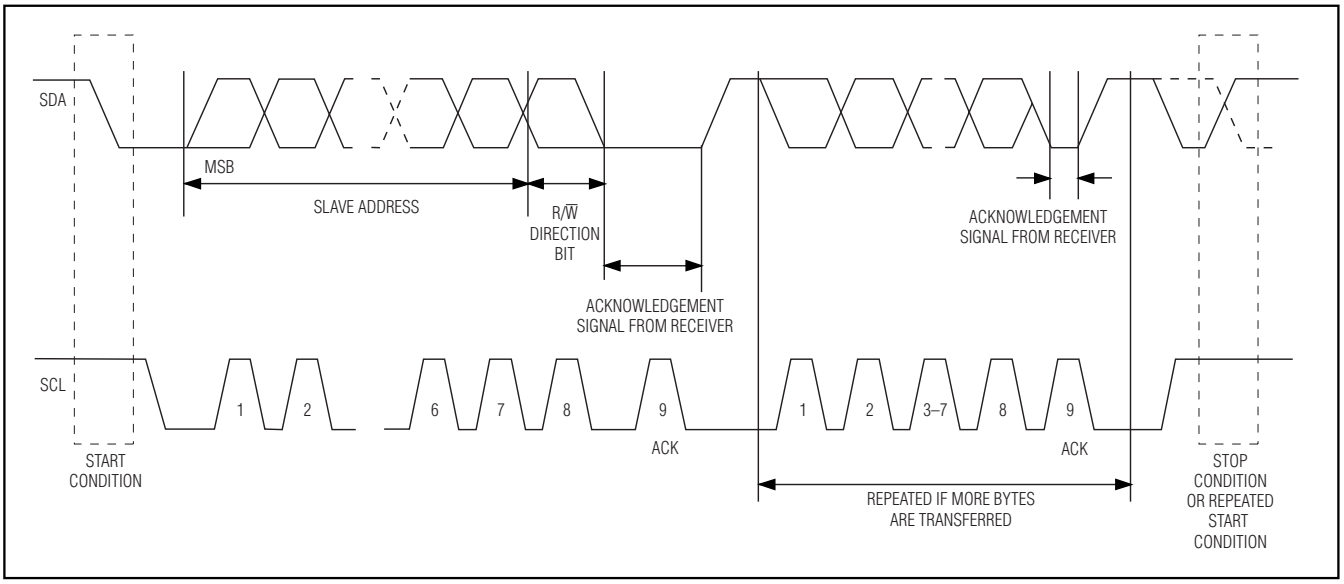


Figure 2. 2-Wire Data Transfer Protocol

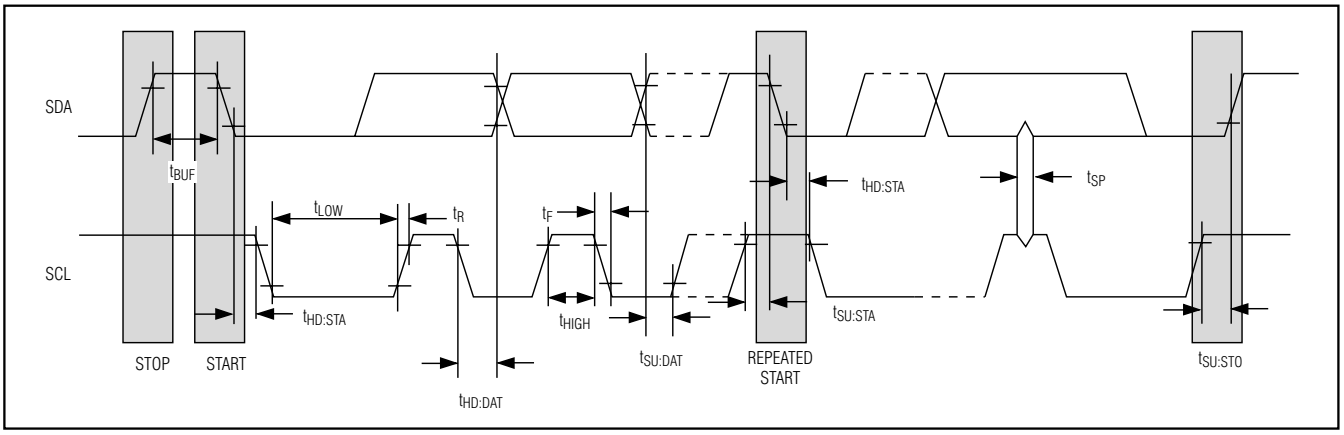


Figure 3. 2-Wire AC Characteristics

Data Valid: The state of the data line represents valid data when, after a start condition, the data line is stable for the duration of the high period of the clock signal. The data on the line can be changed during the low period of the clock signal. There is one clock pulse per bit of data. Figures 2 and 3 detail how data transfer is accomplished on the 2-wire bus. Depending upon the state of the R/$\overline{W}$ bit, two types of data transfer are possible.

Each data transfer is initiated with a start condition and terminated with a stop condition. The number of data bytes transferred between start and stop conditions is not limited and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

Within the bus specifications, a regular mode (100kHz clock rate) and a fast mode (400kHz clock rate) are defined. The DS3904 works in both modes.

Acknowledge: Each receiving device, when addressed, generates an acknowledge after the byte has been received. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is a stable low during the high period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. A

DS3904 Triple 128-Position Nonvolatile Variable Digital Resistor/Switch

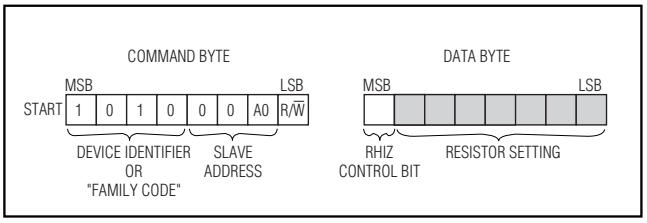


Figure 4. Command and Data Byte Structures

master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line high to enable the master to generate the stop condition.

Data transfer from a master transmitter to a slave receiver. The first byte transmitted by the master is the command/control byte. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte.

Data transfer from a slave transmitter to a master receiver. The master transmits the first byte (the command/control byte) to the slave. The slave then returns an acknowledge bit. Next follows the data byte transmitted by the slave to the master. The master returns NACK followed by a stop.

The master device generates all serial clock pulses and the start and stop conditions. A transfer is ended with a stop condition or with a repeated start condition. Since a repeated start condition is also the beginning of the next serial transfer, the bus is not released.

The DS3904 can operate in the following three modes:

1) **Slave Receiver Mode:** Serial data and clock are received through SDA and SCL, respectively. After each byte is received, an acknowledge bit is transmitted. Start and stop conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after the slave (device) address and direction bit has been received.

2) **Slave Transmitter Mode:** The first byte is received and handled as in the slave receiver mode. However, in this mode the direction bit indicates that the transfer direction is reversed. Serial data is transmitted on SDA by the DS3904 while the serial clock is input on SCL. Start and stop conditions are recognized as the beginning and end of a serial transfer.

3) **Slave Address:** Command/control byte is the first byte received following the start condition from the master device. The command/control byte consists of a 6-bit control code. For the DS3904, this is set as 101000 binary for read/write operations. The next bit of the command/control byte is the device select bit or slave address (A0). It is used by the master device to select which of two devices is to be accessed. When reading or writing the DS3904, the device-select bits must match the device-select pin (A0). The last bit of the command/control byte (R/$\overline{W}$) defines the operation to be performed. When set to a '1', a read operation is selected, and when set to a '0', a write operation is selected.

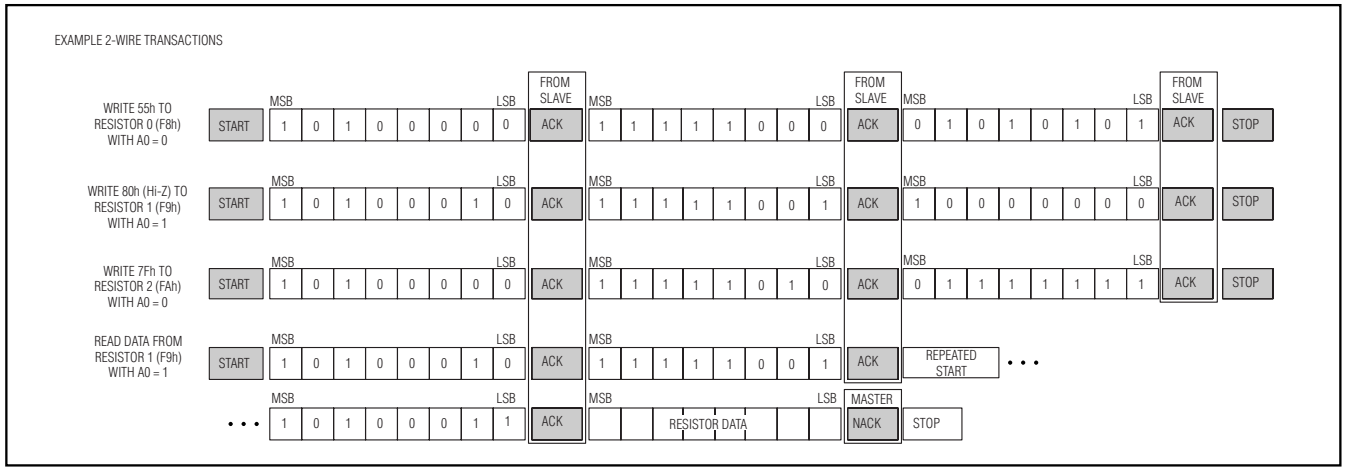


Figure 5. Example 2-Wire Transactions

DS3904 Triple 128-Position Nonvolatile Variable Digital Resistor/Switch

Following the start condition, the DS3904 monitors the SDA bus checking the device-type identifier being transmitted. Upon receiving the 101000 control code, the appropriate device address bit, and the read/write bit, the slave device outputs an acknowledge signal on the SDA line.

Applications Information

Power-Supply Decoupling

To achieve the best results when using the DS3904, decouple the power supply with a 0.01µF or 0.1µF capacitor. Use a high-quality ceramic surface-mount capacitor. Surface-mount components minimize lead inductance, which improves performance, and ceramic capacitors tend to have adequate high-frequency response for decoupling applications.

Using the Resistor as a Switch

By taking advantage of the high-impedance mode, a switch can be created to produce a digital output. Setting one of the resistor registers to 00h creates the low state. Writing 80h into the same resistor register enables the high-impedance state. Furthermore, an external pullup resistor can be used to generate a high state as well.

High Resistor Terminal Voltage

It is possible to have a voltage on the resistor-high terminals that is higher than the voltage connected to V_{CC}. For instance, connecting V_{CC} to 3.0V while one or more of the resistor high terminals are connected to 5.0V allows a 3V system to control a 5V system. The 5.5V maximum still applies to the limit on the resistor high terminals regardless of the voltage present on V_{CC}.

Chip Information

TRANSISTOR COUNT: 9049

SUBSTRATE CONNECTED TO GROUND

Package Information

For the latest package outline information, go to **www.maxim-ic.com/packages**.